On Constructing Lower Power and Robust Clock Tree via Slew Budgeting

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Outline

- Motivation
- Previous Clock Tree Works
- Methodology
  - Check: “Bad slew degrades voltage variation induced skew”
  - Buffer insertion in global view
  - Greedy power minimization in bottom level
- Experimental Result
- Conclusion

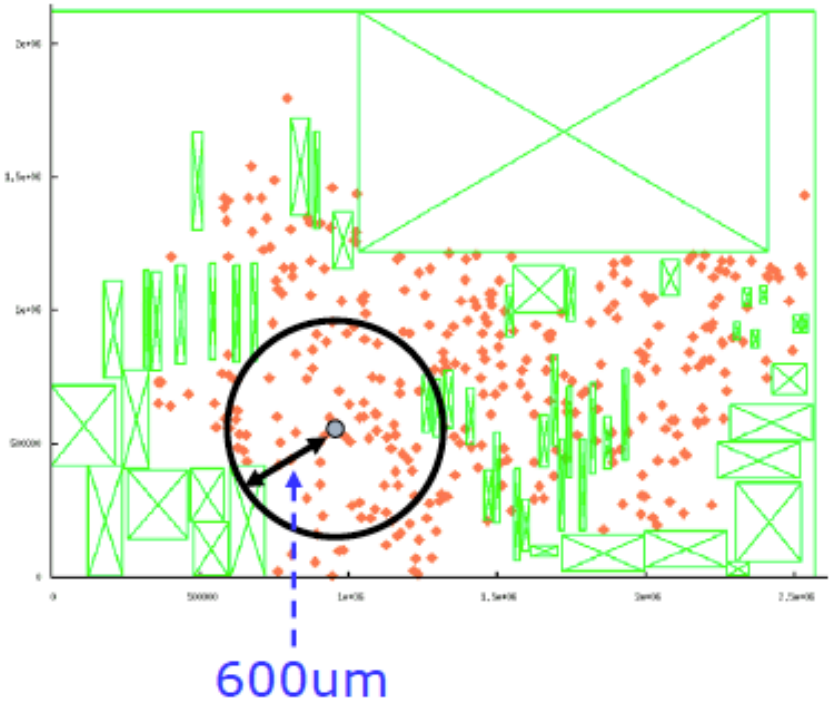
Motivation
High Performance Clock Network

- Low power
  - Clock network contributes 40% power
- Robustness
  - Shrinking down manufacturing has crucial process variation
    - Decreasing VDD
    - Interconnect issue

Problem Definition

ISPD 2010 High Performance Clock Network Synthesis Contest

- Given
  - A set of sinks
  - A set of blockages
  - Inverter/wire library
  - Variation source:
    - Voltage: ±7.5% (uniform distribution)
    - Wire width: ±5% (uniform distribution)
  - Local skew distance
- Objective: minimize power
- Constraints:
  - Skew: 95% LCS < skew limit
  - Signal quality: slew < slew limit
  - Buffer location: a buffer can not overlap with a blockage



Our Contribution

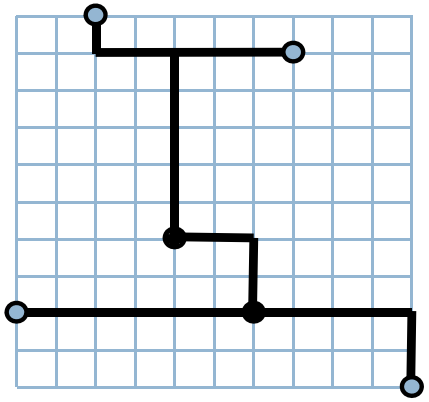
- We check that **slew** is a crucial factor for **voltage variation** induced skew
- To improve power efficiency of buffer insertion
  - **A hybrid structure** was adopted, it makes skew estimation easier
  - With **a skew estimation**, buffer insertion was planned in global view
- Performance Improvement
  - **10% power reduction** than state-of-the-art clock network, [8], on ISPD 2010 benchmark
  - Less number of embedded SPICE simulations is needed

[8]T. Mittal et al. "Cross Link Insertion for Improving Tolerance to Variations in Clock Network Synthesis". In ISPD, pages 29-36, 2011.

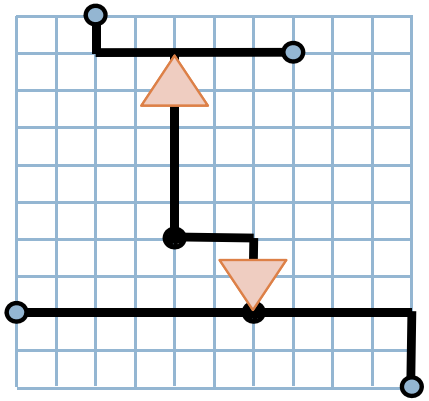
Previous Works (1/3)

Later Fine-Tuning with Two Stage Synthesis [1]

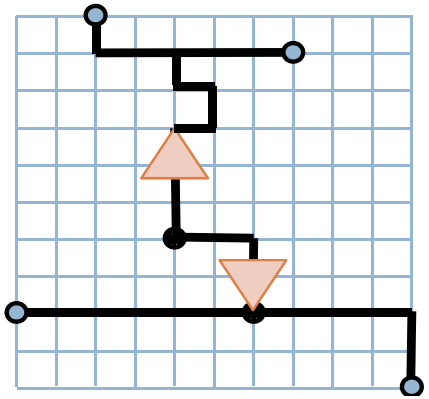
Topology Generation



Buffer Insertion **(latency minimization)**



Fine-tuning

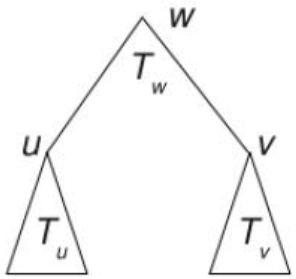


- First generate a topology and perform buffer insertion that minimizes clock latency
  - Buffer insertion may be power inefficient
- Later fine-tuning by delay buffer insertion and wire snacking
  - Much run time

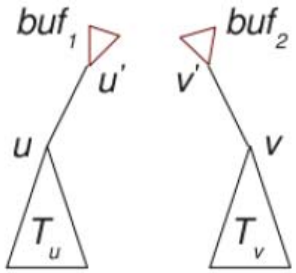
[1] D.J. Lee, M.C. Kim, and I.L. Markov. "Low-Power Clock Trees for CPUs". *In International Conference on Computer-Aided Design*, pages 444-451, 2010. (Contango 2.0)

Previous Works (2/3)

Interleaving Topology Generation and Buffer Insertion with Early Skew Estimation [2]



Checking slew when merging



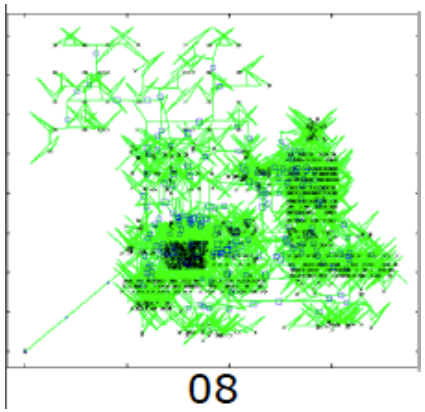
Insert buffer, if slew violation. (The position where the buffer was inserted makes slew of leaf nodes on the constraint boundary.)

- Interleaving topology generation and buffer insertion
  - For each merge, a slew check would decide if buffer is inserted
  - Slew is on constraint boundary
- Early skew estimation
  - To decide buffer size
  - Oversimplification makes buffer insertion power inefficient

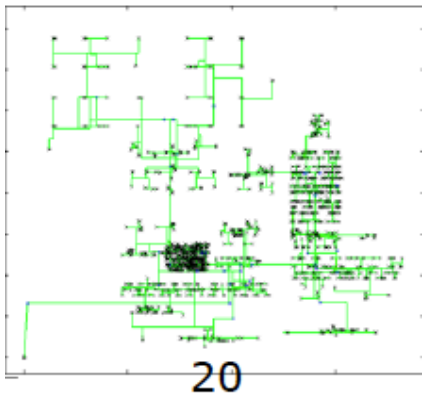
[2] S. Bujimalla and C.-K. Koh. "Synthesis of Low Power Clock Trees for Handling Power-Supply Variations". *In International Symposium on Physical Design*, pages 37-44, 2011.

Previous Works (3/3)

Timing Model Independent Tree [6,7]



Symmetry



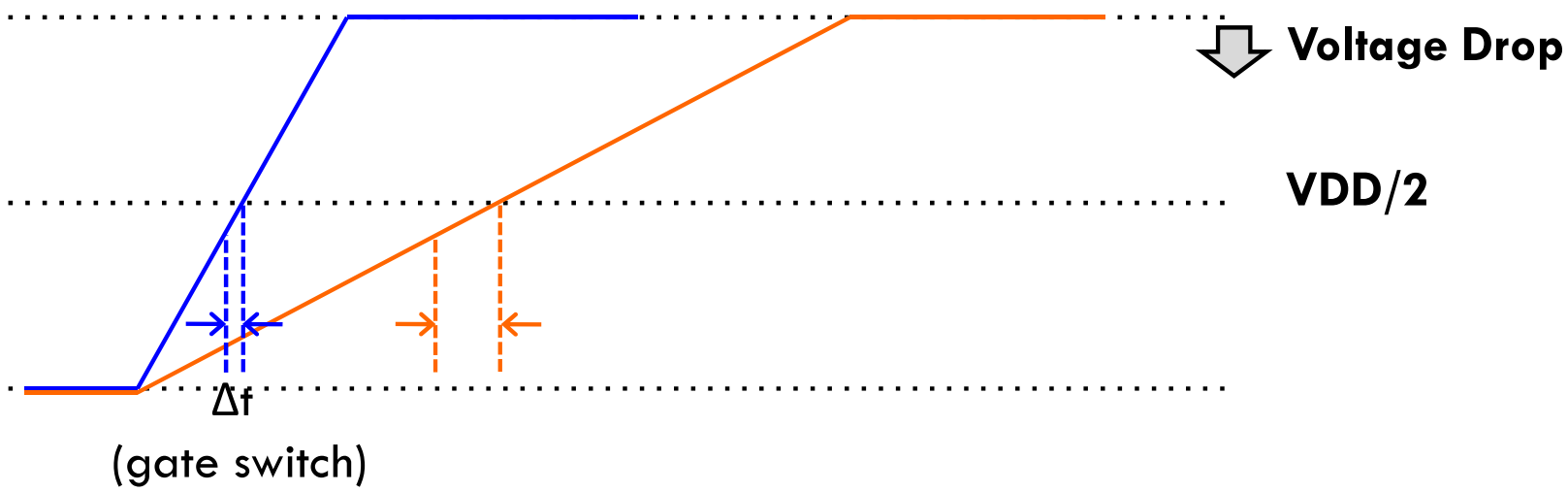
Asymmetry

- Symmetry structure
  - Pro: fast run time
  - Con: power (longer wire)
- Overdesign w/o skew estimation
- Its buffer insertion also makes slew on constraint boundary

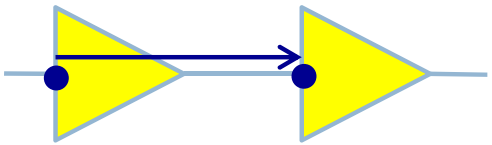
[6] X.W. Shih and Y.W. Chang. "Fast Timing-Model Independent Buffered Clock-Tree Synthesis". *In Design Automation Conference*, pages 80-85, 2010.

[7] X.W. Shih, H.C. Lee, K.H. Ho, and Y.W. Chang. "High Variation-Tolerant Obstacle-Avoiding Clock Mesh Synthesis with Symmetrical Driving Trees". *In International Conference on Computer-Aided Design*, pages 452-457, 2010.

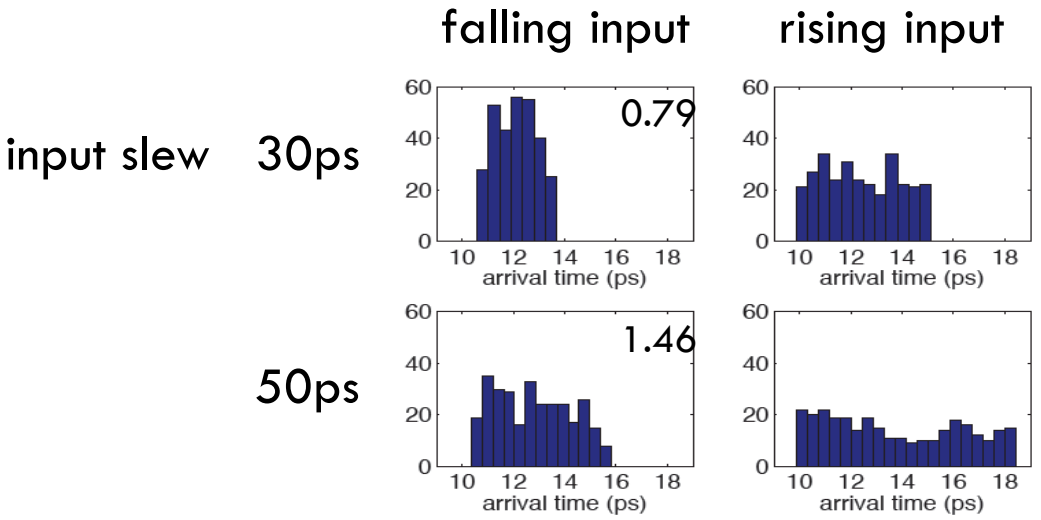
Bad Slew Degrades Skew If Supply Voltage Varies



Measure delay

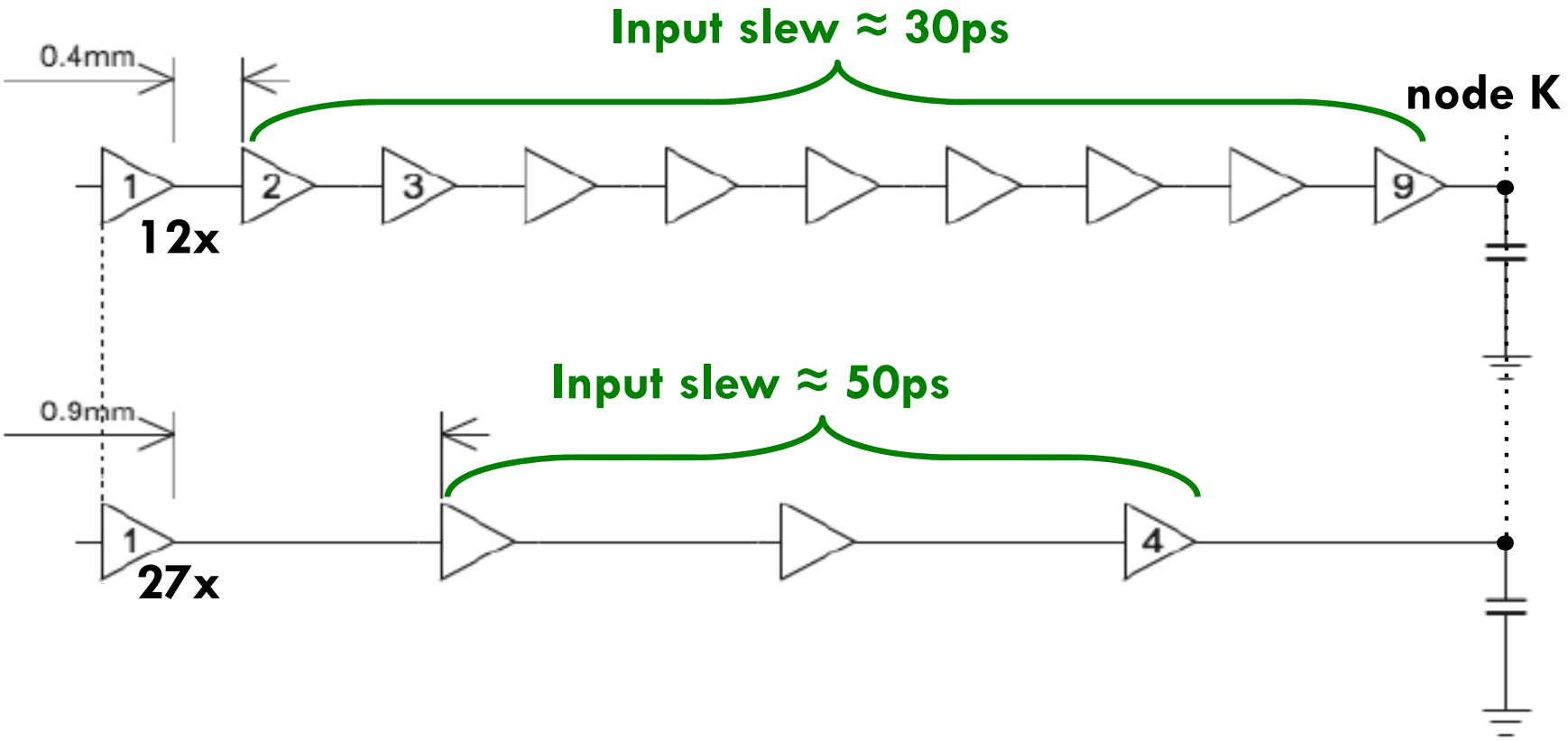


A buffer is 12 type-1 inverters in parallel, and wire length is 0.4mm of type-0

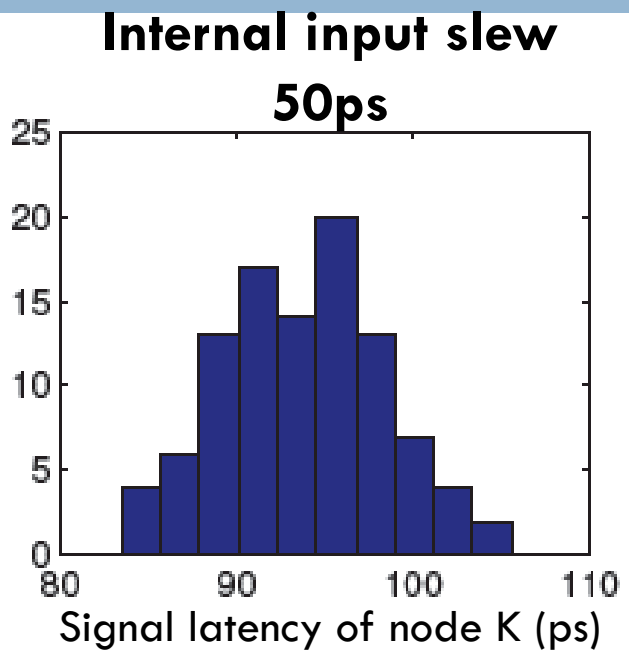


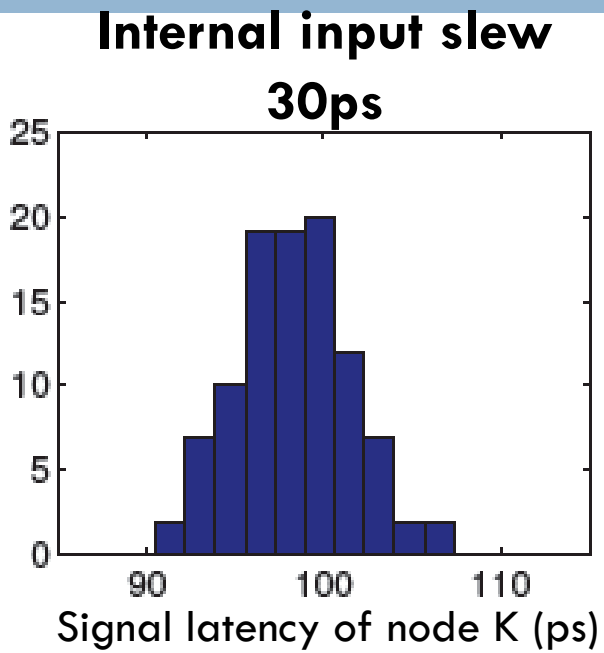
Delay histogram

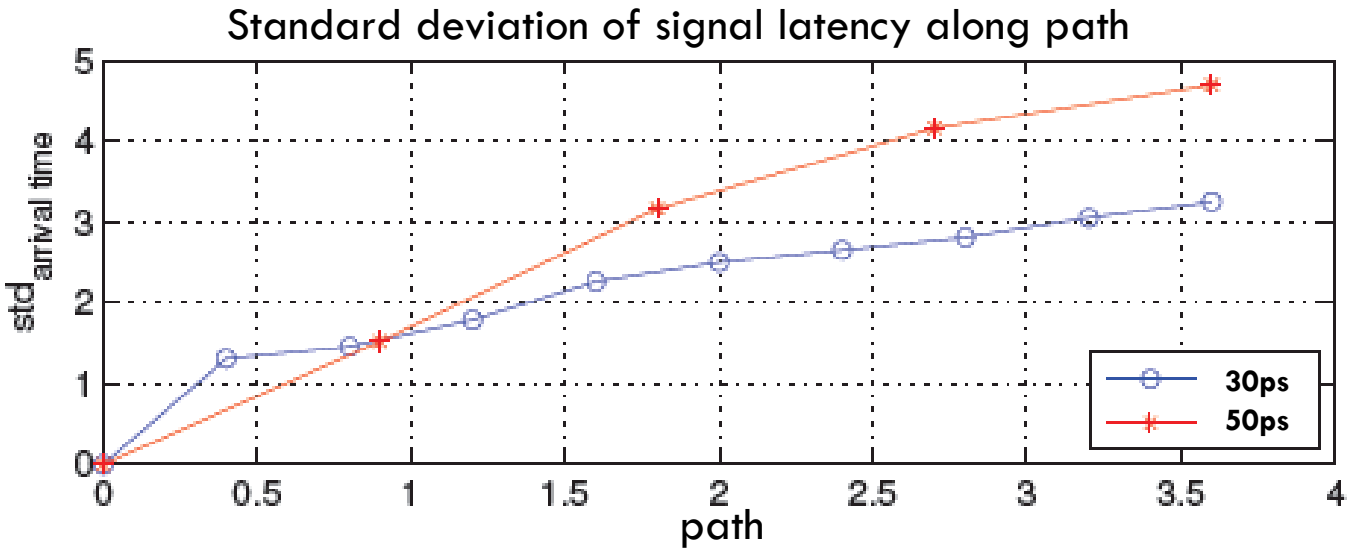
Experiment(1/2)
Signal Latency Variation with Different Internal Slew



Experiment(2/2)
Signal Latency Variation with Different Internal Slew

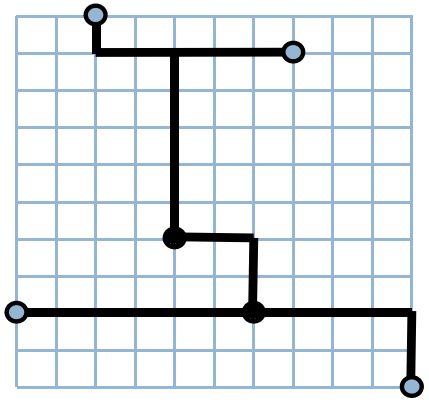




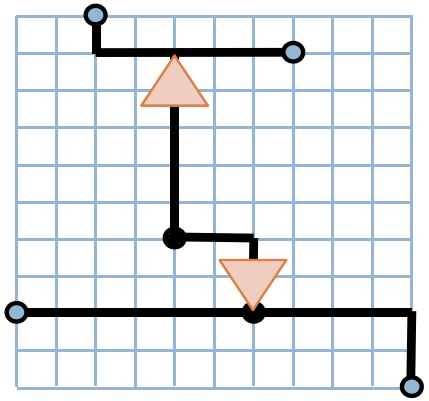


Non-Power Efficient Buffer Insertion in [1]

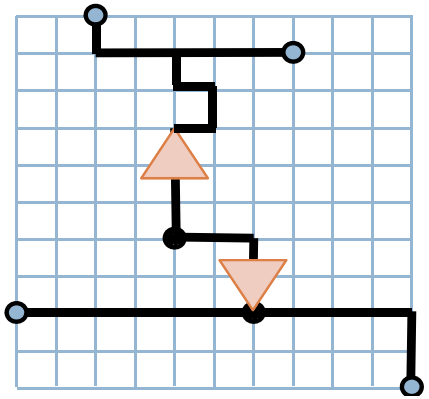
Topology Generation



Buffer Insertion (latency minimization)



Fine-tuning



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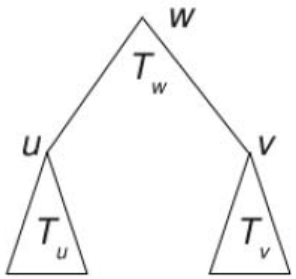

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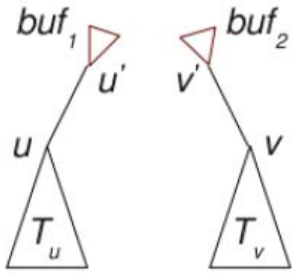

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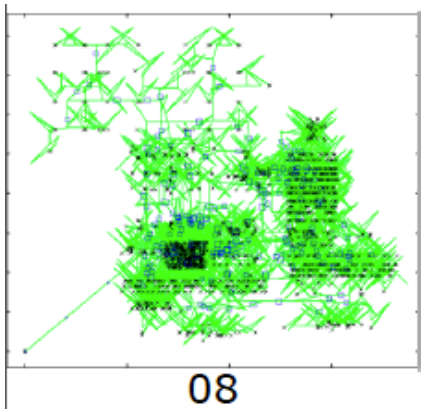
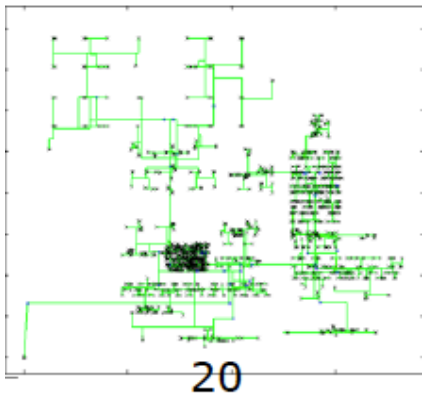
Non-Power Efficient Buffer Insertion in [6,7]



Symmetry



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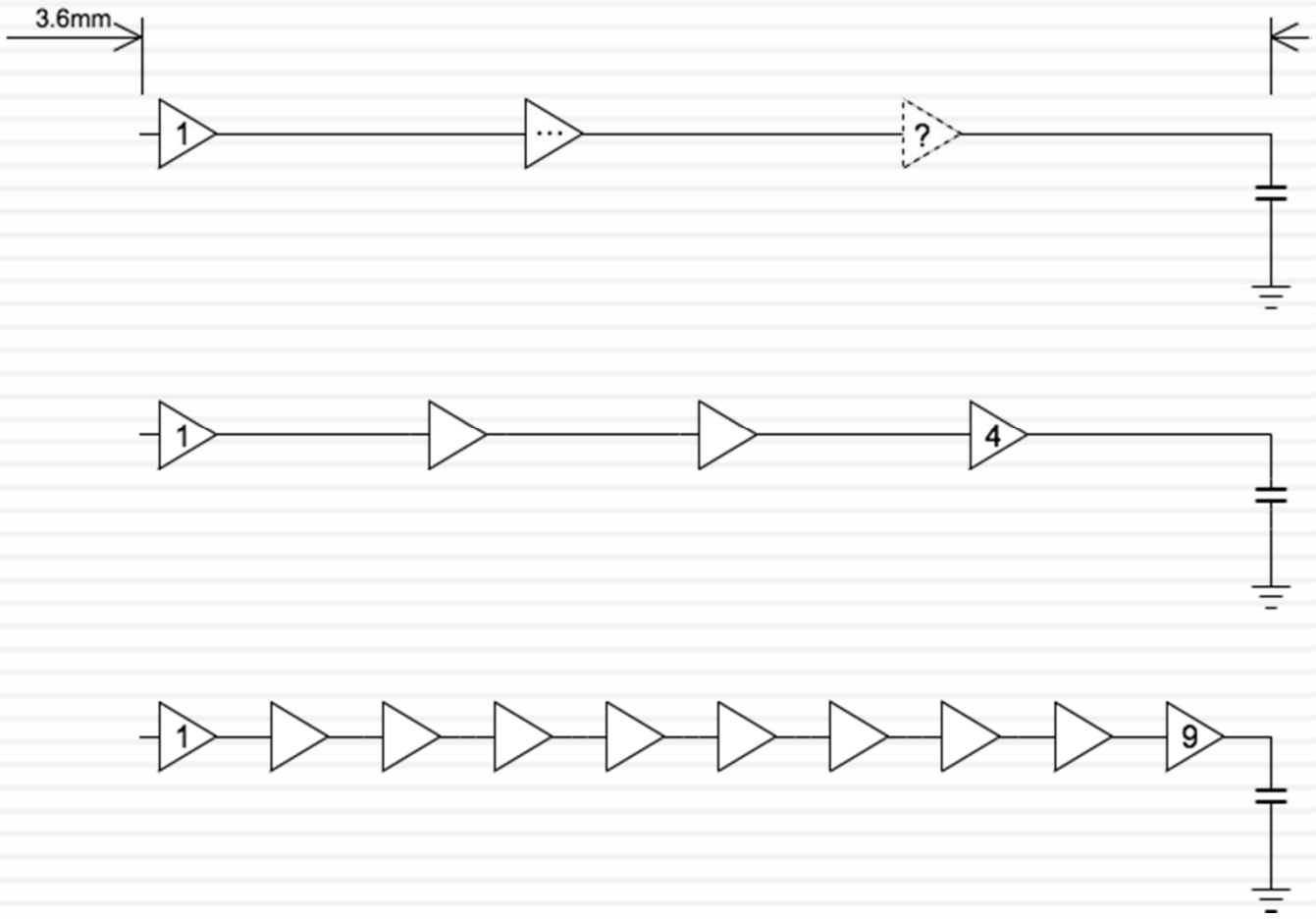
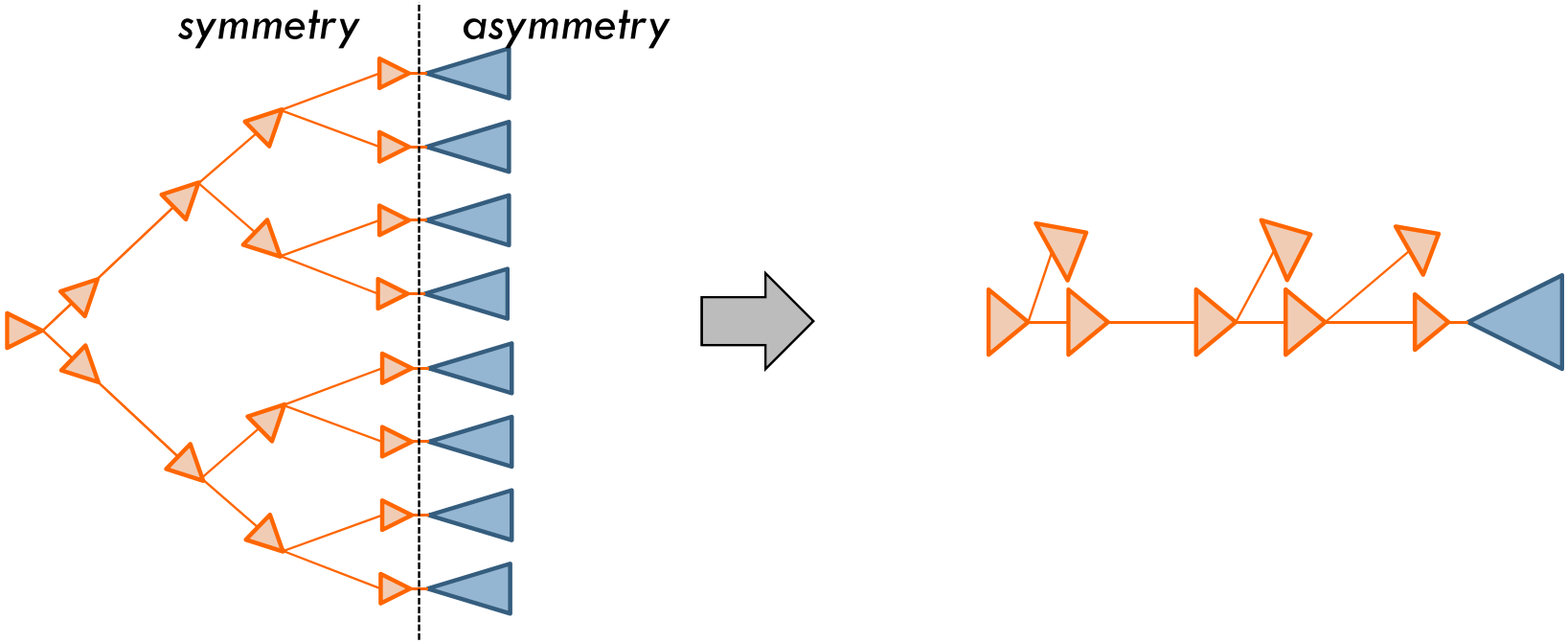
How To Insert Buffer with Slew Consideration?



Our Methodology

- Skew estimation is applied
  - Prevent overdesign
- Hybrid tree structure
  - Symmetry in top level that makes skew estimation simpler
  - Asymmetry in bottom level that saves wire length



Skew Estimation from [2]

N is the number of sinks

σ is the standard deviation of clock latency

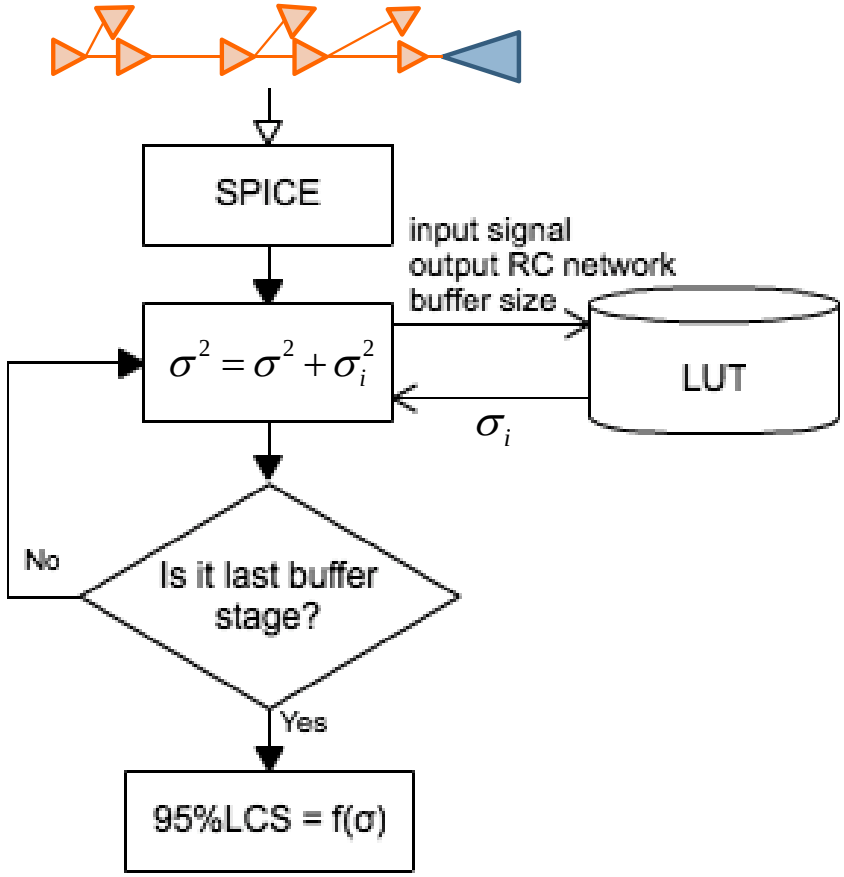
$$95\%LCS = E[skew] + 2\sqrt{Var[skew]}$$

$$E[skew] = \sigma\left[\frac{4\ln N - \ln\ln N - \ln 4\pi + 2C}{(2\ln N)^{1/2}} + O\left(\frac{1}{\log N}\right)\right]$$

$$Var[skew] = \frac{\sigma^2}{\ln N}\frac{\pi^2}{6} + O\left(\frac{1}{(\log N)^2}\right)$$

$\sigma^2 = \sigma_0^2 B$ ⟵ **Oversimplification of [2]**

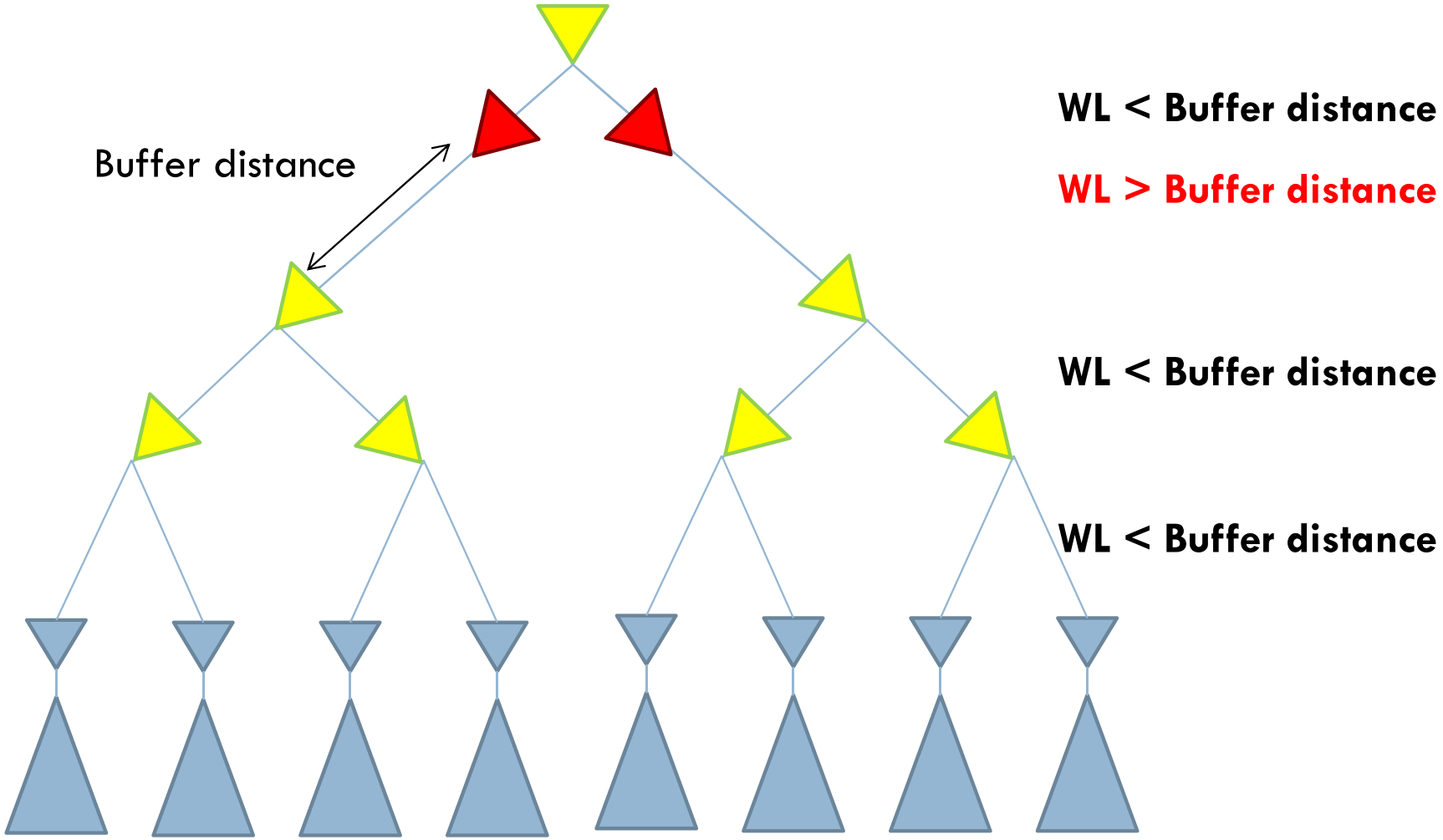
Our skew estimation flow



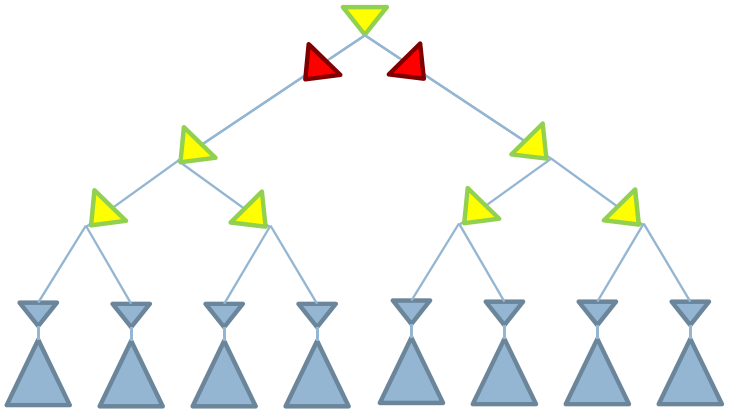
[2] S. Bujimalla and C.-K. Koh, "Synthesis of Low Power Clock Trees for Handling Power-Supply Variations," In *Proceedings of the International Symposium on Physical Design*, pages. 37-44, 2011

[10] S. D. Kugelmass and Kenneth Steiglitz, "An Upper Bound on Expected Clock Skew in Synchronous Systems", *IEEE TRANS. ON COMPUTERS*. vol.39, pp.1475-1477 1990

Buffer Insertion Flow

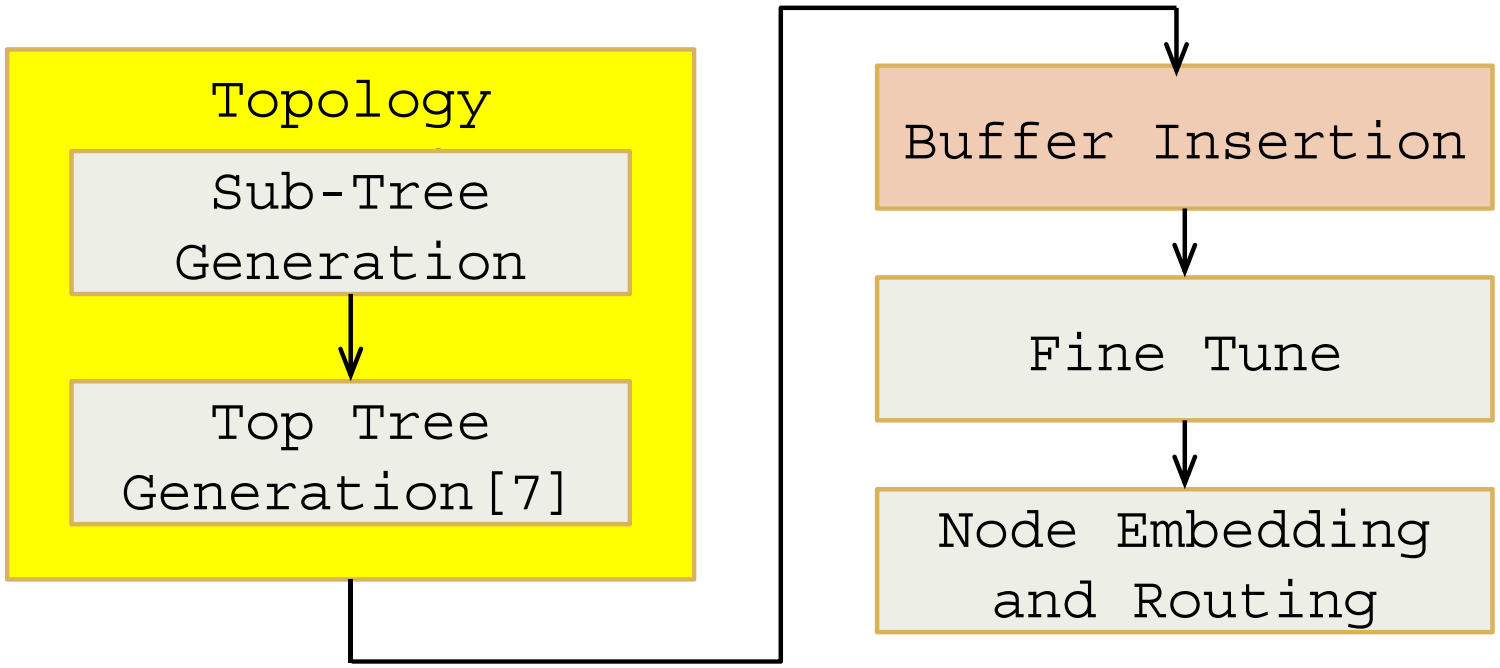


Parameters of Buffer Insertion



- Buffer distance
  - For all possible used buffer sizes, it can maintain good slew
- Buffer size
  - Single value in one solution
  - It was decided by skew estimation

Methodology Flow



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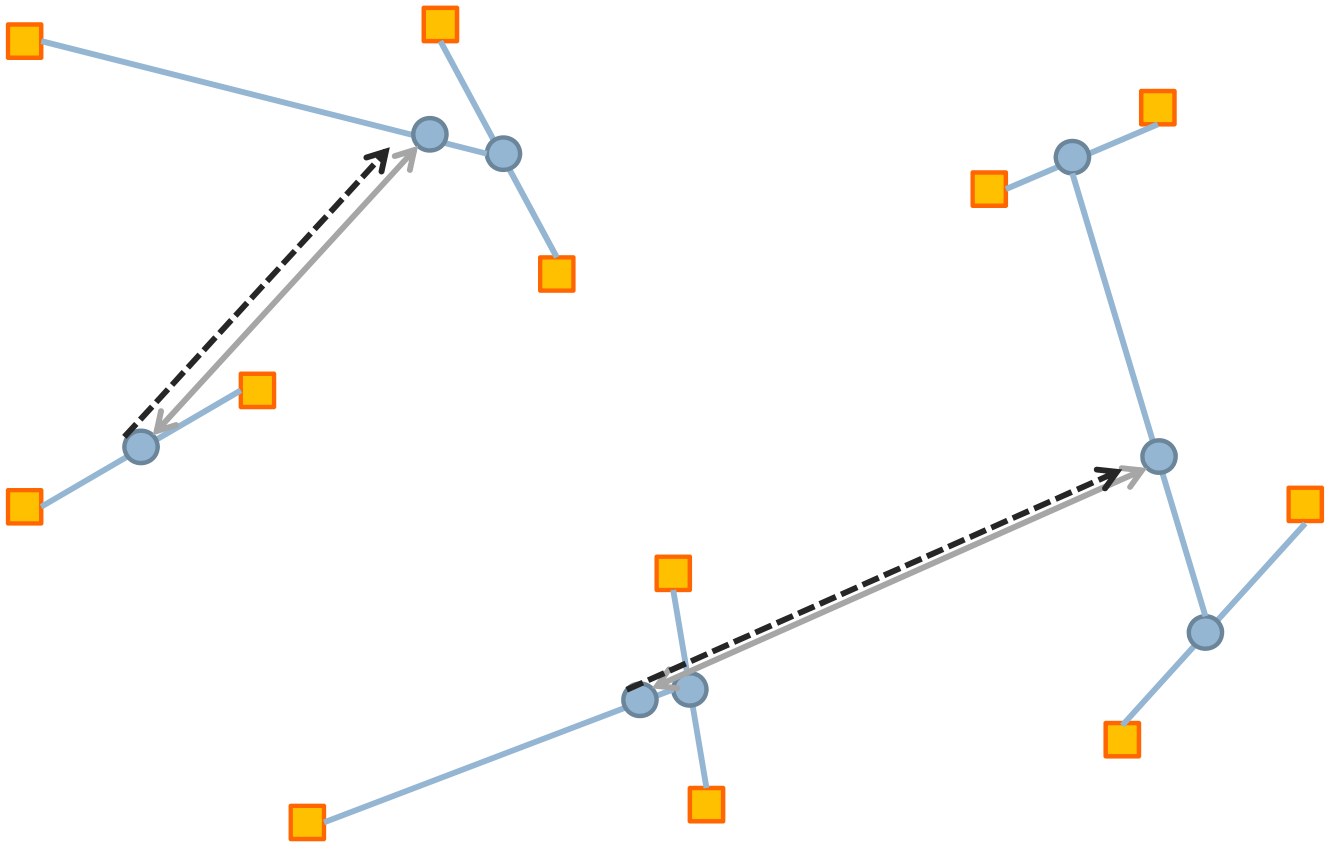
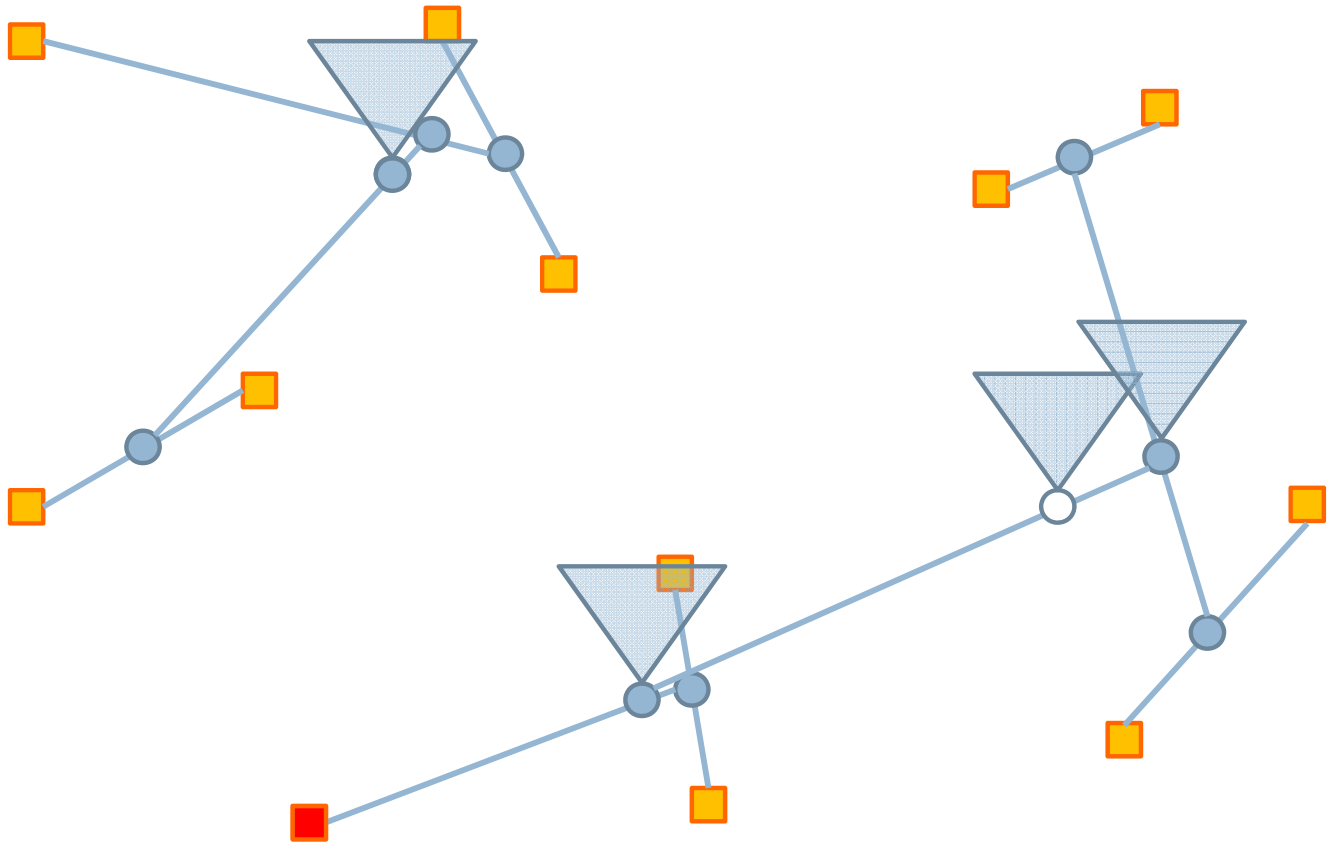
Sub-Tree Generation



Sub-Tree Generation



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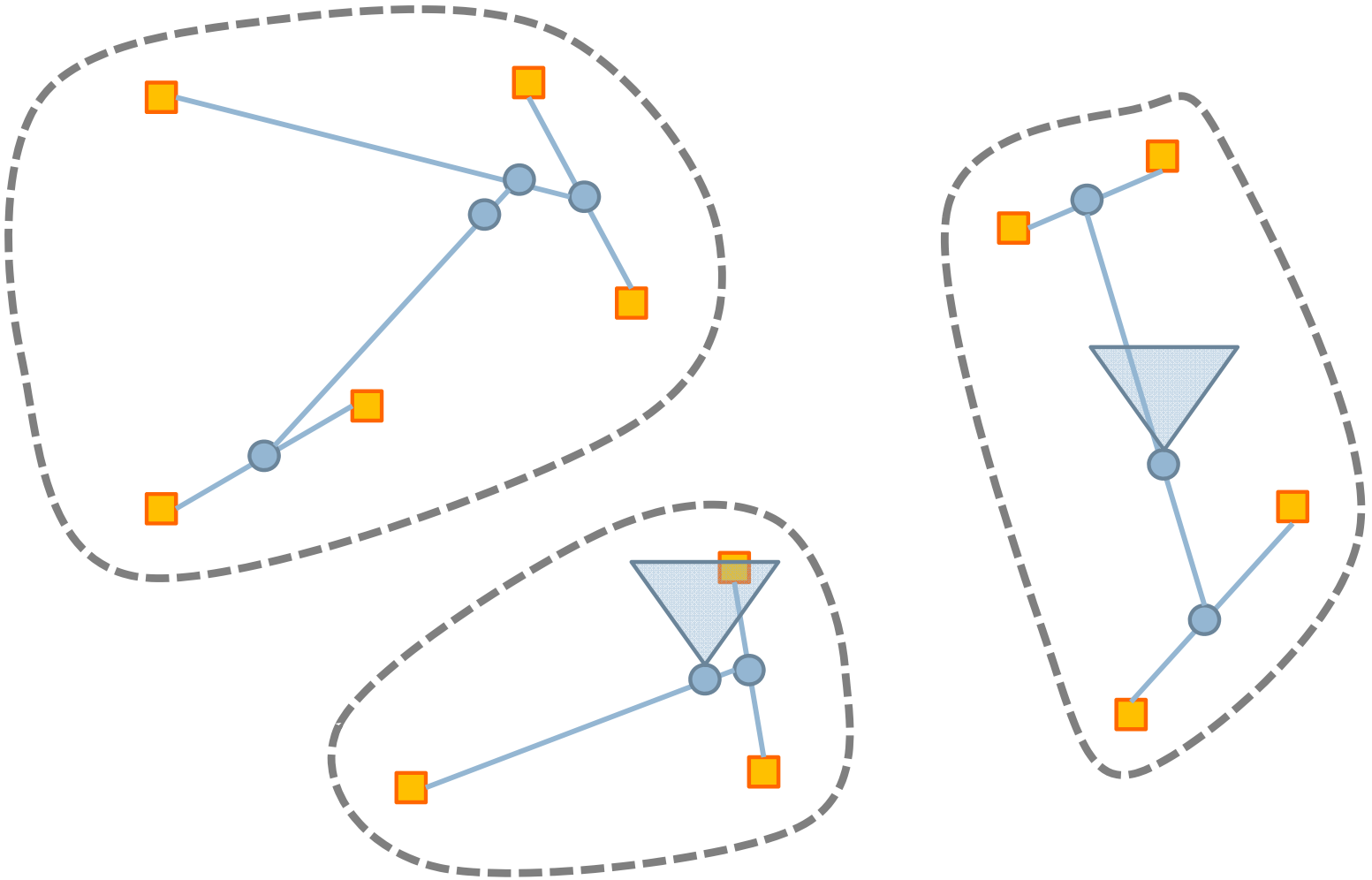
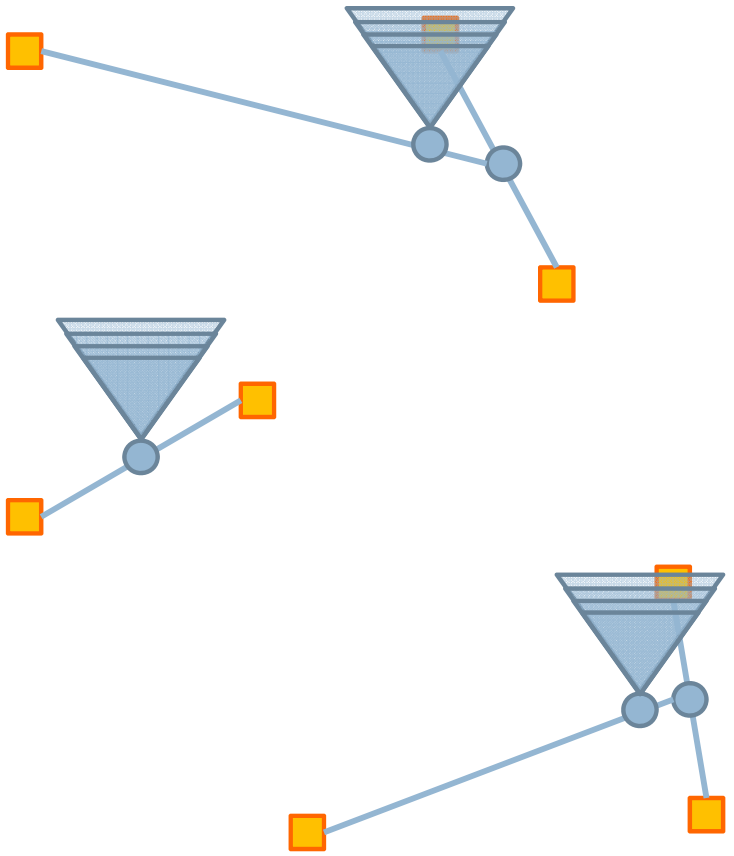
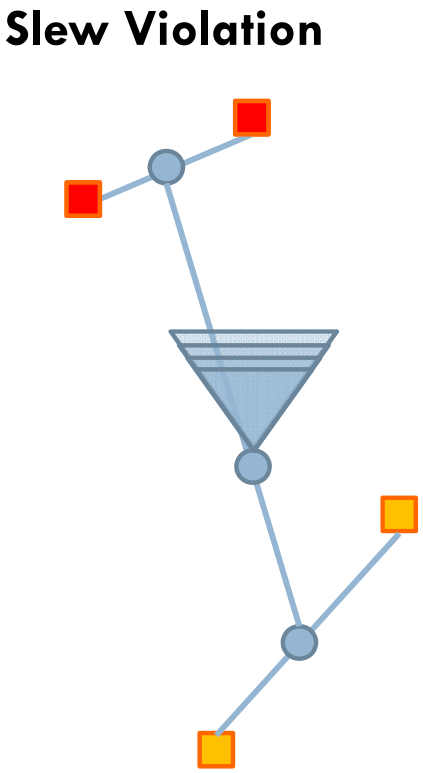
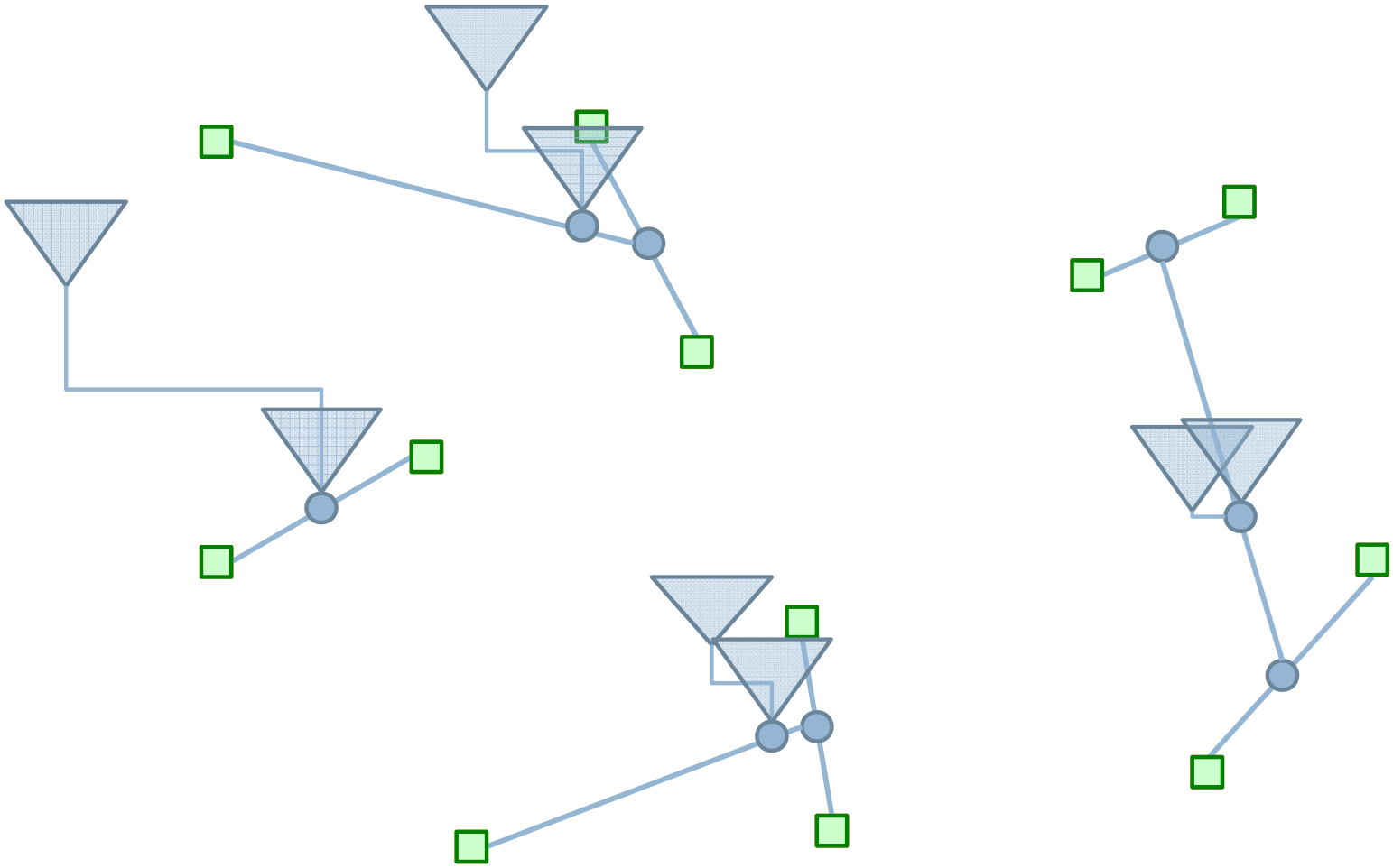


Sub-Tree Generation

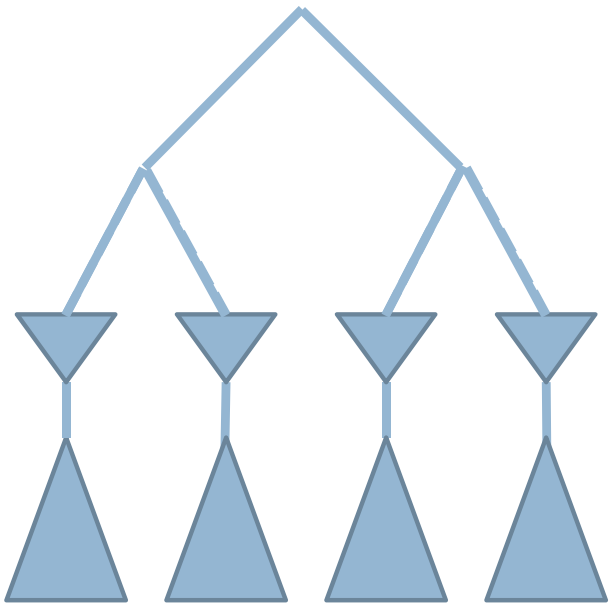


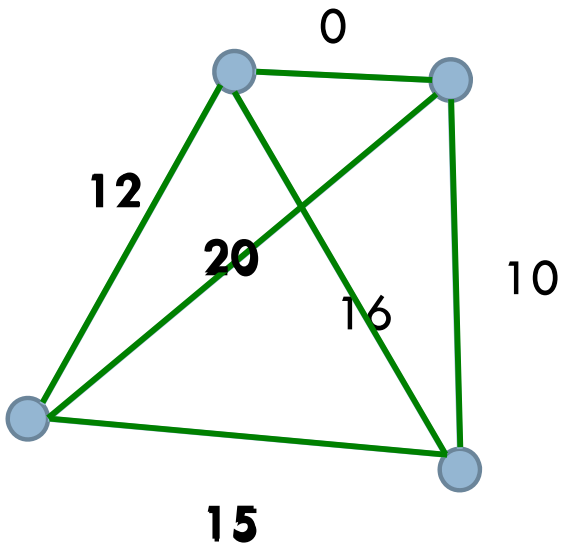


Elongate WL of Sub-trees to slew constraint



Top-Level Tree Generation





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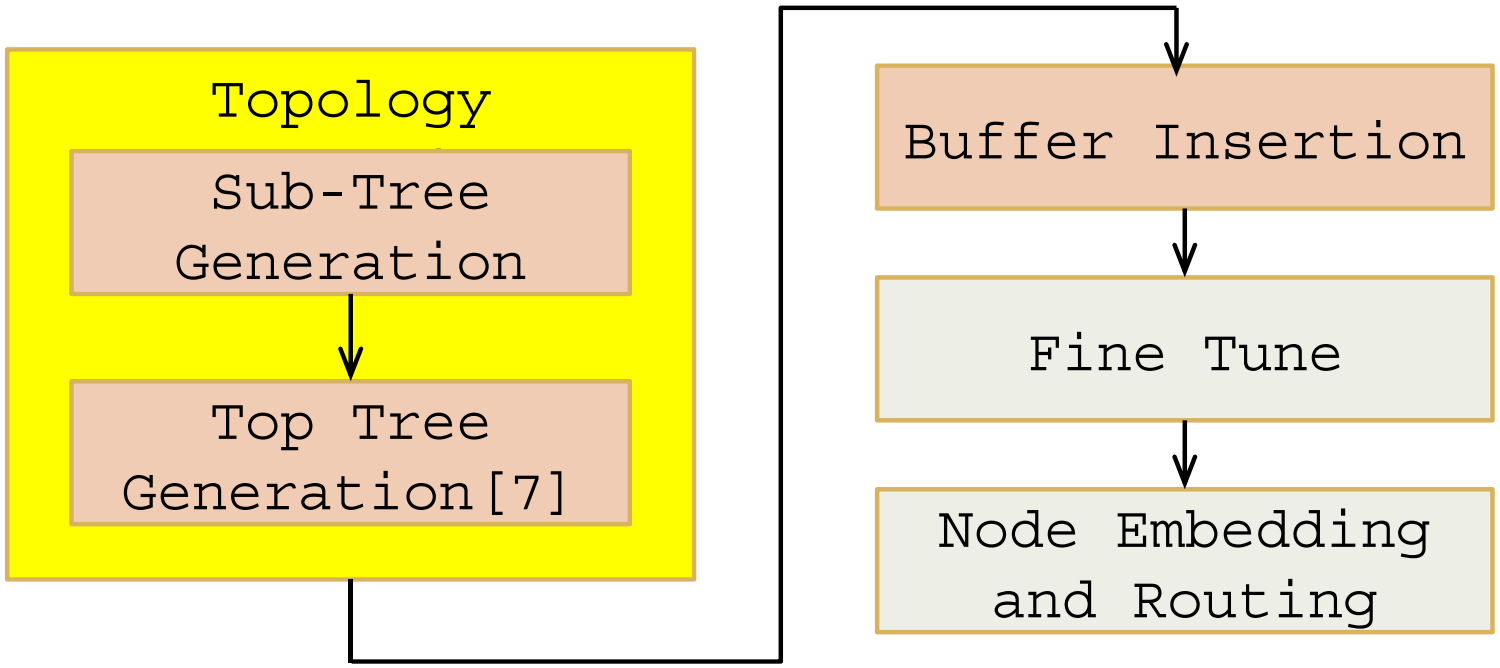
Methodology Flow



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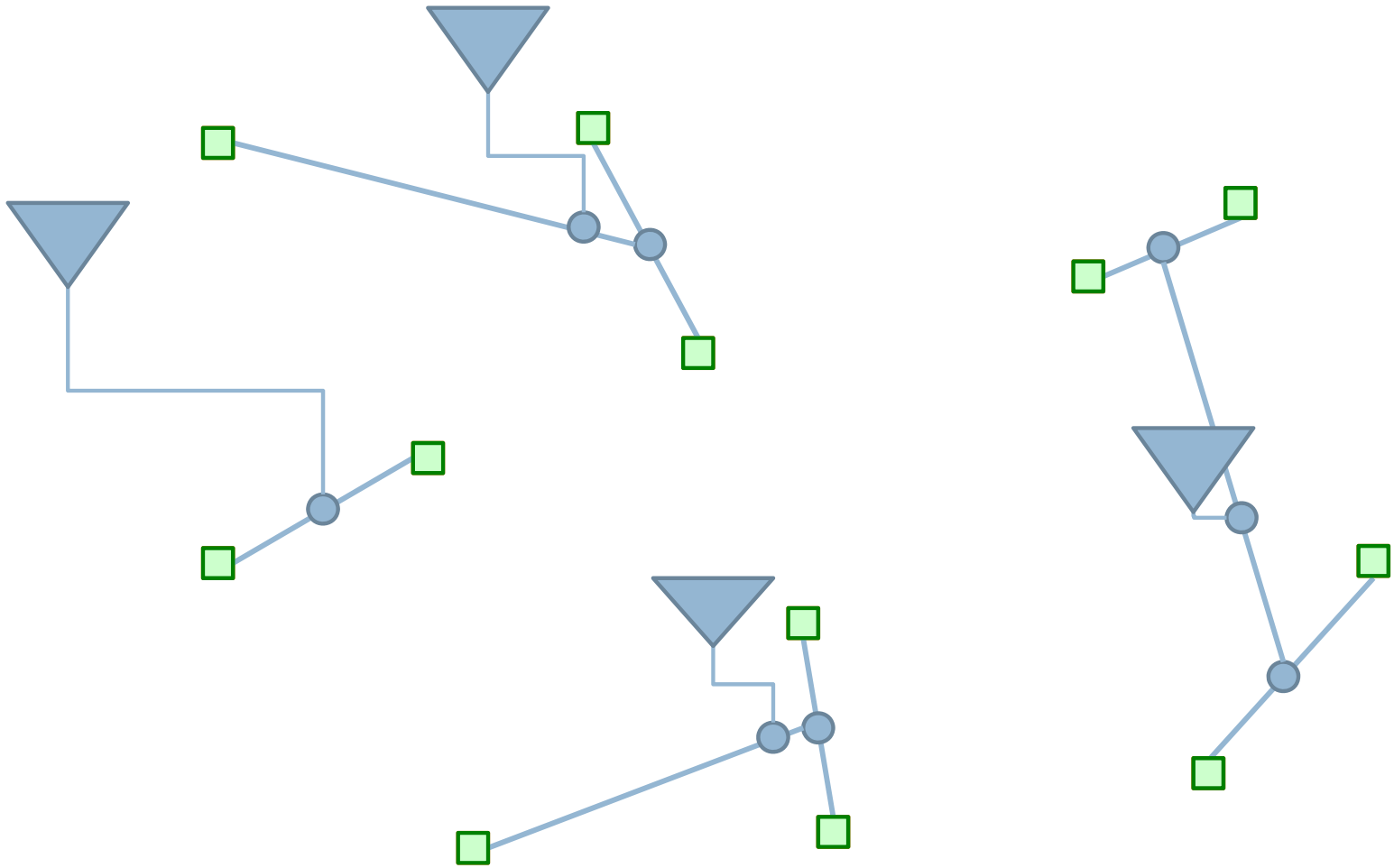
Fine-tuning
Adjust WL of Sub-trees for nominal skew

Iteration N until nominal skew < 1ps



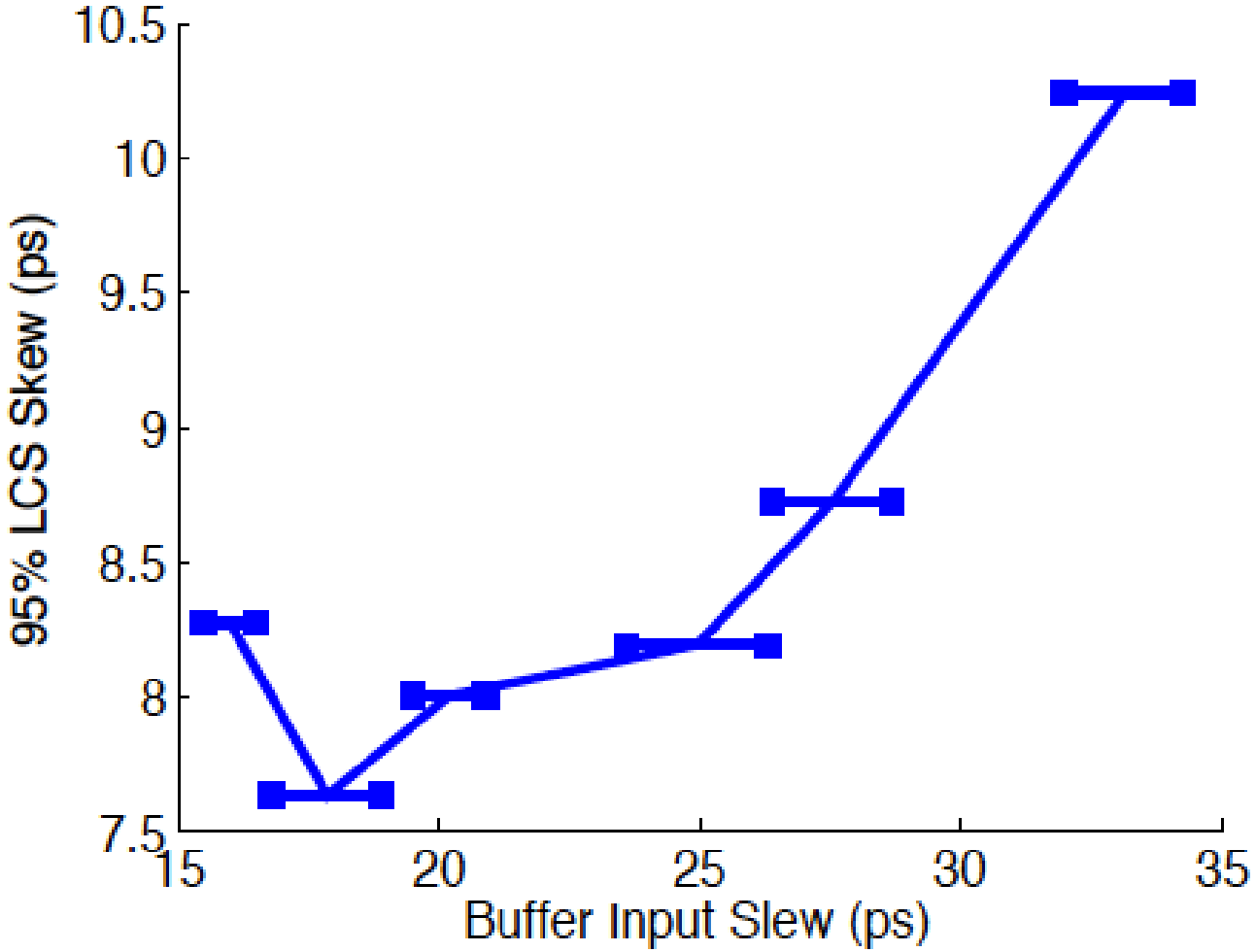
Experimental Results

- Our implementation
  - C++ language
  - On Intel E5620 2.4 GHz with 3.3G memory
- Comparison
  - [1] D.J. Lee et al. "Low-Power Clock Trees for CPUs". *In ICCAD*, pages 444-451, 2010.
  - [2] S. Bujimalla et al. "Synthesis of Low Power Clock Trees for Handling Power-Supply Variations". *In ISPD*, pages 37-44, 2011.
  - [7] X.W. Shih et al. "High Variation-Tolerant Obstacle-Avoiding Clock Mesh Synthesis with Symmetrical Driving Trees". *In ICCAD*, pages 452-457, 2010.
  - **[8] T. Mittal et al. "Cross Link Insertion for Improving Tolerance to Variations in Clock Network Synthesis". *In ISPD*, pages 29-36, 2011.**

		cns01	cns02	cns03	cns04	cns05	cns06	cns07	cns08	Cap Ratio
[7]	95% LCS(ps)	7.16	7.33	4.88	4.01	3.81	7.40	6.24	7.64	4.94
	Cap(pF)	445.3	933.6	183.7	196.3	89.1	160.4	228.2	228.2	
	Run time(sec)	**0.4**	**2.42**	**1.57**	**0.27**	**0.10**	**0.28**	**0.30**	**0.28**	
[1]	95% LCS(ps)	7.01	7.33	4.18	4.46	4.41	6.05	4.58	5.15	1.63
	Cap(pF)	198.3	375.9	55.9	71.8	37.7	47.8	72.7	52.5	
	Run time(sec)	12015	25006	3840	6075	2406	2660	2351	1987	
[2]	95% LCS(ps)	5.79	6.69	3.46	3.79	3.68	4.01	5.65	4.24	1.33
	Cap(pF)	177.4	329.9	50.8	57.4	28.9	36.1	57.9	40.4	
	Run time(sec)	2790	7787	2094	934	1110	1142	2968	1497	
[8]	95% LCS(ps)	7.32	7.42	4.49	6.70	4.78	6.41	5.86	5.07	1.10
	Cap(pF)	142.6	**265.2**	36.6	51.1	25.1	32.7	48.3	32.7	
	Run time(sec)	1092	4314	383	934	278	285	818	327	
ours	95% LCS(ps)	6.48	7.38	4.76	7.14	5.88	5.61	6.62	6.50	1.00
	Cap(pF)	**137.9**	268.3	**34.2**	**42.8**	**22.1**	**28.5**	**43.9**	**28.4**	
	Run time(sec)	**472**	**1450**	**79**	**110**	**40**	**61**	**133**	**54**	

Slew vs. 95%LCS on CNS08

We have to consider slew to control voltage variation induced skew



Summary

- Slew is a crucial factor for voltage variation induced skew
- To perform power efficient buffer insertion with slew consideration
  - A hybrid structure was adopted, it makes skew estimation easier
  - With a skew estimation, buffer insertion was planned in global view
- Performance Improvement
  - 10% power reduction than state-of-the-art clock network
  - Less number of embedded SPICE simulations is needed

Future Work

- Unrealistic ISPD Monte Carlo simulation setup
  - Spatial correlation of supply-voltage variation
- Systematic buffer insertion method
  - Multiple buffer size should be considered
  - Buffer placement decision should be more flexible
  - Extend to asymmetry structure

Thank you

In SLSV(Single Location Single Voltage)