Routability-driven Placement Algorithm for Analog Integrated Circuits

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Outline

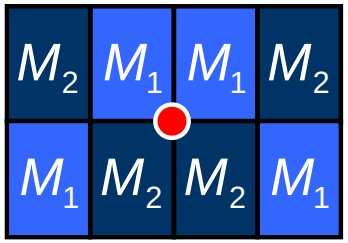
- Introduction to Analog Placement
- Routability-driven Analog Placement
- Congestion Estimation
- Placement Expansion
- Proposed Placement Flow
- Experimental Results
- Conclusion

Analog Placement Considerations

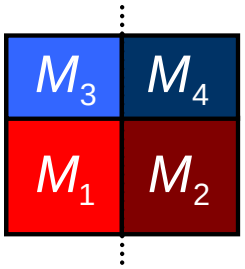
- Basic constraints
  - Matching – interdigitated placement, common-centroid placement
  - Symmetry – symmetric placement
  - Proximity – adjacent placement

- Other considerations
  - Thermal effects, stress gradients, etc.

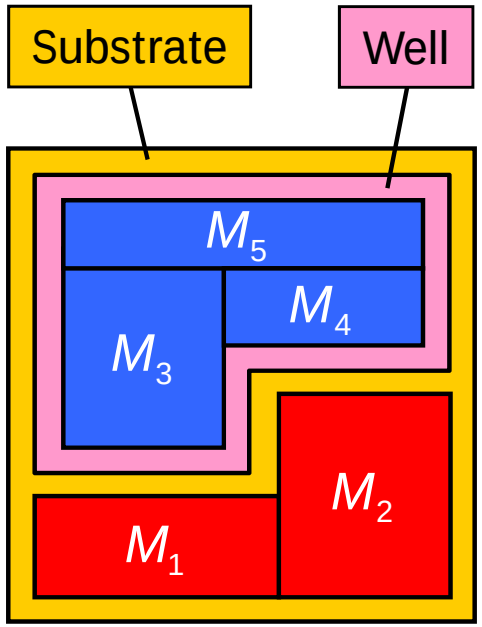
Interdigitated placement



Common-centroid placement



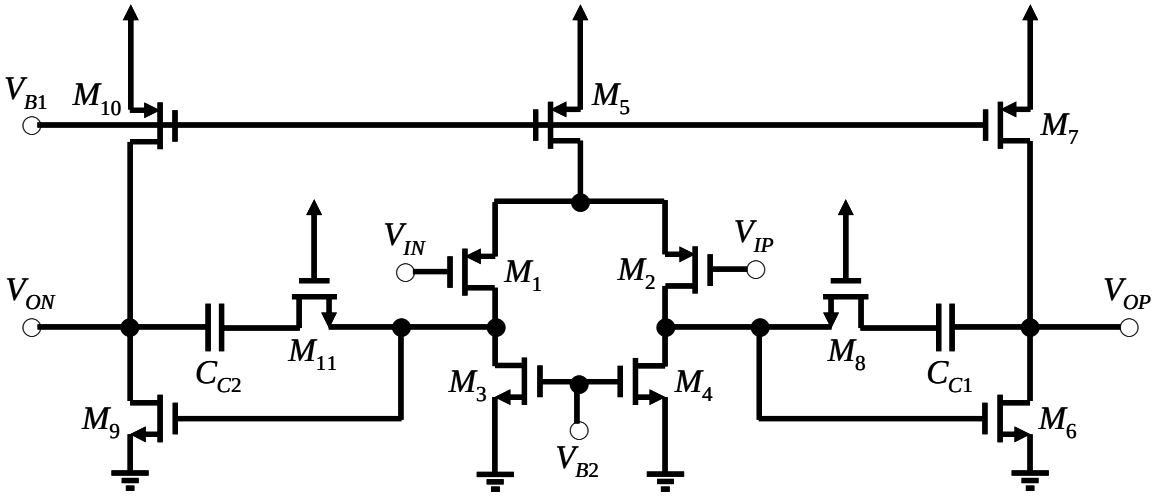
Symmetry constraint

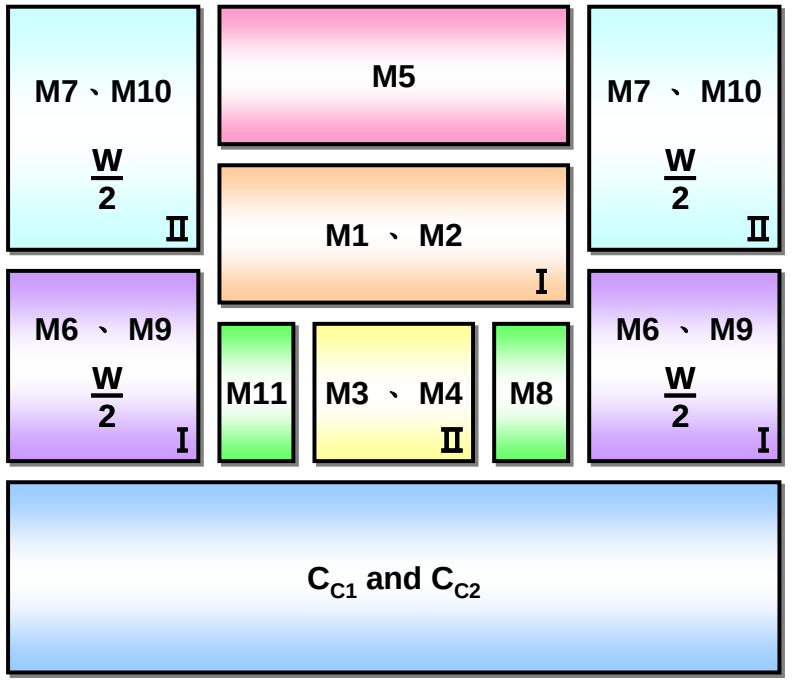


Proximity constraint

Analog Placement Approaches

- Constructive method
  - Generate placement according to schematic topology [Mehranfar, *JSSC*'91] or signal paths [Long et al., ASP-DAC'06]





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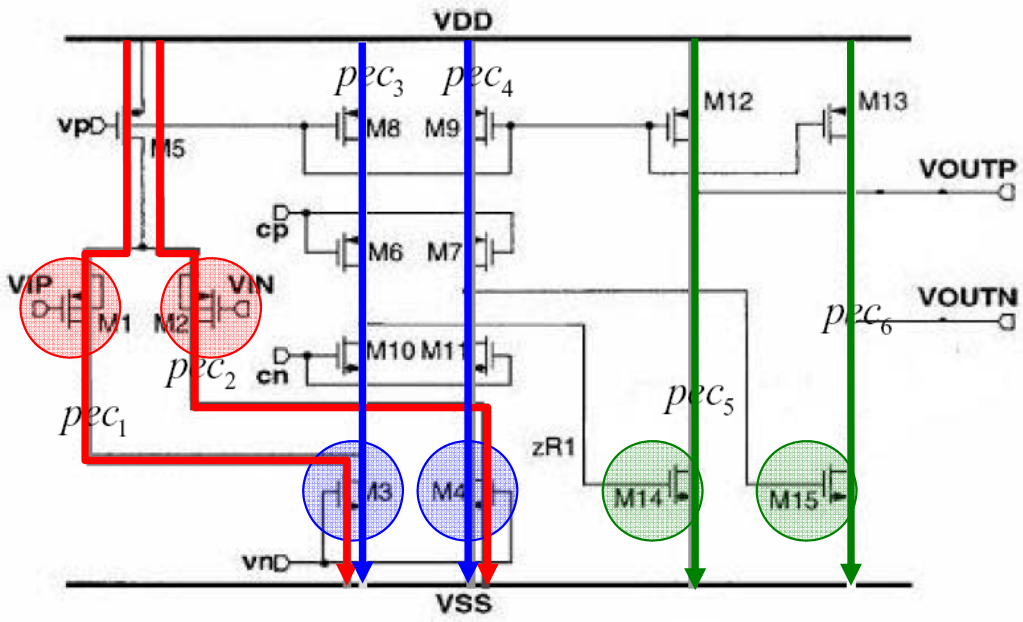
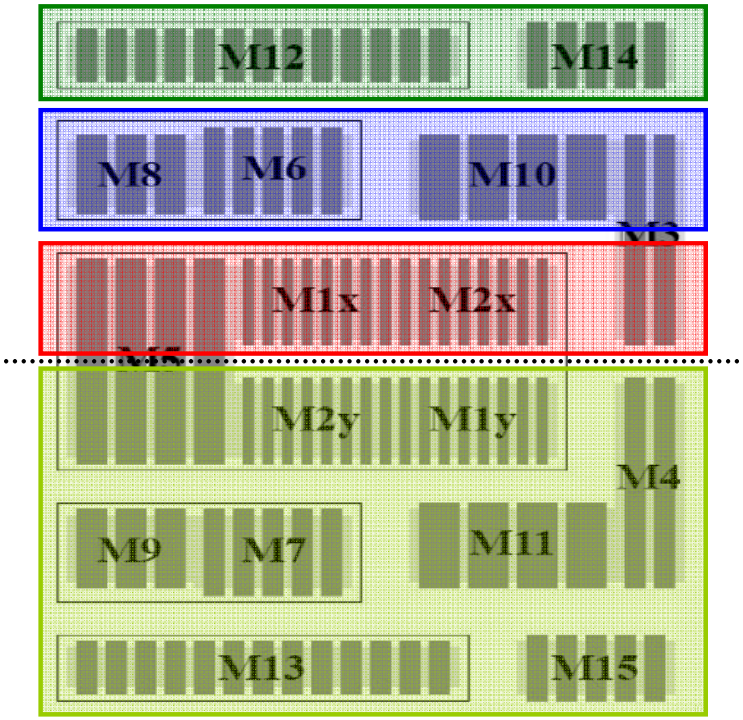
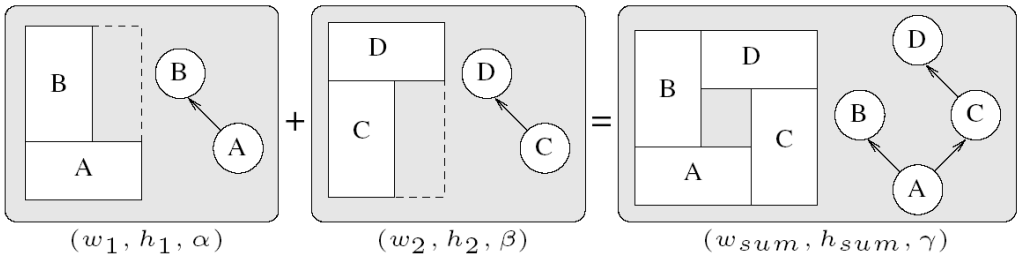
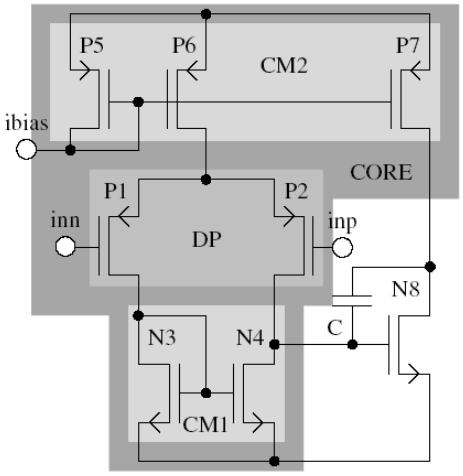


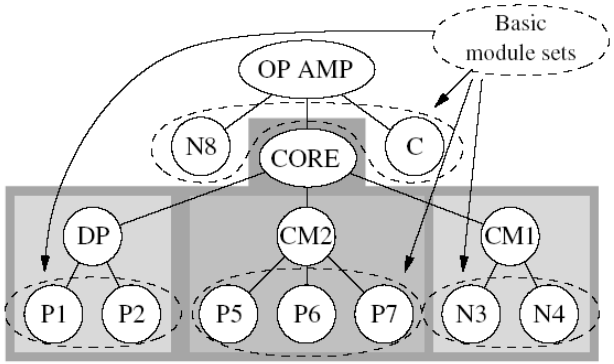


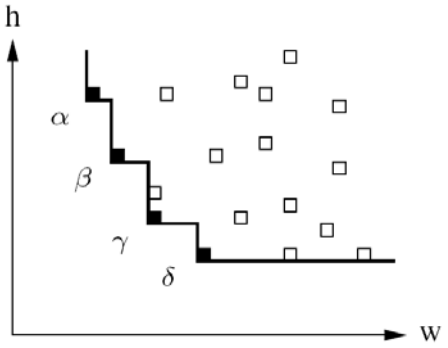
Analog Placement Approaches

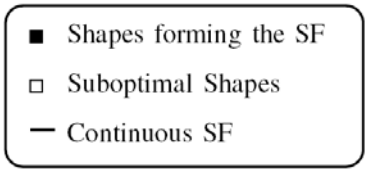
- Constructive method
  - Generate placement according to schematic topology [Mehranfar, *JSSC*'91] or signal paths [Long et al., ASP-DAC'06]
- Deterministic algorithm
  - Enumerate all possible placements for the basic module sets, and then combine these placements hierarchically [Strasser et al., ICCAD'08]











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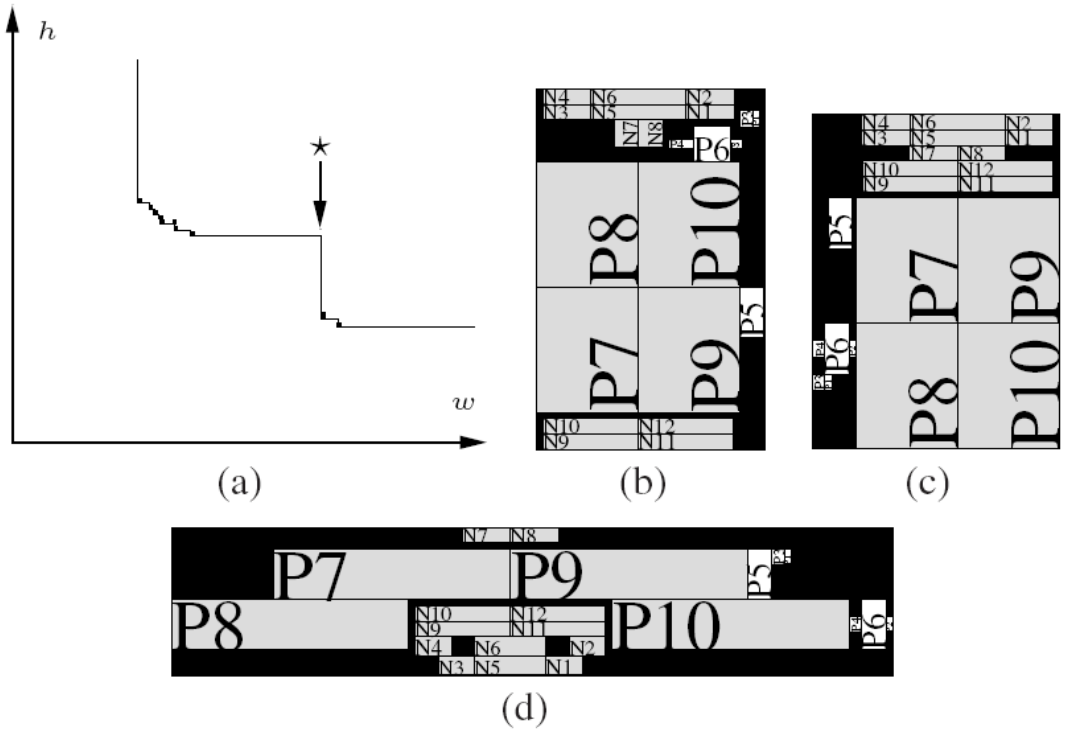

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- Statistical algorithm
  - Apply simulated annealing (SA) algorithm with floorplan representations

Representations for Analog Placement

- Topological representation is a popular method for modern VLSI design
  - Smaller solution space (compared with absolute representation)
  - Need specific techniques to deal with placement constraints
- Previous work of handling symmetry constraint
  - Sequence-pairs [Balasa & Lampaert, DAC'99]
  - O-trees [Pang et al., DAC'00]
  - Binary trees [Balasa, ICCAD'00]
  - TCG-S [Lin et al., ASP-DAC'05]
  - CBL [Liu et al., ASP-DAC'07]
- Previous work of tackling common-centroid constraint
  - C-CBL [Ma et al., ICCAD'07]
  - B*-trees [Strasser et al., ICCAD'08]
  - Sequence-pairs [Xiao & Young, ASP-DAC'09]

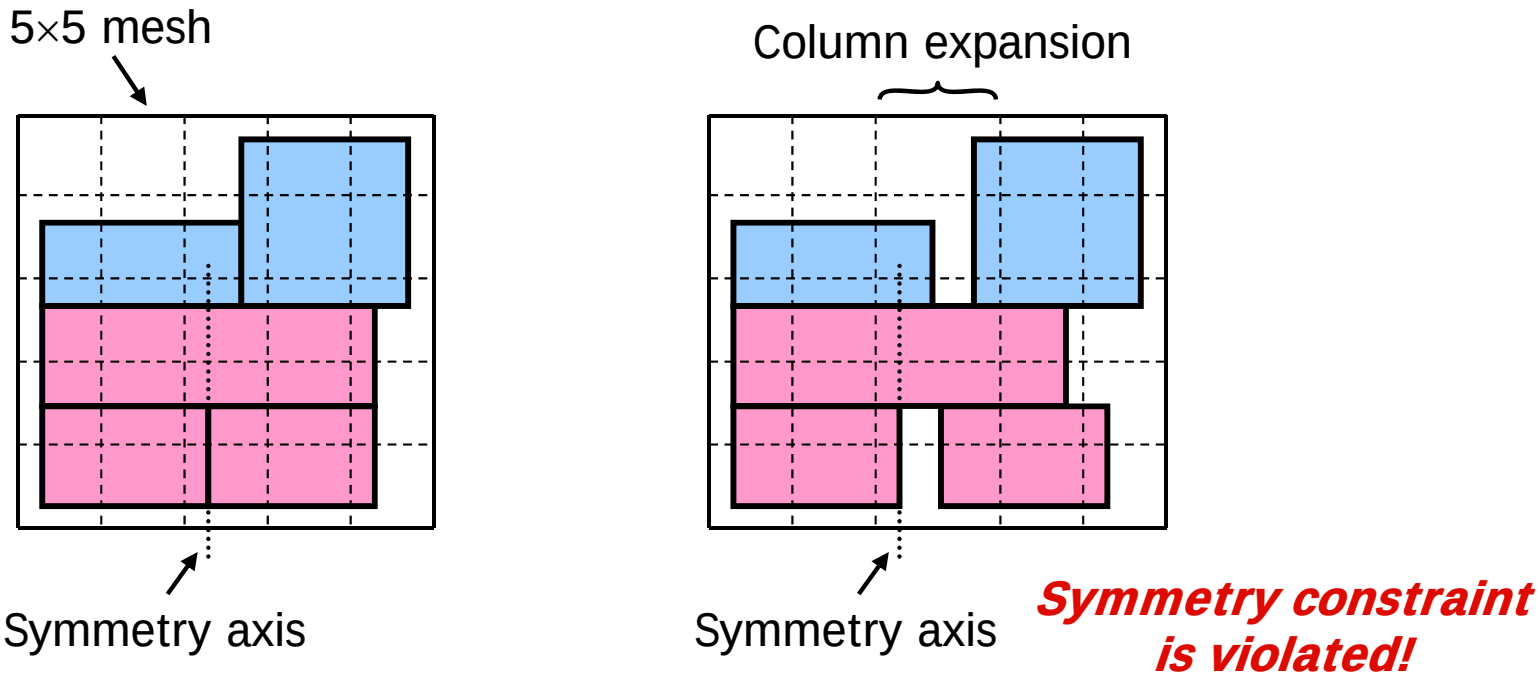
Routability-driven Analog Placement

- One of the objective function in SA algorithm is to minimize chip area, which makes blocks compact to the lower-left corner
- For analog design, a compact placement is not practical
- Routing over the active areas of analog devices is usually avoided to reduce parasitics and cross-talk effects
- Reserve enough spaces between the devices for laying out wires

Review of Congestion-aware Placement

- Congestion-aware placement for analog circuits [Xiao et al., ICCAD'10]
  - Whole placement region is divided into an $n \times n$ mesh, and vertical and horizontal congestions are estimated for each room
  - Rooms are expanded column-by-column and row-by-row based on the congestion map

Symmetry constraint must be satisfied after placement expansion



Problem Formulation

- Given a set of devices and topological placement constraints
  - The active areas of all devices are considered as routing blockages
  - Routing congestion in the resulting placement *P* is minimized
  - All topological constraints are satisfied in the resulting placement *P*
  - Cost function $\Phi(P)$:

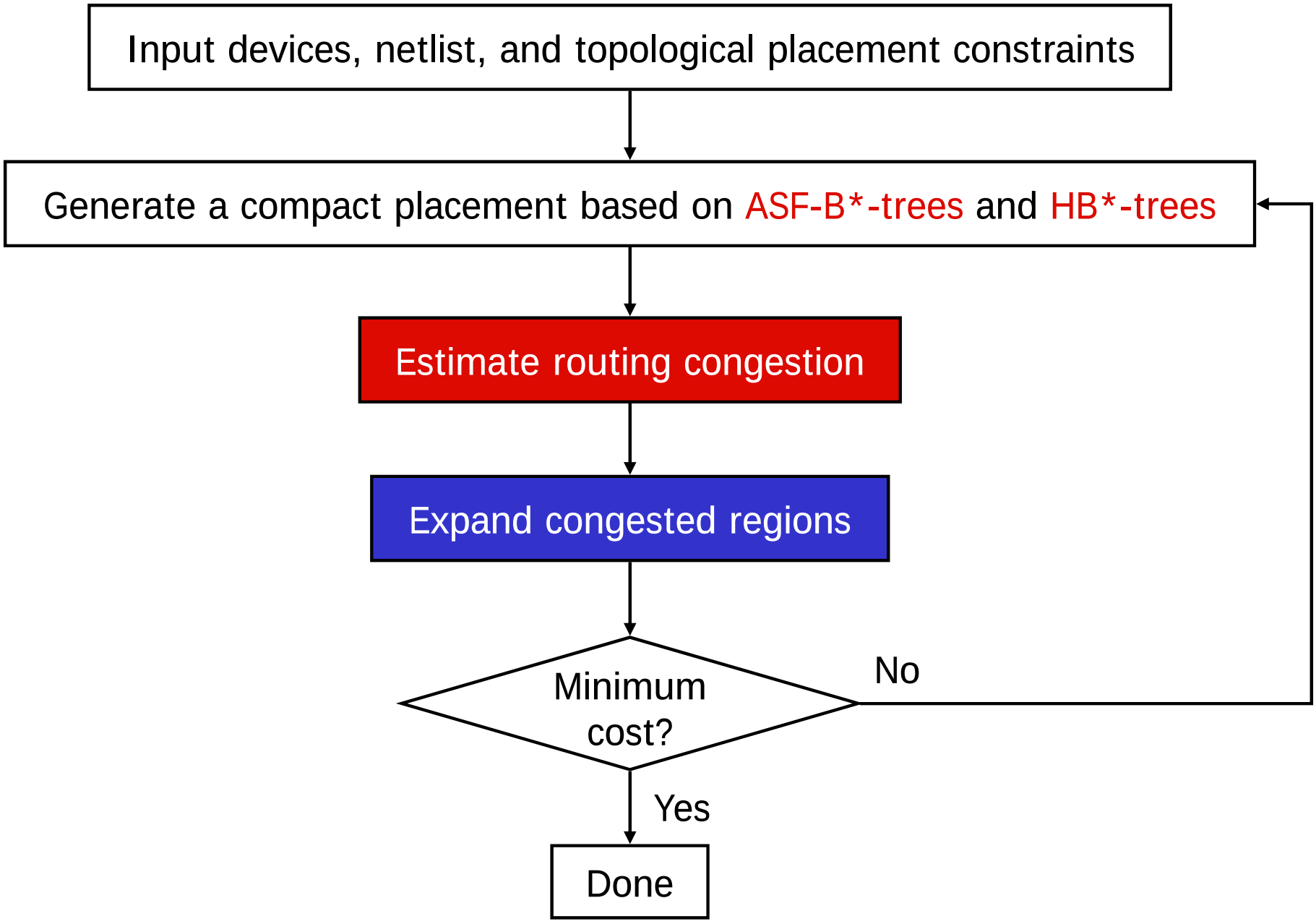
$$\Phi(P) = \alpha \times A_P + \beta \times W_P + \gamma \times C_P$$

A_P: bounding-rectangle area of the placement

W_P: total wire length measured by half-perimeter estimation

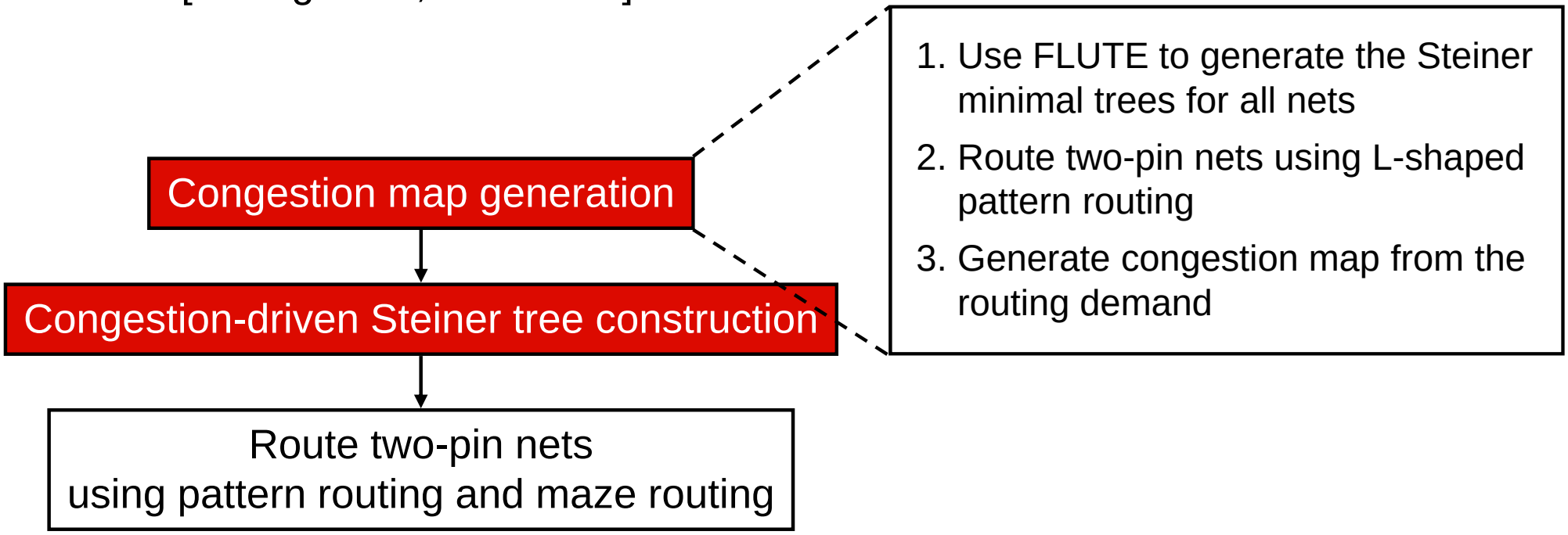
C_P: estimation of routing congestion

Overview of Our Placement Flow



Congestion Estimation

- The way to predict congestion accurately is to use the same technique and parameters in both congestion estimation and global routing [Pan & Chu, ICCAD'06]
  - Congestion-driven Steiner tree construction can be used for congestion estimation and global routing
  - Previous work: FastRoute [Pan & Chu, ICCAD'06], NTHU-Route [Chang et al., ICCAD'08]



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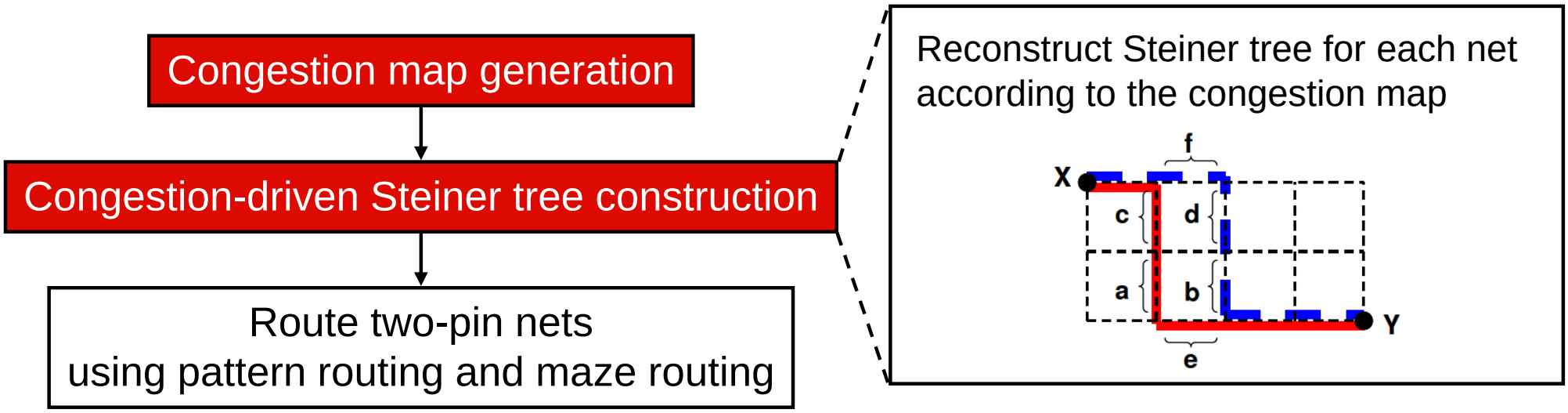

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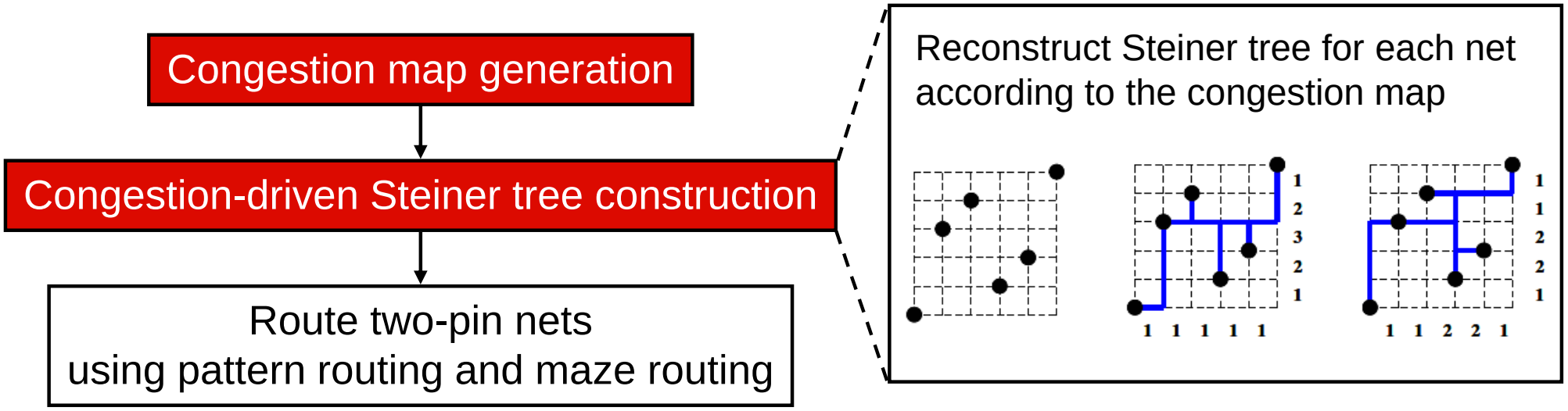

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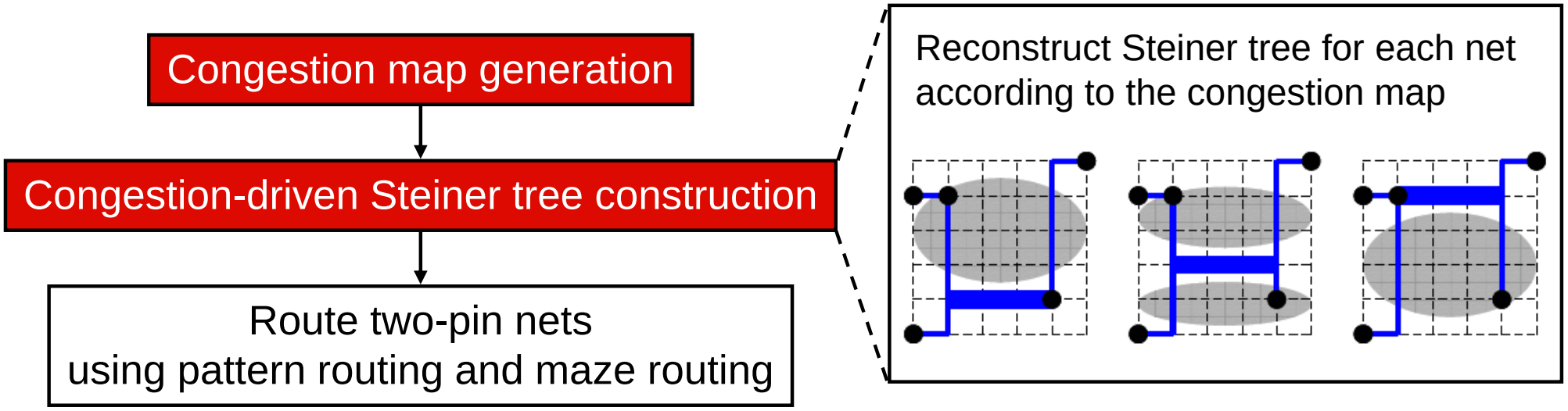

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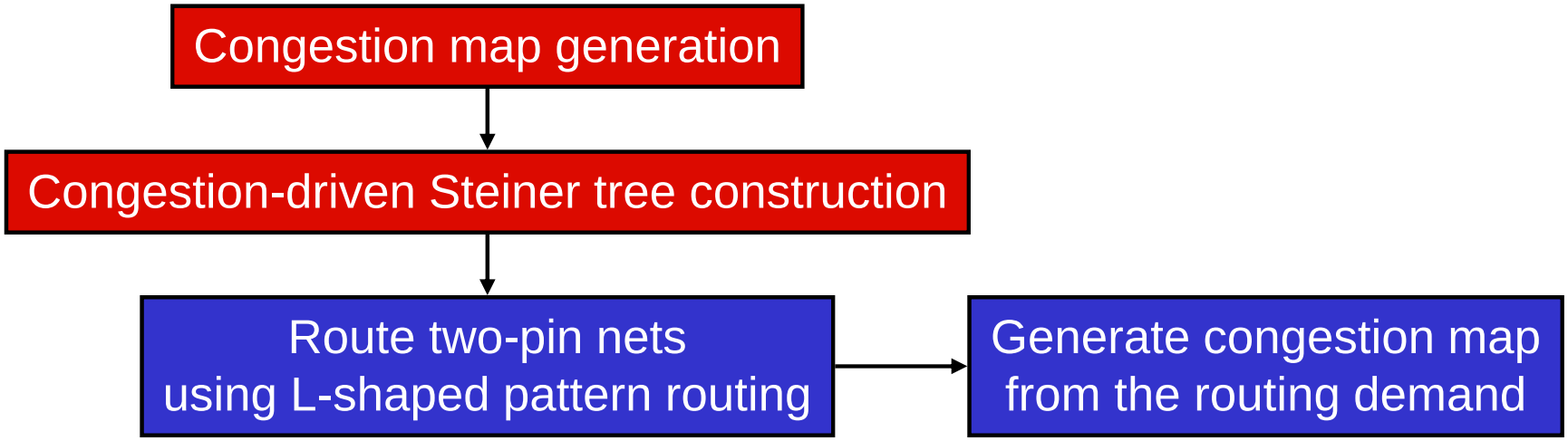
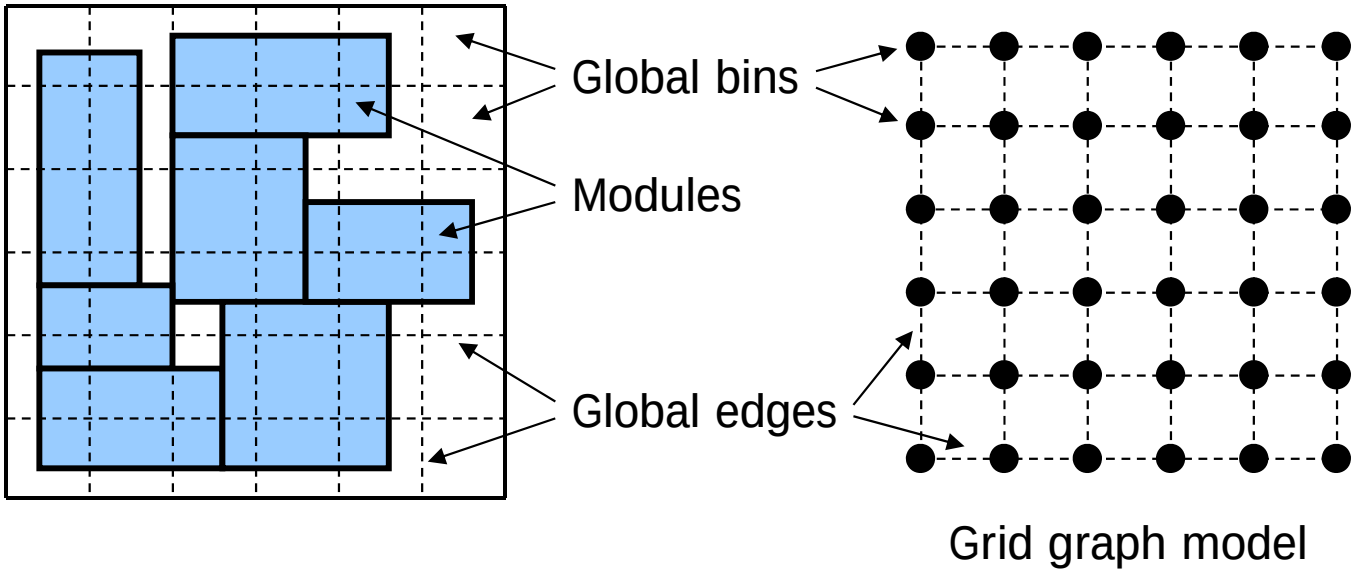
- Proposed congestion map generation:



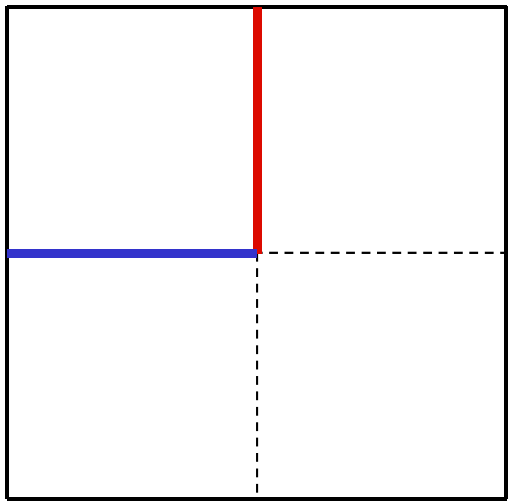
Congestion Map Generation with Analog Devices

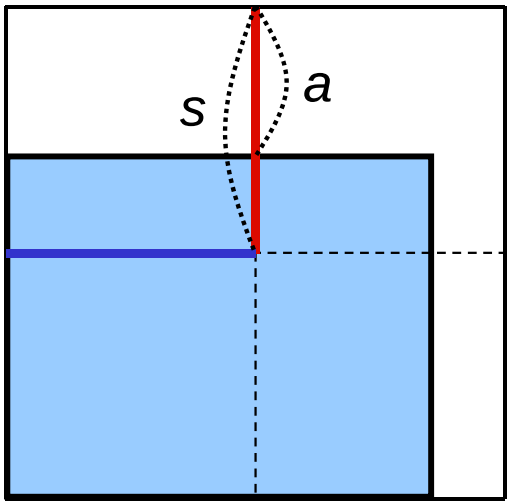
- Grid graph model for global routing:

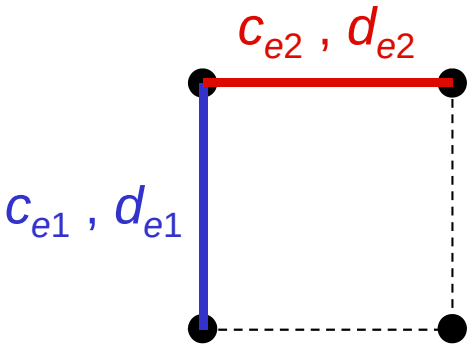


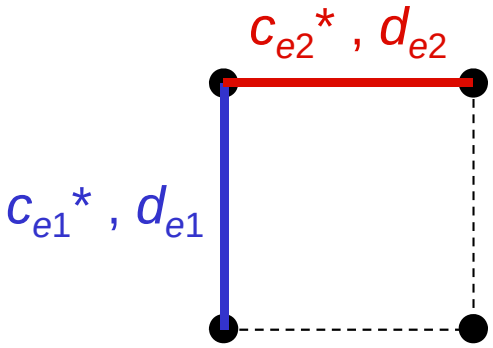
- Since the active areas of all devices are considered as routing blockages, we reduce global edge capacities of a bin if the bin is occupied by some devices

Congestion Map Generation with Analog Devices









Edge capacity: c_e

Routing demand: d_e

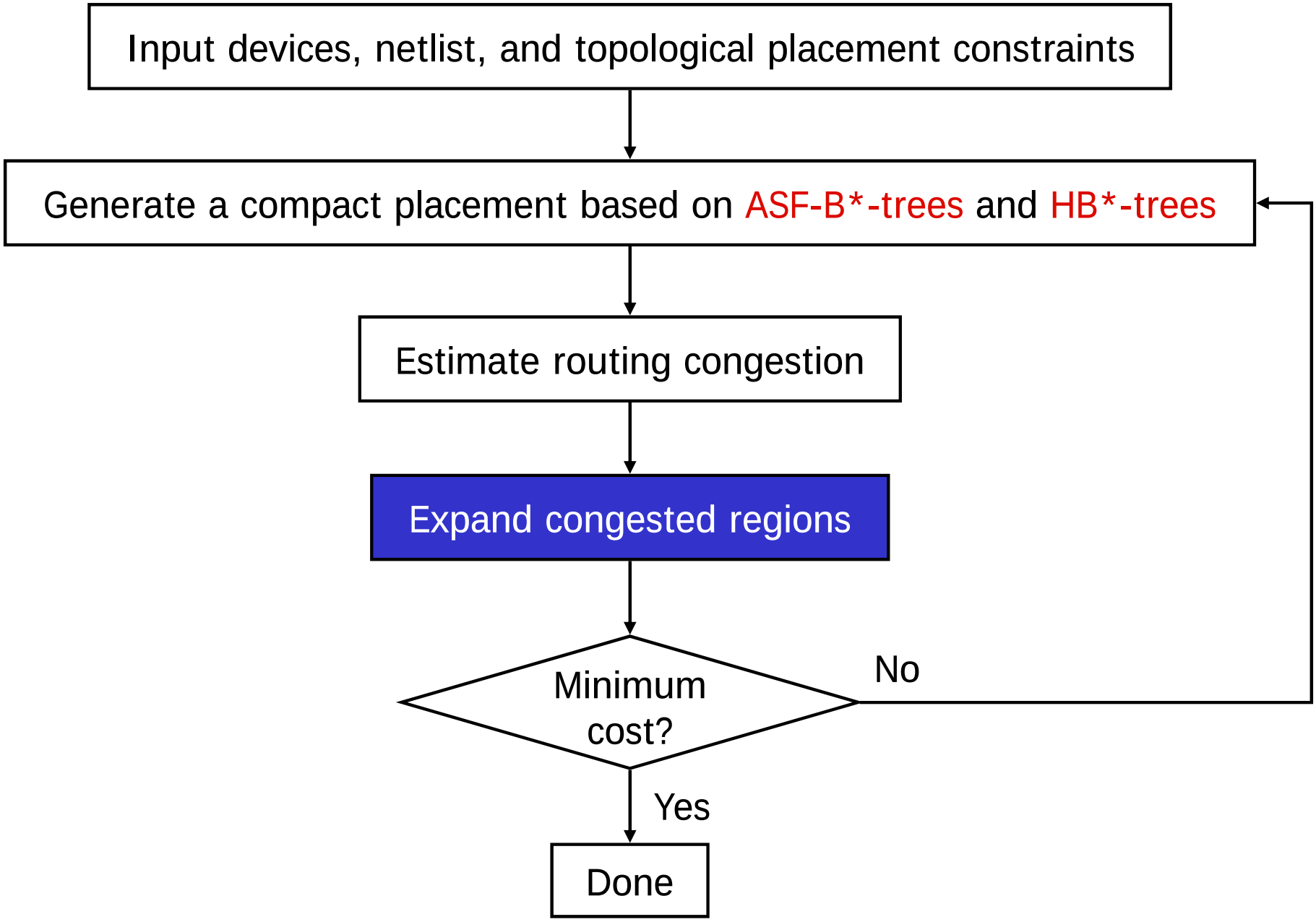
$c_{e1}^* = 0$

$c_{e2}^* = c_{e2} \times \frac{a}{s}$

if $d_e > c_e^*$, $overflow_e = d_e - c_e^*$

otherwise $overflow_e = 0$

Overview of Our Placement Flow

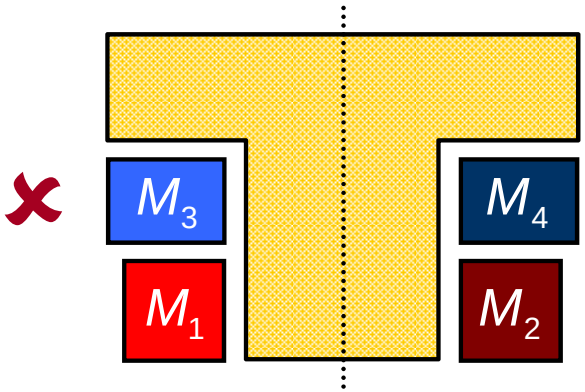


Placement Expansion

- To eliminate routing overflow, we slightly expand congested regions of a compact placement
  - Placement expansion for non-symmetry modules
  - Placement expansion for symmetry groups
- Dummy nodes are inserted into ASF-B*-trees or HB*-trees for placement expansion

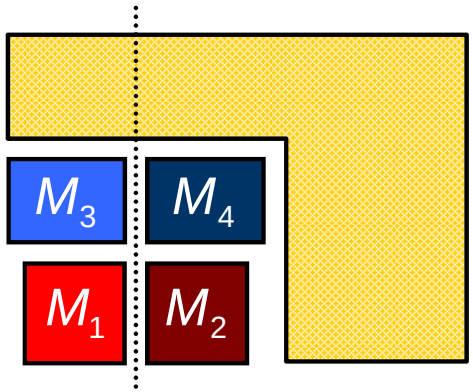
Review of ASF-B*-tree

- Concept of symmetry islands [Lin & Lin, DAC'07]
  - Matching devices should be placed at proximity to reduce mismatch [Pelgrom et al., *JSSC*'89]
  - Each module should abut at least one of the other modules in the same symmetry group
  - A symmetry island defines a symmetric placement, in which devices form a connected placement



Symmetry group:

$S = \{(M_1, M_2), (M_3, M_4)\}$



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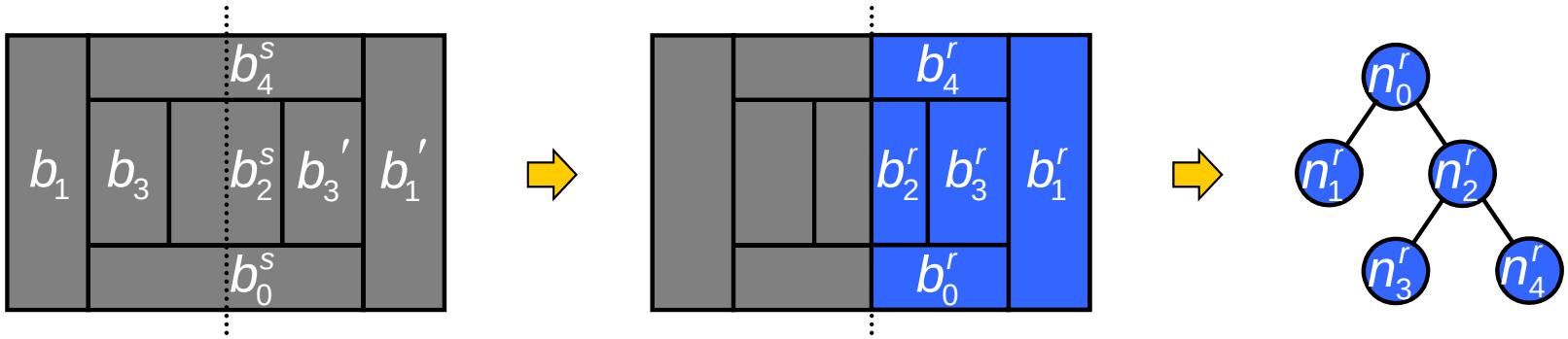
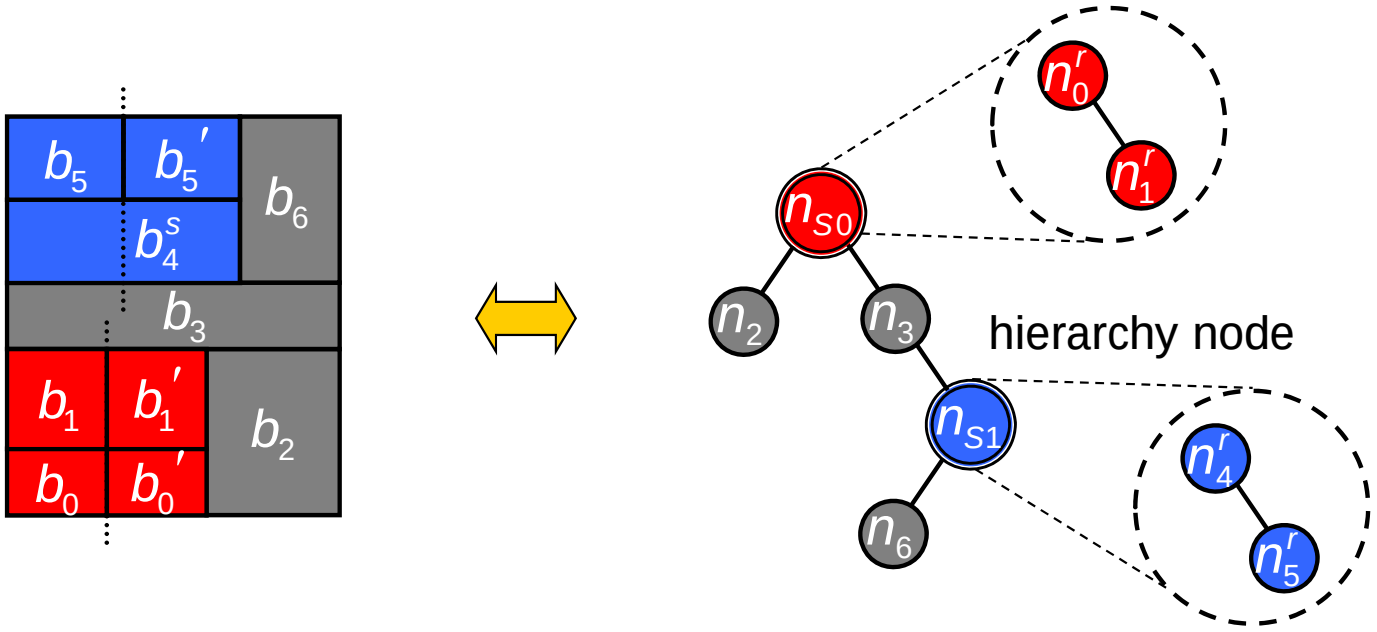
  - A symmetry island defines a symmetric placement, in which devices form a connected placement
- Automatically symmetric-feasible B*-tree (ASF-B*-tree) is used to represent a symmetry island

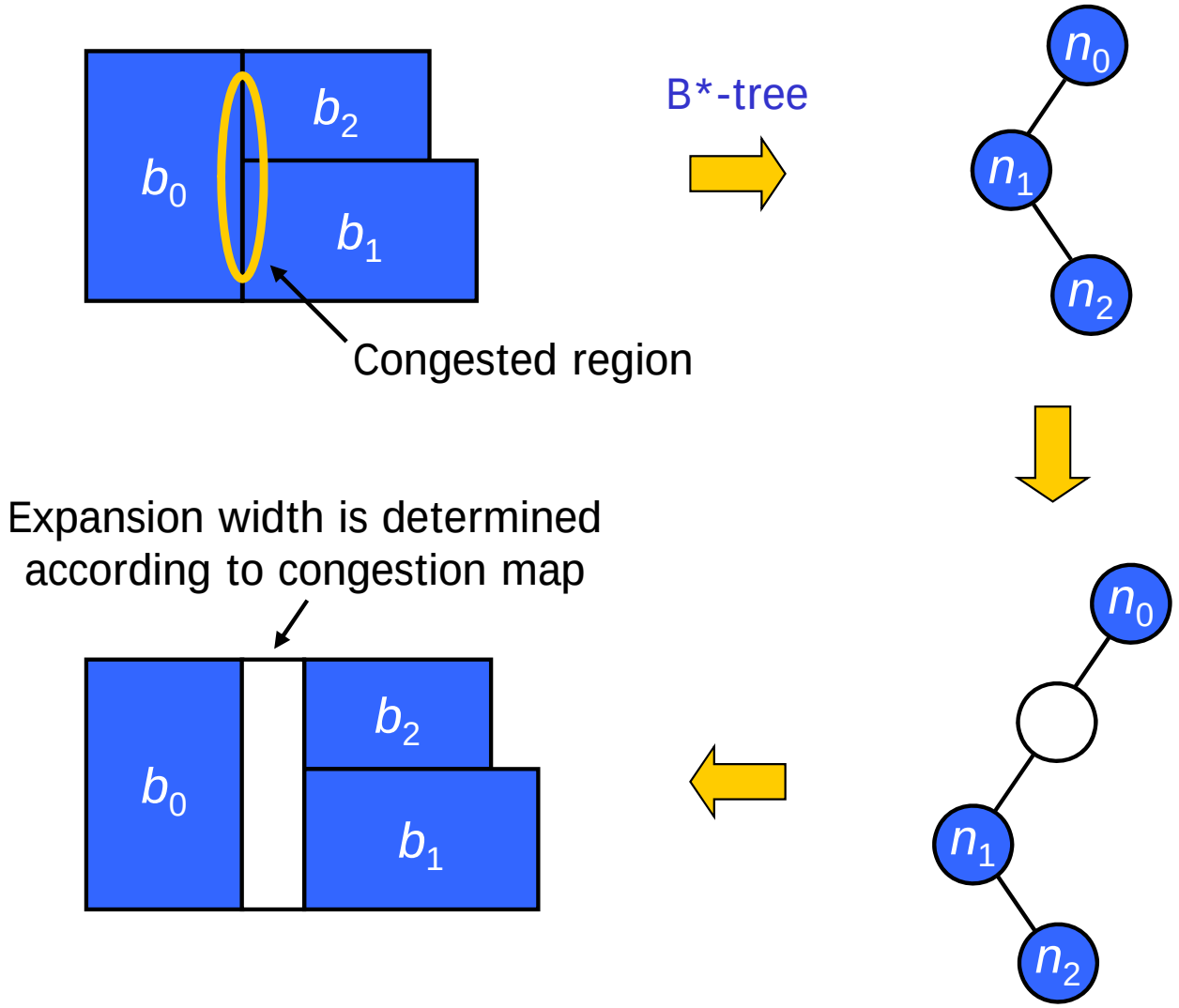


Review of HB*-tree

- Hierarchical B*-tree (HB*-tree) deals with the placement of symmetry islands and non-symmetry modules
- Hierarchy nodes can handle the groups which require matching, symmetry, and proximity constraints



Placement Expansion for Non-symmetry Modules



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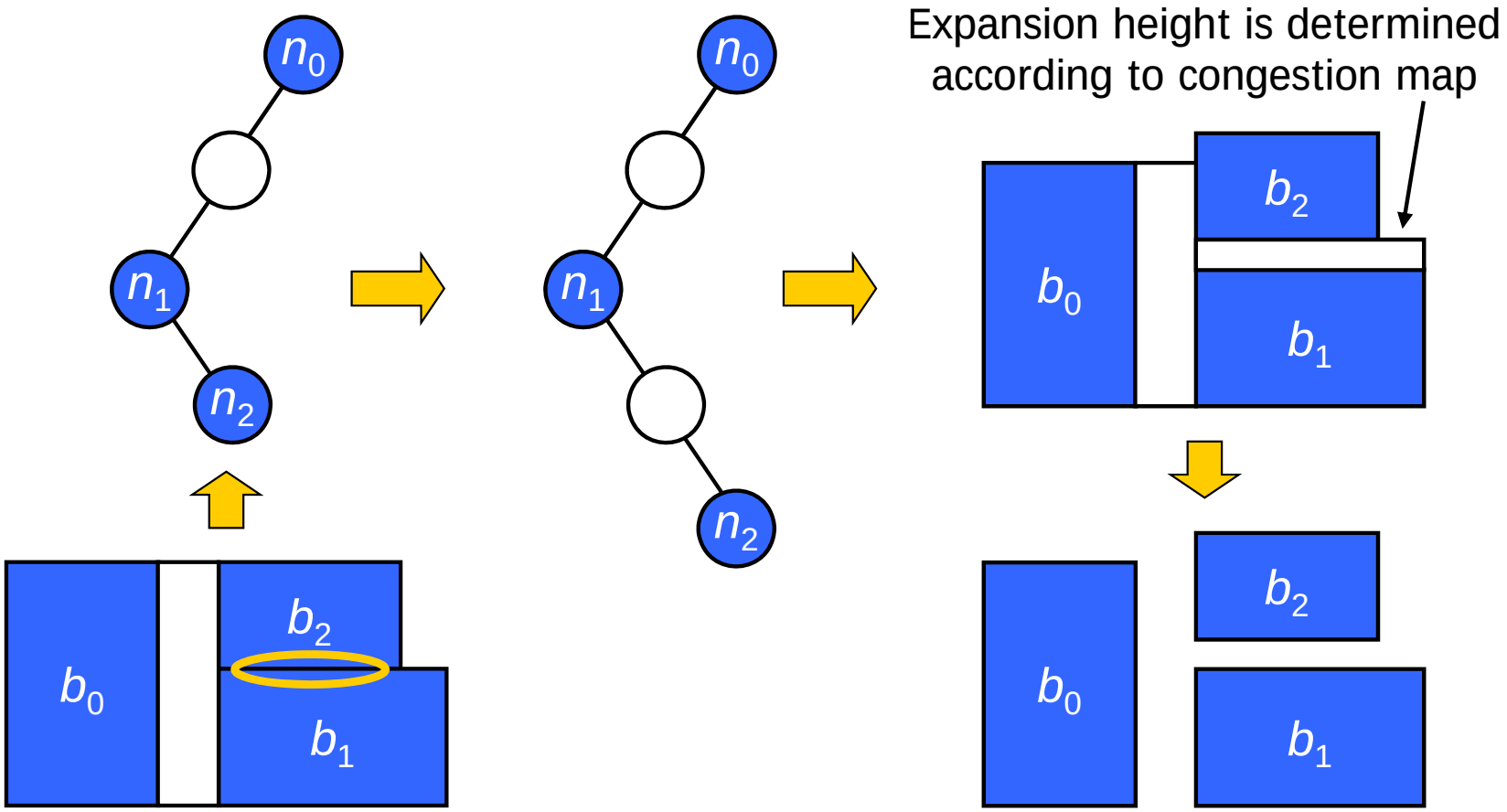

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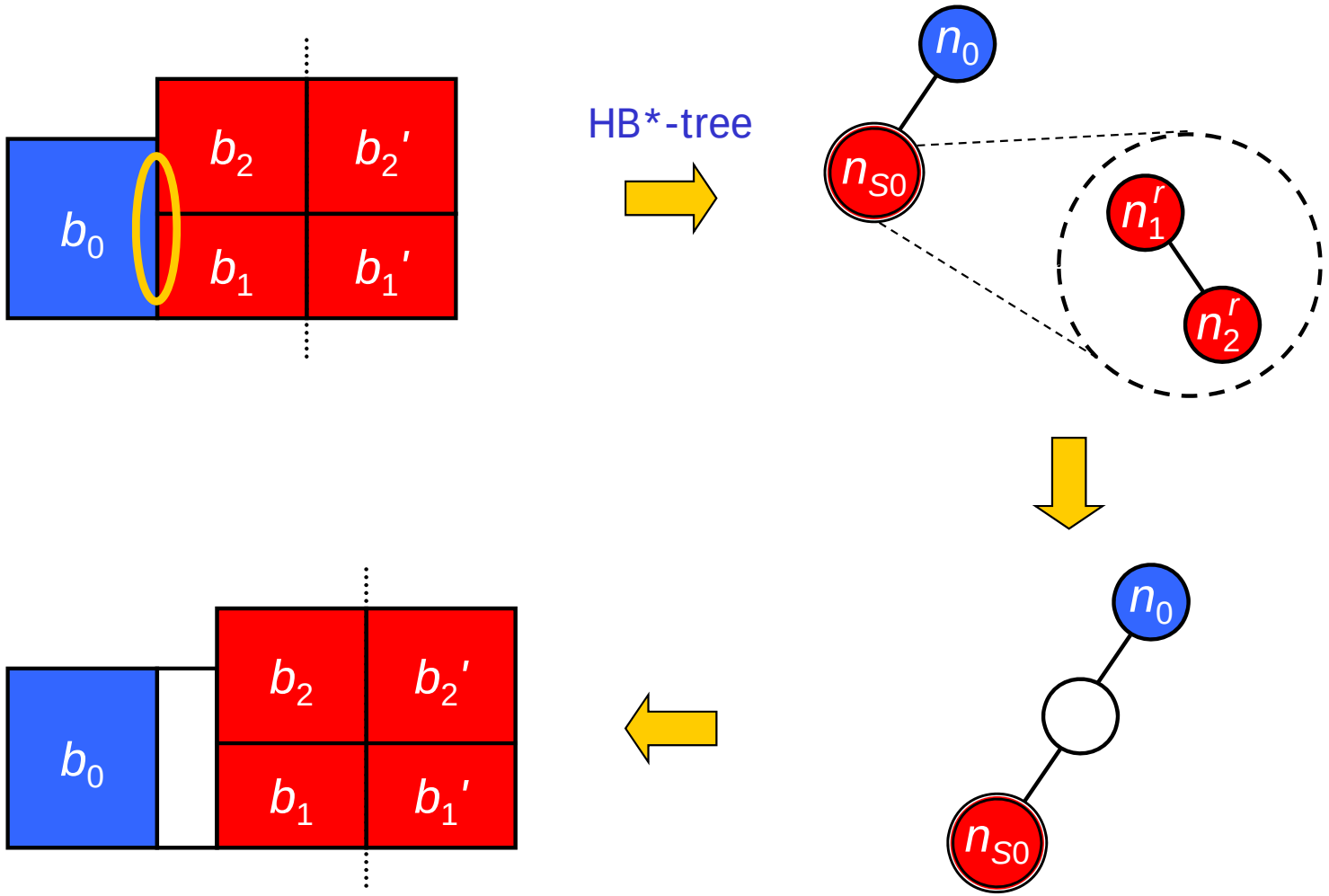
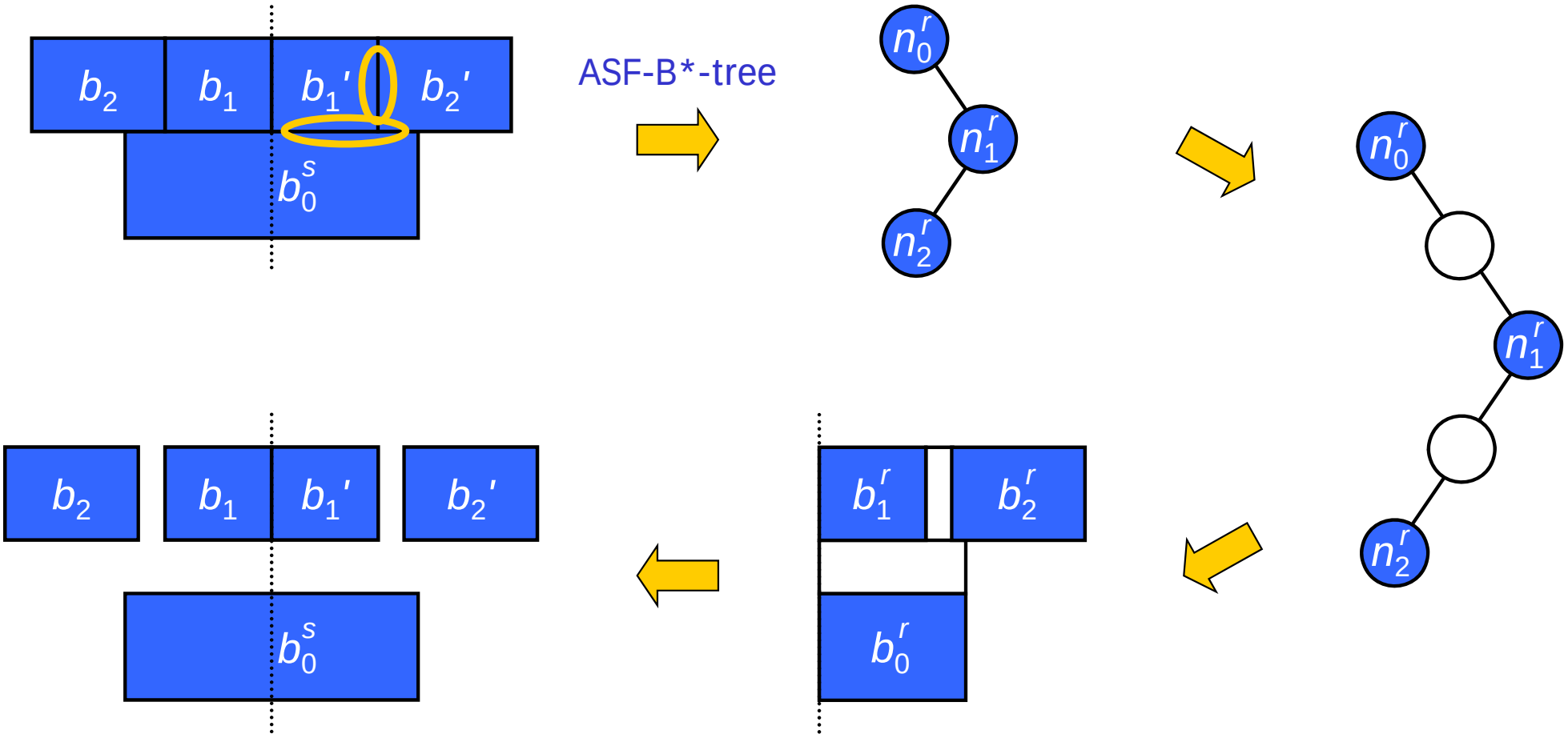
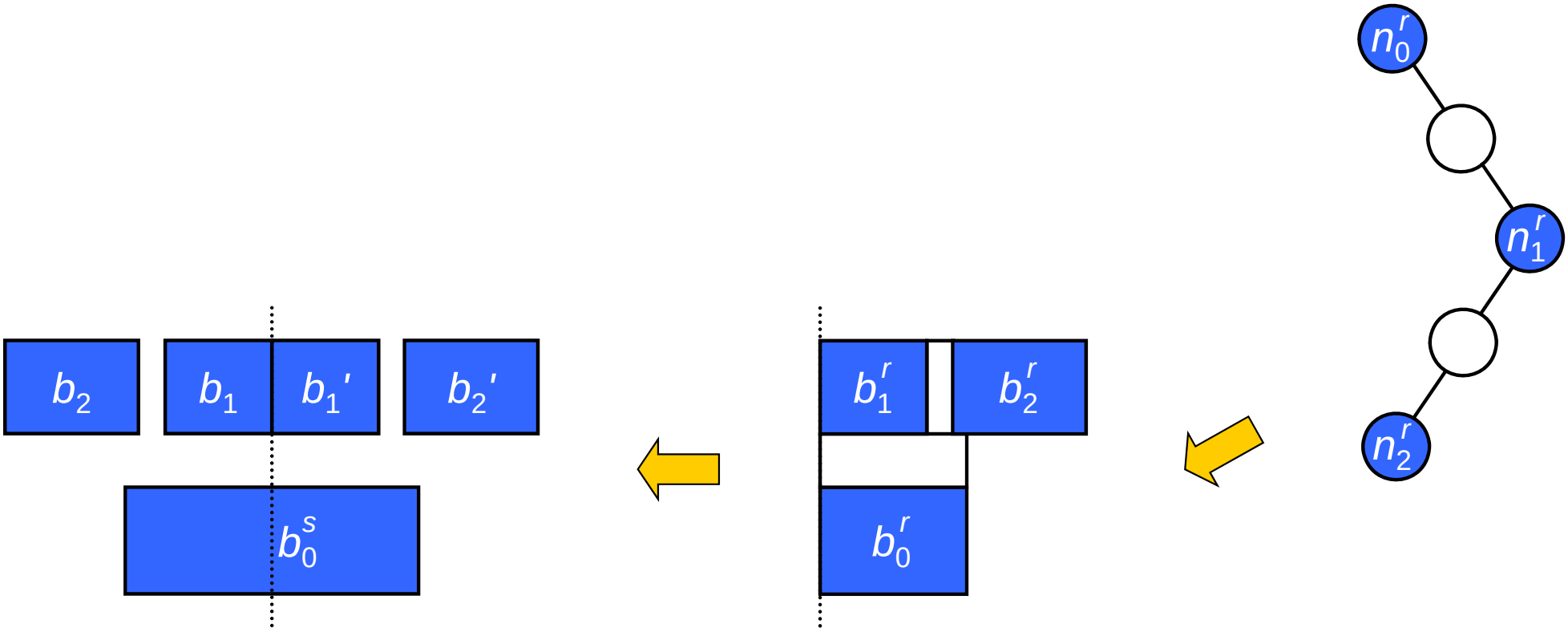


Placement Expansion for Symmetry Groups



Placement Expansion for Symmetry Groups

- ASF-B*-trees guarantee that each symmetry group remains symmetric after placement expansion



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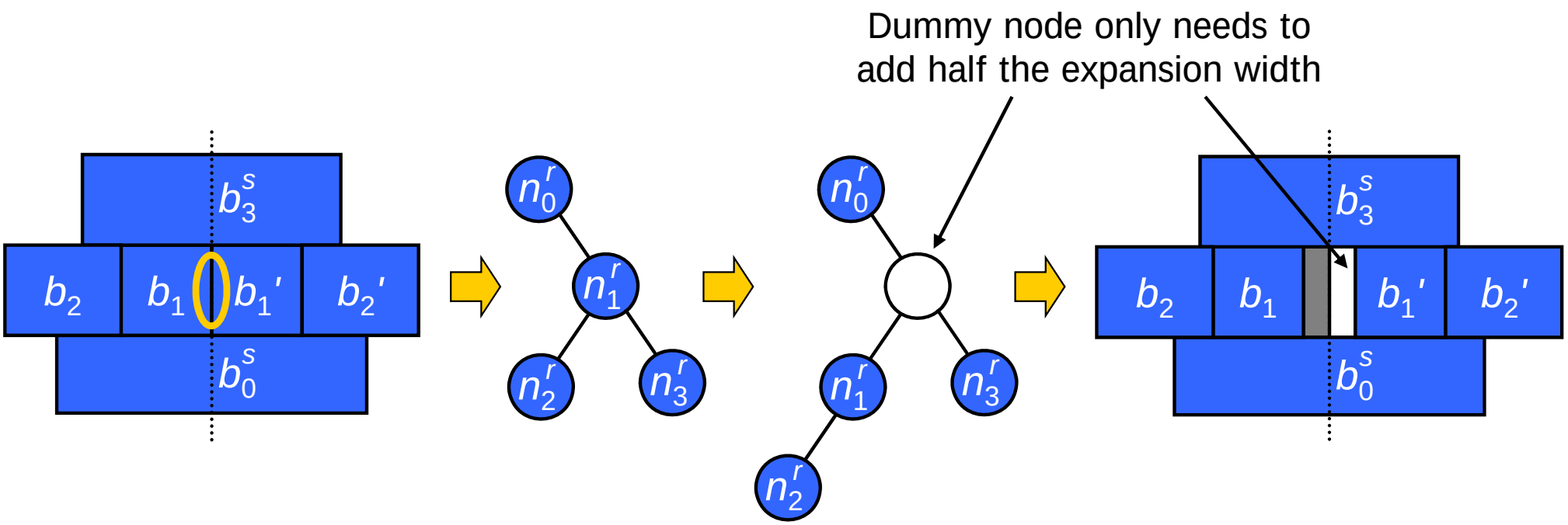

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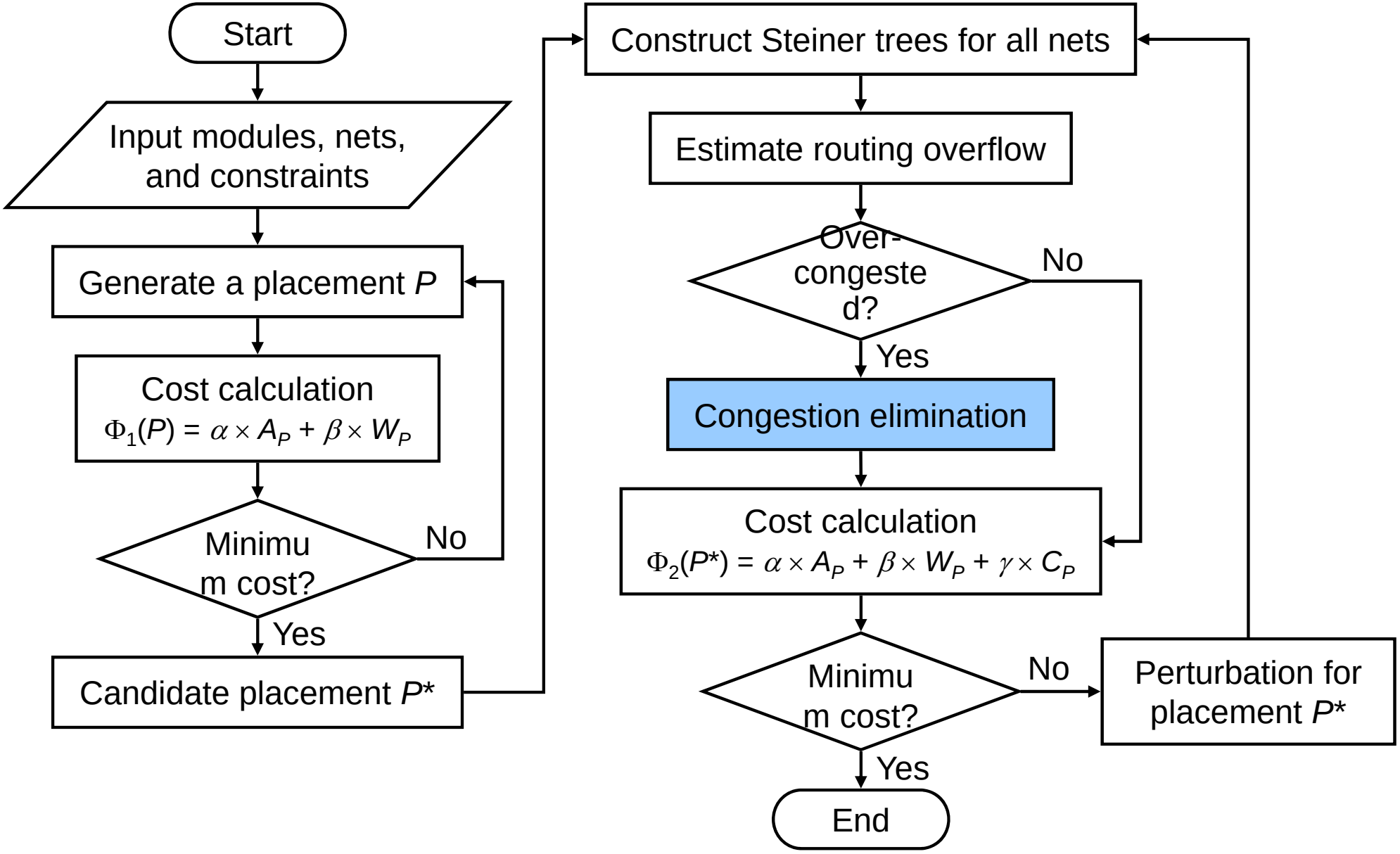

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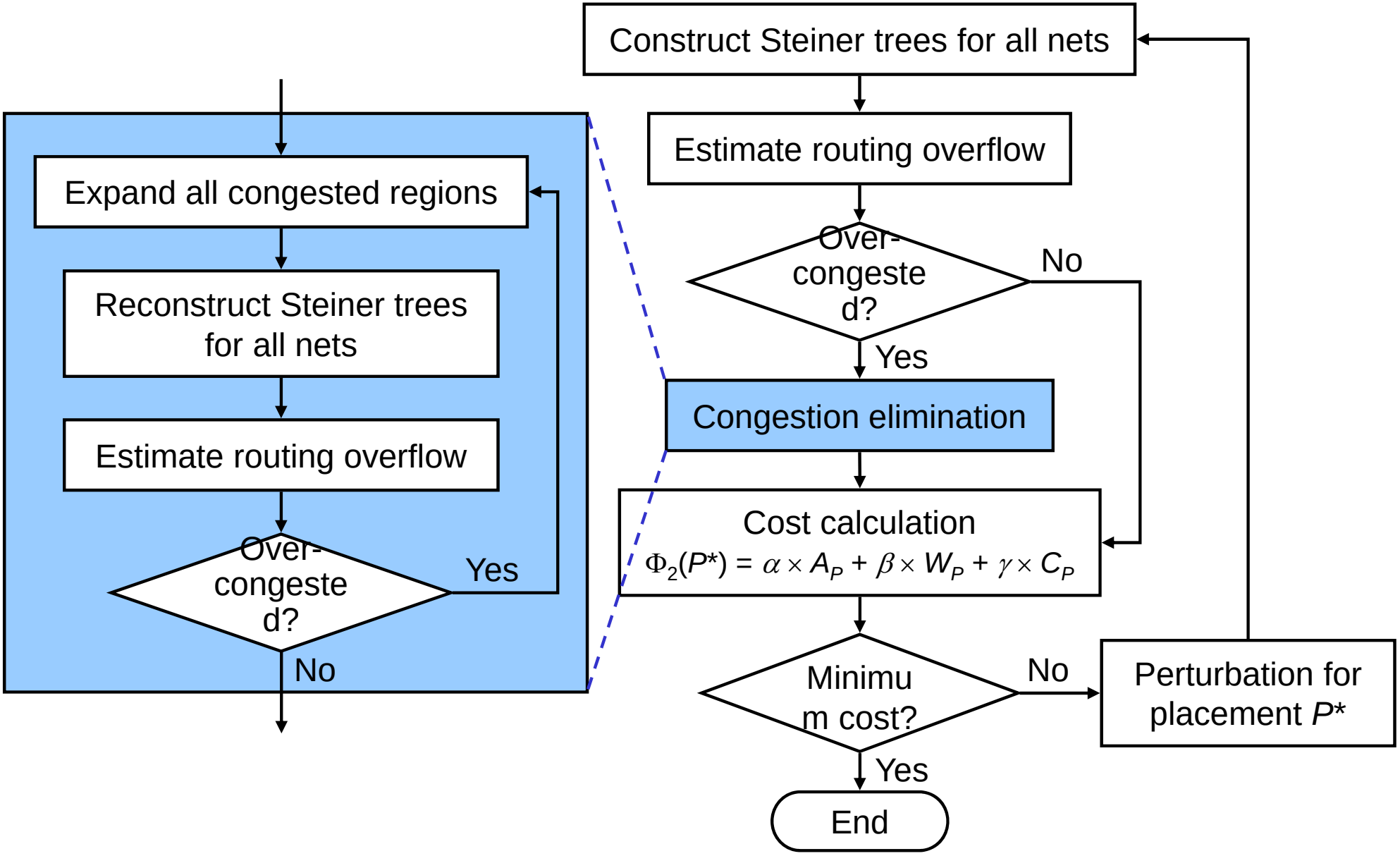


Experimental Results

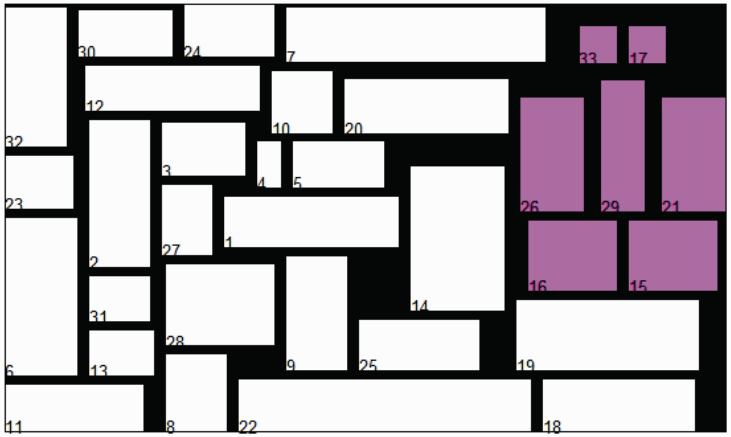
- Platform: 2.5GHz SUN Fire-X4250 workstation with 16GB RAM
- Benchmark: two MCNC benchmark circuits

Circuit	# of mod.	# of sym. mod.	Mod. area (mm^2)
ami33	33	7 (2+2+2+1)	1.16 = 100%
ami49	49	5 (2+2+1)	35.45 = 100%

Experimental Results

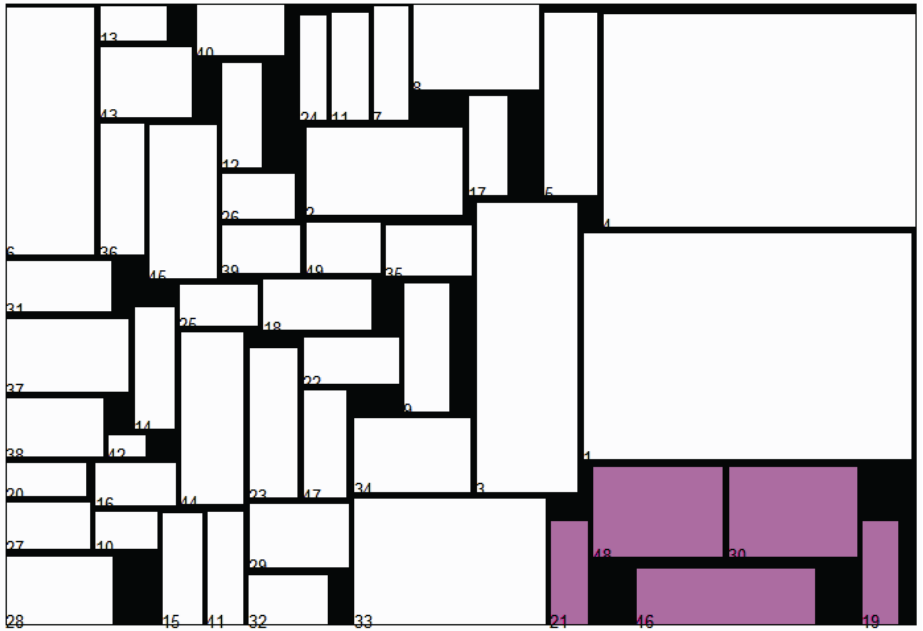
- Platform: 2.5GHz SUN Fire-X4250 workstation with 16GB RAM
- Benchmark: two MCNC benchmark circuits

Circuit	Without placement expansion				With placement expansion			
	Area (%)	HPWL (*mm*)	# of overflow	Time (sec.)	Area (%)	HPWL (*mm*)	# of overflow	Time (sec.)
ami33	107.11	37.38	154	103	113.25	47.73	0	556
ami49	108.44	569.25	253	206	115.32	677.24	0	1337



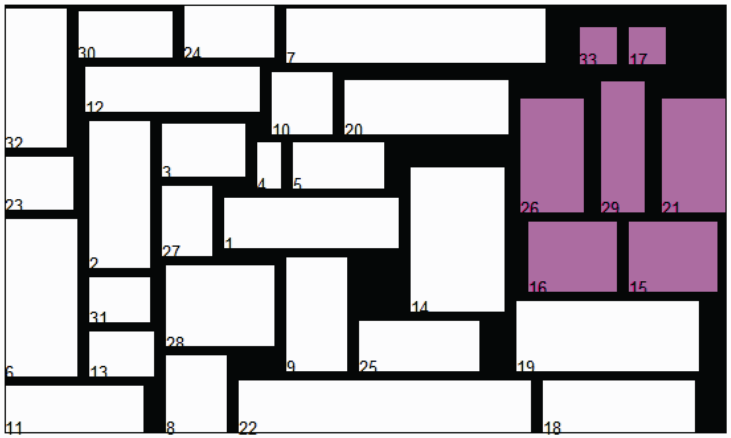
ami33

ami49



Experimental Results

- Platform: 2.5GHz SUN Fire-X4250 workstation with 16GB RAM
- Benchmark: two MCNC benchmark circuits
- Symmetry property is maintained after placement expansion



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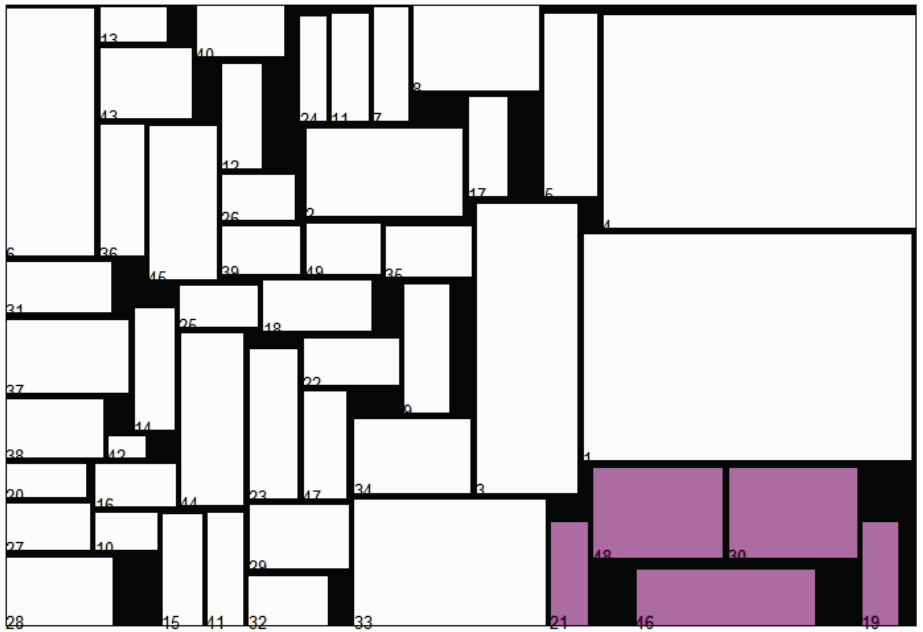

Conclusion

- Analog placement considering routability was introduced
  - The active areas of all devices are considered as routing blockages
  - Routing congestion in the resulting placement is minimized
  - Symmetry constraint must be satisfied after placement expansion
- ASF-B*-trees were used for maintaining the symmetry property after placement expansion
- Future work
  - Consider symmetric routing during the congestion estimation

Questions or Comments

Thank you!