Transforming Ad Hoc EDA to Algorithmic EDA

Jason Cong

Chancellor's Professor, UCLA

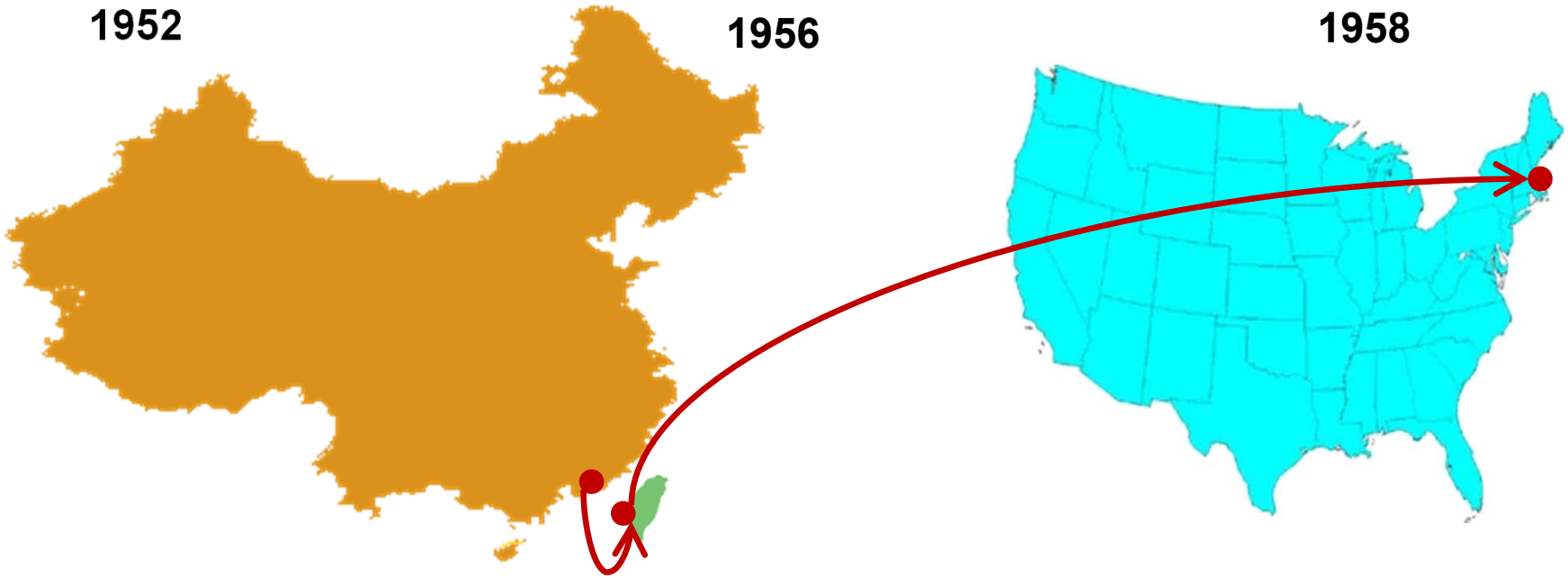
Director, Center for Domain-Specific Computing

The Early Years

蔡高中學
Choikou Middle School
Macau
1952

成功大學
National Cheng Kung University
Taiwan
1956

麻省理工學院
MIT
USA
1958



Graduate Study at MIT (1958 – 1963)

- MS thesis: A Study in Machine-Aided Learning
  - A pioneer work in distant learning
- Advisor: Ronald Howard

A STUDY IN MACHINE-AIDED LEARNING

by

Chung Laung Liu

Submitted to the Department of Electrical Engineering on May 21, 1960 in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

The conventional teaching machines are studied. The advantages and the possibility of using a computer as a teaching machine are investigated. A program using an IBM 704 computer to teach arithmetic and a program using an IBM 704 computer to teach matrix algebra are suggested.

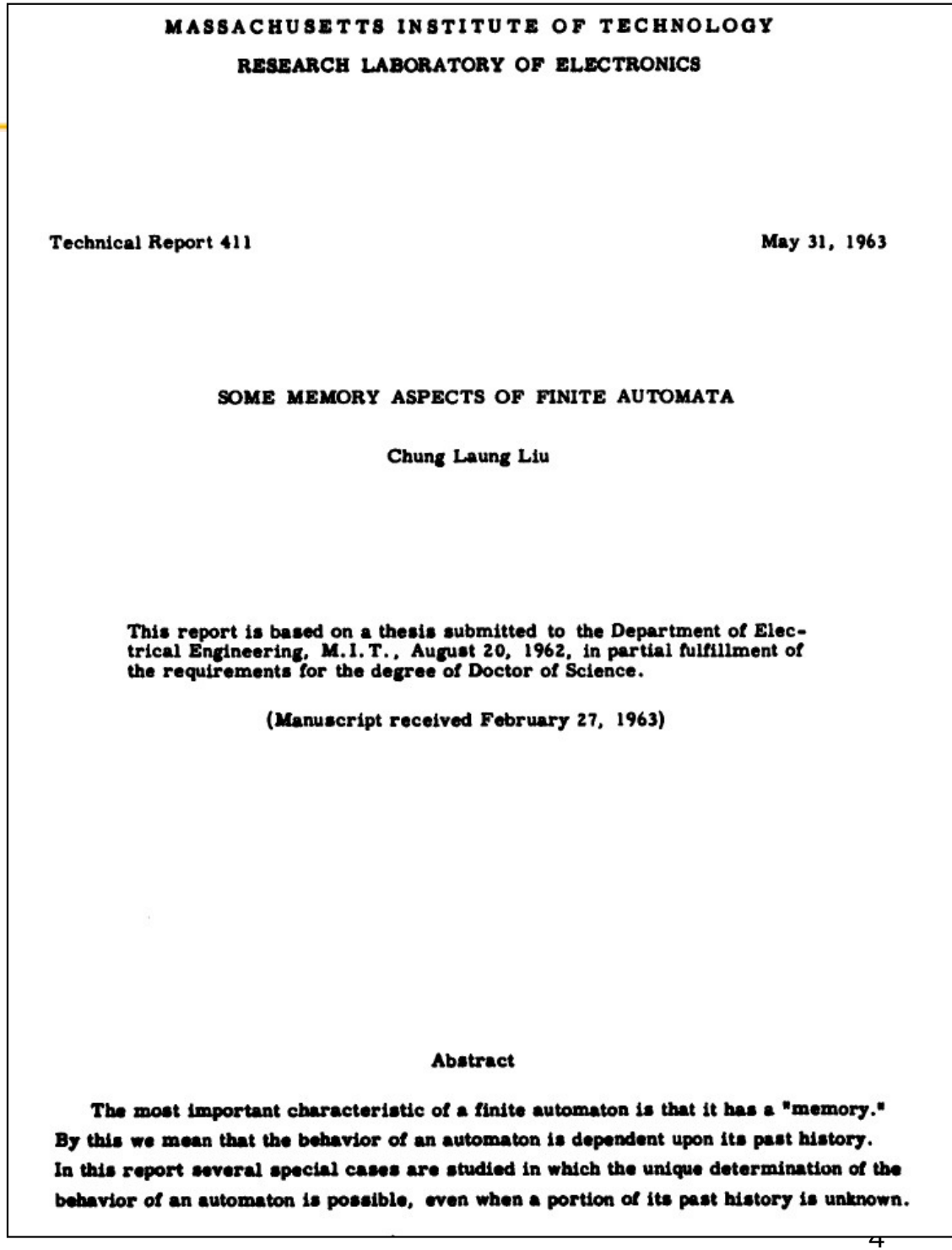
Thesis Supervisor: Ronald A. Howard

Title: Assistant Professor of Electrical Engineering

Graduate Study at MIT

- PhD thesis: “Some Memory Aspects of Finite Automata” (1963)

- Advisor: Dean Arden
  - Professor of EE, MIT, 1956-1964
  - Involved with Whirlwind Project
  - Also PhD advisor of Jack Dennis
    - Jack was PhD advisor of Randy Bryant -- another Phil Kaufman Award Recipient (2009)



MASSACHUSETTS INSTITUTE OF TECHNOLOGY

RESEARCH LABORATORY OF ELECTRONICS

Technical Report 411 May 31, 1963

SOME MEMORY ASPECTS OF FINITE AUTOMATA

Chung Laung Liu

This report is based on a thesis submitted to the Department of Electrical Engineering, M.I.T., August 20, 1962, in partial fulfillment of the requirements for the degree of Doctor of Science.

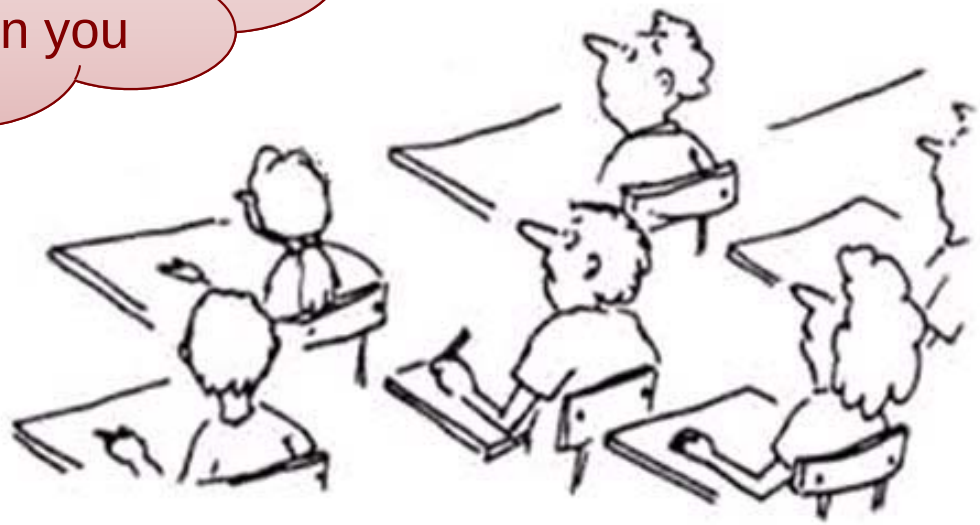
(Manuscript received February 27, 1963)

Abstract

The most important characteristic of a finite automaton is that it has a "memory." By this we mean that the behavior of an automaton is dependent upon its past history. In this report several special cases are studied in which the unique determination of the behavior of an automaton is possible, even when a portion of its past history is unknown.

Side Story: Dean Arden's Visit to UIUC in 1992

I am glad that I have better students than you



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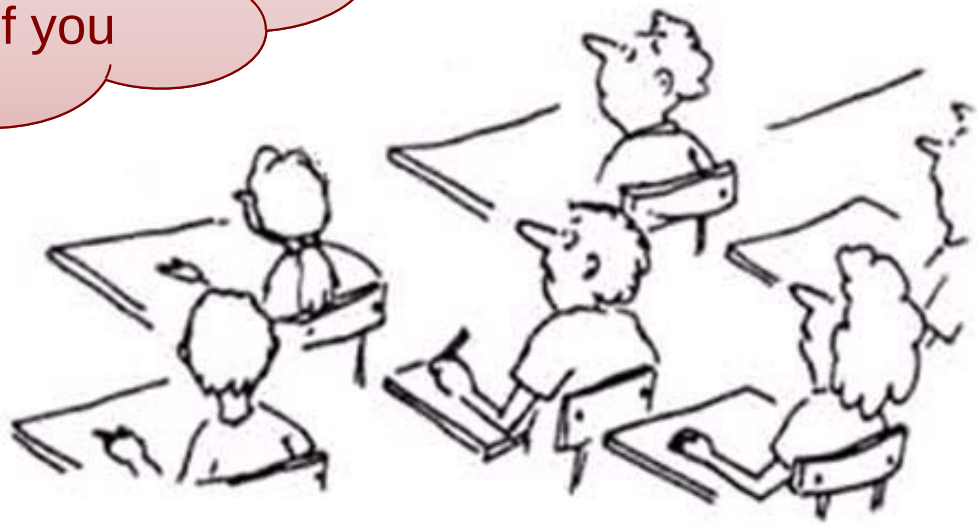
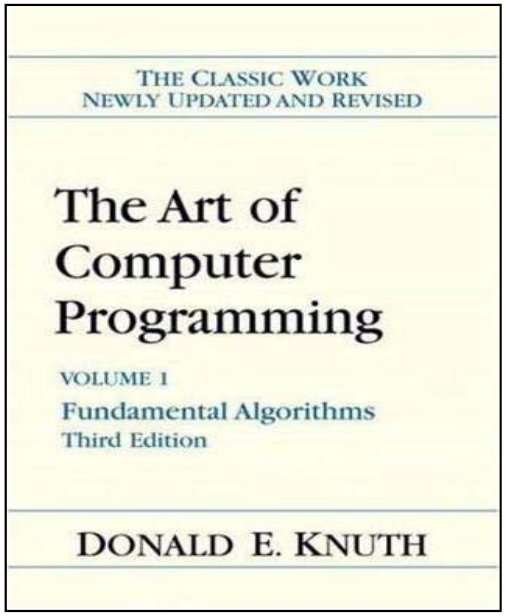
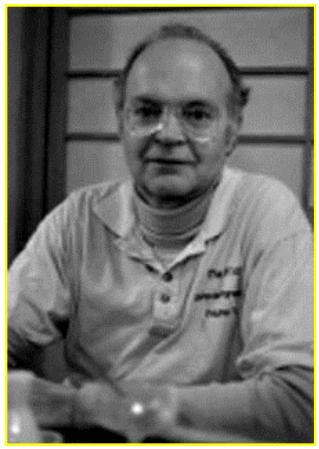


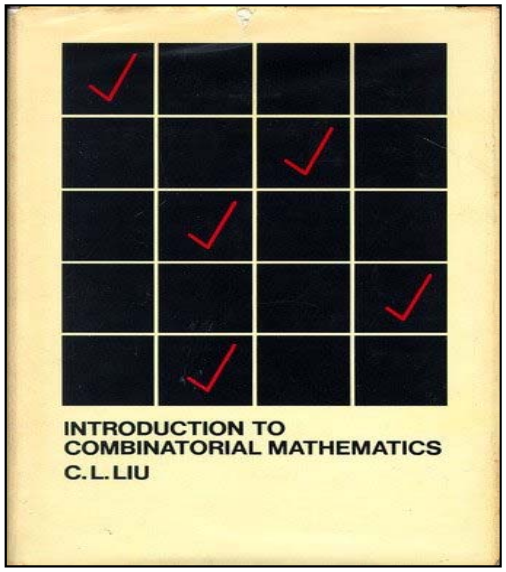
Two Important Books in Computer Science in 1968

- The Art of Computer Programming, Vol. 1, Fundamental Algorithms, Donald E. Knuth, 1968





- Introduction to Combinatorial Mathematics, C. L. Liu, 1968



Sample Chapters in "Introduction to Combinatorial Mathematics"

- Chapter 3: Recurrence Relations
- Chapter 6: Fundamental Concepts in the Theory of Graphs
- Chapter 7: Trees, Circuits, and Cut-sets
- Chapter 10: Transport Networks
- Chapter 11: Matching Theory
- Chapter 12: Linear Programming
- Chapter 13: Dynamic Programming

Project MAC

- Project MAC (Project on Mathematics and Computation) was launched 7/1/1963
  - Backronymed for Multiple Access Computer, Machine Aided Cognitions, or Man and Computer
- Had a strong "AI Group" including Marvin Minsky (the director) and John McCarthy
- System effort led by Fernando Corbato
  - Development of a successor to CTSS (first time-sharing system), Multics
- Featured in 1966 Scientific American September thematic issue
  - Having about 100 TTY terminals
  - Mostly on campus but with a few in private homes
- Dave's participation
  - Combinatorial mathematics, graph algorithms, optimization techniques, table-driven compiler systems

Landmark Result – "Scheduling Algorithms for Multiprogramming in a Hard-Real-Time Environment"

- In Journal of Association of Machinery (1973) with J. W. Layland

Scheduling Algorithms for Multiprogramming in a Hard-Real-Time Environment

C. L. LIU

Project MAC, Massachusetts Institute of Technology

AND

JAMES W. LAYLAND

Jet Propulsion Laboratory, California Institute of Technology

ABSTRACT. The problem of multiprogram scheduling on a single processor is studied from the viewpoint of the characteristics peculiar to the program functions that need guaranteed service. It is shown that an optimum fixed priority scheduler possesses an upper bound to processor utilization which may be as low as 70 percent for large task sets. It is also shown that full processor utilization can be achieved by dynamically assigning priorities on the basis of their current deadlines. A combination of these two scheduling techniques is also discussed.

KEY WORDS AND PHRASES: real-time multiprogramming, scheduling, multiprogram scheduling, dynamic scheduling, priority assignment, processor utilization, deadline driven scheduling

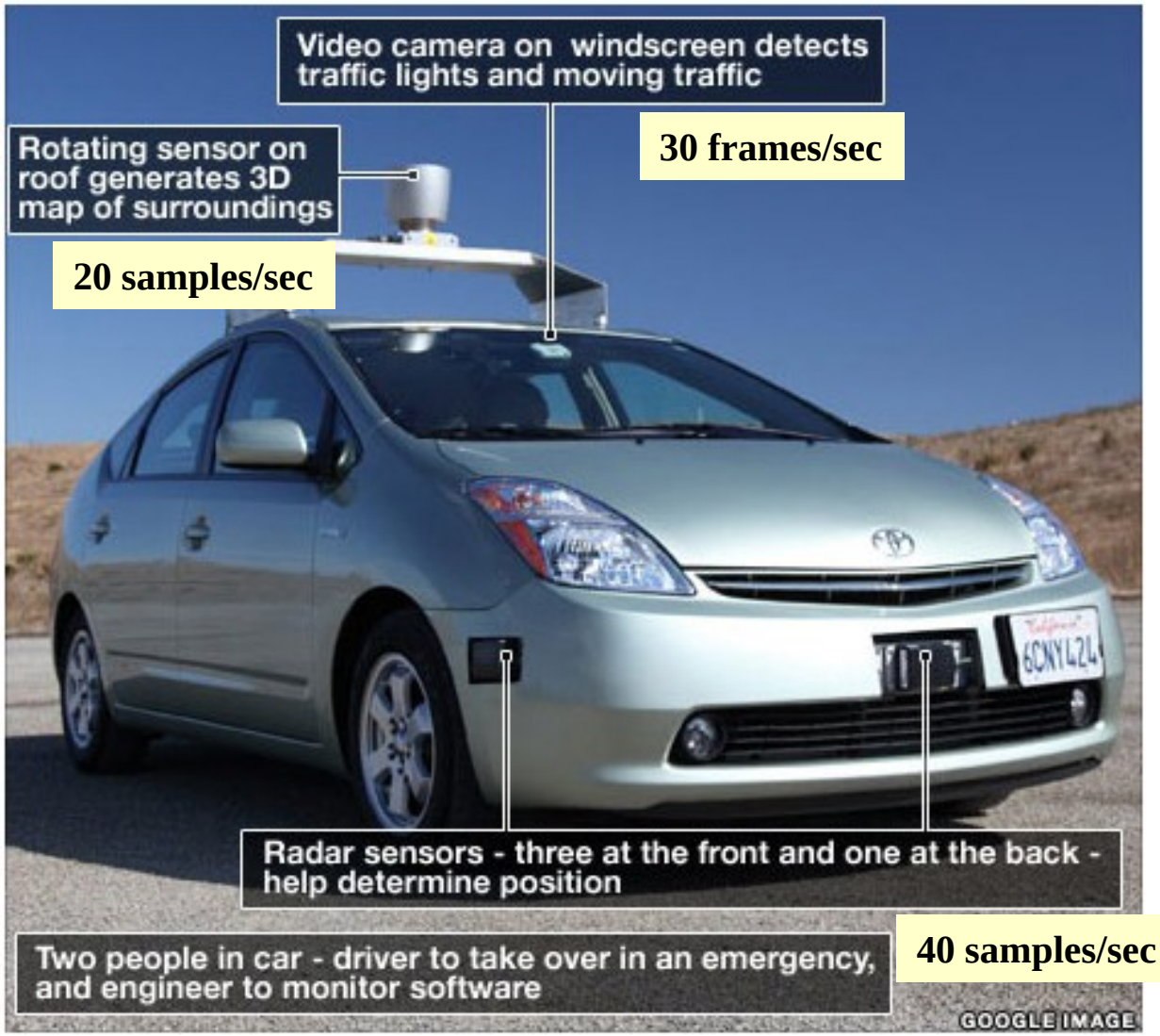
CR CATEGORIES: 3.80, 3.82, 3.83, 4.32

Key Results (An Illustration)

- Static scheduling
  1. Radar sensor (40/s)
  2. Video camera (30/s)
  3. Rotating sensor (20/s)

  Utilization >= 78% (guaranteed!)

  Called rate-monotonic scheduling
- Dynamic scheduling
  - Deadline-driven scheduling
  - Guaranteed full utilization
- Mixed scheduling, e.g.,
  - Radar scheduled first
  - Deadline-driven scheduling fc video and rotating sensor



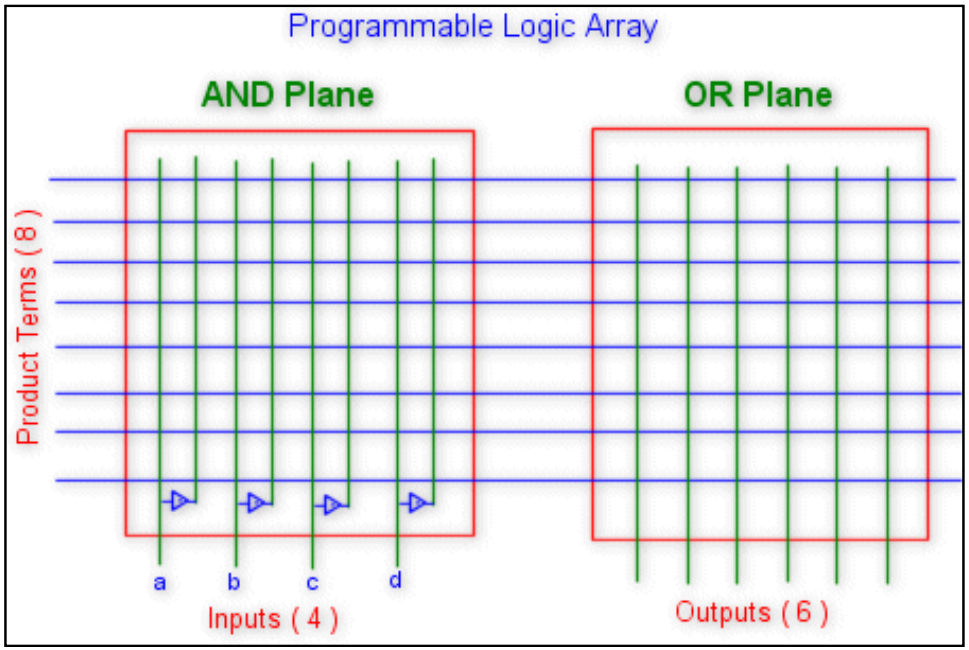
A classical paper with 7000+ citations!

Dave's First DAC Paper – 1982 DAC in Las Vegas

- J. R. Egan and C. L. Liu

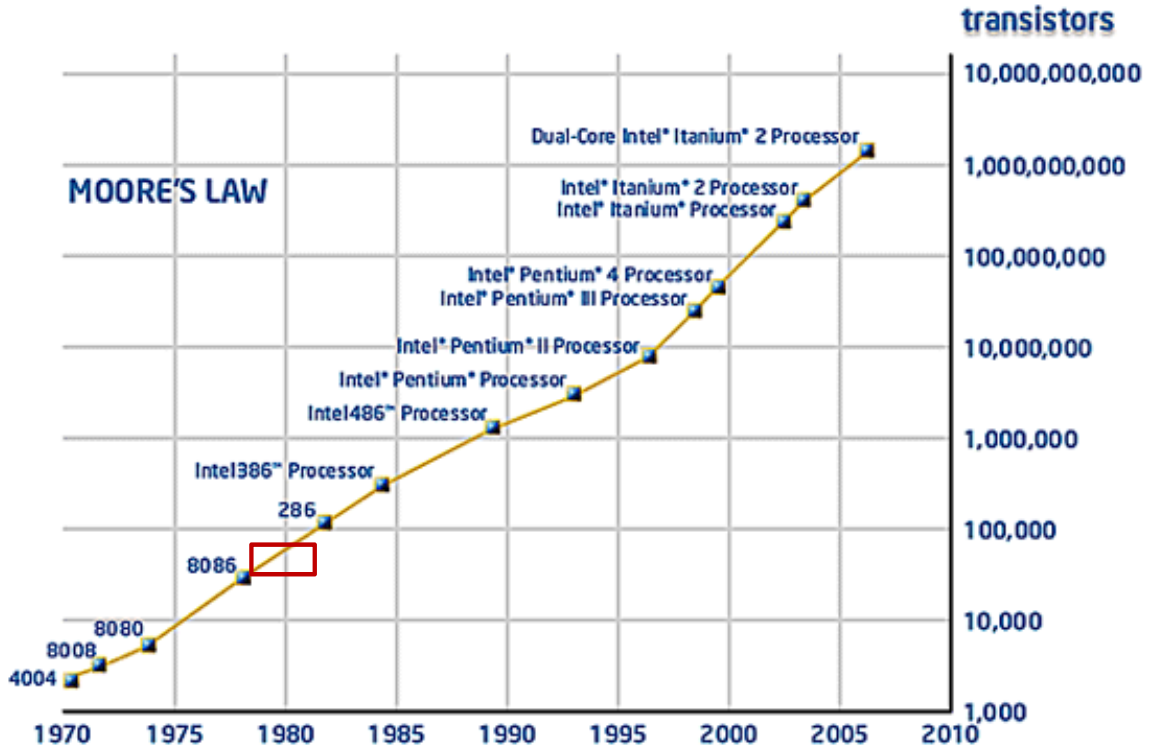
  "Optimal Bipartite Folding of PLA"

  pp. 141-146, 1982 DAC



Backdrop: IC Industry in 1981

- IBM introduced its PC
  - Ran on a 4.77 MHz Intel 8088 microprocessor and
  - Used Microsoft's MS-DOS operating system.
- Apollo Computer unveiled the first workstation, its DN100
  - Offered more power than some minicomputers at a fraction of the price
  - With good support of computer-intensive graphics programs common in engineering
- Design complexity: Intel 8088
  - 16-bit internal bus
  - 8-bit external bus
  - Transistor count: 29,000



Backdrop: EDA in 1981

- Commonly used physical design methods
  - Circuit partitioning
    - Iterative refinement (pairwise exchanges)
  - Circuit placement
    - Greedy construction
    - Min-cut based placement
  - PCB routing
    - Line probe + maze routing
  - IC routing
    - Channel routing

Dave's Contributions

- Dave brought a great deal of combinatorial optimization techniques and experiences to EDA, with rigor, elegance, and much better efficiency
- Timely solutions to many EDA problems as VLSI technology advances
- Many techniques are timeless

A Classical Example: Automatic Floorplan Design

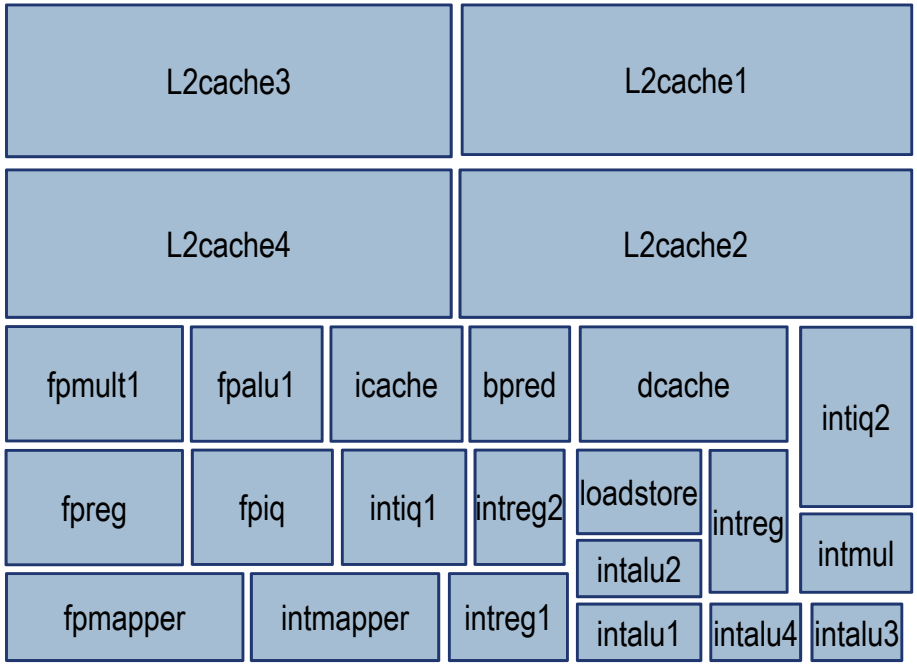
- Best paper award at 1986 DAC
- Pioneering work in floorplan design

A NEW ALGORITHM
FOR FLOORPLAN DESIGN*

D. F. WONG
C. L. LIU

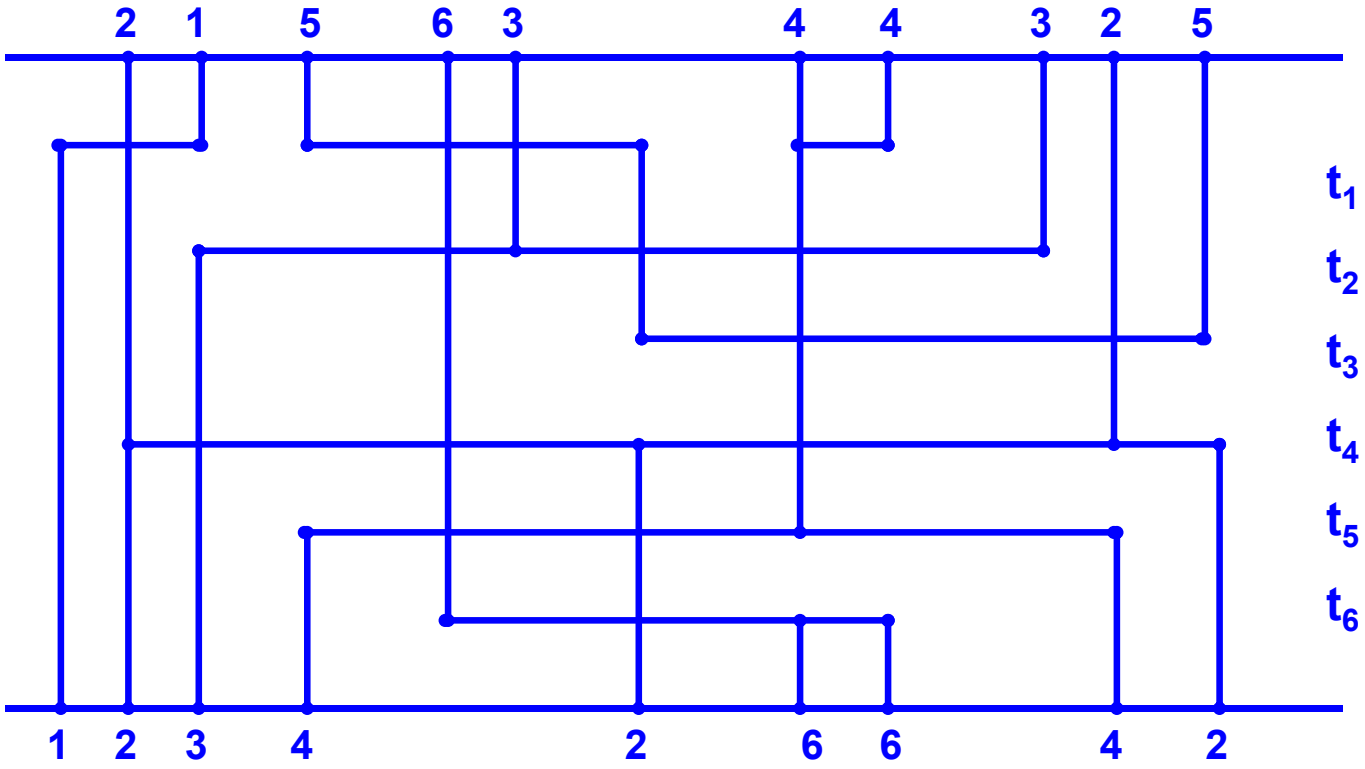
DEPT. OF COMPUTER SCIENCE
UNIV. OF ILLINOIS
AT URBANA–CHAMPAIGN

*This work was partially supported by the Semiconductor Research Corporation, by the General Electric Company, and by the Sandia Laboratories

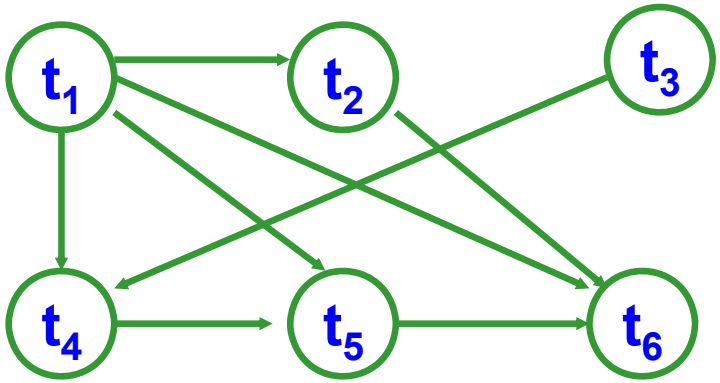


Multi-Layer Routing

J. Cong, D. F. Wong and C. L. Liu, "A New Approach to Three- or Four-Layer Channel Routing", ICCAD'87



Optimal Pairing = Two Processor Scheduling



The Task Precedence Graph

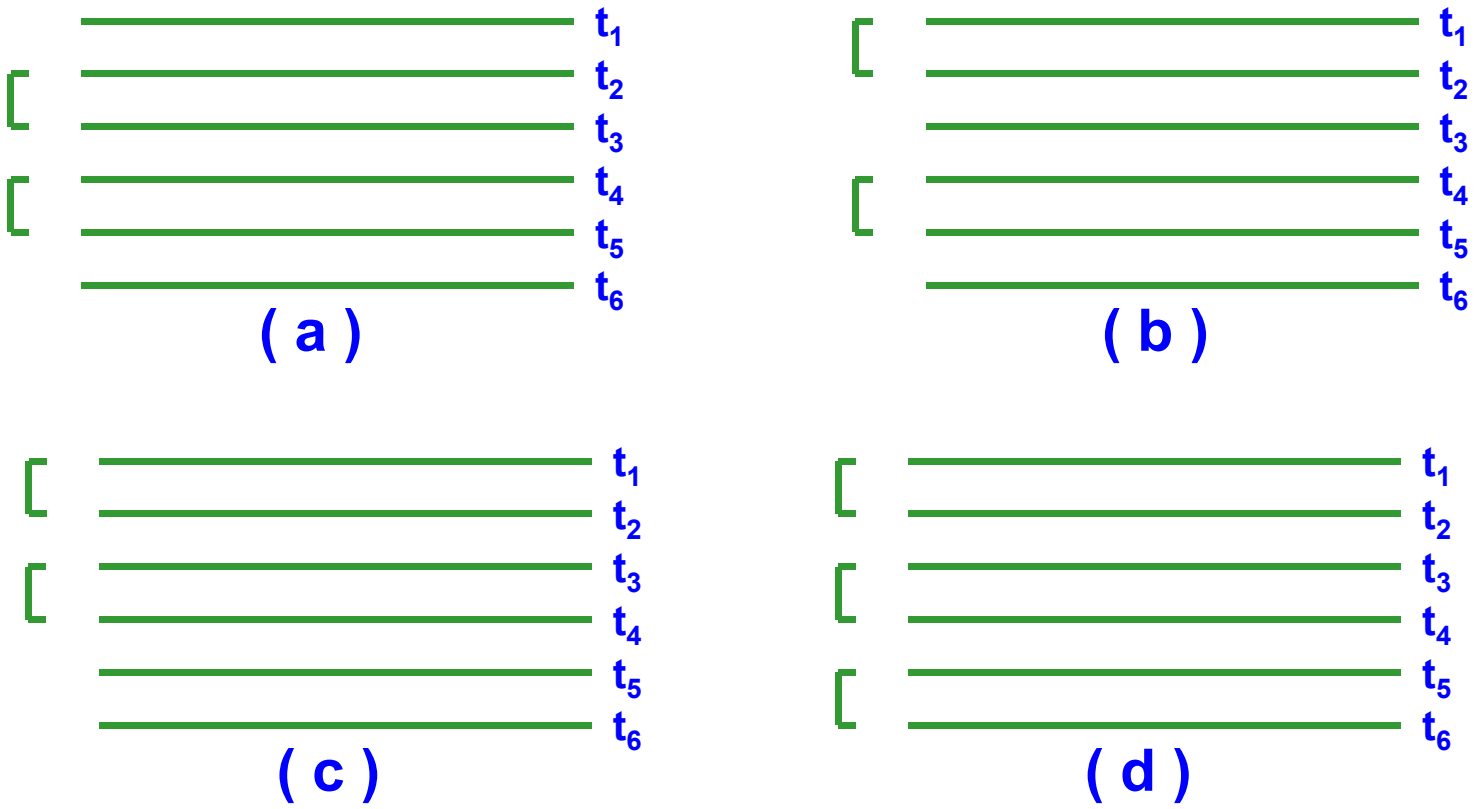
	P_1	P_2
Time=1	t_1	t_3
2	t_4	t_2
3	t_5	
4	t_6	

An Scheduling SOlution

The best track permutation ⇔
the optimal two processor scheduling solution

Solved in linear time

Local Rerouting and Singular Track Shifting

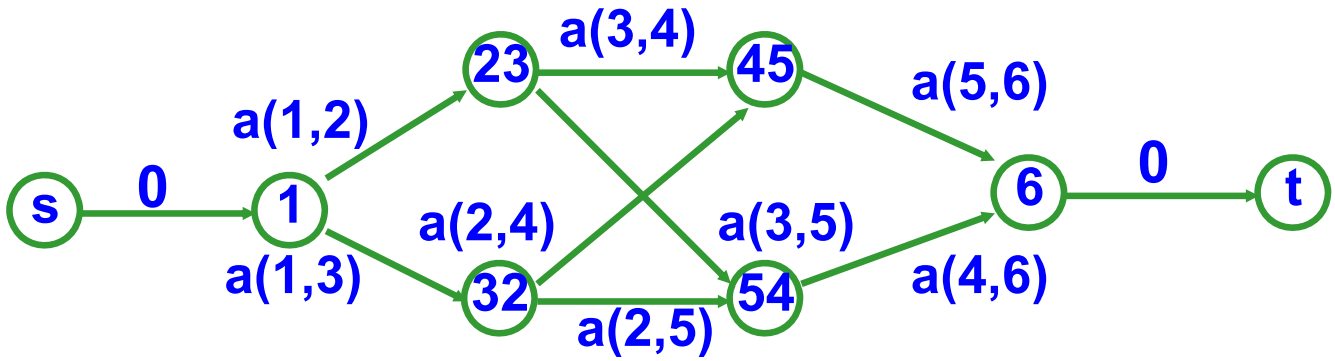


Singular Track Shifting.

Minimize the total # of adjacent vias

Decide Relative Ordering Within Each Track Pair

Track group state graph



The track group state graph for the example

Shortest s-t path ⇔
optimal relative ordering for every track pair

Solved in quadratic time

Timing-Driven Placement for FPGAs

- With Anmal Mather (ICCAD'94)
- A two-phase approach —compression and relaxation.
  - Compression: identifies critical paths and attempts to fix these by moving the clusters in the critical path closer
  - Relaxation: moving overlapping clusters to neighboring logic blocks in their "slack neighborhood."
- Explore a much larger, more global neighborhood structure in local search.
- Also used to incremental placement for (ICCAD'95) and fault-tolerant placement for FPGAs (DATE'96).

FPGA Mapping with Retiming

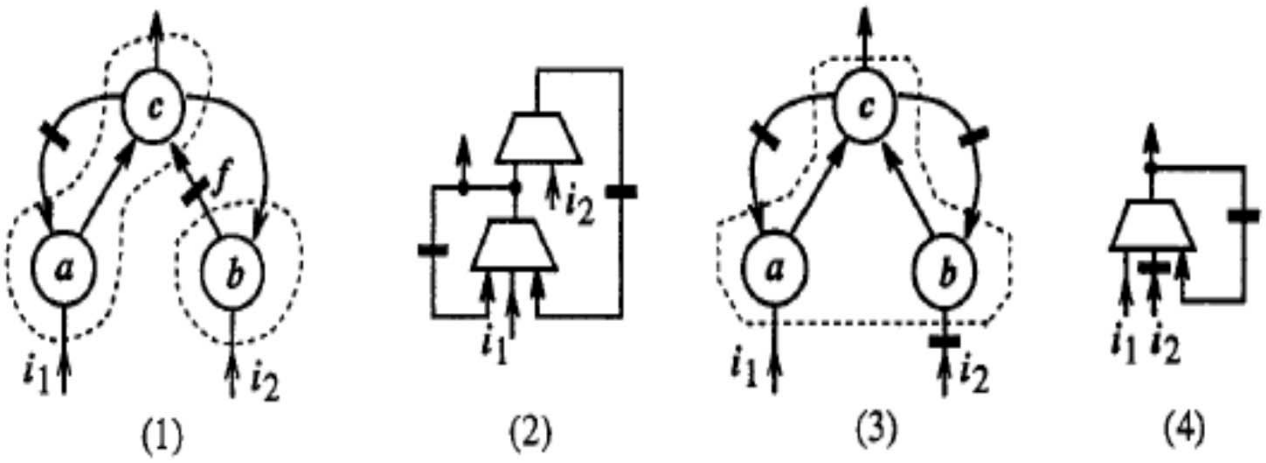


Fig. 1. Advantage of combining technology mapping with retiming.

- (1) Original netlist, (2) a mapping solution, (3) a retimed netlist, and (4) a mapping solution of the retimed netlist which is better in both timing and area than the mapping solution in (2).

Problem Definition

- Given a sequential netlist and a target clock period, find a mapping solution with the given clock period assuming registers can be retimed.

The problem has a large solution space as there are many ways to retime a netlist. We can't enumerate all retimings.

The Algorithm

- Two important concepts introduced by the paper
  - *Sequential cuts*: cuts that can extend across register boundaries
  - *Sequential arrival times*: labels that are strongly tied to whether a design can meet a target clock period using retiming
- Overall algorithm
  - Dynamic programming plus successive approximation
  - Provable convergence and polynomial runtime

High-level Synthesis: Scheduling

- T. Kim and J. W. S. Liu, and C. L. Liu
  A Scheduling Algorithm for Conditional Resource Sharing
  International Conference on Computer Aided Design (ICCAD), pp. 84-87, November 1991
  - Dave's first work in high-level synthesis
  - Borrowed the idea from Dave and Janes' real-time job scheduling experience
  - Dave's first co-work with Jane in high-level synthesis
- C. Park, T. Kim, and C. L. Liu
  Register Allocation for Dataflow Graphs with Conditional Branches and Loops
  European Design Automation Conference (EURO-DAC), pp. 586-590, September 1993
  - Extended the scheduling algorithm to address the register allocation problem in high-level synthesis
  - Showed the potential powerfulness of the scheduling algorithm to diverse applications

Dave Liu's High-level Synthesis Works: Allocation

- T. Kim and C. L. Liu

  Utilization of Multiport Memories in Data Path Synthesis

  Design Automation Conference (DAC), pp. 298-302, June 1993

  - Showed that the multiport memory allocation problem can be transformed into 2-D bin-packing problem
  - Consistently referenced by HLS EDA community when allocating multiport memories is involved.

- T. Kim, K.-S. Chung, and C. L. Liu

  A Stepwise Refinement Data Path Synthesis Procedure for Easy Testability

  European Design and Test Conference (EDAC), pp. 586-590, February 1994

  - Testability issue in HLS was a hot topic in early 1990s.
  - Contains Dave's insight on algorithmic approach to the testability enhancement problem in high-level synthesis

-

Dave Liu's High-level Synthesis Work: Arithmetic

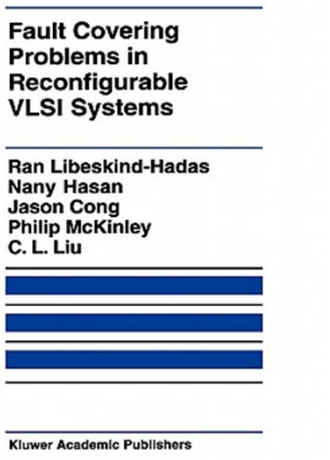
- J. Um, T. Kim and C. L. Liu
  Optimal Allocation of Carry-Save-Adders in Arithmetic Optimization
  International Conference on Computer-Aided Design (ICCAD), pp. 410-413, November 1999 (and IEEE Transactions on Computers, Vol. 50, pp. 215-233, March 2001)
  - Opened a new HLS research area on algorithmic optimization for the arithmetic circuit design
  - Influenced the algorithmic design paradigm to the EDA industry as well as academia
  - One of the most frequently referred works in the algorithmic arithmetic circuit synthesis
- J. Um, T. Kim, and C. L. Liu
  A Fine-Grained Arithmetic Optimization for High-Performance / Low-Power Data Path Synthesis
  Design Automation Conference (DAC), pp. 98-103, June 2000
  - A new insight on the classical Wallace tree generation algorithm with more accurate timing model

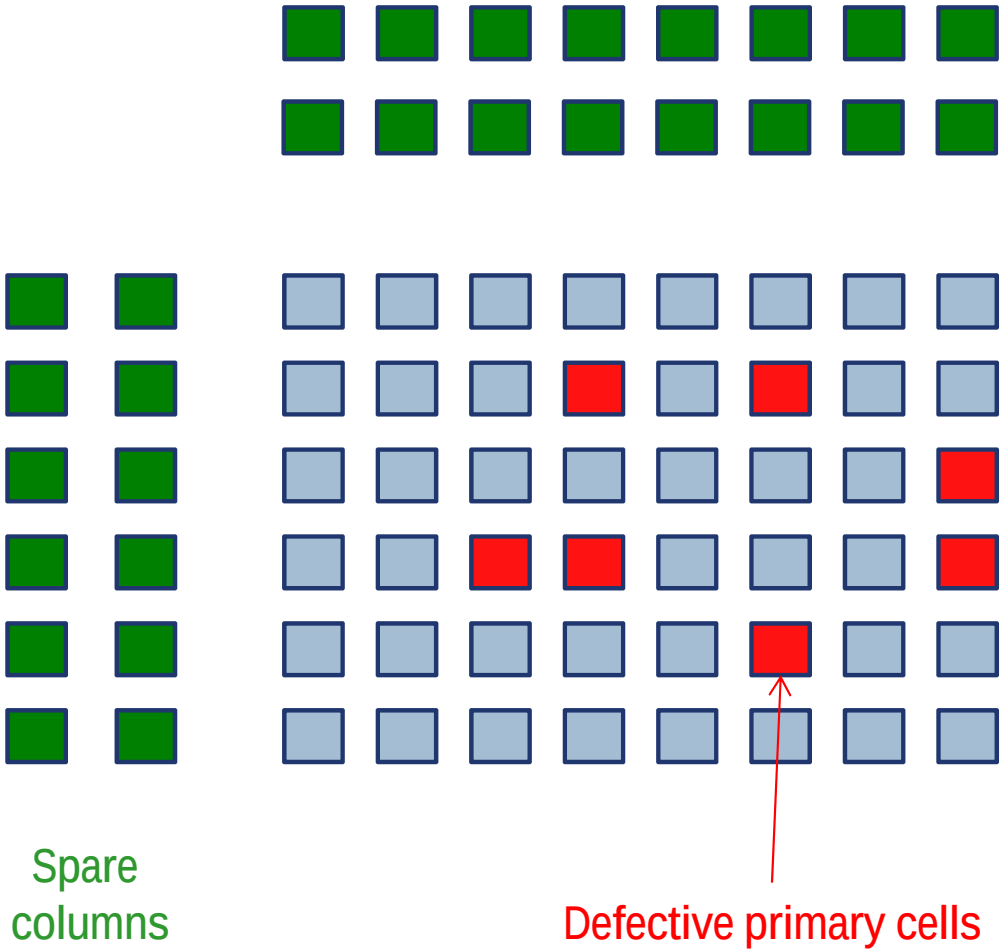
Fault Tolerant RAMs and Processor Arrays

Determining whether a faulty array can be repaired is NP-complete…

… but graph theoretic methods can be used to find efficient and good reconfiguration heuristics

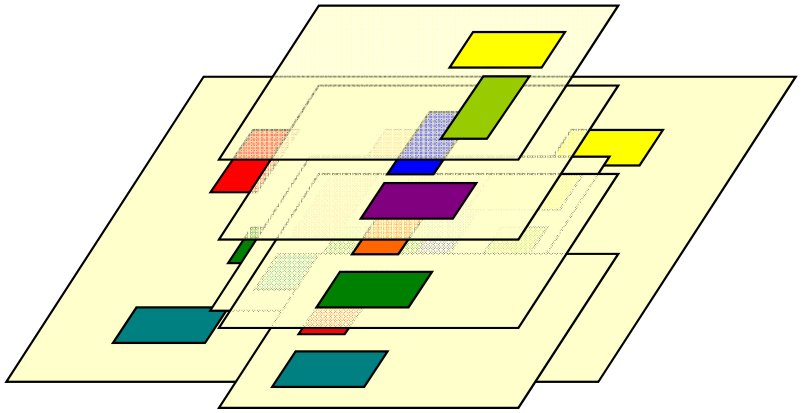
These results can be generalized to heterogeneous arrays as well





3D Placement [Luo, Zhang, Cong, ASPDAC'07]

2D to 3D Transformation by Local Stacking – leveraging the best 2D placers (e.g. mPL6)



1. **2D placement on area K*A**
   - For 3D chip with K device layers and each with area A
2. **Shrink:** $(x_i, y_i) \rightarrow (x_i/\sqrt{K}, y_i/\sqrt{K})$
3. **Tetris-style 3D legalization**
   - Cost R = αd + βv + γt
   - Minimize displacement, #via and thermal cost

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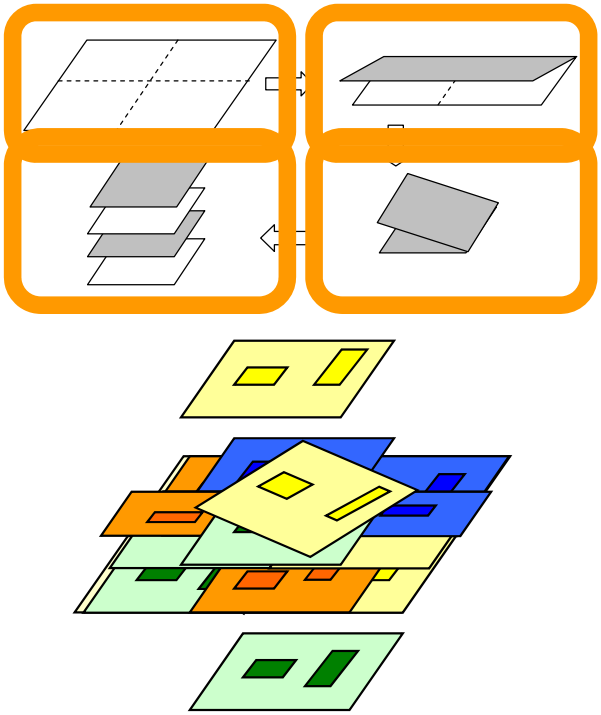
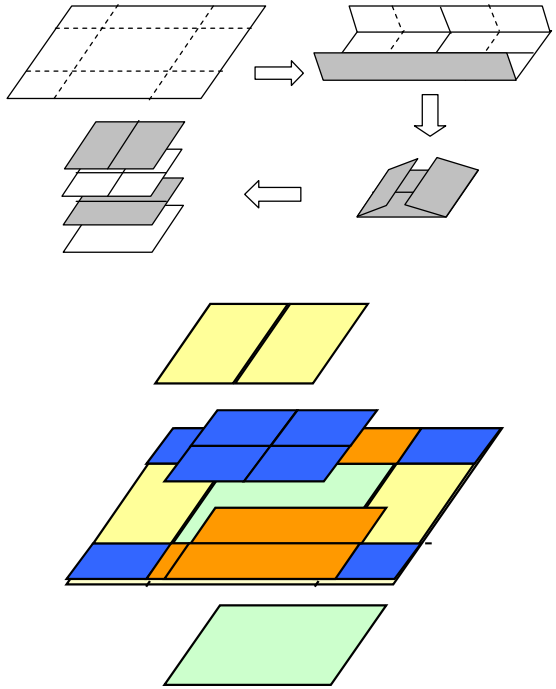
2D to 3D Transformation by Folding

- **Layer assignment and location mapping according to the folded order**
  - **Folding-2**



  - Folding-4



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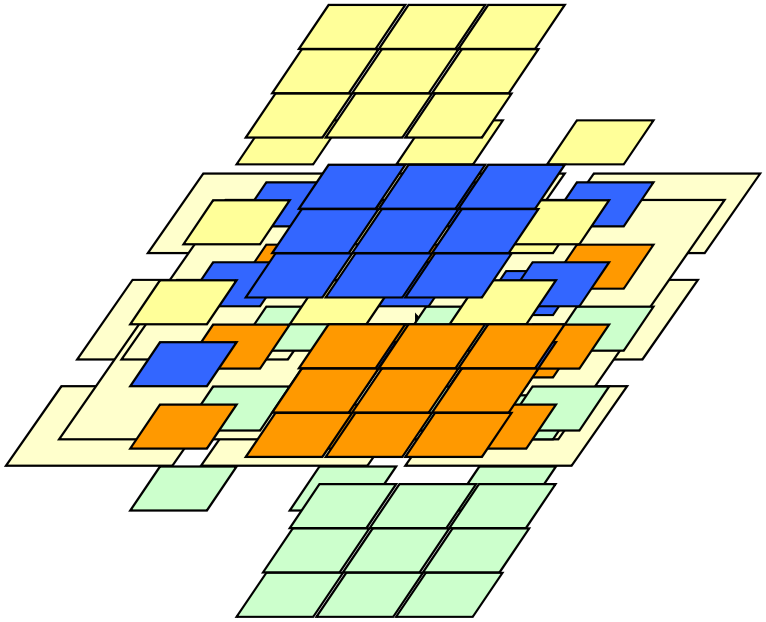
Window-based Stacking / Folding



1. Divde 2D placement into NxN windows
2. Apply stacking or folding in a window

- Effect of stacking or folding would be spreaded out, and trade-offs are achieved by varying N

Dave's PhD S

1. Murray Edelburg
2. Nai Chen
3. Andrew Yao
4. Hung-Ping Tsao (1976)
5. Donald K. Friesen (1978)
6. Shmuel Zaks (1979)
7. K. M. Chung (1980)
8. Prakash Ramanan (1984)
9. Dana Richards (1984)
10. Hon-Wai Leong
11. Jim Lewandowski (1986)
12. Pravin Vaidya (1986)
13. Martin Wong
14. Xiaojun Shen (1989)
16. Nany Hasan (1990)
17. Taewhan Kim
18. Ran Libeskind-Hadas (1993)
19. Sai-Keung Dong
20. Tong Gao
21. Srilata Raman
22. Yachyang Sun
23. Anmol Mathur
24. Peichen Pan (1995)
25. Chaeryung Park
26. Ki-Seok Chung
27. Prashant Saxena
28. Unni Narayanan (1998)

Founder and president of Aplus (acquired by Magma); co-founder and CTA of AutoESL (acquired by Xilinx)

Jason Cong

Chancellor's Professor at UCLA & former dept chair

Tsinghua Univ. (winner of 2000 ACM Turing Award)

Seoul National University

Professor and Department Chair, Harvey Mudd College

Synopsys Fellow

CTO and co-founder of Calypto Design System

National University of Singapore

UIUC

UT Austin & UIUC

Head of Engineering at Aplus (acquired by Magma) & AutoESL (acquired by Xilinx)

Founder and CEO of Primary Global Research

A Partial List of Dave's Honors and Awards

- IEEE Fellow (1986)
- Guggenheim Foundation Fellowship (1987)
- ACM Karl V. Karlstrom Outstanding Educator Award (1990)
- IEEE Computer Society Taylor L. Booth Education Award (1992)
- IEEE Education Medal (1994)
- ACM (Inaugural) Fellow (1994)
- Technical Achievement Award from IEEE Circuits and Systems Society (1998)
- ACM/SIGDA Distinguished Service Award (1999)
- Technical Achievement Award from IEEE Real-Time Systems Committee (1999)
- IEEE Millennium Medal (2000)
- IEEE Circuits and Systems Society Golden Jubilee Medal (2000)
- ….

Quotes from Pioneers and Leaders in Industry on Impact of Dave's Contributions to EDA

- Paul Huang, Founder of EDAC, Pie, Novas. Kaufman Award 2000
  - He, together with his students, has successfully and convincingly demonstrated the power and elegance of algorithmic EDA over the last 25 years. The impact of their work is immense.
  - We use his teaching and guidance for our product development, particularly in floorplanning, place and route, and partition.

- Ajoy Bose, CEO and President of Atrenta
  - As a case in point, Atrenta's architectural-level floorplanning tool, SpyGlass Physical, heavily utilizes Dave's work published in DAC-86.

- Chi-Foo Chan, President and COO of Synopsys
  - Leading products such as Astro and IC Compiler directly benefited from Prof. Liu's research results and insights on automated floorplanning, placement, and routing.

VLSI and Theoretical Computer Science in 1980s

- STOC 1985
  - Alok Aggarwal: Tradeoffs for VLSI Models with Subpolynomial Delay
  - Charles E. Leiserson, F. Miller Maley: Algorithms for Routing and Testing Routability of Planar VLSI Layouts
  - Prabhakar Raghavan, Clark D. Thompson: Provably Good Routing in Graphs: Regular Arrays.
- FOCS 1985
  - Alok Aggarwal, Maria M. Klawe, David Lichtenstein, Nathan Linial, Avi Wigderson: Multi-Layer Grid Embeddings
  - Paul M. B. Vitányi: Area Penalty for Sublinear Signal Propagation Delay on Chip
  - Richard Cole, Alan Siegel: On Information Flow and Sorting: New Upper and Lower Bounds for VLSI Circuits
  - Mikhail J. Atallah, Susanne E. Hambrusch: Solving Tree Problems on a Mesh-Connected Processor Array
  - Ming-Deh A. Huang: Solving Some Graph Problems with Optimal or Near-Optimal Speedup on Mesh-of-Trees Networks.

VLSI and Theoretical Computer Science

- Many theoreticians left, but Dave stayed and made a huge impact
- Questions to EDA community
  - How do we engage with the theory community again?
    - NSF workshop report (IEEE Design & Test, March 2010)
  - How do we attract the next Dave Liu?

Thank you, David

For leading the transformation from Ad Hoc EDA to Algorithmic EDA