Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips

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Outline

Introduction

- Digital microfluidic biochips (DMFB)
- Design flow of DMFBs
- Our contributions

Fluidic-Chip Co-design Methodology

Experimental Results

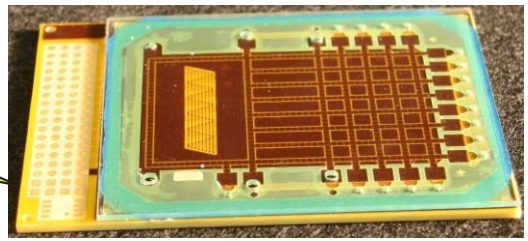
Conclusions

Motivation for Biochips

- 15 billion tests/year in 10 years
- 90% of cost and 95% of time today is associated with sample collection, transport, preparation

Conventional Biochemical Analyzer

Shrink



nl-pl sample

Higher throughput, minimal human intervention, smaller sample/reagent consumption, higher sensitivity, increased productivity

- Clinical diagnostics, e.g., healthcare for premature infants, point-of-care diagnosis of diseases
- Massive parallel DNA analysis, automated drug discovery, protein crystallization

Hemophilia

Digital Microfluidic Biochips (DMFBs)

- Digital Microfluidic Biochips
  - **Droplets:** biological sample carrier; basic units to perform the laboratory procedures on DMFBs
  - **2D microfluidic array:** set of basic cells for biological reactions
  - **Reservoirs/dispensing ports:** for droplet generation
  - **Optical detectors:** detection of reaction result

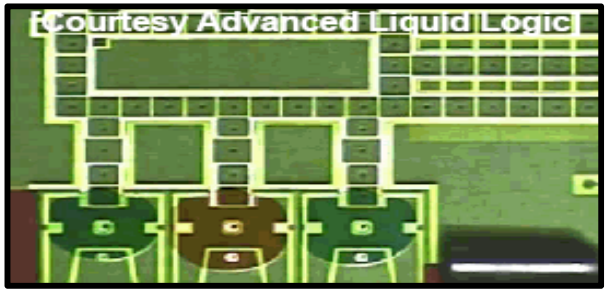
Droplets

2D microfluidic array

Optical detector

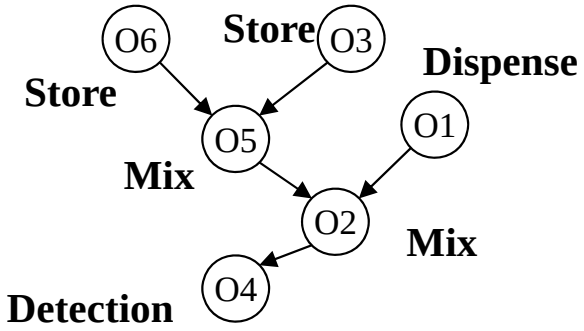
Reservoirs/dispensing ports

CAD Tools Needed!



Schematic view of a DMFB (Duke Univ.)

Fluidic-Level Synthesis (1/2)



Resource	Area	Time
Mixer	2x2-array	7
Mixer	1x3-array	4
LED	1x1 cell	10
Storage	1x1 cell	N/A

Max. Area: 5x5 array

Max. Completion Time: 50 seconds

Sequencing Graph

Microfluidic Module Library

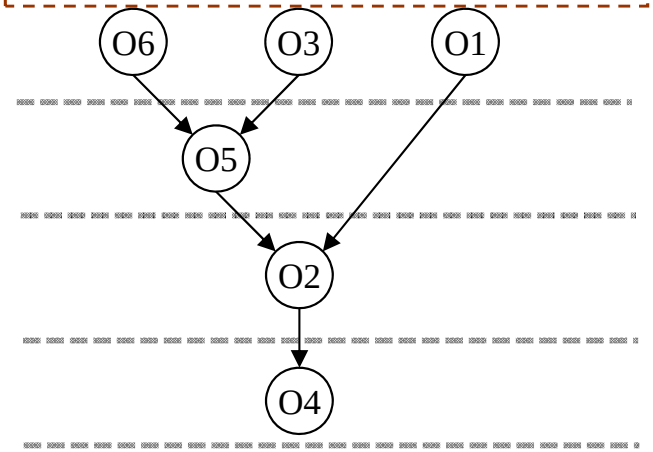
Design Spec.

Architectural-Level Synthesis

Resource Binding

Operation	Resource
O1	On-chip
O2	2x2-array
O3	1x1 cell
O4	LED
O5	1x3-array
O6	1x1 cell

Scheduling

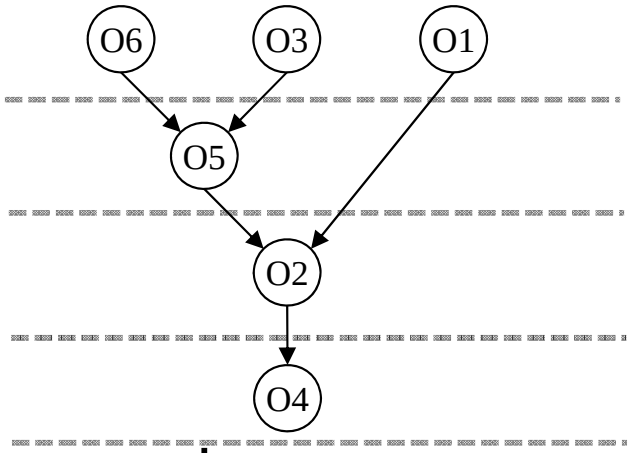


Fluidic-Level Synthesis (2/2)

Resource Binding

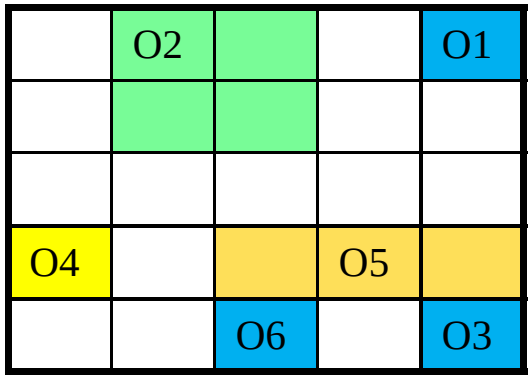
Operation	Resource
O1	On-chip
O2	2x2-array
O3	1x1 cell
O4	LED
O5	1x3-array
O6	1x1 cell

Scheduling

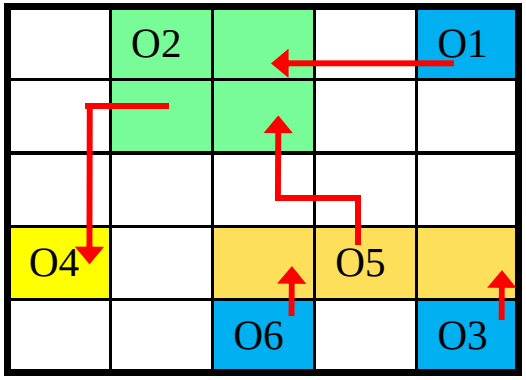


Physical-Level Synthesis

Placement

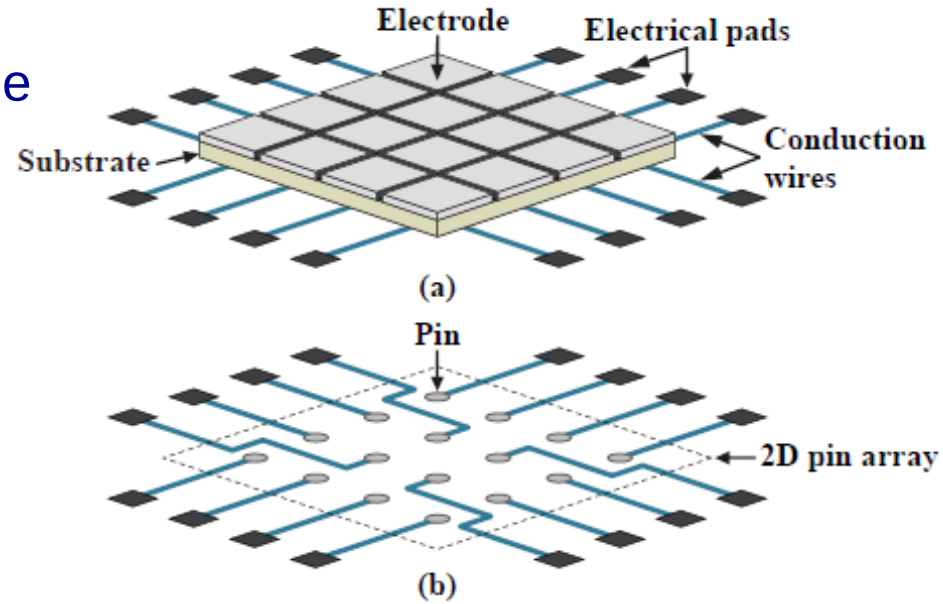


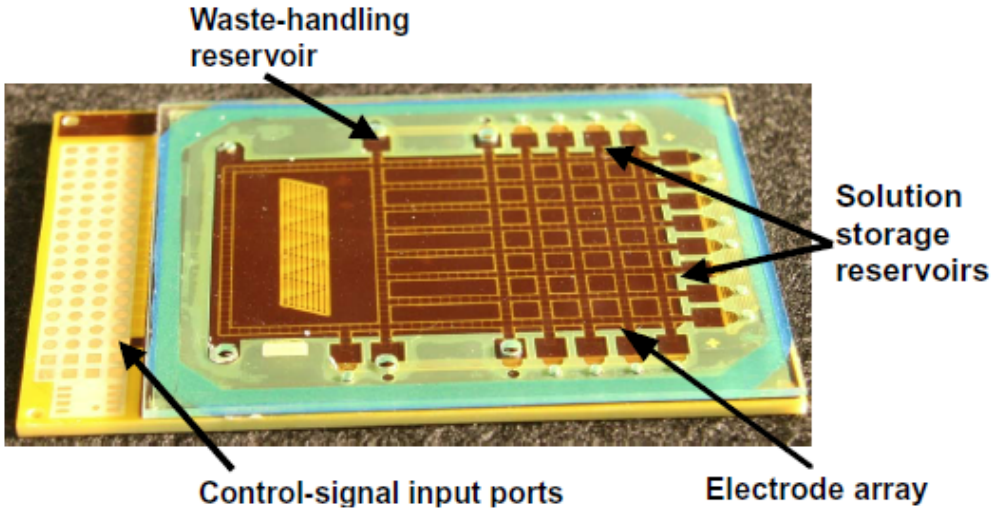
Routing

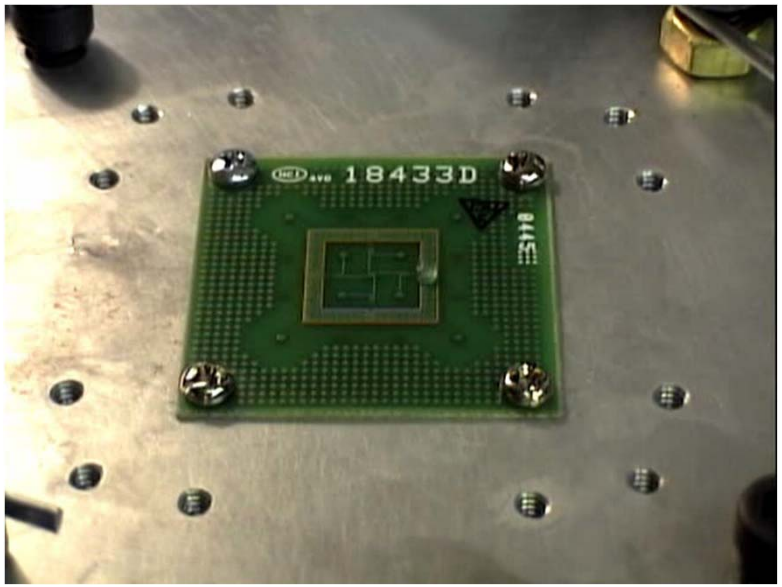


Chip-Level Design

- Direct-addressing method
  - Dedicated control pin for each electrode
  - Maximum freedom of droplets
  - High demanded control pins
- For large arrays
  - Too many control pins ⇒ high fabrication cost
  - Wiring plan is not available





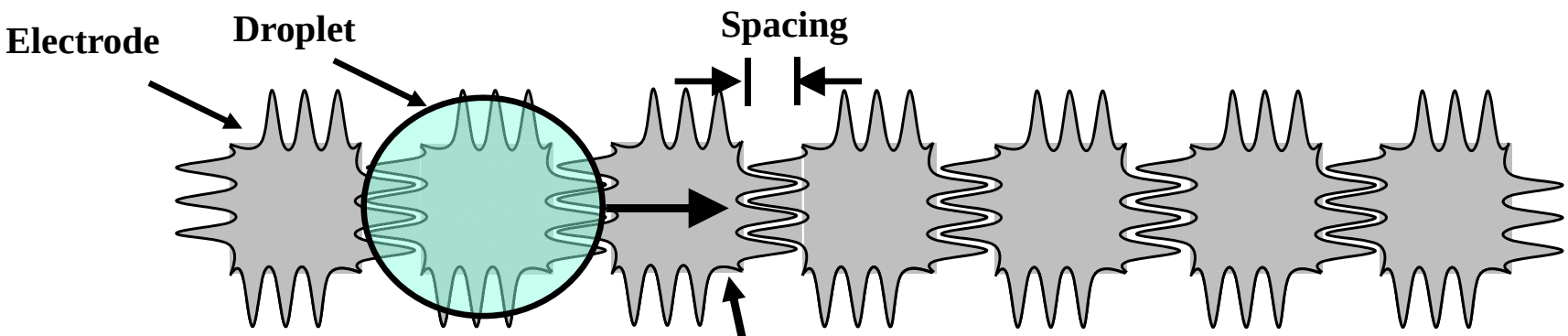


A fabricated DMFB for PCR

- over 1000 electrodes

- only 64 signal ports

Electrode Addressing for Signal Merging



High voltage to generate an electrical field

Actuation sequence

time

0	0	1	0	X	X	X
X	0	0	1	0	X	X
X	X	0	0	1	0	X
X	X	X	0	0	1	0
X	X	X	1	0	0	1
		0	0	0	1	0
			1	0	0	1

7 pins -> 4 pins

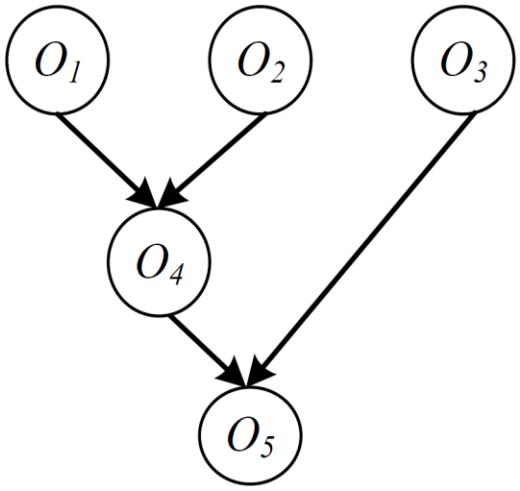
Broadcast addressing

Pin

Wire

External controller

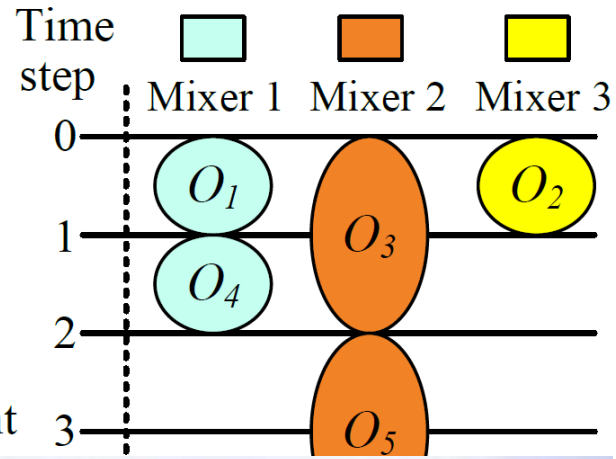
Design Flow of DMFB



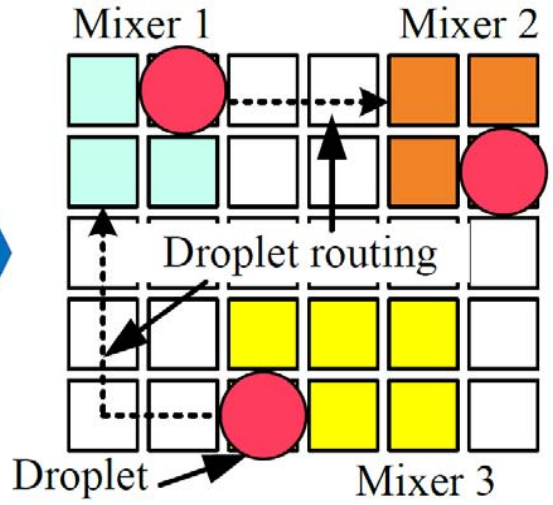
Sequence graph

Device binding

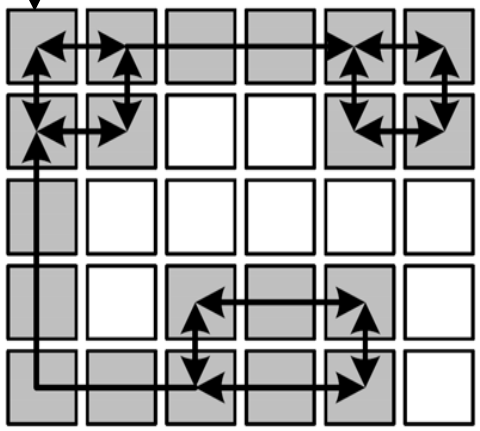
Time-step assignment



Chip layout



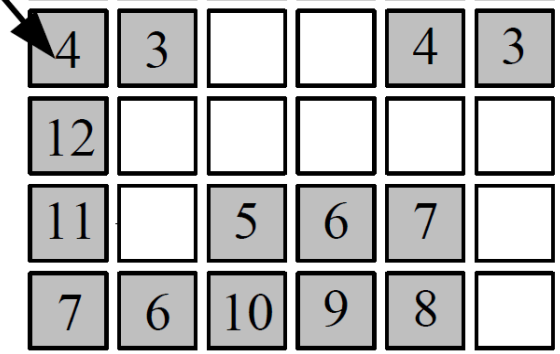
Placement & Droplet routing



Used electrodes

Signal merging

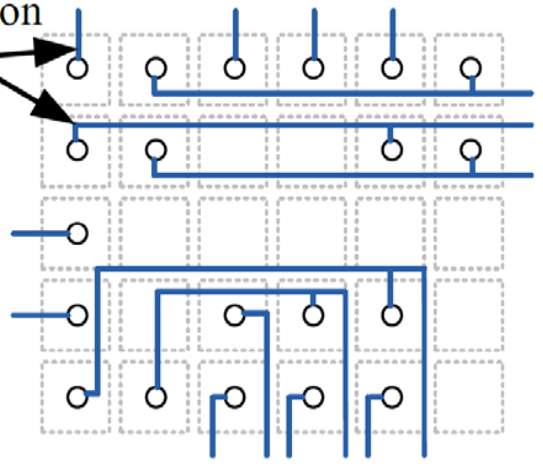
Cont pins



Electrode addressing

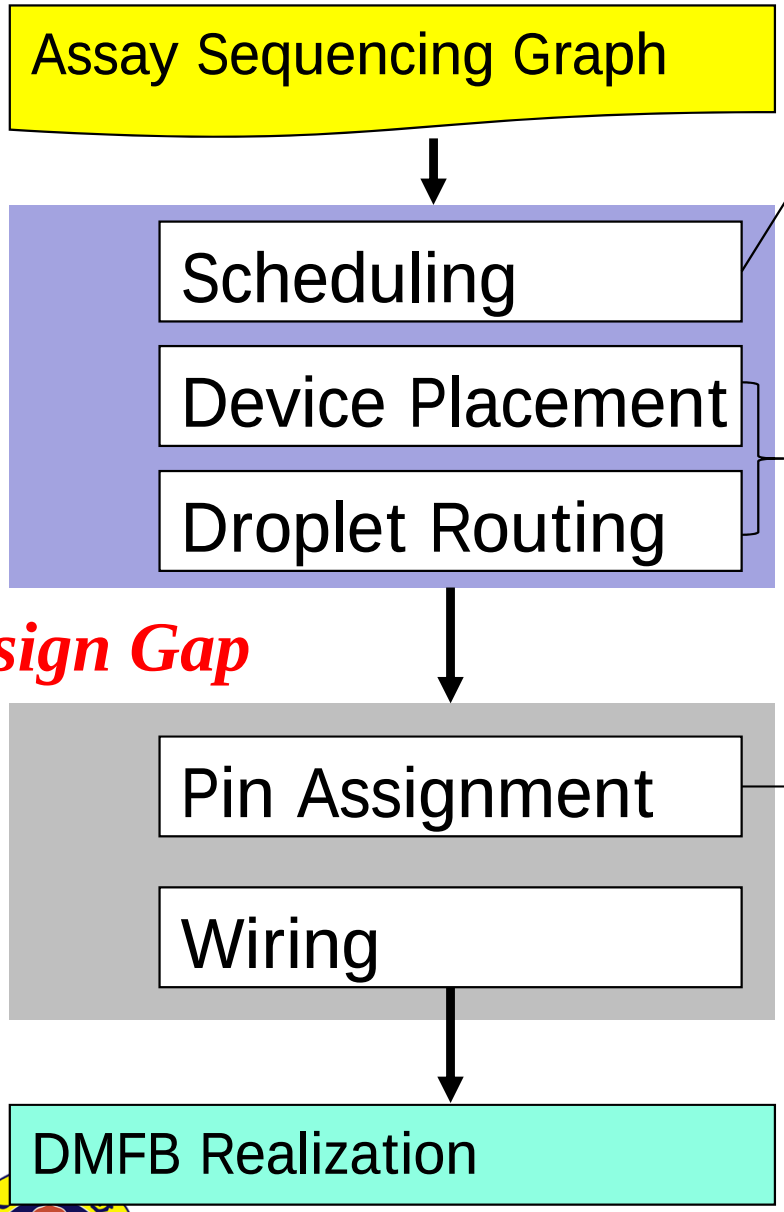
Escape to I/O pads

Conduction wires



Wire routing

Design Gap of Conventional Flow



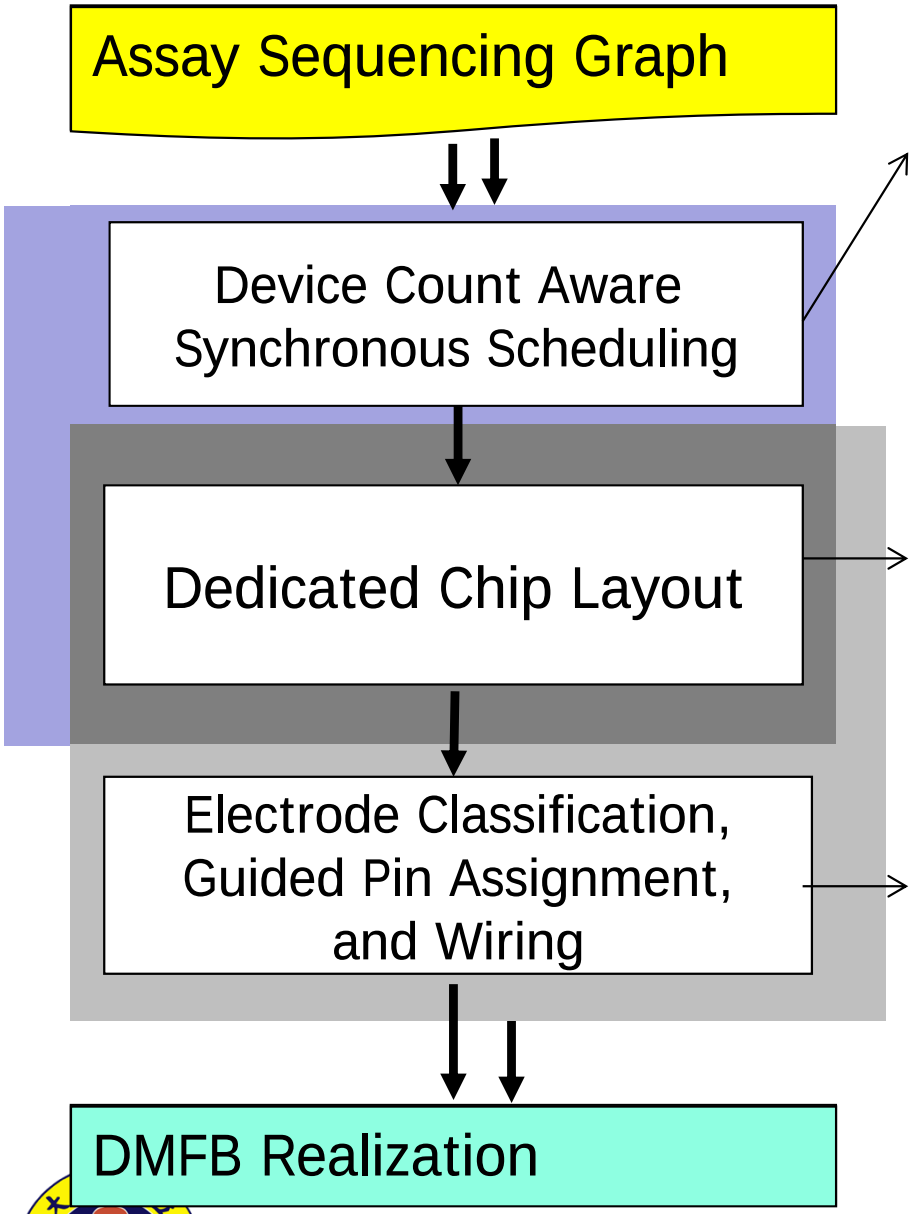
Focus on parallel controls of assay operations to increase throughput

Allow devices and droplets to be arbitrarily moved in area and time domain

Conduct signal merging throughout the entire electrode set without considering wire routing

- Problems of design gap
  - Pin re-assignment, wire re-routing, design re-synthesis
  - Extra pin counts or PCB layers

Fluidic-Chip Co-design Flow



Reduce the required pin-count and wiring effort

Simultaneously determine the 2D orientation of devices and routing paths

Assign control pins with minimum wiring interference around different control signals and reduce pin-count and wirelength

Outline

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Fluidic-Chip Co-design Methodology

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Fluidic-Chip Co-design Methodology

Device Count Aware
Synchronous Scheduling

Dedicated Chip Layout

Electrode classification,
Guided Pin Assignment, and
Wiring

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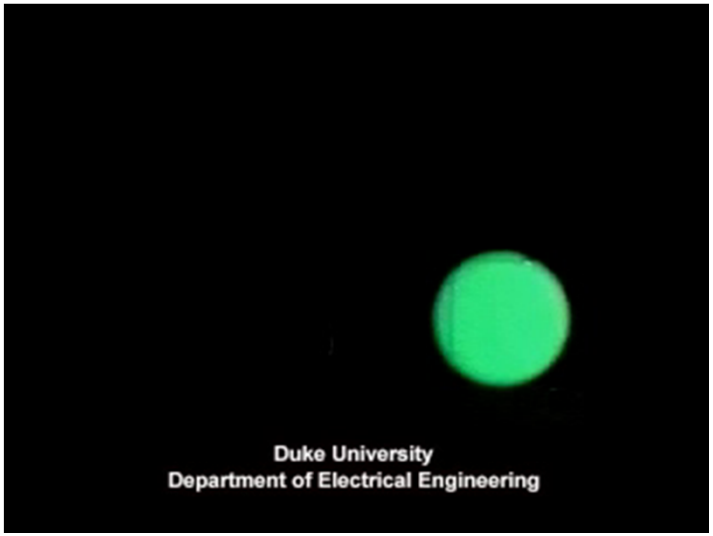
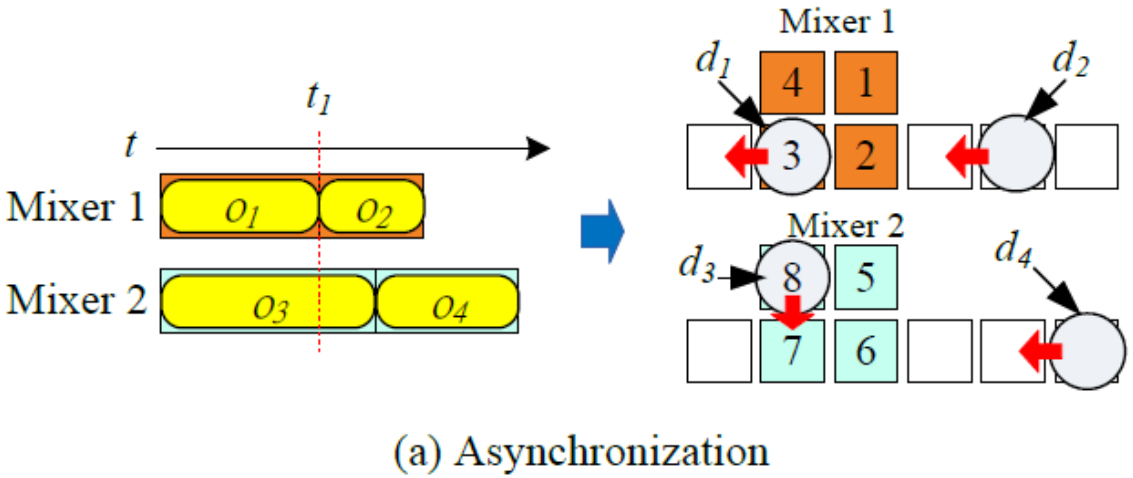
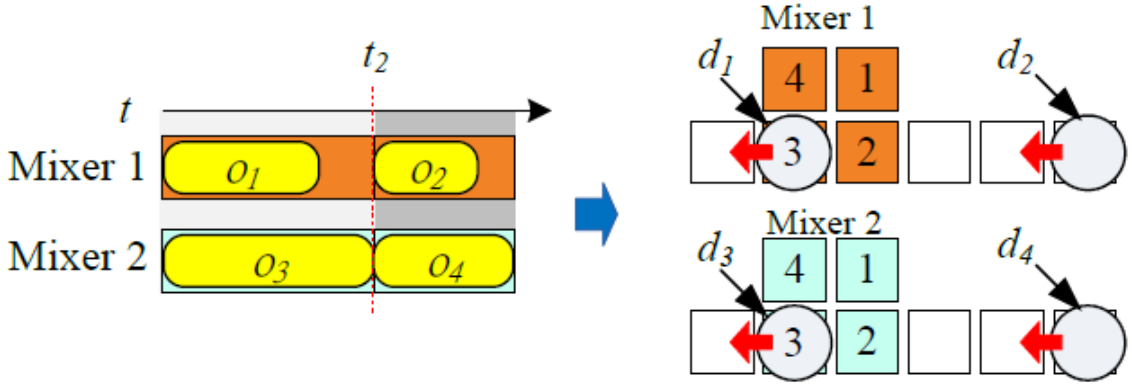
Synchronous Reactions

- Facilitate the control signal merging for pin-count reduction by deriving a series of execution stages for synchronous control*





(a) Asynchronization

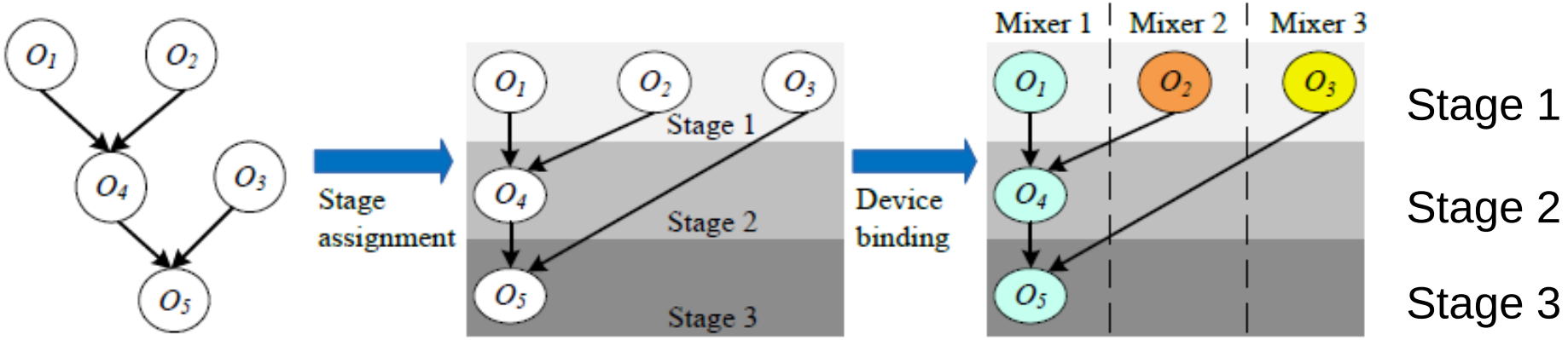


(b) Synchronization

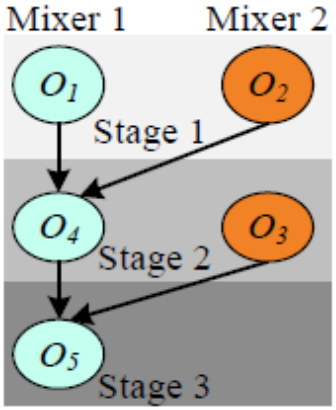
*C. C.-Y. Lin and Y.-W. Chang, "ILP-based pin-count aware design methodology for microfluidic biochips," *Proc. ACM/IEEE DAC*, pp. 258-263, 2009

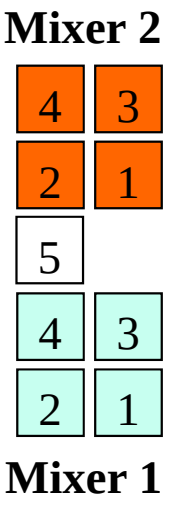
Synchronous Scheduling

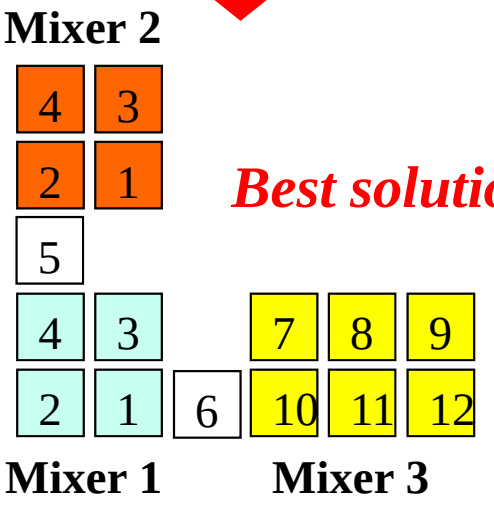
- Assign operations to different stages



Idea: reduce pin counts by minimizing device counts







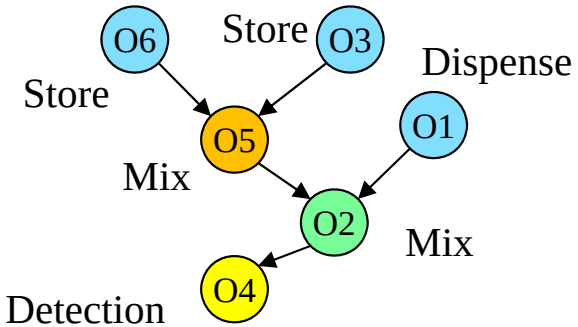
Best solution?

Synchronous controlling

12 => 5!!

Device Count Aware Synchronous Scheduling

- **Given:** *A sequencing graph of operations and a device library*



Resource	Area	Time
Mixer	2x2-array	7
Mixer	1x3-array	4
LED	1x1 cell	10
Storage	1x1 cell	N/A

Sequencing Graph

Microfluidic Module Library

- **Objective:** *Derive a set of execution stages of synchronous execution and bind all operations with appropriate devices to these stages, while minimizing the* ***device count***
- ***Solve by Integer Linear Programming (ILP)***

ILP Formulation

Notation	
O	An operation set with each operation indexed by *i*
D	A device set with each device indexed by *j*
S	A stage set with each stage indexed by *k*
D_i	A available device set *D* for operation i, $\forall_i \in O, Di \subseteq D$
T_j	Execution time T_j for device *j*, $\forall j \in D$
$o_{i,j,k}$	0-1 variable, operation *i* is bound with device *j* and executed in stage *k*
b_k (f_k)	Begin (finish) time for stage *k*
r_j	Required number for device *j*

ILP Formulation

- Objective: minimize the total required device count
- Subject to:

$$Minimize: \sum_{j \in D} r_j$$

  - 1. Exclusivity constraints

$$\sum_{j \in D_i} \sum_{k \in S} o_{i,j,k} = 1, \forall i \in O$$

  - 2. Timing constraints

$$0 \leq b_k \leq f_k \leq T_{max}, \forall k \in S$$

  - 3. Synchronization constraints

$$f_{k_1} \leq b_{k_2}, \forall k_1 \in S, \forall k_2 \in S, k_1 < k_2$$

$$f_k - b_k - T_j o_{i,j,k} \geq 0, \forall k \in S, \forall i \in O, \forall j \in D_i$$

  - 4. Dependency constraints

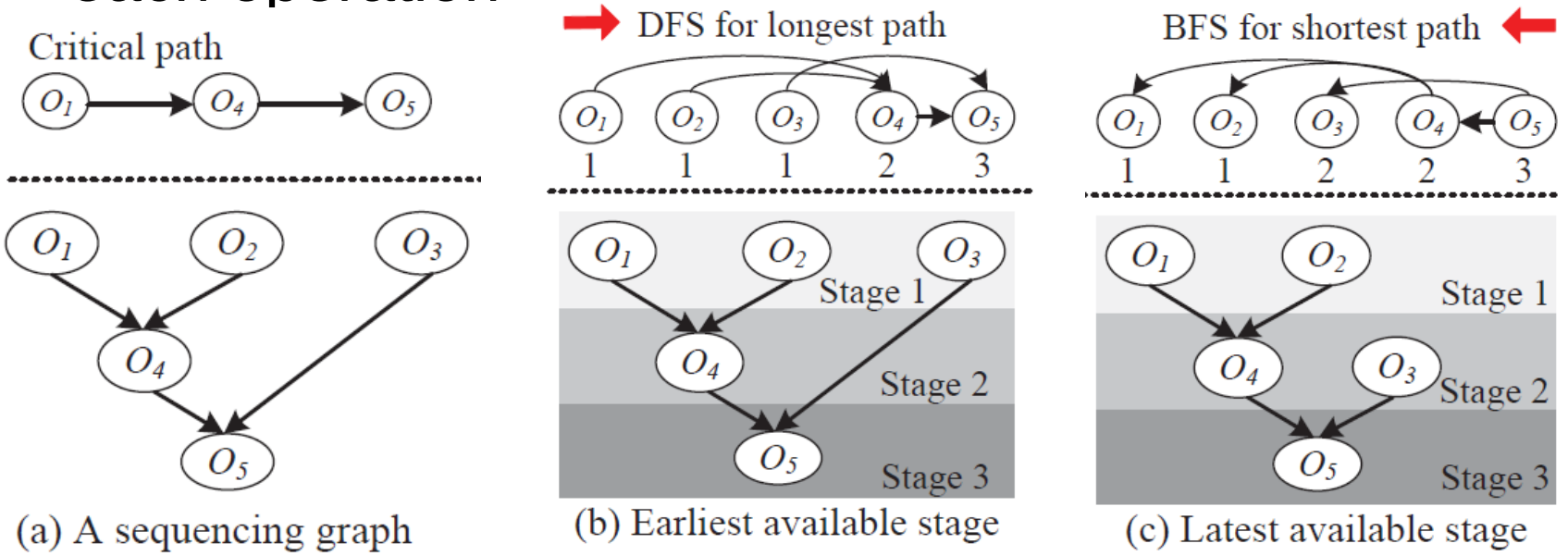
$$f_{k_1} - b_{k_2} + M(o_{i_1,j_1,k_1} + o_{i_2,j_2,k_2} - 2) \leq 0,$$
$$\forall i_1 \rightarrow i_2, j_1 \in D_{i_1}, j_2 \in D_{i_2}, k_1 \in S, k_2 \in S$$

  - 5. Device requirement

$$r_j \geq \sum_{i \in O} o_{i,j,k}, \forall j \in D, \forall k \in S$$

Solution Space Reduction

- The number of execution stages for each operation causes huge computation time
  - Ex: O_1 can be executed in stage *1, 2, …, n*
- Reducing the complexity by assigning stage interval to each operation



  - => O_1 can only be executed in stage *1*
  - => O_3 can be executed during stage *1~2*

Fluidic-Chip Co-design Methodology

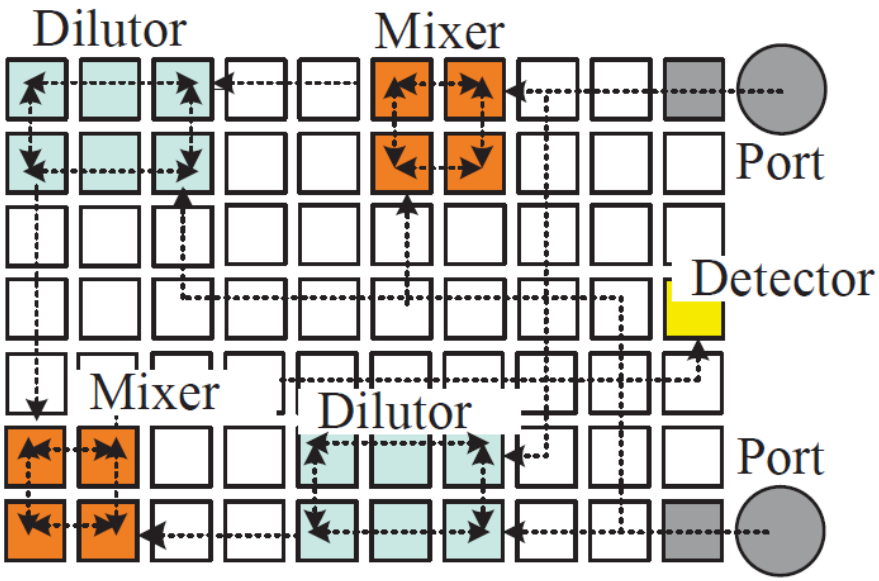
Device Count Aware
Synchronous Scheduling

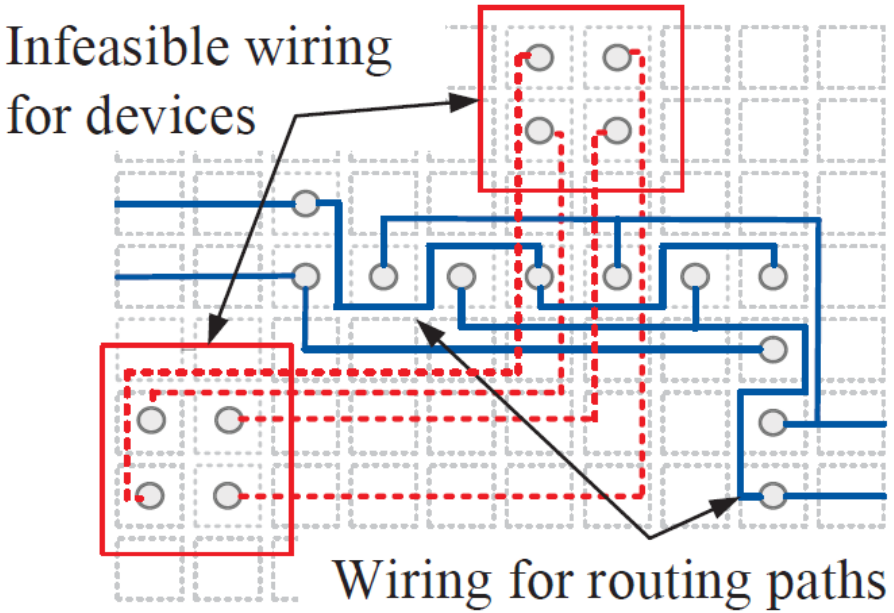
Dedicated Chip Layout

Electrode classification,
Guided Pin Assignment, and
Wiring

Wiring Problem

- Conventional design flow spread out the droplet routing paths around device

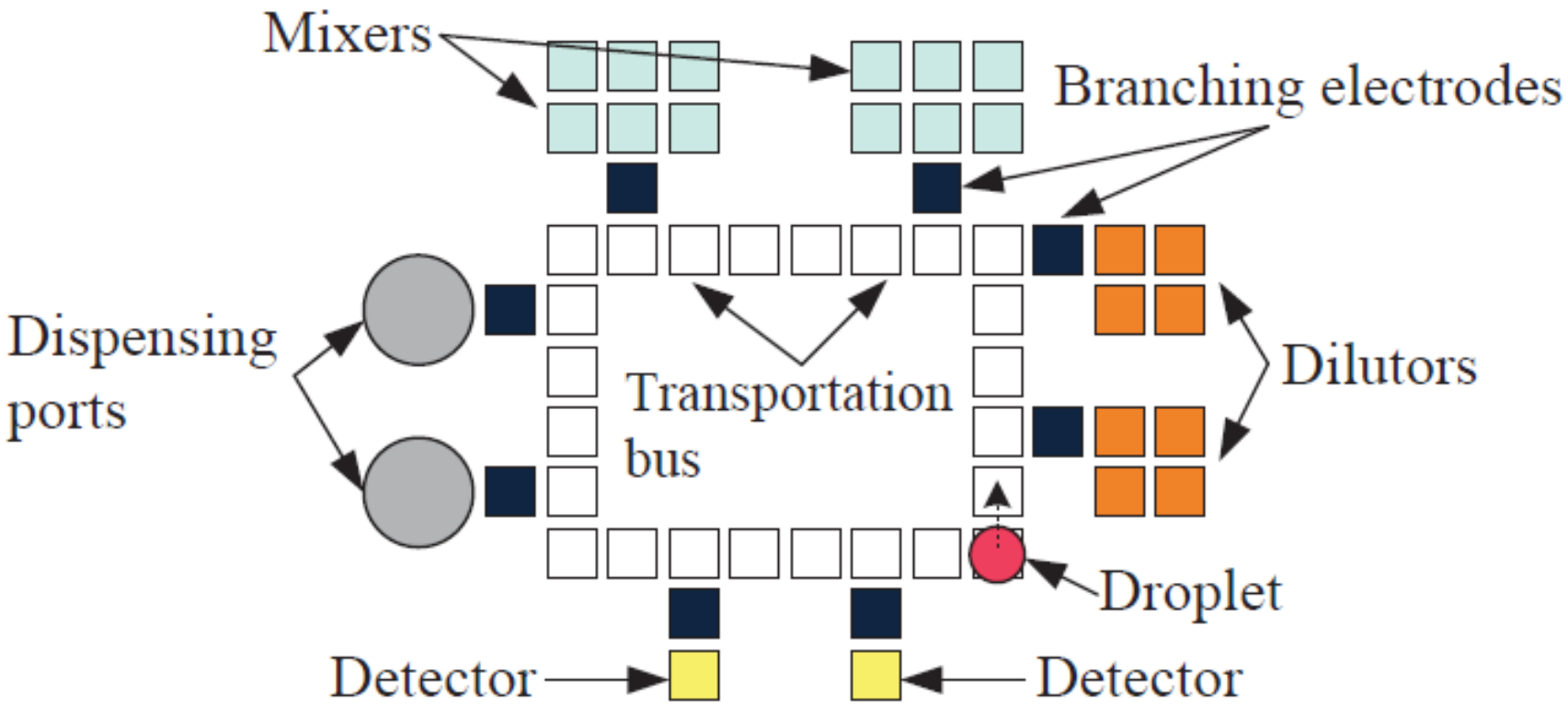




- Wiring complexity may trigger many blocking or detouring problems

Dedicated Chip Layout

- Surrounding devices
- Branching electrodes
- Central transportation bus



Advantages of Dedicated Chip Layout

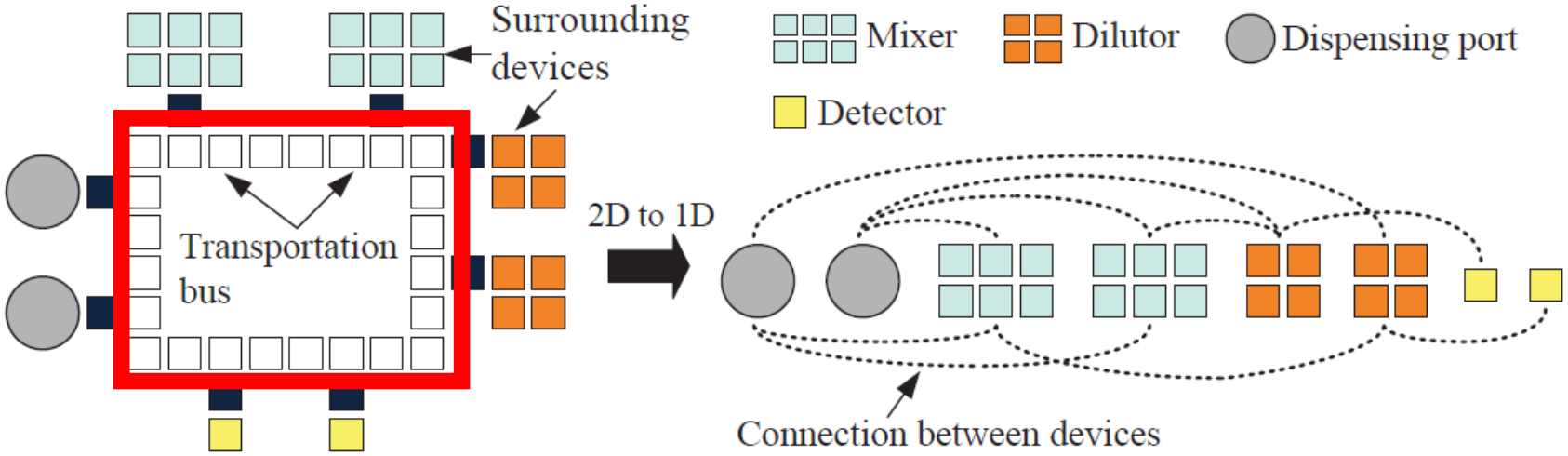
- Since the outside surrounding devices are fixed without arbitrary movements and the inside bus is independently oriented without interference with devices, the wiring problem can be avoided

- In addition to routing droplets, the central transportation bus can serve as storages for intermediate droplets. Thus, extra storing devices for holding droplets are omitted and thus the design effort can be reduced

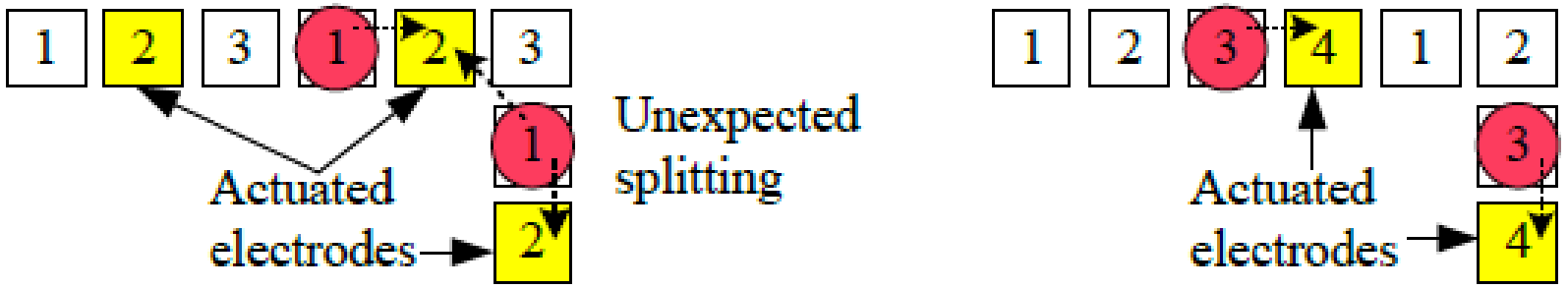
- Instead of constructing the chip layout in 3D configuration, the proposed layout focuses on determining the 2D orientation of devices are transportation bus, which the design complexity can be reduced

Linear Assignment for Device Ordering

- Determine the device ordering to minimize the transportation time



- Transportation bus-length determination



(a) 3 pins for droplet routing

(b) 4 pins for droplet routing

Length = 4 x 4 = 16

Fluidic-Chip Co-design Methodology

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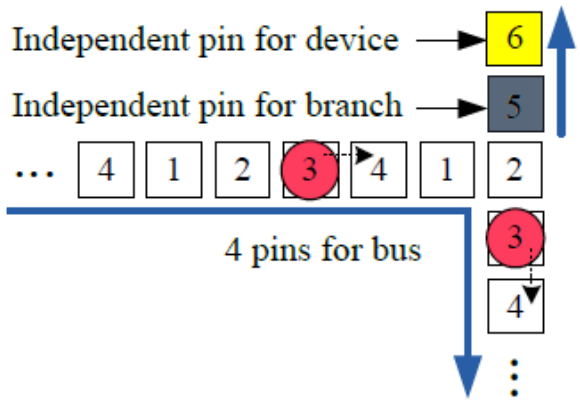
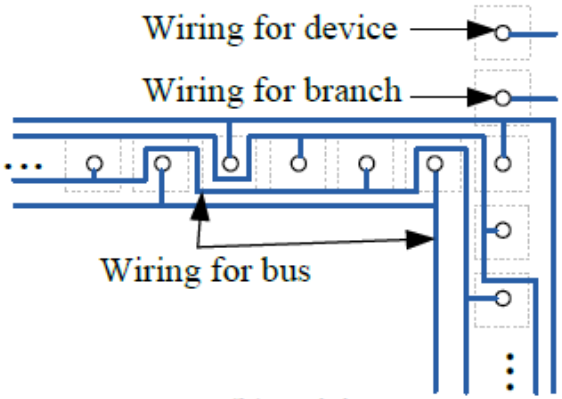
Electrode classification,
Guided Pin Assignment, and
Wiring

Electrode Classification, Guided Pin Assignment and Wiring

- Electrode classification
  - Bus
  - Branch
  - Device

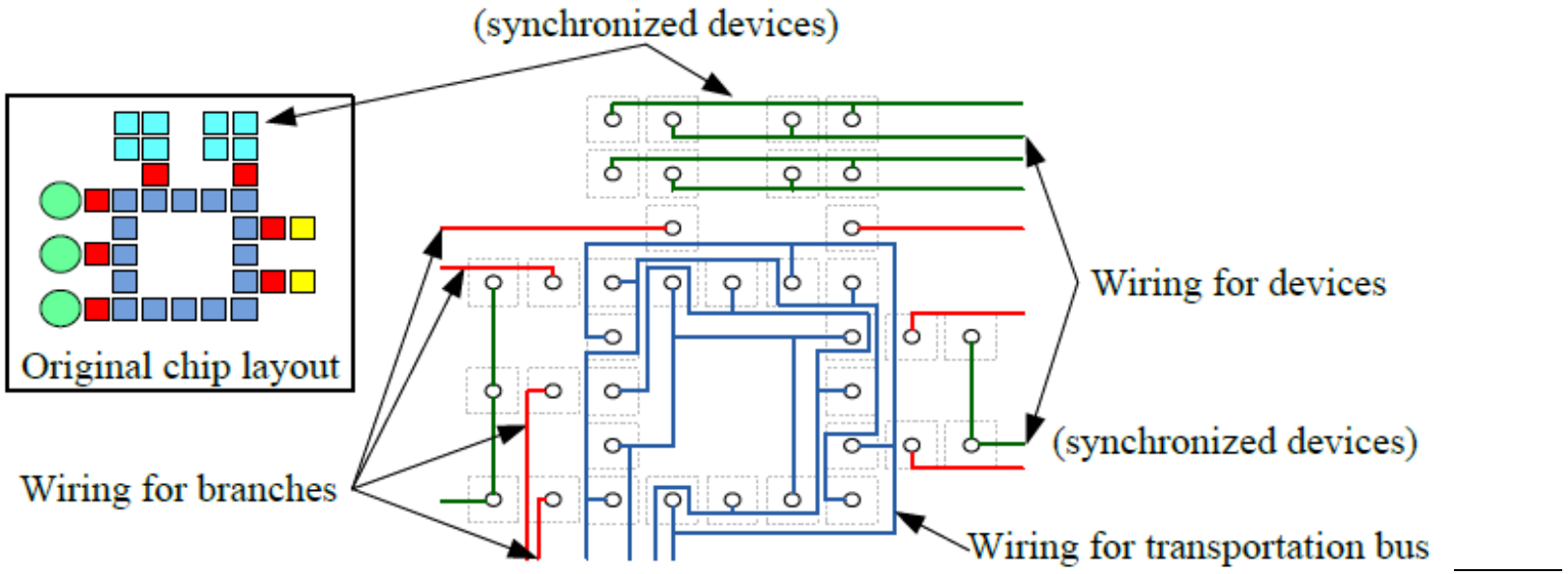


(a) Pin assignment



(b) Wiring

- Guided pin assignment and wiring



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Experimental Settings (1/2)

- Implement our algorithm in C++ language on a 2 GHz 64-bit Linux machine with 16GB memory
  - Use GLPK as ILP solver
- Evaluate with 4 real-life chips
  - Multiplexed assay
  - DNA sequencing assay
  - In-vitro diagnostic assay
  - PCR amplification assay

Experimental Settings (2/2)

- Comparison between conventional design flow and ours
- 4 state-of-the-art works from the same group from Duke Univ.
  - F. Su and K. Chakrabarty, “Architectural-level synthesis of digital microfluidics-based biochips”, IEEE/ACM ICCAD’04
  - F. Su and K.Charkrabarty, “Module placement for fault-tolerant microfluidics-based biochips”, ACM TODAES’06
  - F. Su, W. Huang and K. Chakrabarty, “Droplet routing in the synthesis of digital microfluidic biochips”, IEEE/ACM DATE’06
  - T. Xu and K. Charkrabarty, “Broadcast electrode-addressing for pin-constrained multi-functional digital microfluidic biochips”, IEEE/ACM DAC’08

Experimental Results (1/3)

Assay	Conventional design				Ours			
	#D	T	#P	#WL	#D	T	#P	#WL
Multiplexed	7	63	25	N/A	6	67	14	562
DNA	11	67	38	1094	9	79	22	610
Diagnostic	11	50	26	N/A	9	63	18	748
PCR	14	26	14	N/A	10	47	18	820
Total	43	206	95		34	256	72	

#T: assay completion time (sec.) #D: device count #P: pin-count
#WL: wirelength (measured by the number of used grids)

Experimental Results (2/3)

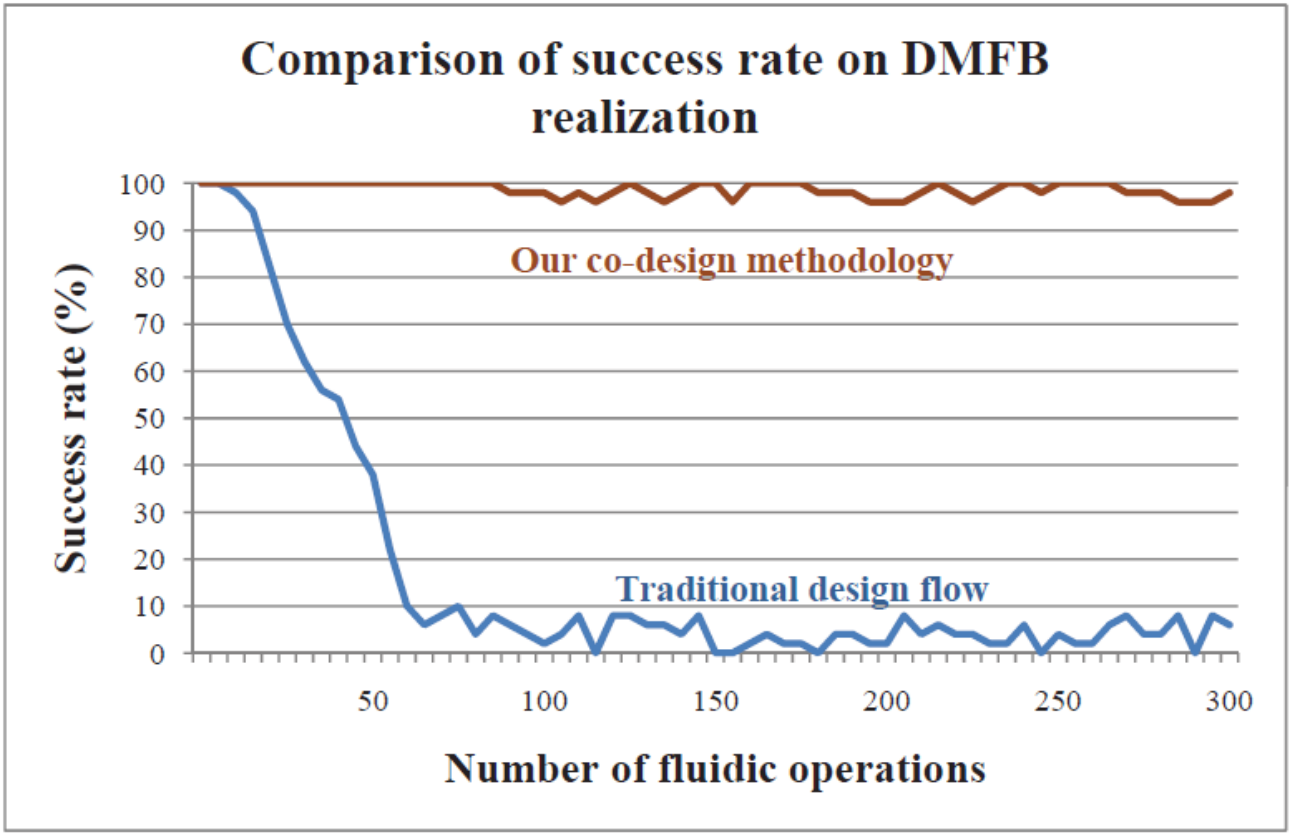
- Comparison between optimal ILP and reduced ILP

Assay	Optimal ILP		Reduced ILP		
	#D	CPU	#D	Error	CPU
Multiplexed	6	> 1 day	6	0%	0.04
DNA	11	> 1 day	11	0%	0.07
Diagnostic	7	> 1 day	9	29%	0.12
PCR	9	> 1 day	10	11%	0.10

#D: device count CPU: cpu run time in seconds

Experimental Results (3/3)

- Comparison of success rate on DMFB realization between ours and conventional design flow
  - For each problem size we simulate the fluidic operations and generate 50 assays to test the success rate of DMFB realization



Outline

Introduction

Fluidic-Chip Co-design Methodology

Experimental Results

Conclusions

Conclusions

- We presented the first integrated fluidic-chip co-design methodology for DMFBs
- We also comprehensively identified the factors that would affect DMFB realization and explore properties that are favorable for bridging the fluidic-chip performance gap
- Experimental results demonstrated that our methodology can achieve high success rate of DMFB realization over the conventional flow

Thank You for Your Attention!