Flexible Self-aligned Double Patterning Aware Detailed Routing with Prescribed Layout Planning

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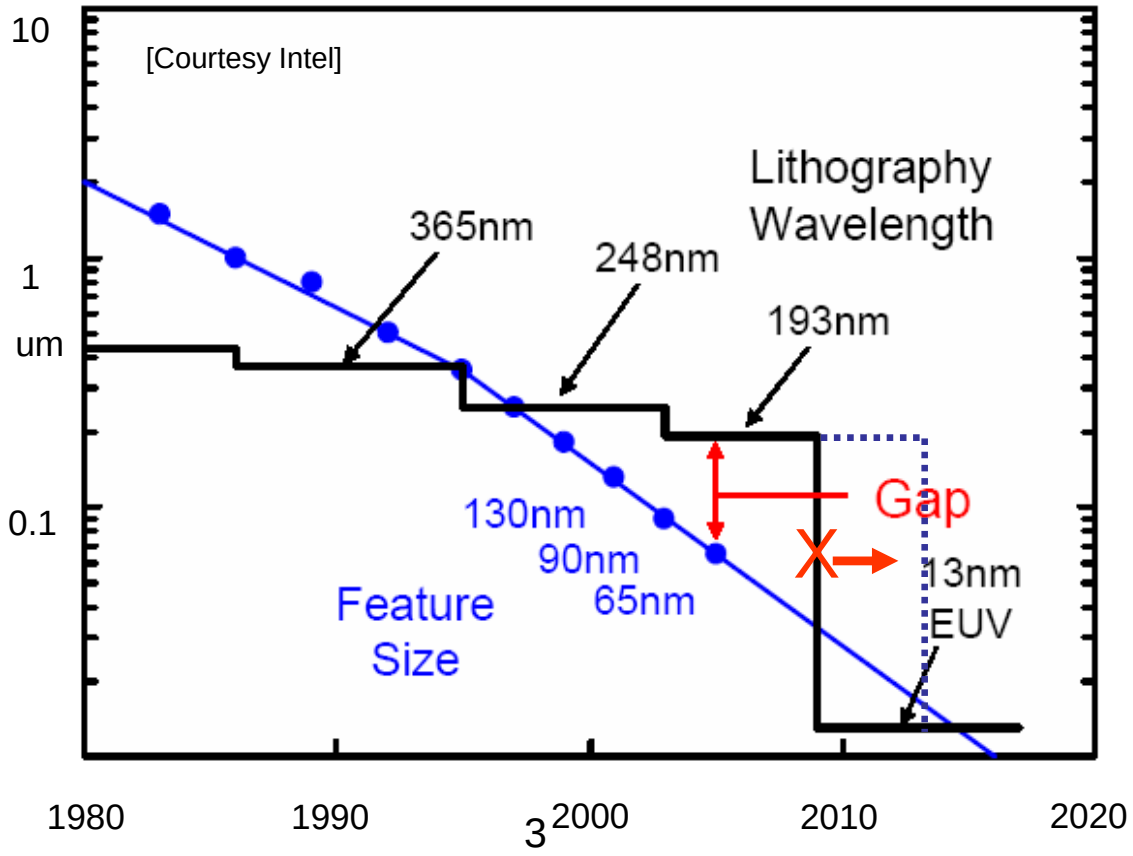
Outline

- Introduction
- Motivation
- SADP-Compliant Routing Guidelines
- SADP-Aware Detailed Routing
- Experimental results
- Conclusion

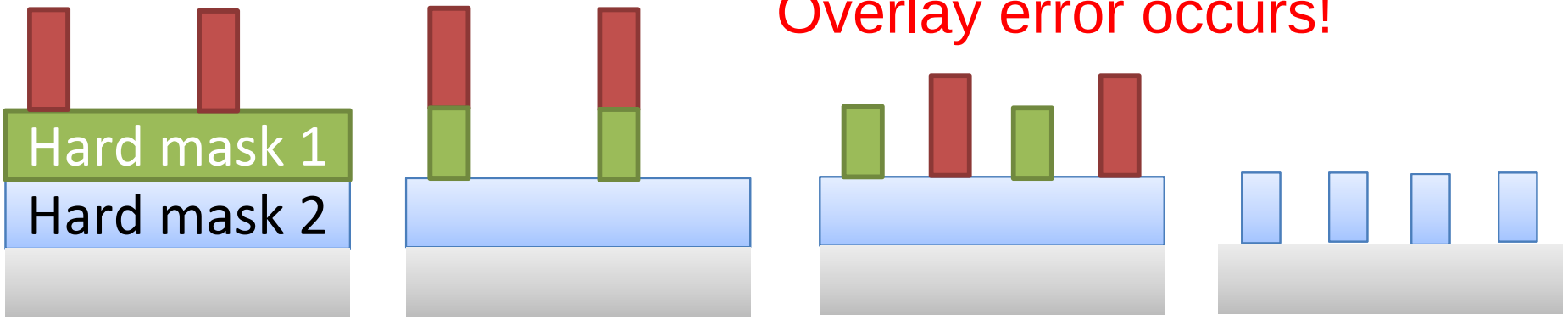
Introduction

- 193nm lithography reaches its limit for sub-22nm
- Next generation lithography not yet ready
  - EUV, E-beam, …
- DPL/MPL is necessary to meet current demand



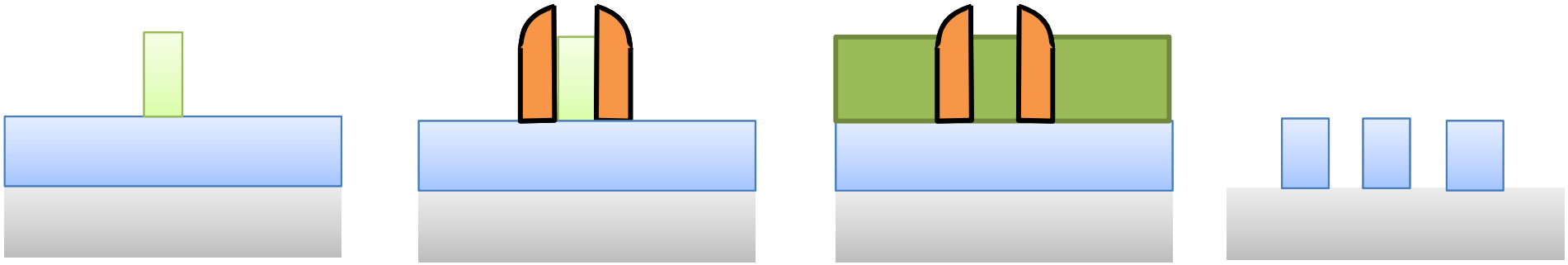
SADP Advantage

- Conventional LELE DPL: 2 exposures



1st exposure | etch | 2nd exposure | etch

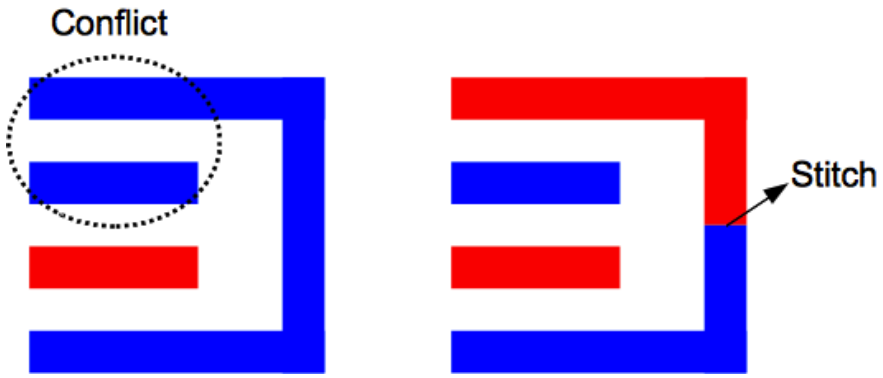
- SADP: 1 exposure + automatic aligned
  - Better overlay control



mandrel mask exposure | Spacer deposition | Substrate material filling | trimming

SADP Challenges

- No stitch allowed to split conflicting patterns



- Patterns interaction affects printing image quality
- Layout decomposition more complicated for 2D patterns

→Might be too late to apply SADP after routing is done

Previous Works

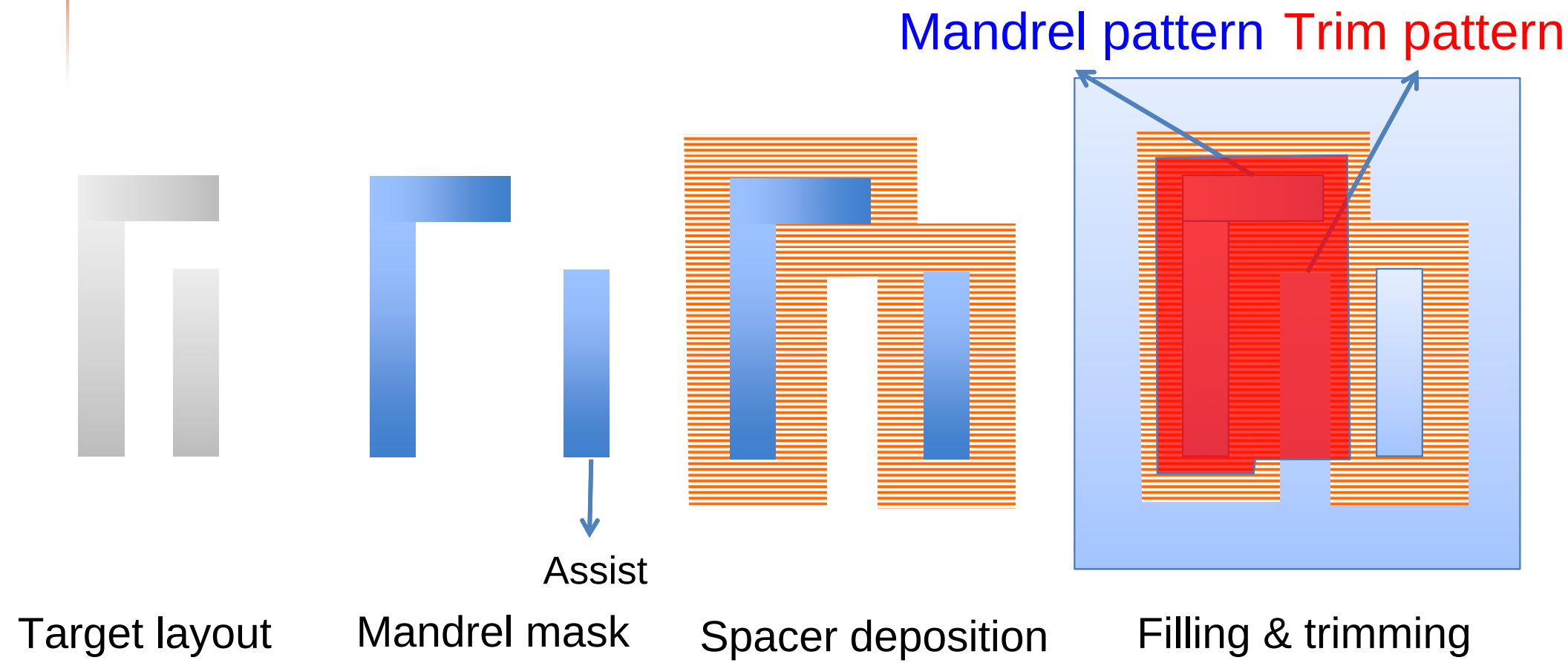
- LELE DPL-friendly routing
  - Main optimization goal: stitch minimization to reduce overlay error
    - M. Cho et al [ICCAD 2008], K. Yuan et al [DAC 2009], X. Gao et al [DATE 2010], etc
- SADP
  - Most works focus on layout decomposition
    - H. Zhang et al DAC 2011, Y. Ban et al DAC 2011, etc
  - SADP-aware routing
    - M. Mirsaeedi et al SPIE 2011
    - Improve pattern quality by increasing spacer alignment
    - Lack of solution for conflicts

Main Contribution

- Consider SADP compliancy in detailed routing stage
  1. Perform simultaneous routing and layout decomposition
  2. Propose SADP-compliant routing guidelines to prevent negative pattern interaction
  3. Perform multi-layer routing to prevent conflicts by proper layer assignment

Preliminaries

- Mandrel pattern: directly defined by mandrel mask
- Trim pattern: indirectly reserved by trim mask



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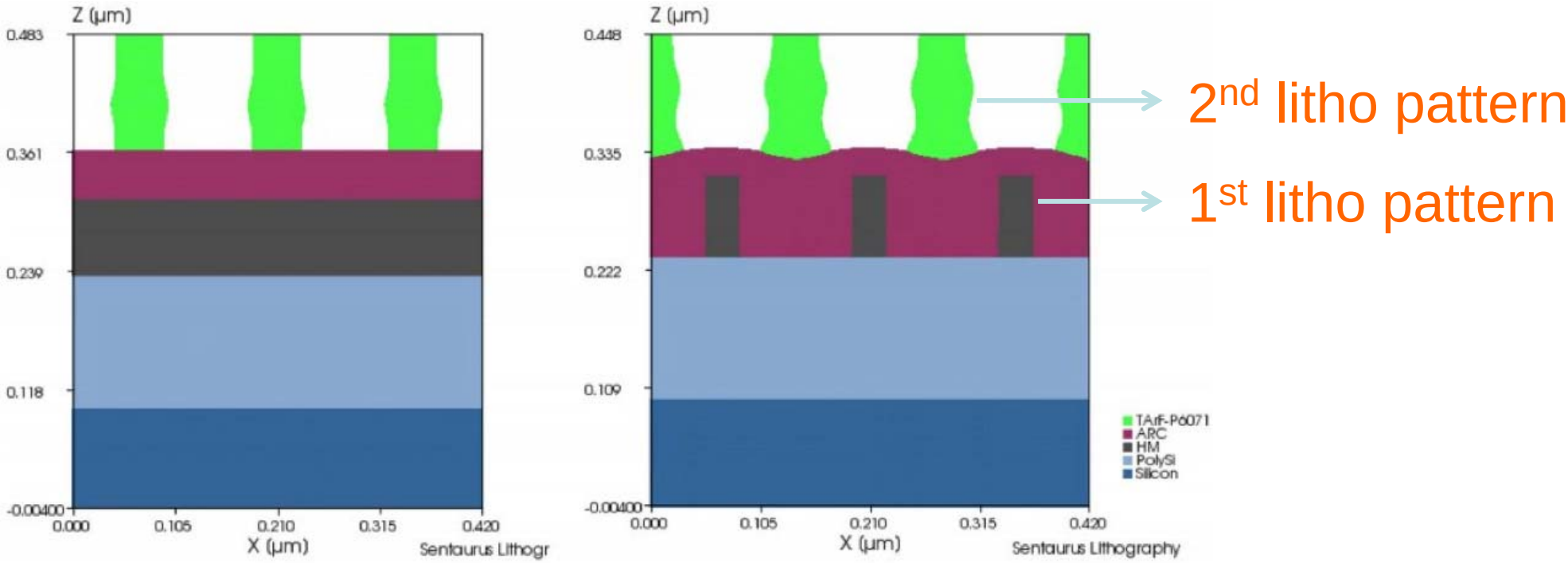
SADP-Compliant Routing Guidelines

- When a routing path *p* is to be assigned to either mandrel or trim mask
  1. Prefer mandrel mask when assigning *p* to mandrel and trim are both conflict-free
  2. Seek to aligned to more spacer when *p* is assigned to trim mask
  3. Encourage mandrel pattern and trim pattern to be separated by at least “forbidden spacing”

SADP-Compliant Routing Guideline 1

- Prefer mandrel (1st mask lithography)
  - Printability degrades for trim mask (2nd mask lithography) due to the topography generated by 1st lithography on the wafer
  - Printability for mandrel pattern is more guaranteed



Curtesy [K. Lucas et al, JM3 2009]

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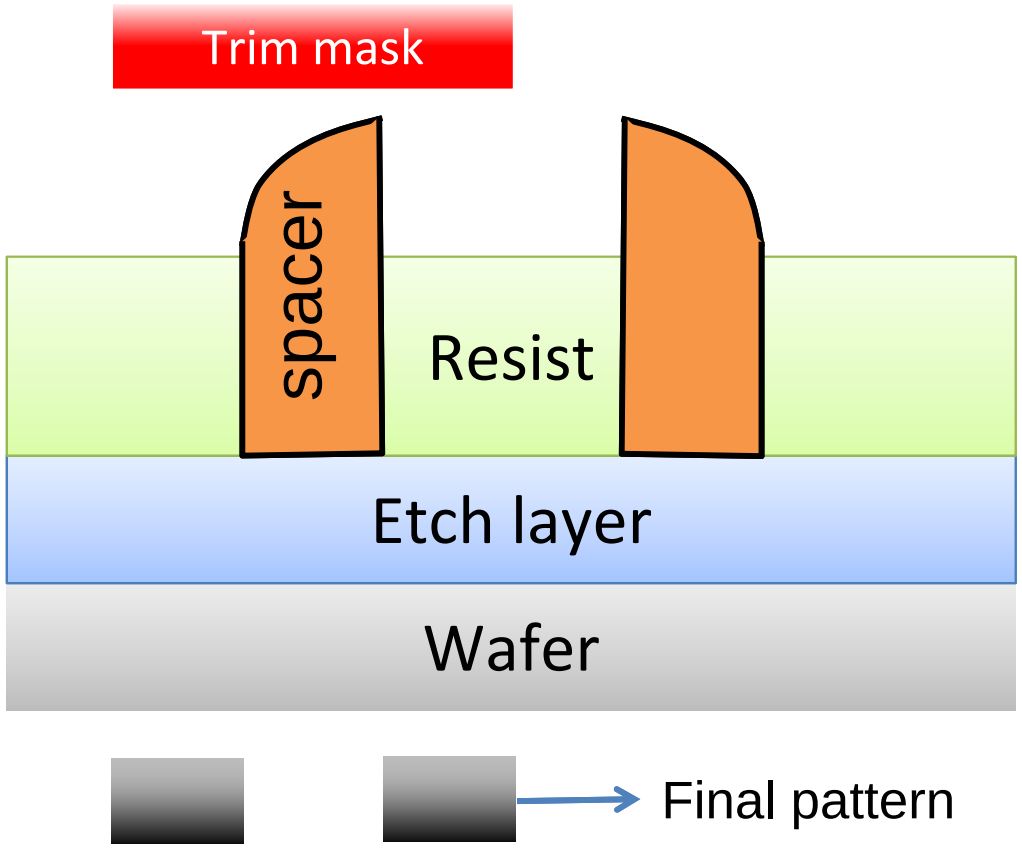
SADP-Compliant Routing Guideline 2

- Trim pattern seek to aligned to more spacer
- Case 1: trim pattern not aligned to spacer



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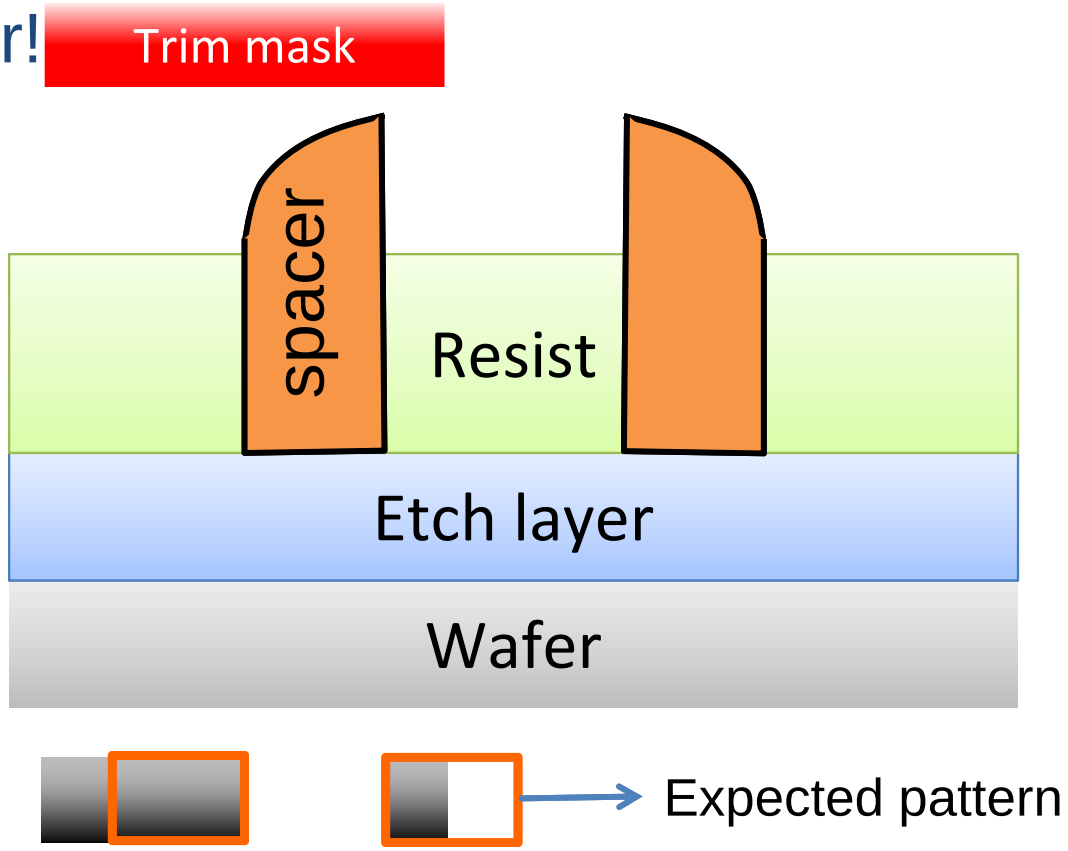
Overlay error!



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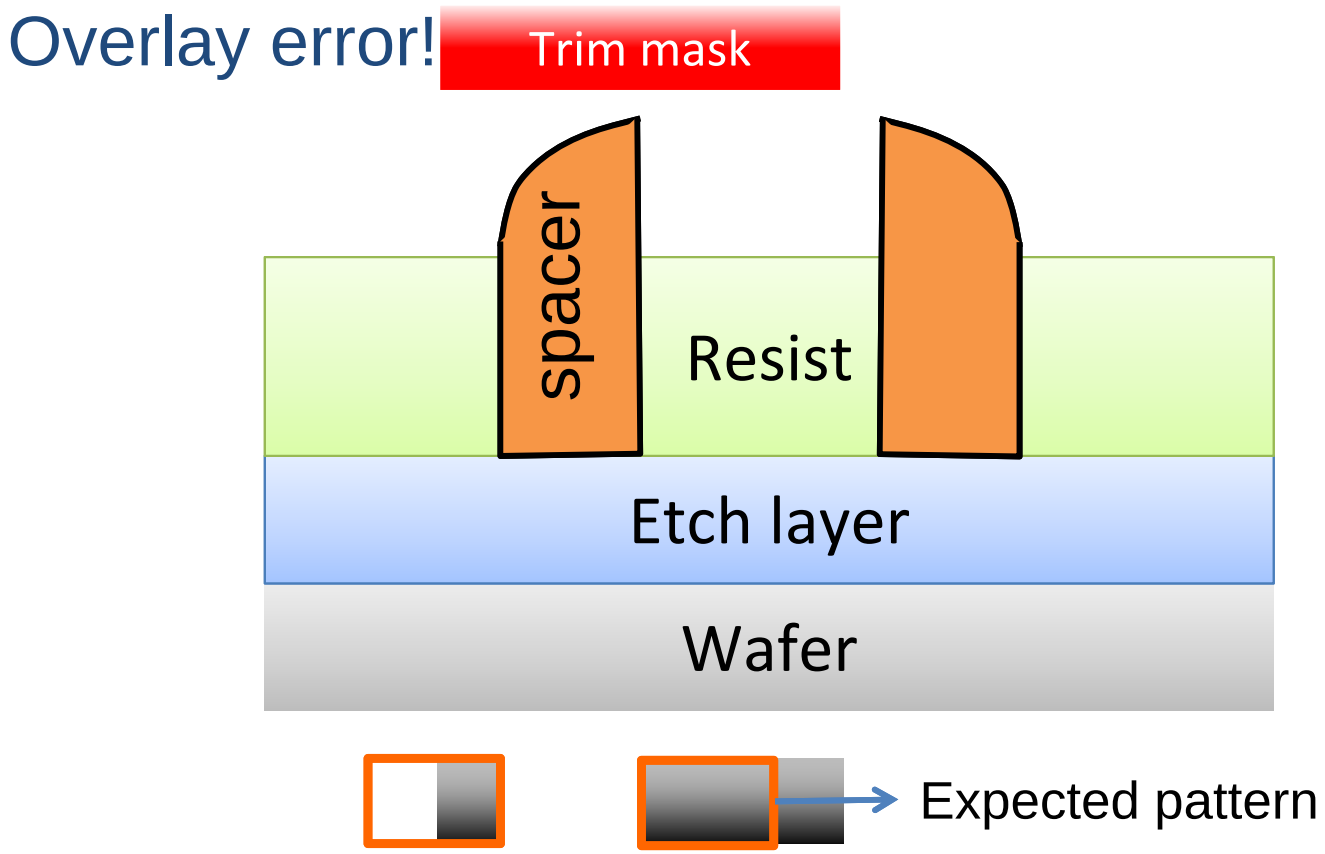
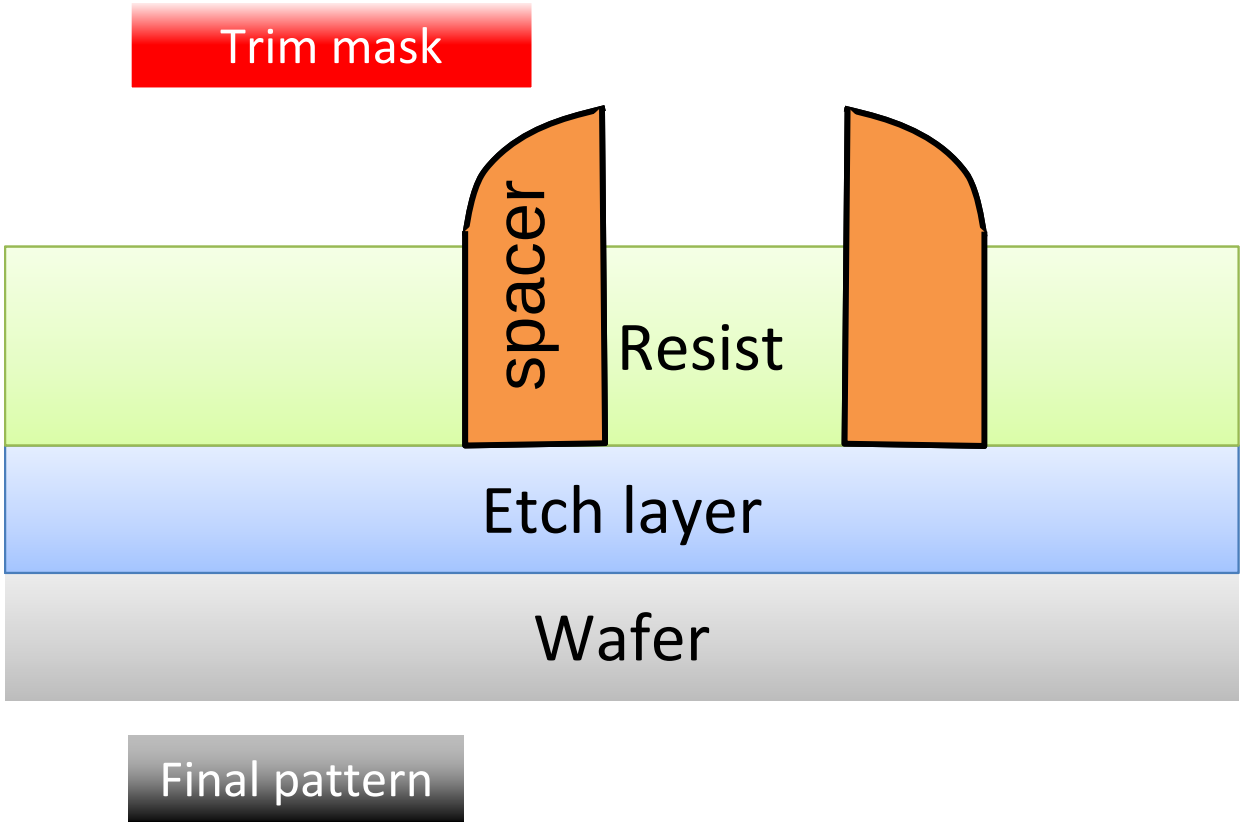


SADP-Compliant Routing Guideline 2

- Trim pattern seek to aligned to more spacer
- Case 2: 1 side of trim pattern aligned to spacer



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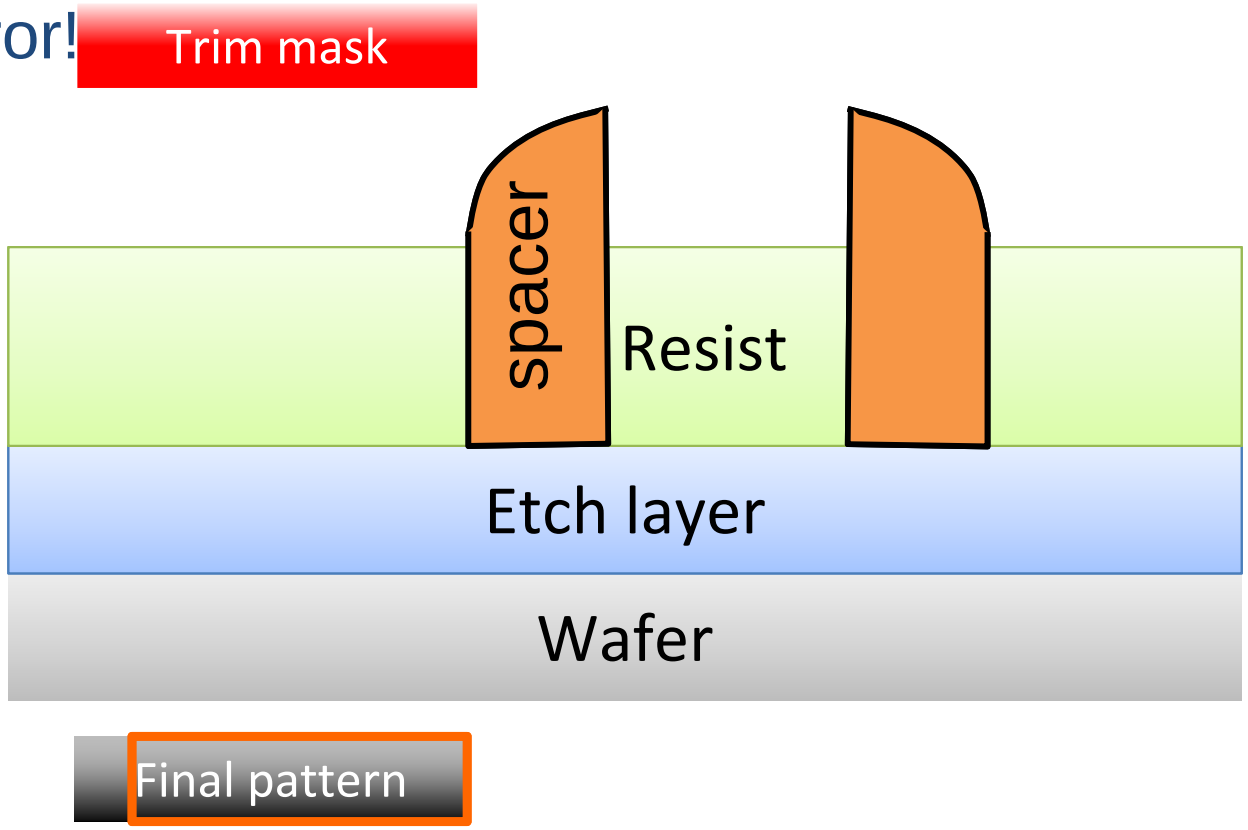

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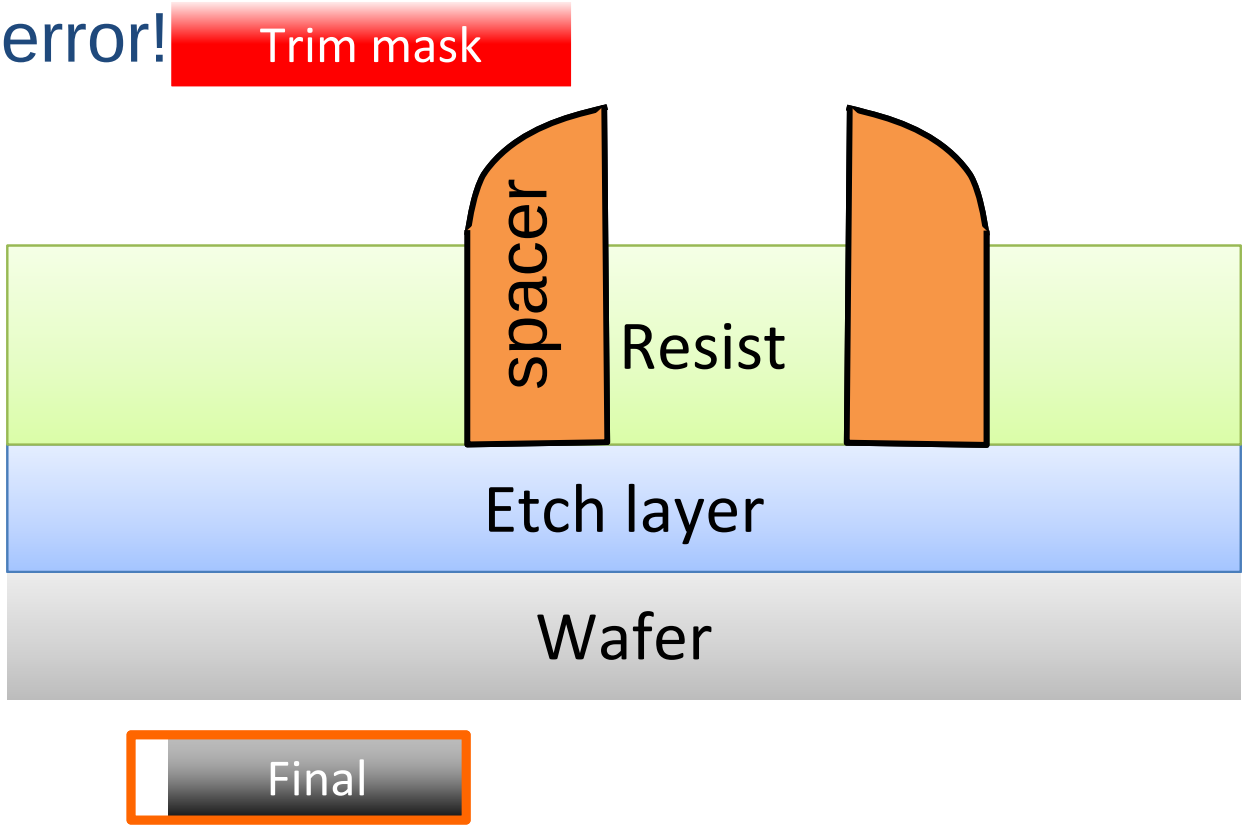
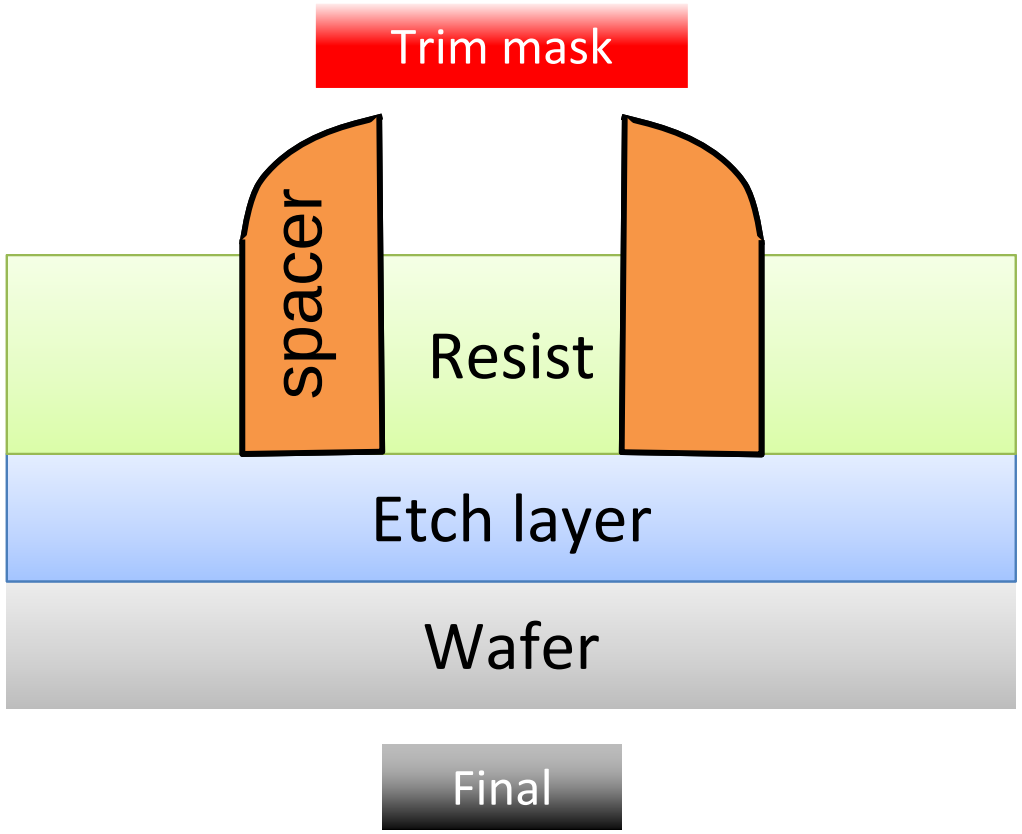


SADP-Compliant Routing Guideline 2

- Trim pattern seek to aligned to more spacer
- Case 3: both sides of trim aligned to spacer



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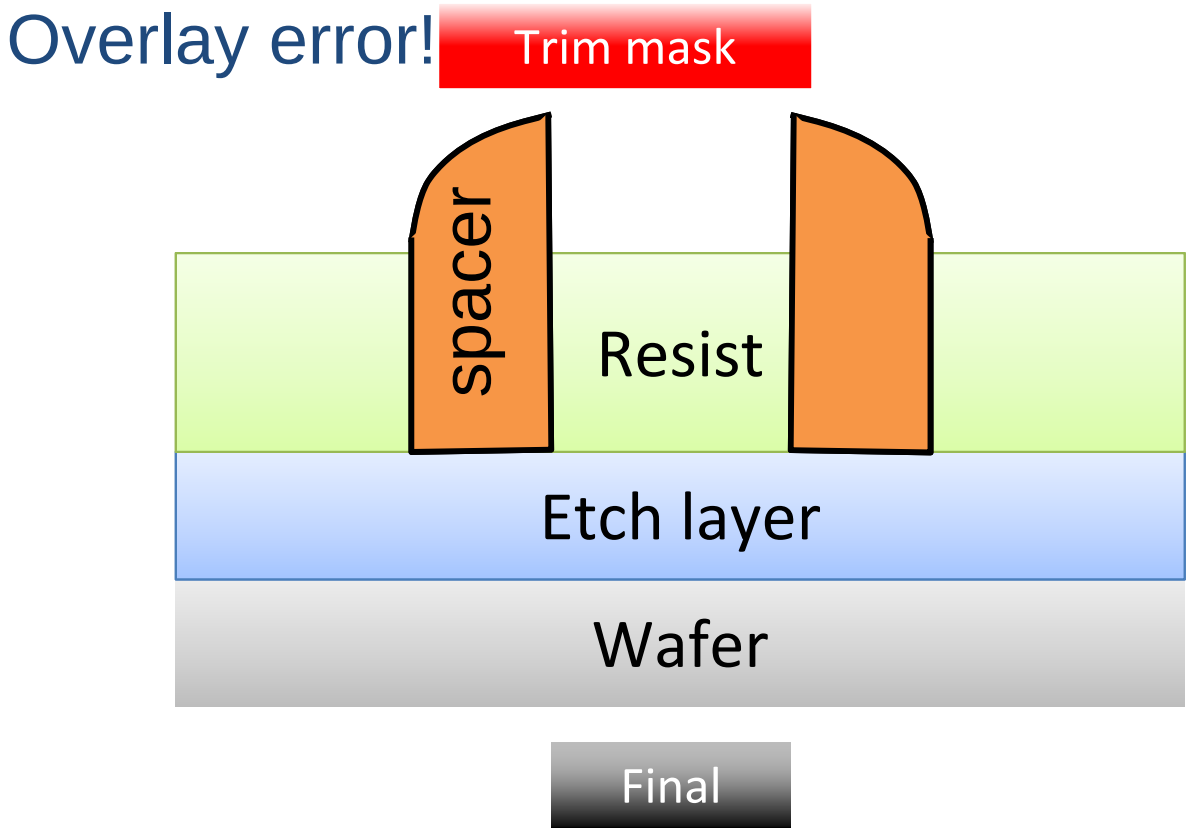

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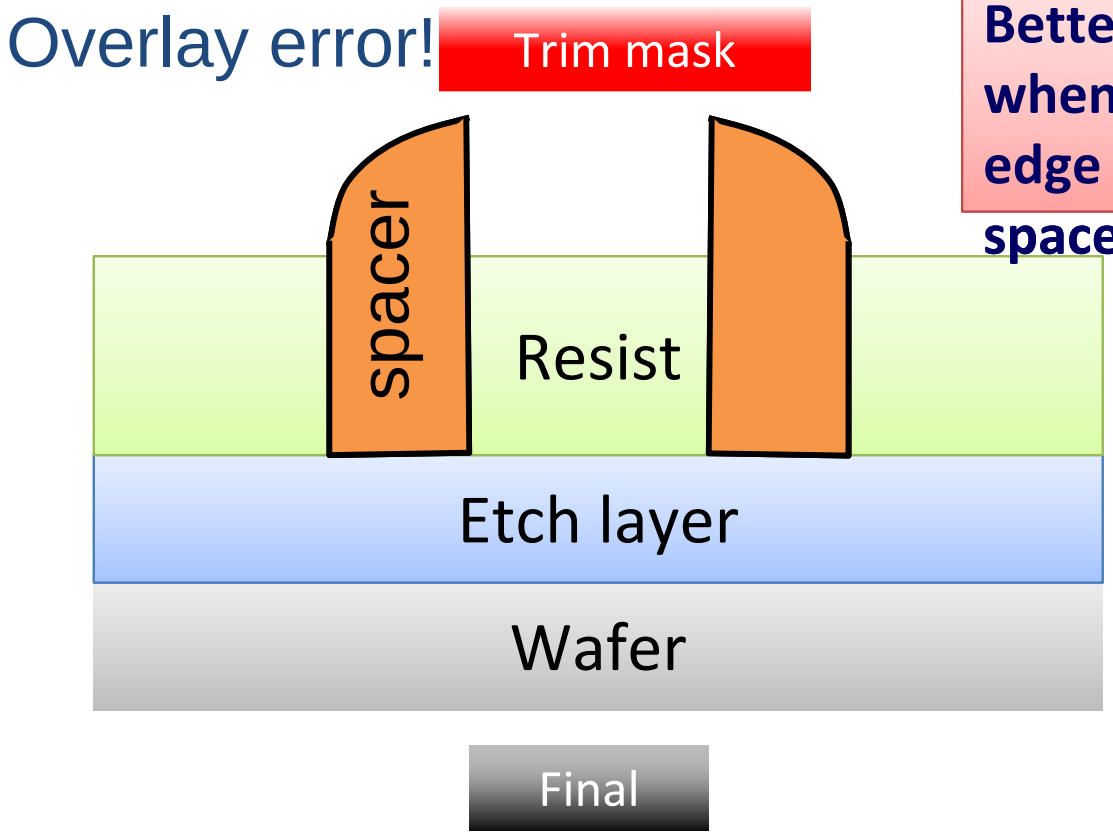

Better overlay control when more pattern edge is protected by spacer

SADP-Compliant Routing Guidelines

- When a routing path *p* is to be assigned to either mandrel or trim mask
  1. Prefer mandrel mask when assigning *p* to mandrel and trim are both conflict-free
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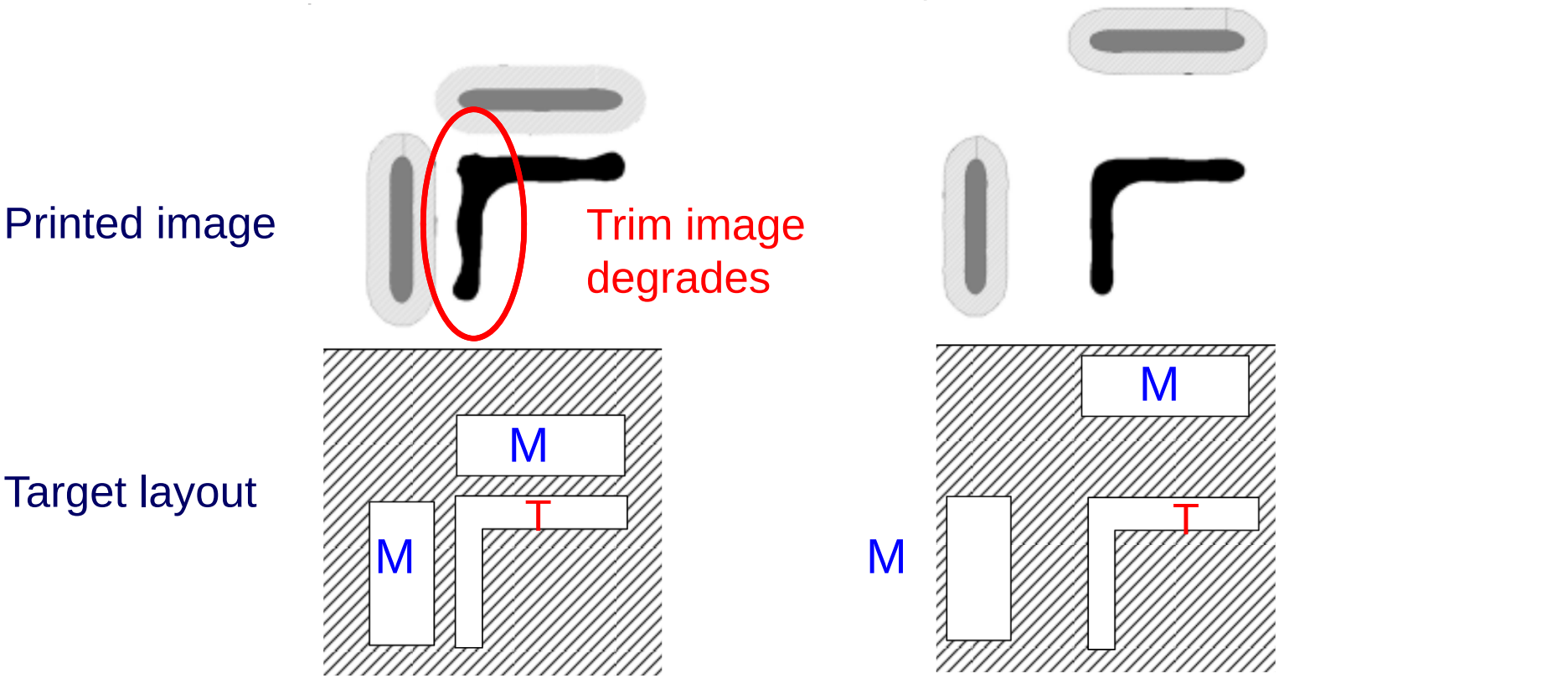
SADP-Compliant Routing Guideline 3

- Separate mandrel pattern and trim pattern by at least forbidden spacing
  - Trim pattern image interfered by close mandrel pattern
  - Forbidden spacing: recommended spacing for affordable trim pattern image degradation



Curtesy [M. Mirasaeedi et al, SPIE 2011]

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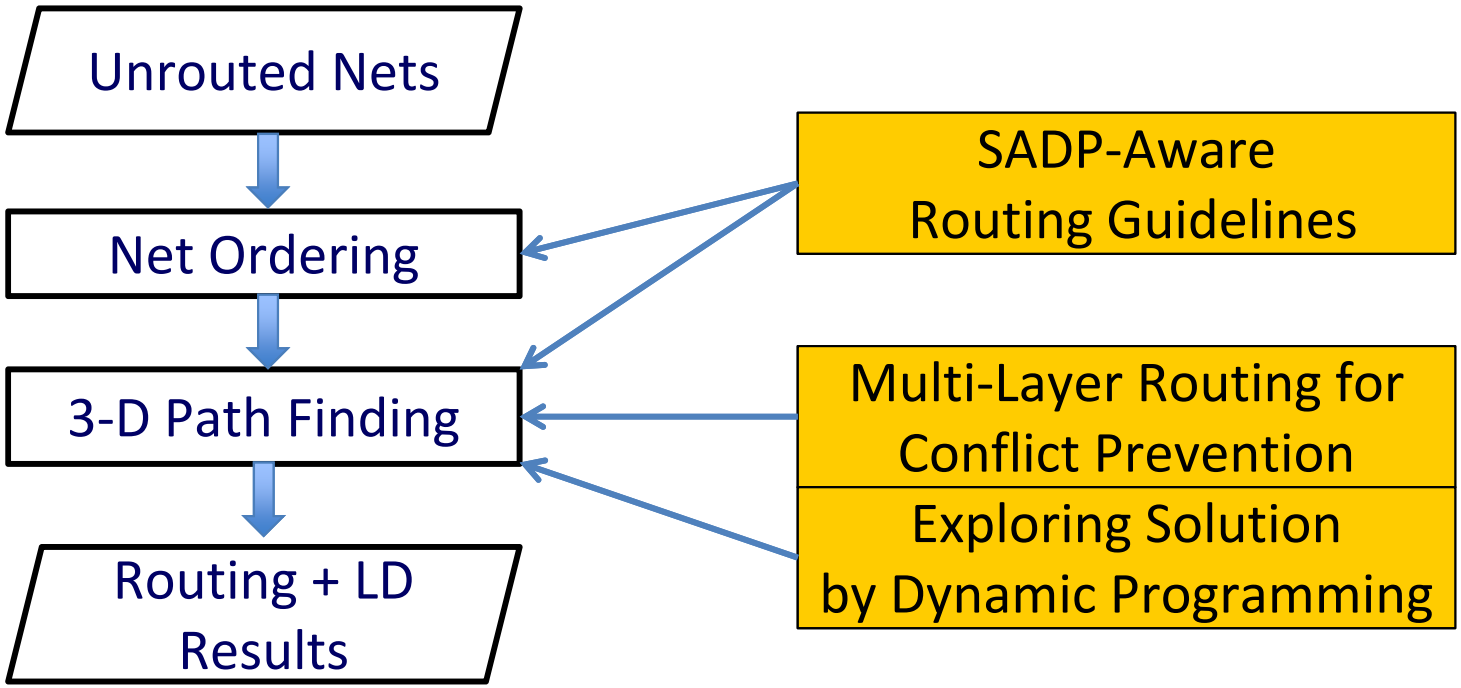
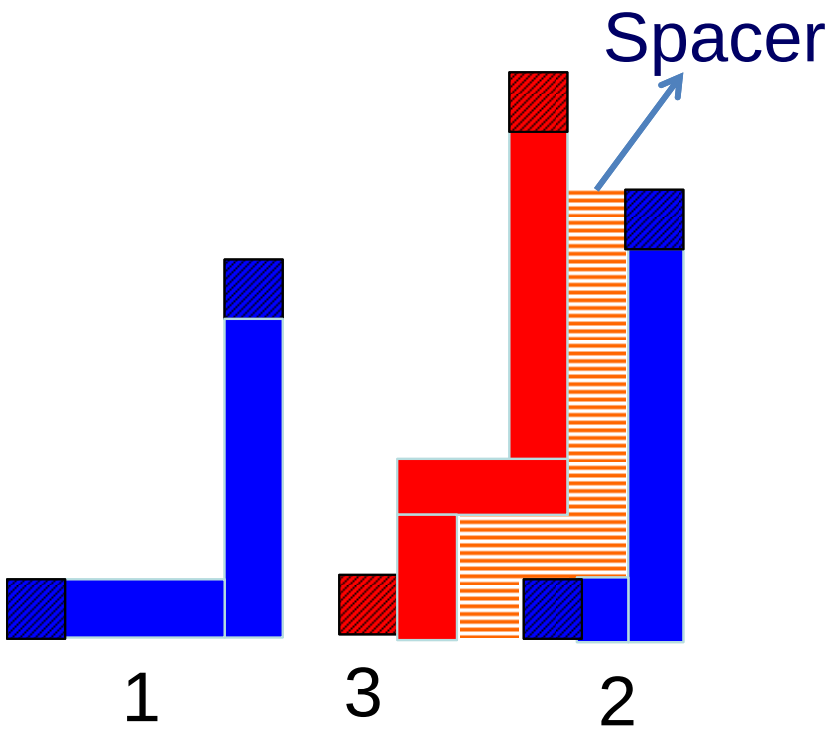
SADP-Aware Detailed Routing

- Correct by construction
  - Routing and layout decomposition result is done simultaneously
  - Objective
    - Conflict-free DPL mask assignment
    - Low wirelength
    - Good printed image



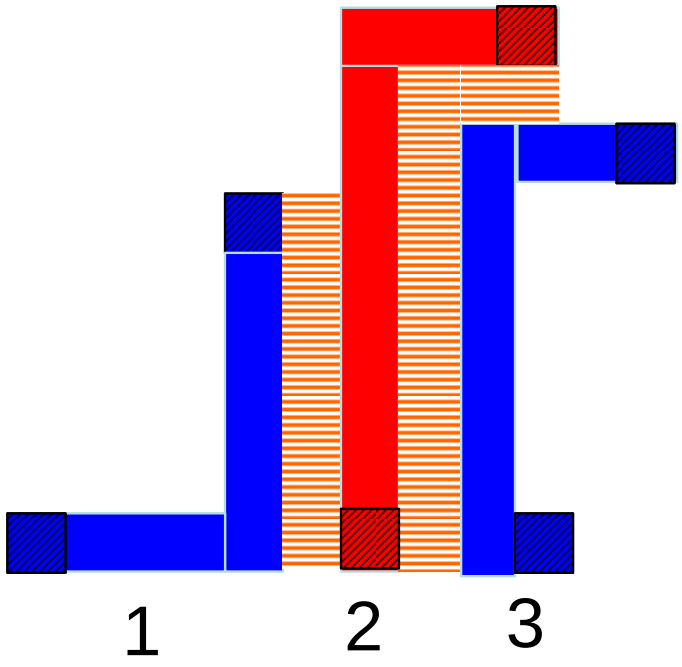
Pattern Quality Affected by Routing Order

- Good ordering encourages trim pattern to align to more spacer
  - Trade-off with wirelength



Ordered by net bbox size

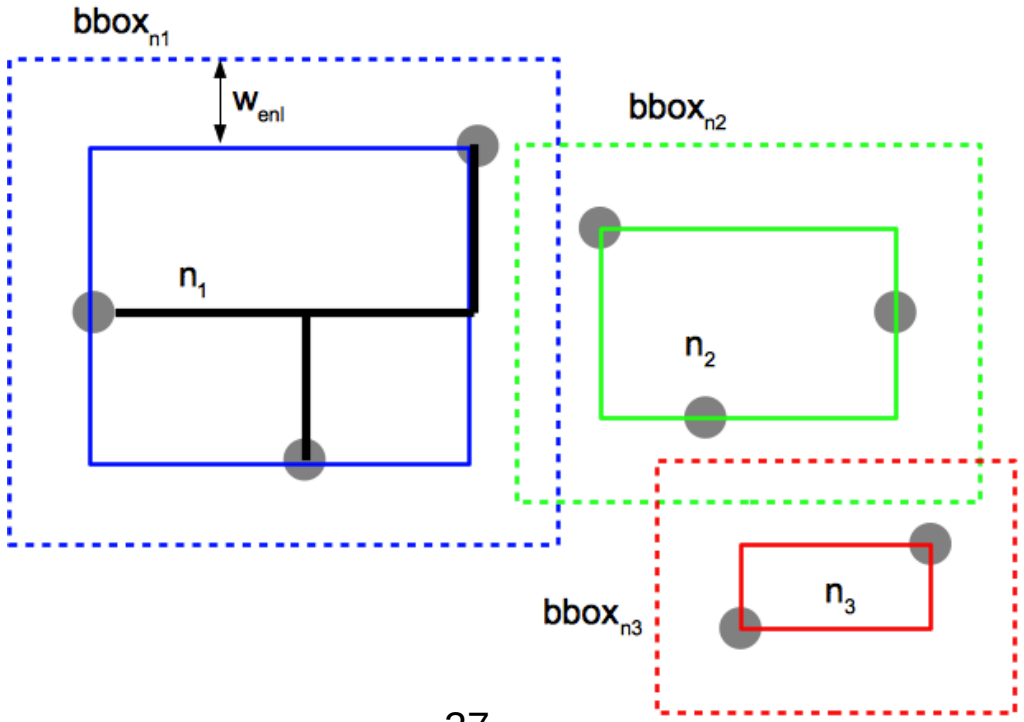
Aligned to more spacer



Route neighboring net together

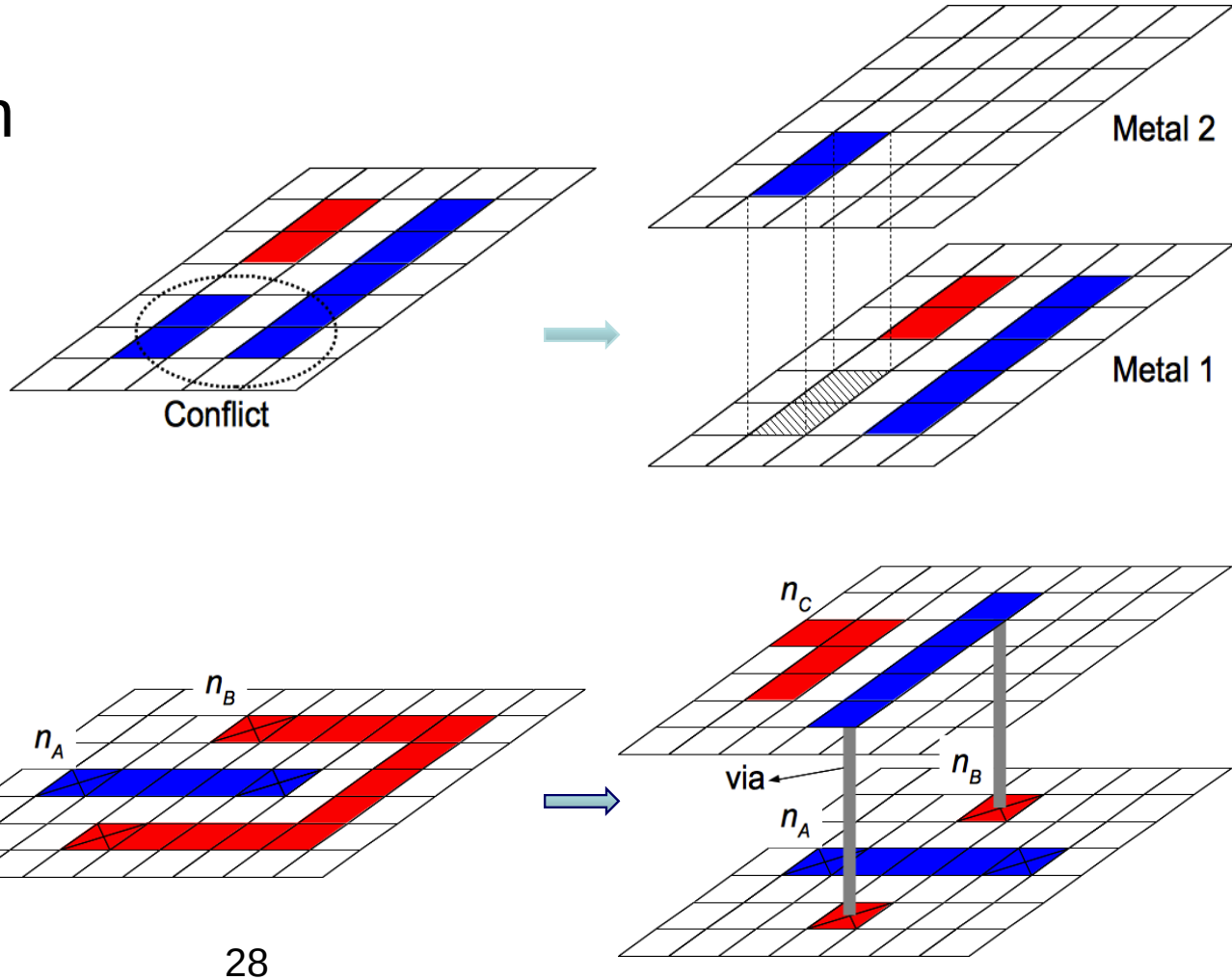
Neighborhood-based Net Ordering

- Give neighboring nets higher chance to share spacer
  - Each net is represented by its expanded bbox
  - Nets with overlapped bbox will be routed in series
  - Try to align to more spacer with affordable wirelength overhead



Conflict Prevention with Multi-Layer Routing

- Previous DPL-aware routing: single layer
- Multi-layer routing: solution space much larger
- Advantages
  - Conflict prevention
  - Detour avoidance
  - Flexible layout decomposition
  - More chances to align to spacer



Routing Cost Function

- $cost_j(m)/cost_j(t)$: accumulated cost from source to grid *j* when *j* is assigned to mandrel/trim mask
- Accumulated cost from grid g_i to its neighbor g_j
  - Same layer

Mandrel/trim
Pattern interaction
Spacer

$$\begin{cases} cost_j(m) = cost_i(m) + \alpha \cdot WL_{ij} + \beta \cdot SADPC_j(m) \\ cost_j(t) = cost_i(t) + \alpha \cdot WL_{ij} + \beta \cdot SADPC_j(t) \end{cases}$$

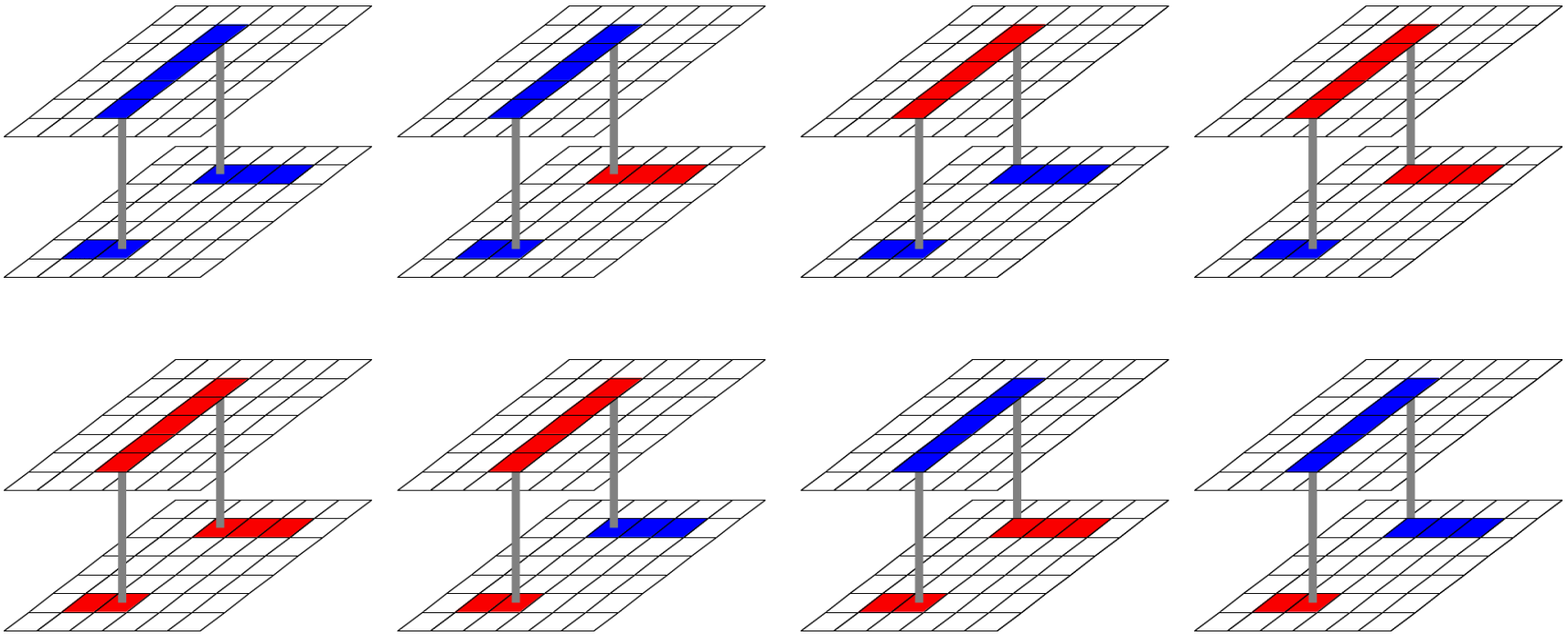
  - Different layer

Flexible layout decomposition

$$\begin{cases} cost_j(m) = \min\{cost_i(m), cost_i(t)\} + \\ \quad \alpha \cdot WL_{ij} + \gamma \cdot VIA + \beta \cdot SADPC_j(m) \\ cost_j(t) = \min\{cost_i(m), cost_i(t)\} + \\ \quad \alpha \cdot WL_{ij} + \gamma \cdot VIA + \beta \cdot SADPC_j(t) \end{cases}$$

3-Dimensional Path Finding

- Simultaneously routing and layout decomposition
- Whenever a grid is reached
  - Consider assigning it to mandrel or trim
  - Candidate solutions blow when exploring paths



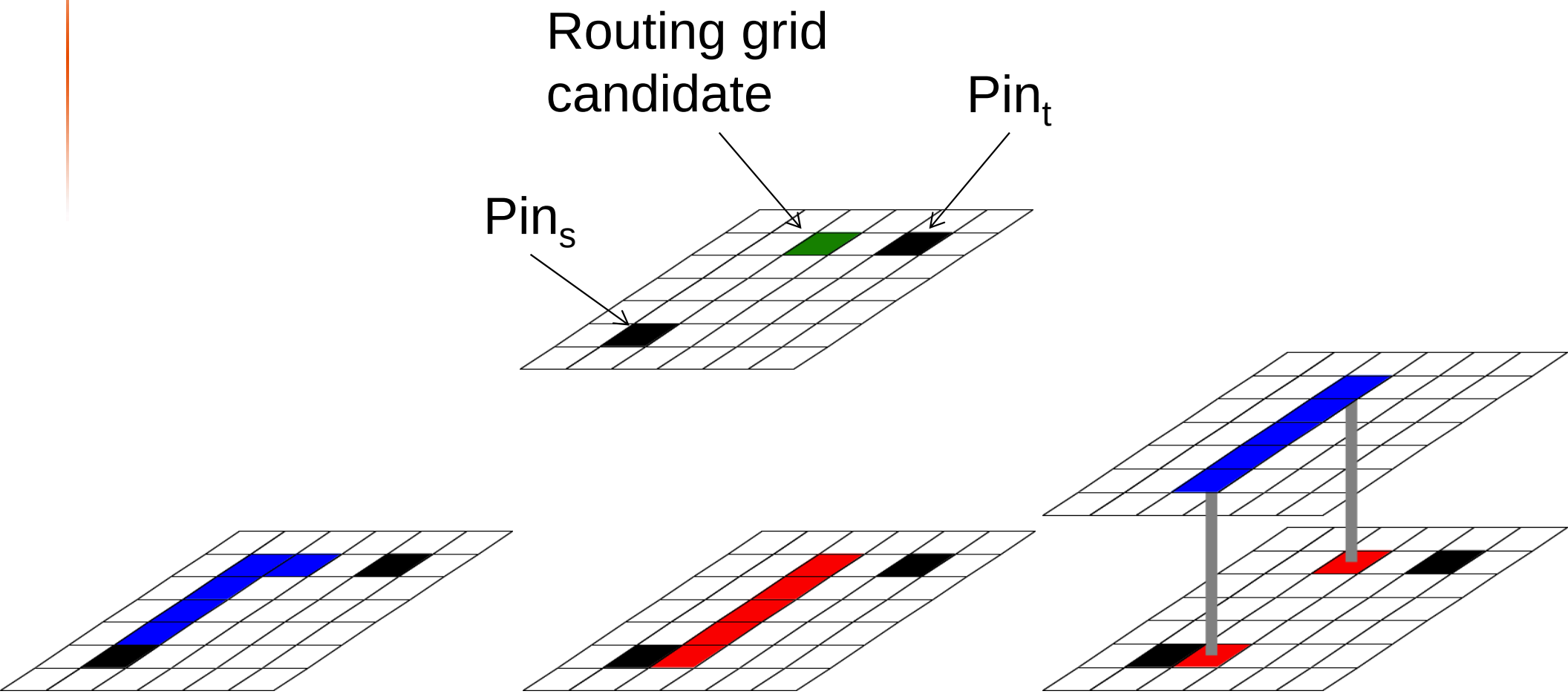
3-D Path Finding by Dynamic Programming

- Efficiently solved by dynamic programming

$$R(path_{s,t}, LD(path_{s,t})) = R(path_{s,i}, LD(path_{s,i})) + R(path_{i,t}, LD(path_{i,t}))$$

- Maintain only two best solutions for each grid
  - Minimum cost(m) and cost(t)
  - Works as an upper bound to prevent unnecessary search
- Still keep optimality

Path Finding Example



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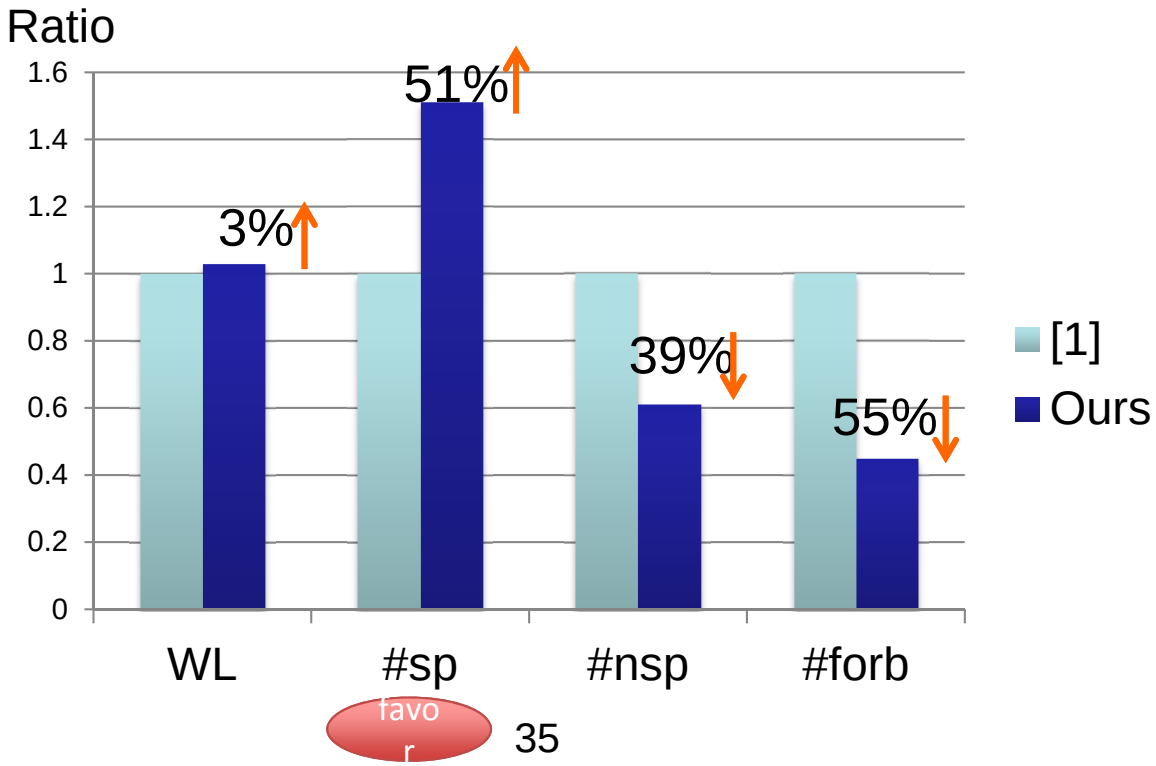
Experimental Results

- Platform
  - Intel Core2 2.66GHz CPU, 4Gb Memory
- DPL Setup
  - Scale all benchmarks to 22nm technology
  - PatternWidth = SpacerWidth = MinSpacing = 50nm
    ForbSpacing = 100nm
- Benchmarks
  1. Randomly generated single layer benchmarks
  2. Industrial two-layer benchmarks
- Compared terms
  - WL, VIA, #Conflicts, Runtime
  - #sp: number of trim grids which is aligned to spacer (favor)
  - #nsp: number of trim grids which is not aligned to any spacer
  - #forb: number of trim grids which violates forbidden spacing rule

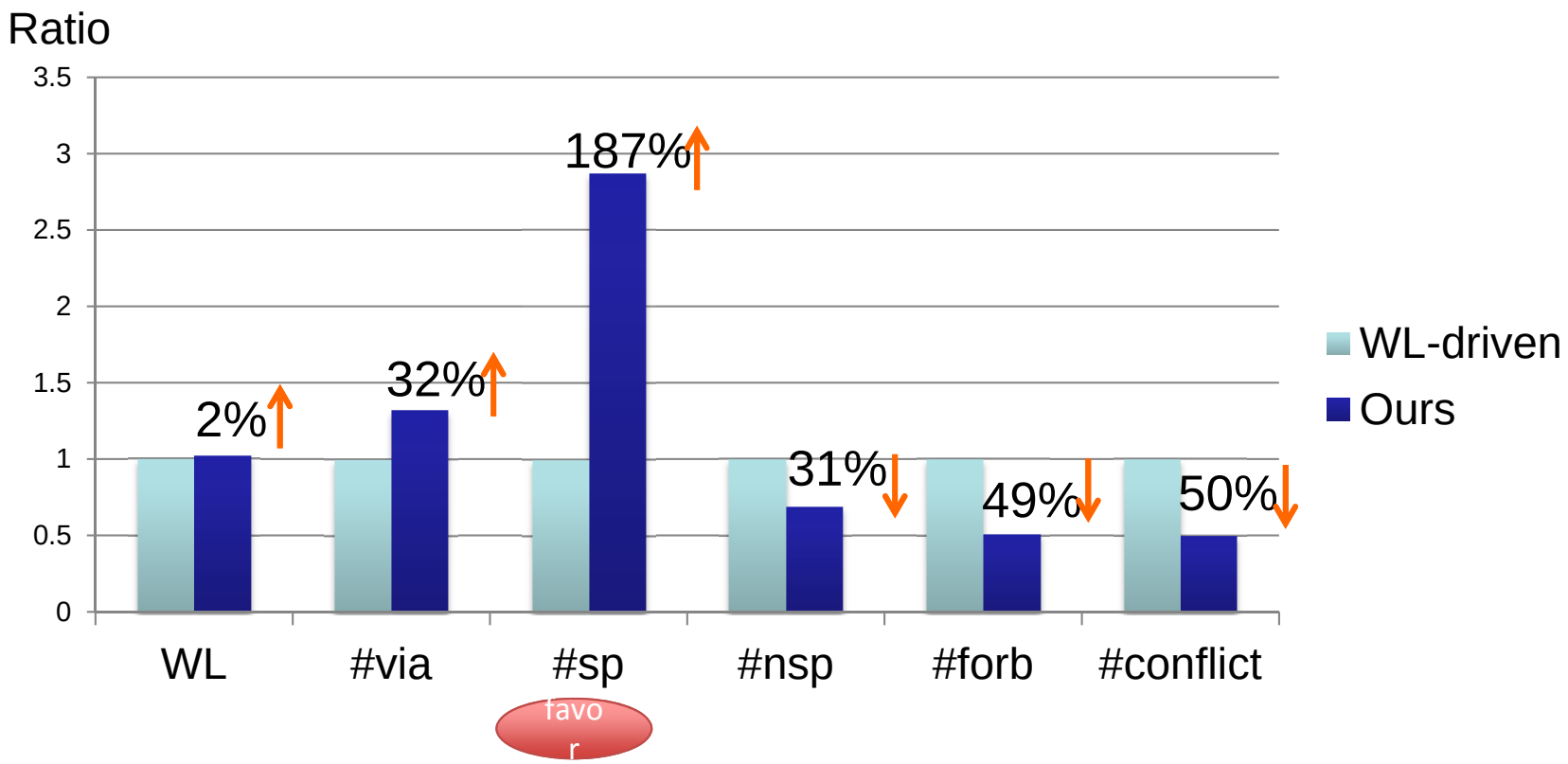
Single Layer Results

- Compared with previous SADP-aware router [M. Mirasaeedi et al SPIE 2011]
  - Simpler cost function: Minimize un-aligned trim patterns
- No conflicts for both routers
- Runtime overhead due to complex cost function: 3.82X
- Achieve better SADP-friendly result



Multiple Layer Results

- Compared with WL-driven routing
- Runtime overhead: 4.69X
- Improve SADP-compliancy with little wirelength overhead



Conclusion

- Consider SADP-compliancy in earlier stages is necessary for successful SADP manufacturing
- Provide SADP-compliant routing guidelines for routing tools to follow
- Improve layout decomposition capability
- Improve pattern image quality
  - Obtain more than 50% self-aligned patterns with comparable wirelength
- Future works
  - More routing guidelines
    - Jogs, U-shape, Z-shape patterns
  - Post routing/layout perturbation

Thank you