IBM Austin Research Lab

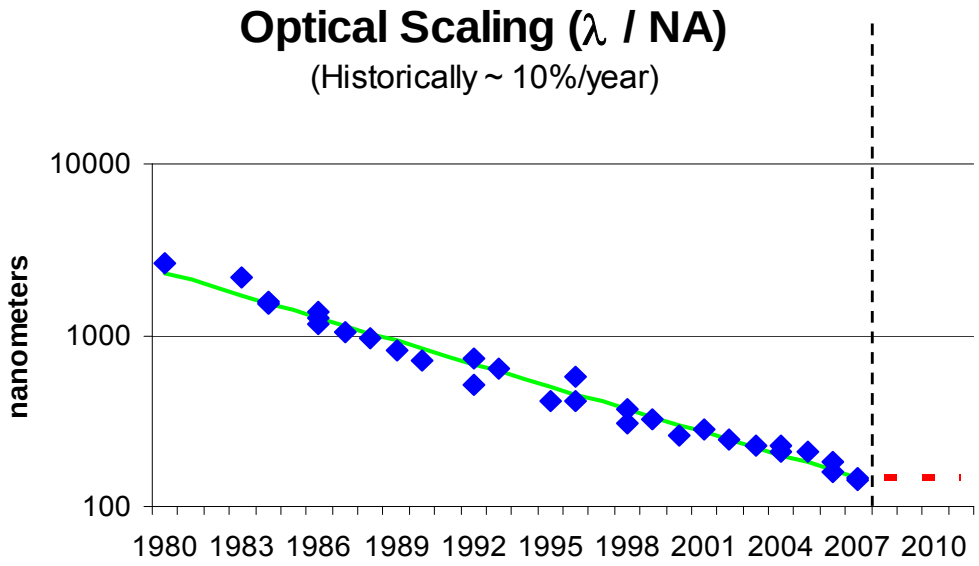
Design Aware Lithography

Kanak Agarwal, Shayak Banerjee, Sani Nassif

Challenges of Sub-wavelength Lithography

- **Semiconductor technology scaling has historically been driven by advancements in optical lithography**
- **Currently facing a plateau in optical scaling**
  - λ (193 nm) with NA (1.35) remains the main technology for production
  - Migration to NGL delayed
  - Low k_1 regime
  - Shapes increasingly difficult to manufacture
  - High sensitivity to manufacturing (focus, dose) variations

$$\text{Resolution} = k_1 \frac{\lambda}{NA}$$

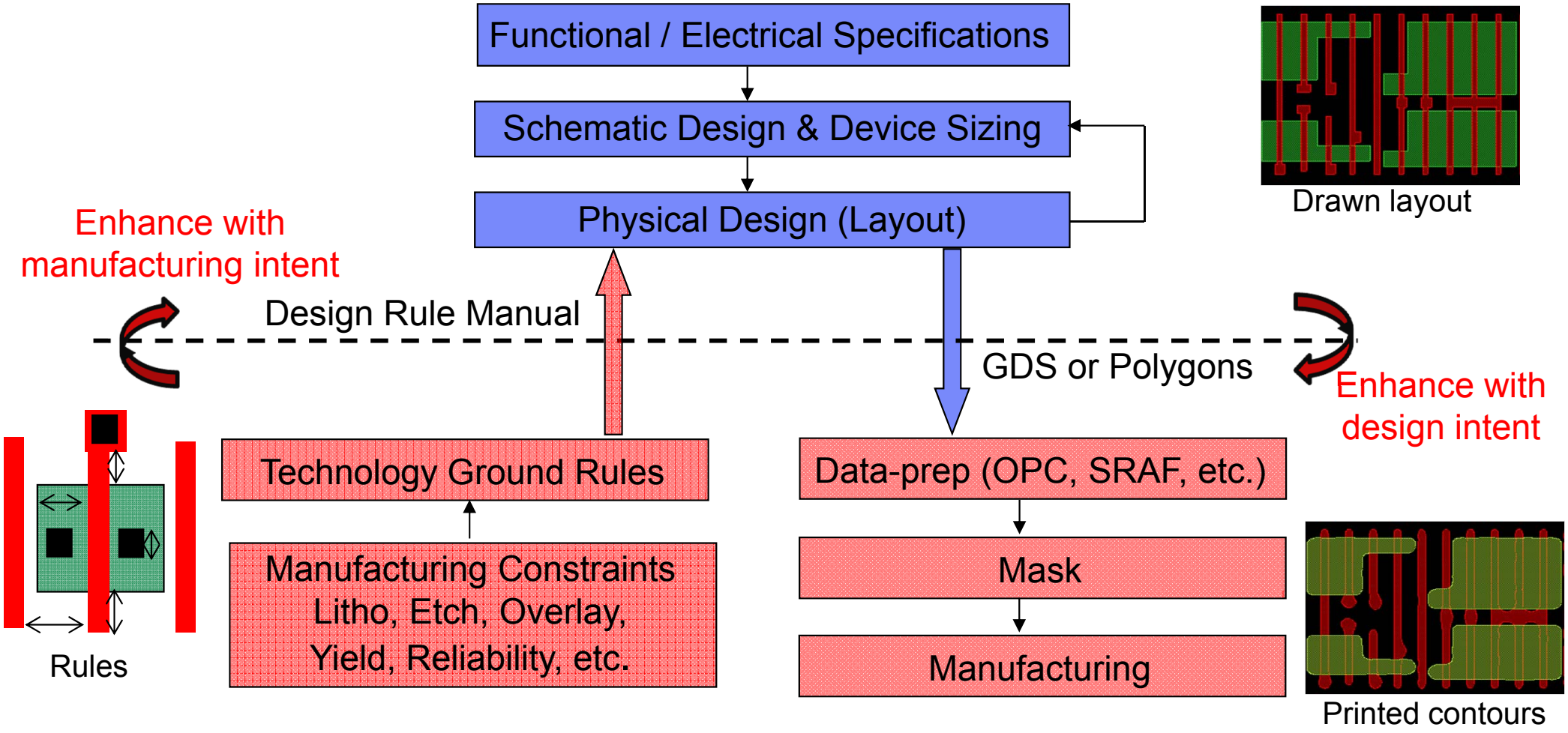


How to Continue Scaling with λ/NA Discontinuity?

- **Design – Manufacturing Co-optimization : aggressive DfM**
  - Design – aware lithography
    - Improve process limited yield (PLY) subject to design constrains
  - Lithography – aware design
    - Improve circuit limited yield (CLY) subject to lithographic constrains
- **Computational Scaling : aggressive RET**
  - Rigorous mask synthesis (pixilated masks, inverse lithography techniques, etc.), Source Mask Optimization (SMO)
- **Design restrictions : aggressive RDR**
- **Physical scaling : double / triple patterning**
  - Wafer level frequency multiplication using Pitch Split (PS) and Sidewall Image Transfer (SIT) multiple patterning processes

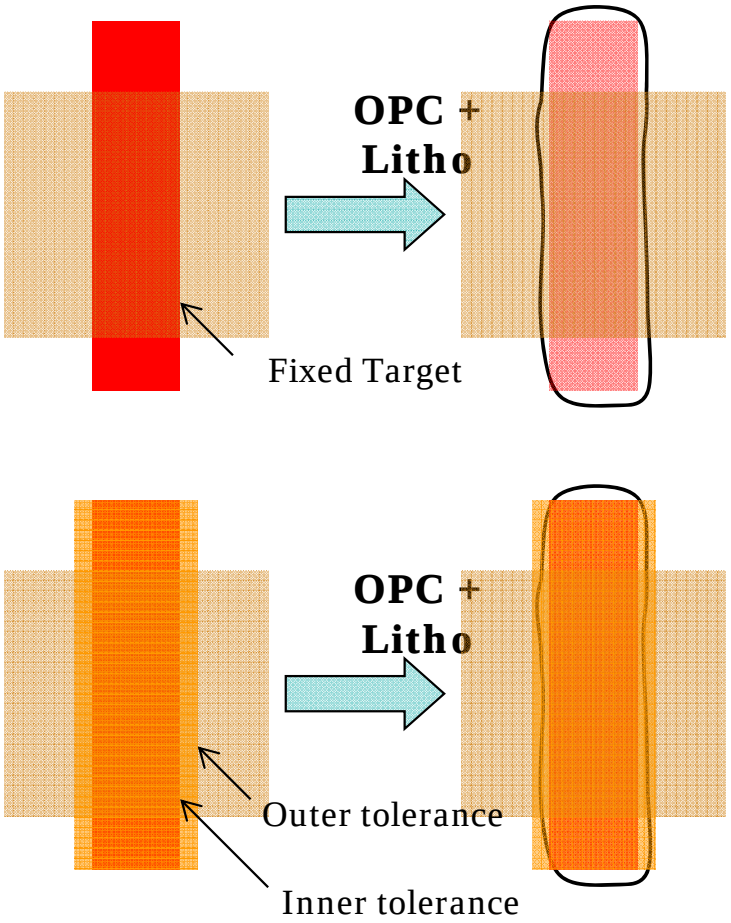
Design – Manufacturing Co-optimization

- **Current design – manufacturing interface**



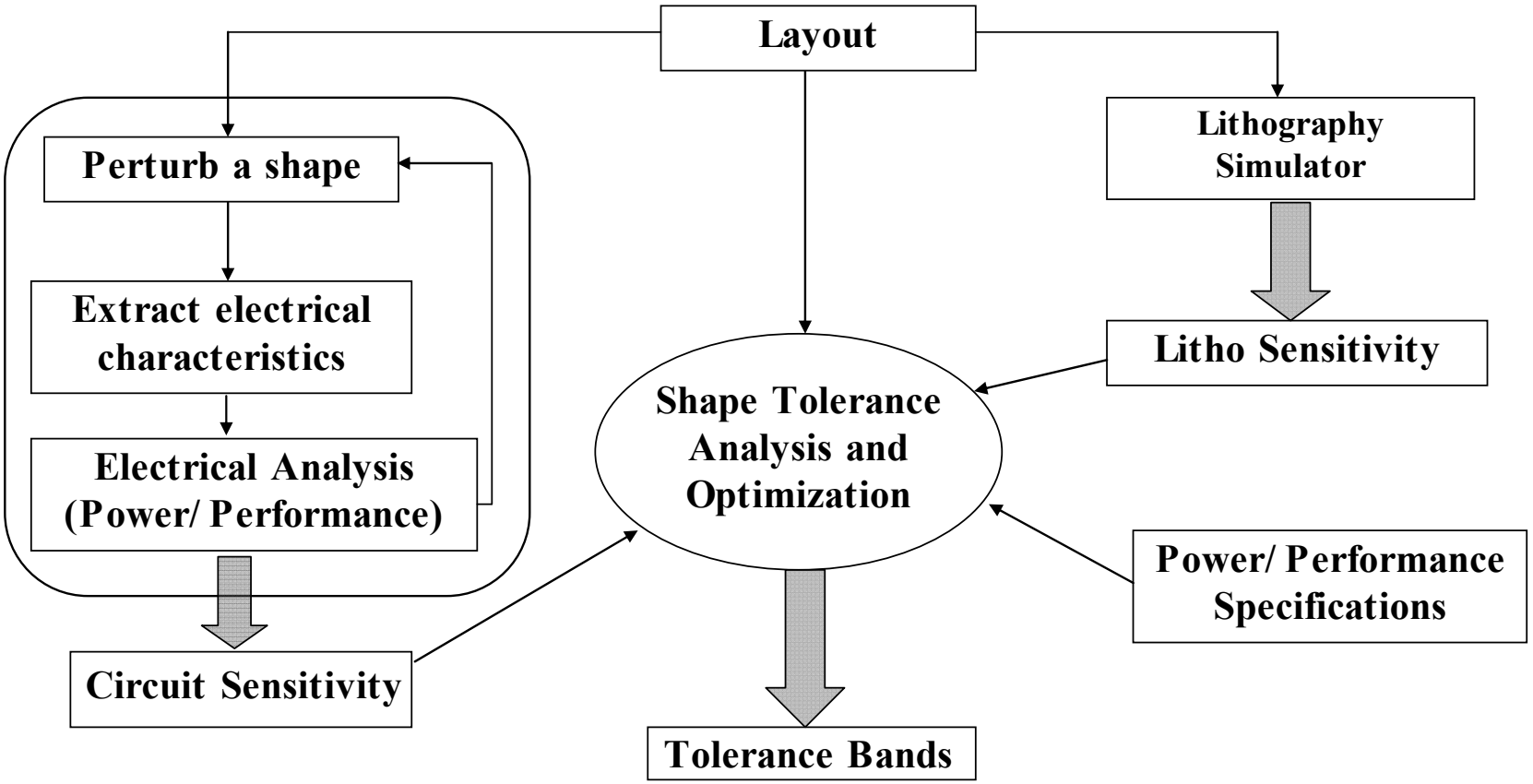
Enhancing Shape-Based Handoff

- **No need to treat all target polygons as fixed requirement for lithography**
  - Flexible shapes
  - Options that provide same functionality and performance but with different manufacturability
- **Enhance shape-based hand-off by passing design-aware tolerance bands to manufacturing**
  - Identifies “safe” layout perturbations
  - Allows manufacturing tools to find best solution



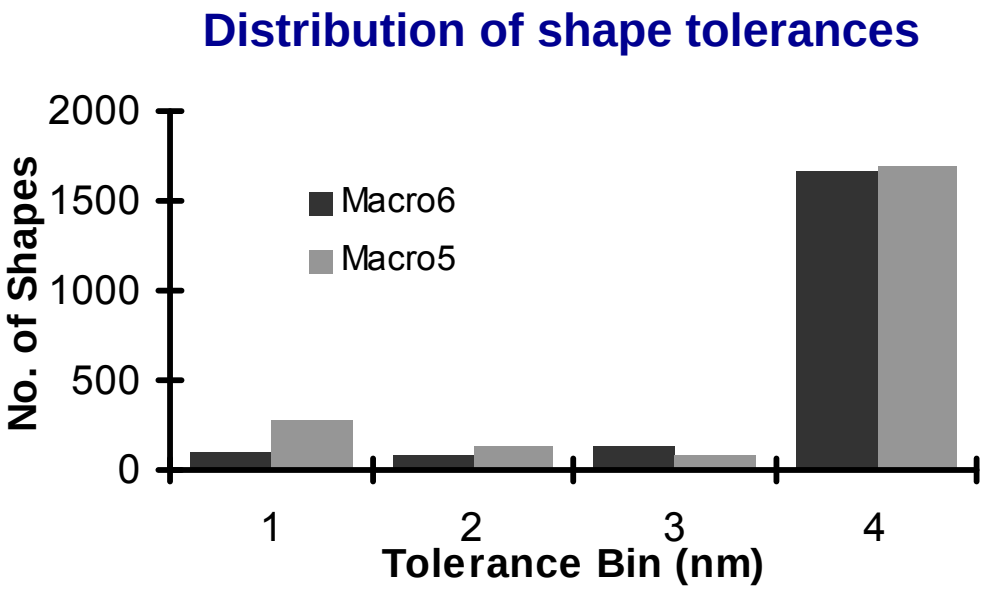
Electrical Slack to Shape Slack

- **Delay slack in design – measure of tolerable variability**
- **Conversion to shape slack based on**
  - High electrical criticality => lower tolerance
  - High litho sensitivity => higher tolerance



Shape Slack Generation

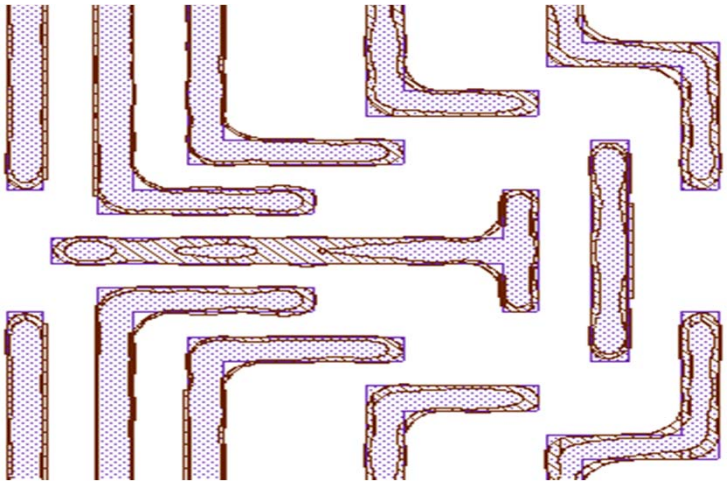
- **Phase I : Distribute slack available at primary outputs to generate delay bounds on cells**
  - Slack budgeting (linear program)
- **Phase II: Generate shape slack from delay bounds**
  - Formulated as an optimization problem: maximize lithographic process window subject to delay bounds (Quadratic Program)



Shape Slack for Different Layers

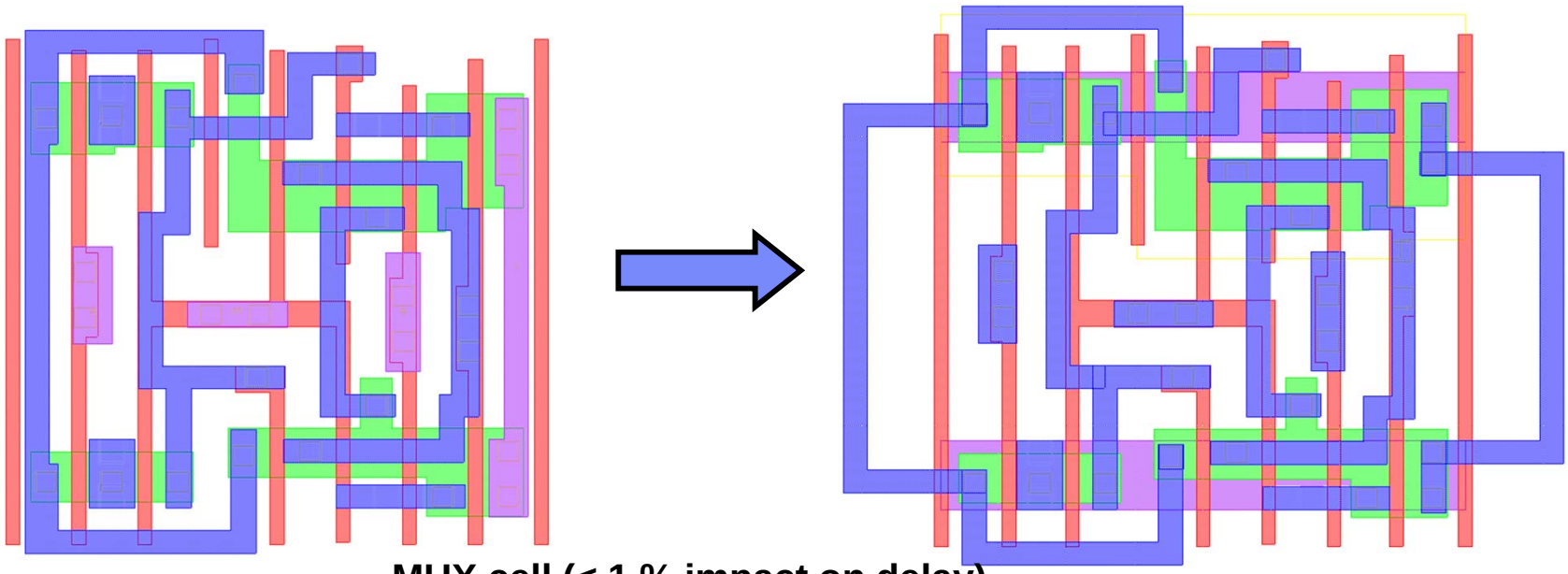
- **Delay based shape slack approach layers**
  - Useful for timing critical layers like Poly / Active
  - Limited benefits in the RDR regime : unidirectional on grid poly with heavily tailored RET
- **Significant benefits of shape slack can be realized for low level metal (e.g. M1) layers**
  - Bi-directional, tight pitch, free-hand routing with limited design restrictions
  - Design rules cannot cover all possible shape constructs
  - Variations in lithographic process result in catastrophic fails (opens/shorts)

PV Bands for DRC Clean Layout



Shape Slack for Local Interconnects

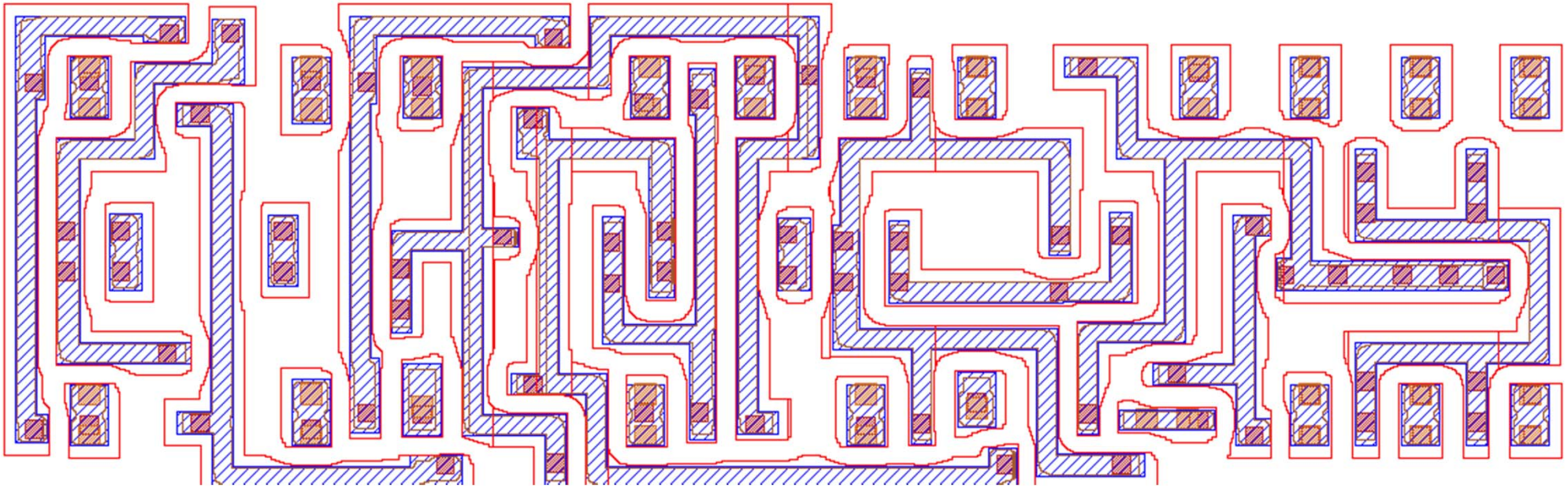
- **A large number of shapes on local interconnects (M1) are electrically non-critical**
  - Resistances and capacitances very small compared to device impedances
  - Shapes, if considered as drawn, can be very challenging for litho
  - The non-critical shapes can be safely perturbed during litho if electrical connectivity and ground rule constraints are maintained



MUX cell (< 1 % impact on delay)

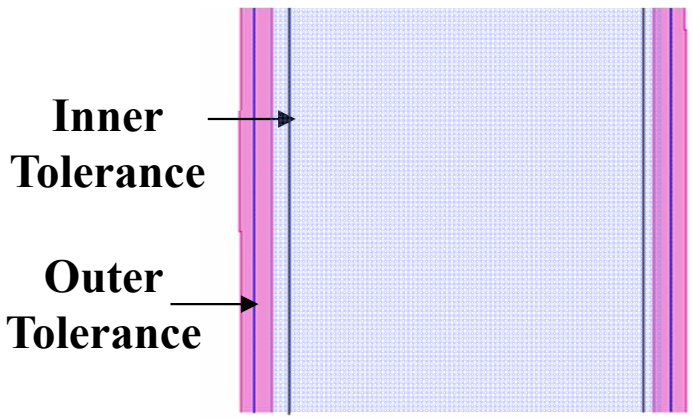
M1 Ground Rule Slack

- **Generate tolerance bands for local M1 interconnect by considering ground rules (GR) and electrical connectivity**
  - Consider rules such as min width/spacing, min contact/ via overlap
  - Use GR slack to create tolerance bands
  - Examples show significant GR based slack that can be exploited during litho without impacting circuit yield

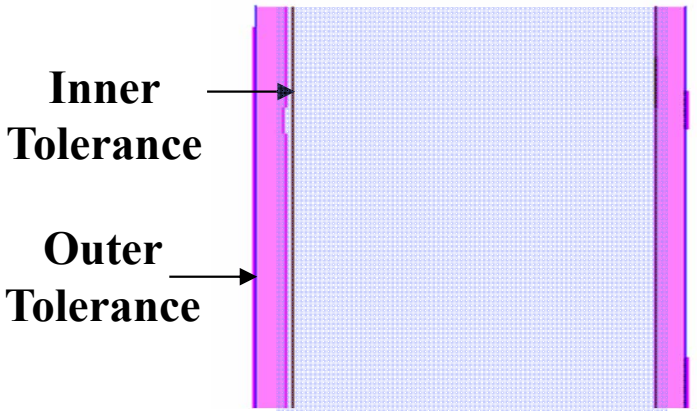


Using Shape Slack in Manufacturing

- **Optical Proximity Correction (OPC) for mask generation**
  - Algorithm based on minimizing edge placement error (EPE) between wafer **contour** at nominal conditions and fixed **target**
  - Design may be violated by process variations
- **Tolerance bands can be exploited during manufacturing through Tolerance Driven OPC**
  - Algorithm based on minimizing process variability (PV) band deviation from tolerance band



PV Band (OPC)

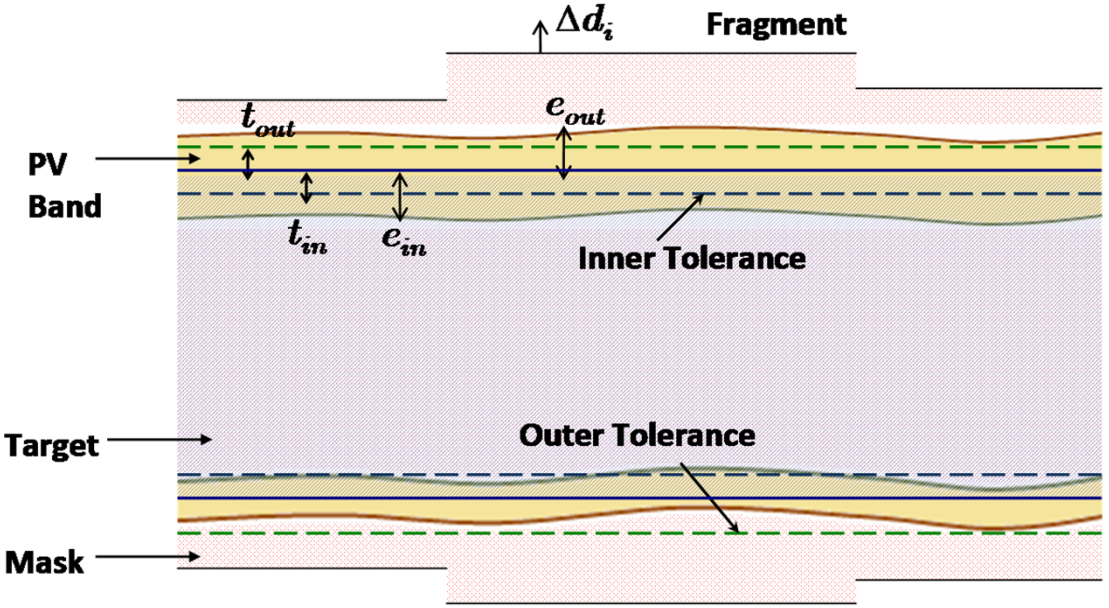


PV Band (Tolerance driven OPC)

Tolerance Driven OPC

- **OPC for using generated tolerances**
  - Identify lithographic corners (dose/focus/mask errors) giving worst case behavior
  - Define outer (e_{outer}) and inner (e_{inner}) EPE
  - Use EPEs to define TD-OPC cost function (C_{TDOPC})

$$C_{TDOPC} = \sum_{i=1}^{N} \left[w_0 e_{nom,i} + w_1 \, exp\left(e_{out,i} - t_{out} \right) + w_2 \, exp\left(e_{in,i} - t_{in} \right) \right]$$



12

Optimization using Gradient Descent

- **Cost function (C_{TDOPC}) minimized using gradient information**

$$\frac{\partial C_{TDOPC}}{\partial d_i} = w_0 \frac{\partial e_{nom,i}}{\partial d_i} + w_1 \frac{\partial e_{out,i}}{\partial d_i} exp\left(e_{out,i} - t_{out,i}\right) + w_2 \frac{\partial e_{in,i}}{\partial d_i} exp\left(e_{in,i} - t_{in,i}\right)$$

  - $\partial e/\partial d$ is the mask error enhancement factor (**MEEF**)
  - Analytically computed at image simulation time

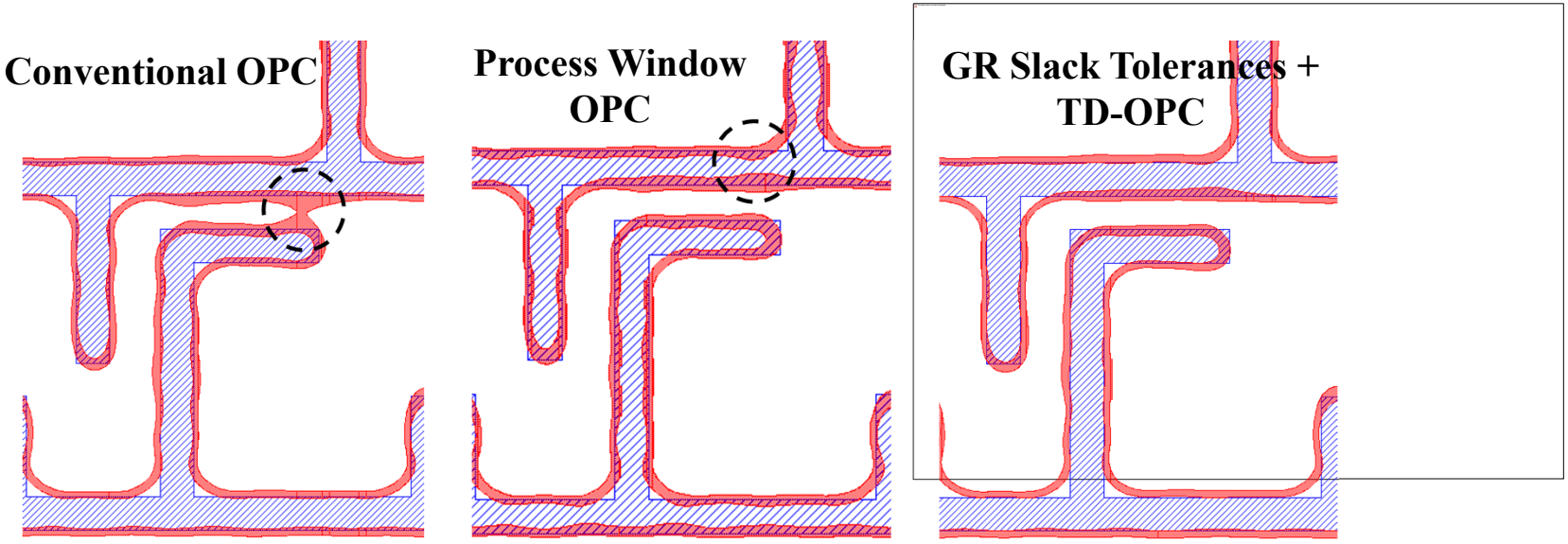
$$\frac{\partial e_{nom,i}}{\partial d_i} = \alpha_{nom}, \quad \frac{\partial e_{out,i}}{\partial d_i} = \alpha_{out}, \quad \frac{\partial e_{in,i}}{\partial d_i} = \alpha_{in}$$

  - Mask fragment then moved by fraction of derivative

$$\Delta d_i = -\eta \frac{\partial C_{TDOPC}}{\partial d_i} = -\eta\left(w_0\alpha_{nom} + w_1\alpha_{out} exp\left(e_{out,i} - t_{out,i}\right) + w_2\alpha_{in} exp\left(e_{in,i} - t_{in,i}\right)\right)$$

TD-OPC Benefits

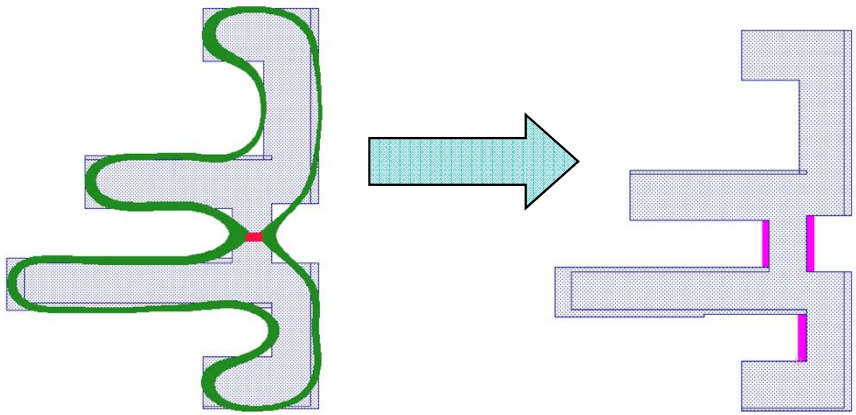
Clip	PW-OPC		TD-OPC		% Red. In PV Area	% Red. In ORC Marker Area
	PV Band Area	ORC Marker Area	PV Band Area	ORC Marker Area		
1	1.5	1.7	1.4	0.9	8.5	47.8
2	6.1	16.7	5.3	5.7	12.4	66.2
3	16.4	17.8	14.3	6.0	13.3	66.4
4	15.5	59.0	13.3	12.9	14.8	78.1
5	229.7	568.1	184.8	216.9	19.5	61.8
6	133.6	376.6	110.4	190.1	17.3	49.5
7	148.4	422.2	124.1	160.6	16.4	62.0
Average					17.7	59.4



14

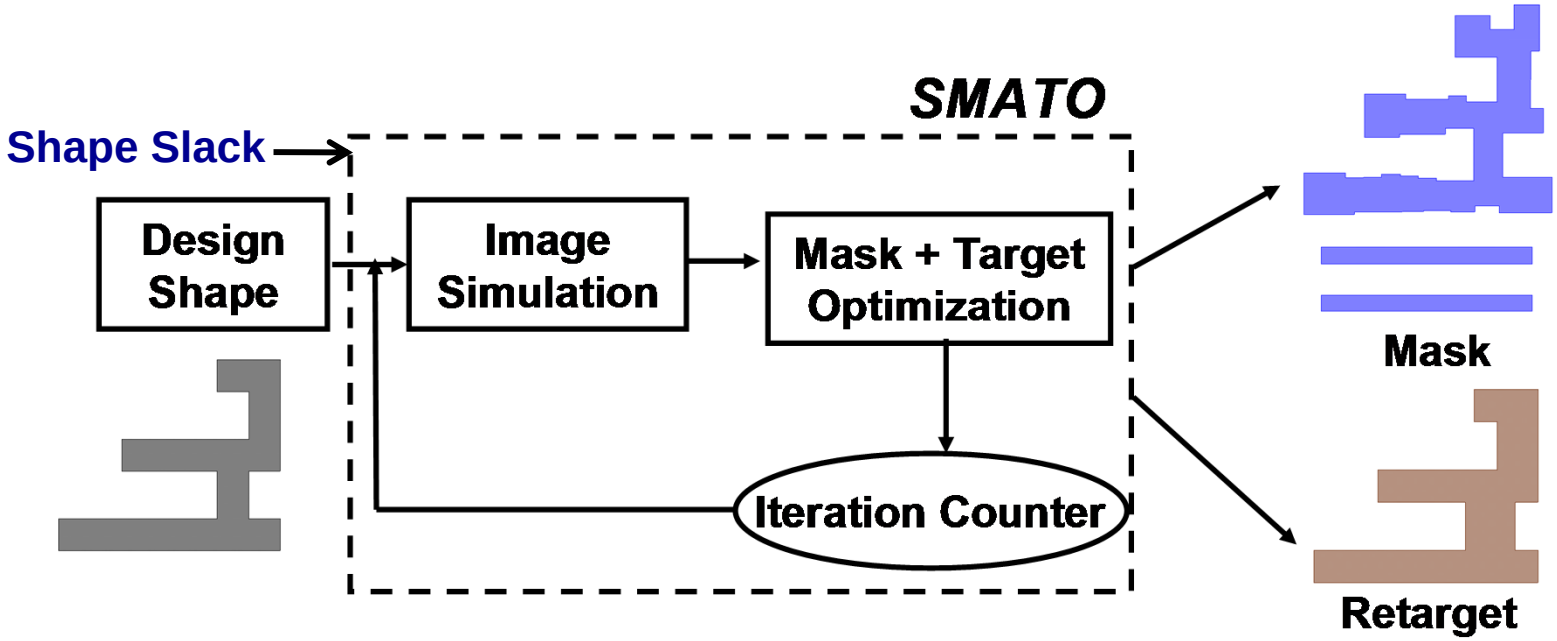
Using Shape Slack in Manufacturing : Retargeting

- **Conventionally, shapes provided by the designer == target shapes for lithography**
- **Retargeting modifies the shapes provided by the designer during manufacturing**
  - Generate new target shapes that have better printability
  - Different from mask optimization (OPC) which changes mask shapes instead of target layout
  - Amount of allowed perturbation constrained by shape slack



Simultaneous Mask and Target Optimization

- **SMATO: Optimize both mask and target simultaneously**
  - Model based flow for retargeting that integrates retargeting with OPC
  - More degrees of freedom during RET for printability improvement
  - Uses shape slack information to determine the acceptable range of target movement

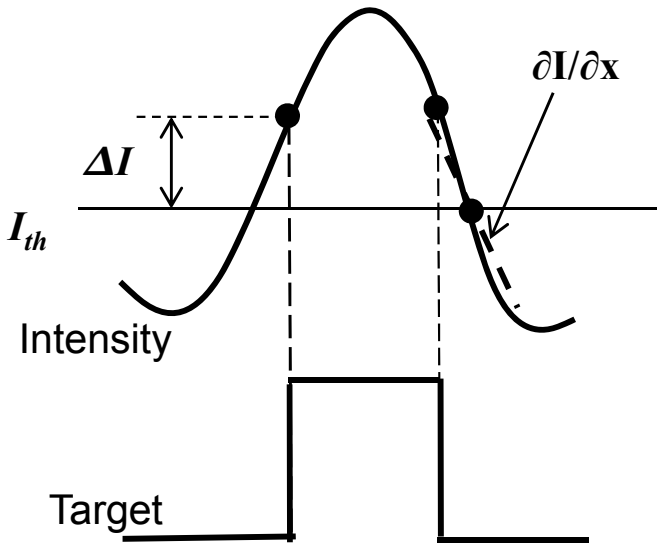


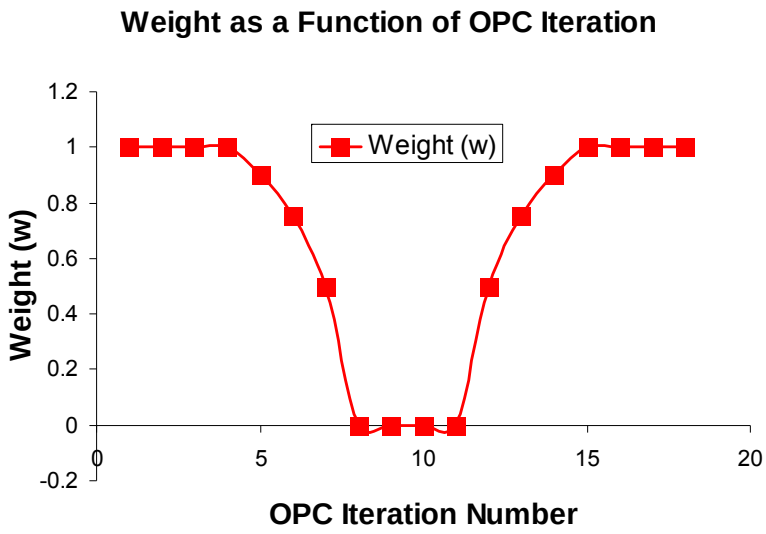
Cost Function for SMATO

- **Cost function based on EPE (fidelity) and slope (robustness)**
  - Minimize error in intensity at target (ΔI)
  - Maximize slope ($\partial I/\partial x$)

$$C_{SMATO} = w_i \left(I_{tgt} - I_{th}\right)^2 + \frac{\left(1-w_i\right)}{\left|\partial I / \partial x\right|}$$

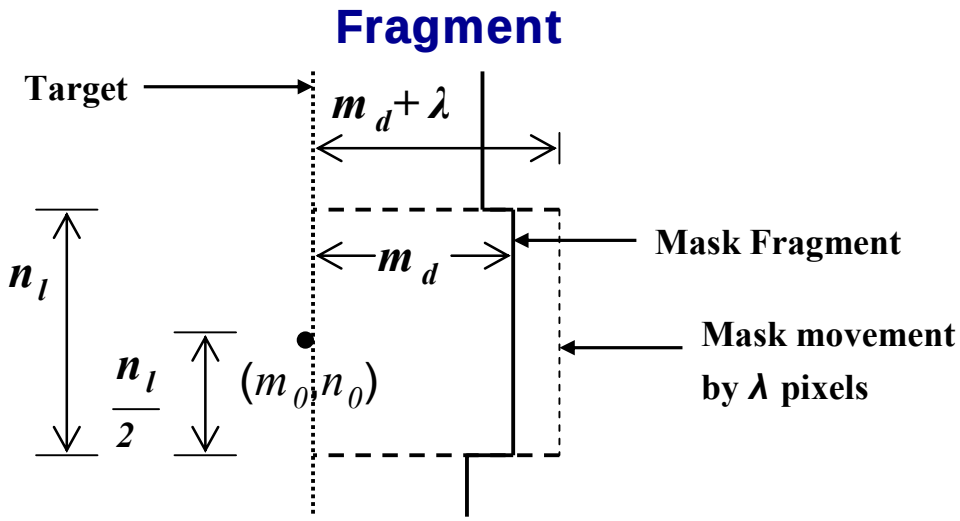
- **Weight (w_i) can be dynamically tuned over SMATO iterations (i)**
  - Initially minimize ΔI to match target
  - Then retarget to maximize slope
  - Finish by matching contour to retarget





SMATO Fragment Movement

- **Solve for best pair of target *and* mask movement for each fragment**
  - 9 point local search
  - Target movement ($-\eta, 0, +\eta$)
  - Mask movement ($-\lambda, 0, +\lambda$)
  - Pick local minimum of C_{SMATO}



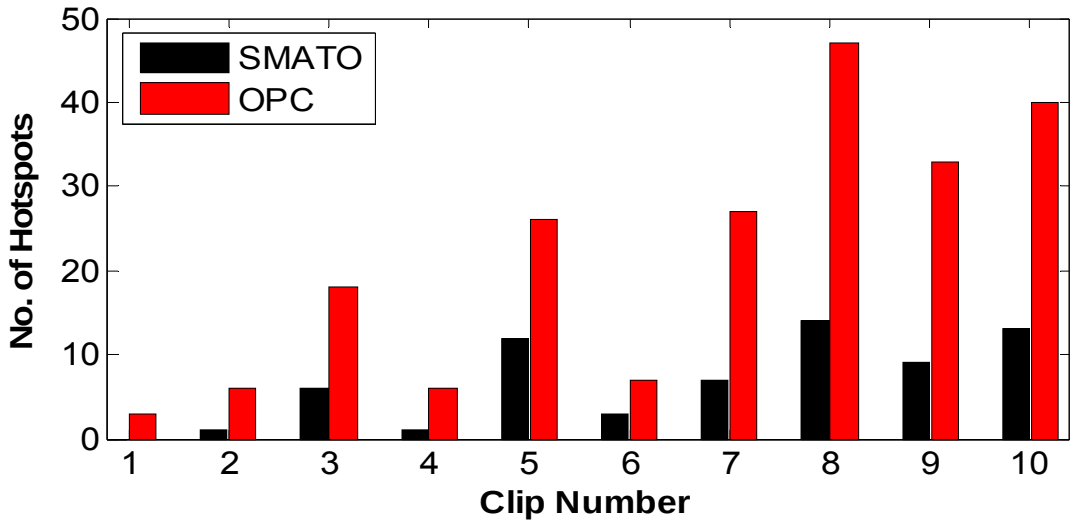
- **For each possible move, compute**
  - Change in intensity
  - Change in image slope
  - Analytical evaluation of impact of mask and target movement on intensity / slope given a single simulation

$$\begin{bmatrix} C_{SMATO}(m_0, n_0 - \eta, -\lambda) & C_{SMATO}(m_0, n_0 - \eta, 0) & C_{SMATO}(m_0, n_0 - \eta, +\lambda) \\ C_{SMATO}(m_0, n_0, -\lambda) & C_{SMATO}(m_0, n_0, 0) & C_{SMATO}(m_0, n_0, +\lambda) \\ C_{SMATO}(m_0, n_0 + \eta, -\lambda) & C_{SMATO}(m_0, n_0 + \eta, 0) & C_{SMATO}(m_0, n_0 + \eta, +\lambda) \end{bmatrix}$$

Tolerance Driven Retargeting Benefits

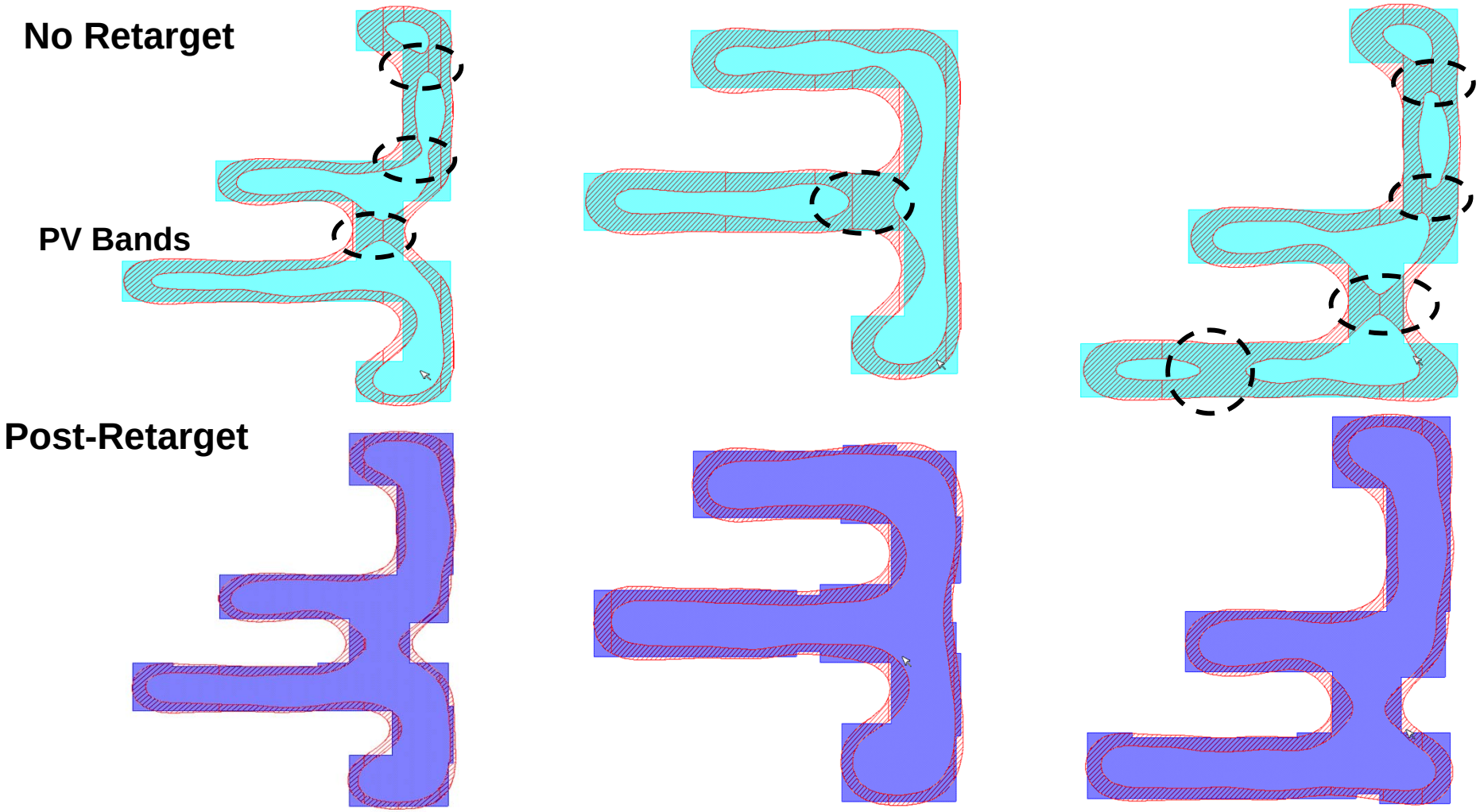
Clip	Area (μm^2)	PMI [OPC]	PMI [SMATO]	% PMI Redn. over OPC	% Runtime Incr. over OPC
1	2.2	6.95	5.66	18.5	3.7
2	2.9	5.57	4.68	16.0	6.1
3	3.0	3.46	3.11	10.2	5.9
4	4.5	7.24	6.29	13.1	3.1
5	4.9	6.36	5.54	12.9	8.4
6	7.2	5.18	4.63	10.5	7.2
7	8.2	8.24	6.96	15.5	7.6
8	8.7	8.27	6.92	16.4	4.8
9	8.8	7.72	6.43	16.8	5.0
10	9.3	7.96	6.58	17.3	4.4
Average				15.5	5.4

$$PMI = \frac{Area\,of\,PV\,Band}{Area\,of\,Layout}$$



Retargeting Examples

- **Tolerance band aware retargeting + OPC can fix certain hot-spots that are not fixable by just mask optimization**



Conclusion

- **Knowledge of design information**
  - Can be used to improve manufacturing
    - Make printed shapes more robust – improve litho process window
- **Different ways to propagate electrical information**
  - Map delay slack to shape slack
  - Utilize GR slack - hardest to print local metal interconnects (M1) and contact / via layers have the highest shape slack
- **Different ways to use information**
  - Tolerance driven OPC
  - Tolerance driven Retargeting

Backup

Limitations of Current Design-Manufacturing Contract

- **Current design flows treat ground rules as required constraints for manufacturability**
  - Very hard to represent all complex 2-D optical interactions as rules
  - Limitation: layouts that follow the ground rules but not the manufacturers' intent
- **Current manufacturing flows treat target layout shapes as a fixed requirement for lithography**
  - Not always necessary to get all printed edges at drawn edges
  - Limitation: manufacturing optimizations geared towards mimicking the drawn polygons but not the designers' intent
- **Opportunity in enhancing design-manufacturing interface with (rules + manufacturing intent?) and (shapes + design intent?)**