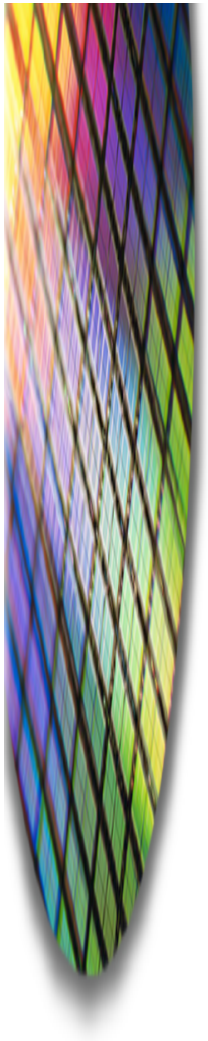

E-Beam Lithography Stencil Planning and Optimization With Overlapped Characters

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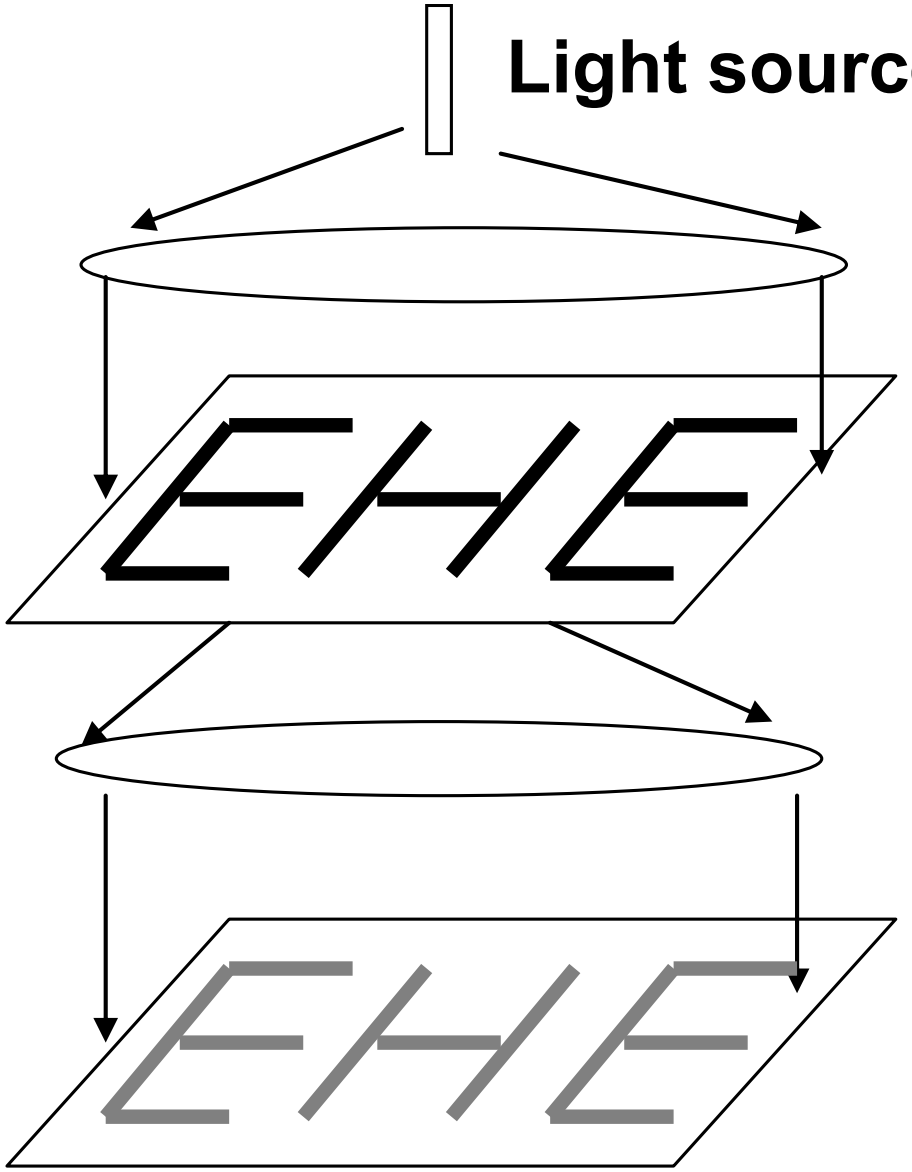
Outline

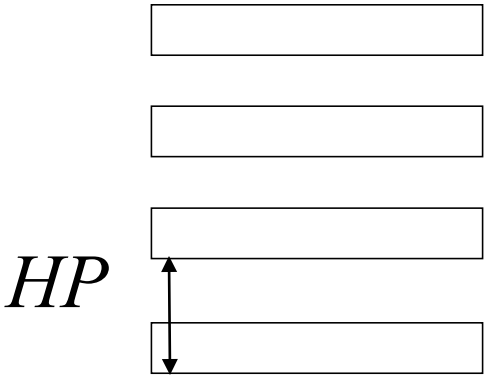
- Introduction and Motivation
  - Electronic Beam Lithography (EBL)
  - Overlapped Characters
- EBL Stencil Planning/Optimization
  - One-Dimensional Stencil Design
  - Two-Dimensional Stencil Design
- Experimental Results
- Conclusion

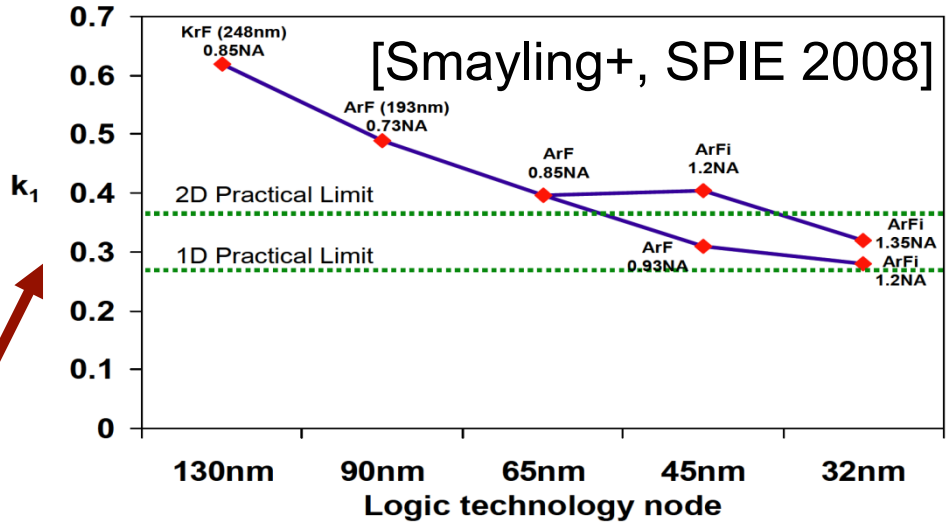
Conventional Optical Lithography



Scaling Woos

- Aggressive scaling of min. printable half pitch HP





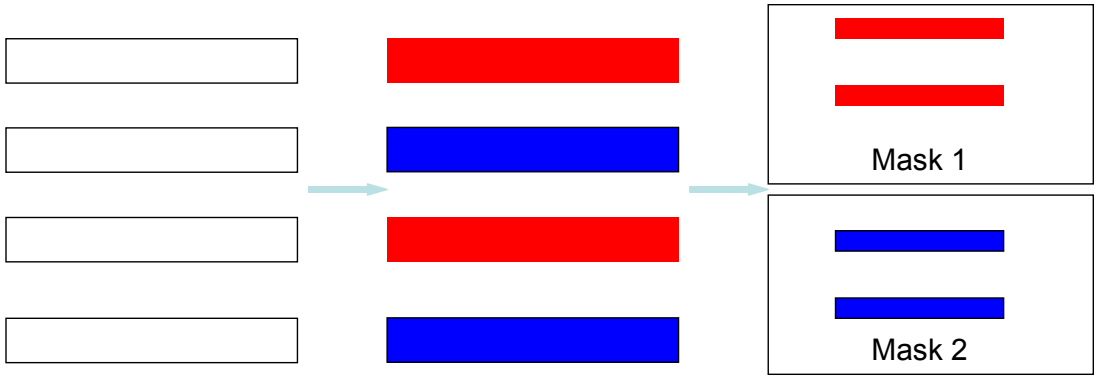
$$HP = k_1 \frac{\lambda}{NA}$$

k_1: process difficulty
NA: numerical aperture
λ: wavelength of source

- λ is stuck at 193nm
- k_1: limit is 0.25
- NA = 1.5, close to the limit
- EUV (13.5nm): Still many, many challenges!

Mask Cost !!!

Alternative solution for 32nm/22nm and below



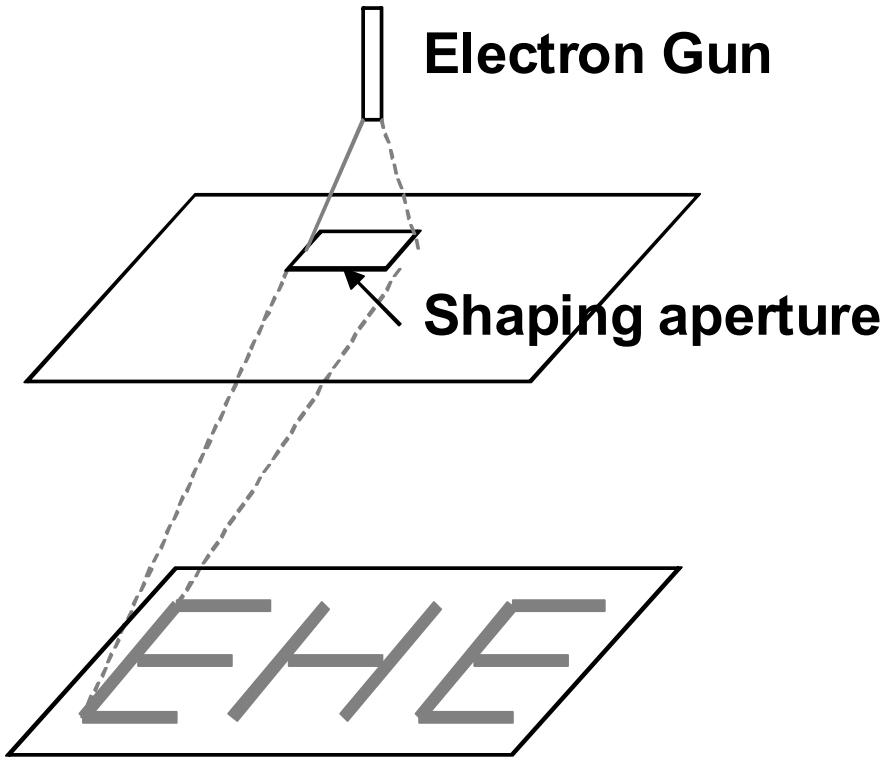
Double Patterning

Or even triple/quadruple patterning!

But mask cost will be proportionally higher!

Electron Beam Lithography

- **Maskless** technology, which shoots desired patterns directly into the silicon wafer
  - 4x better resolution [Solid State Technology 2011]
  - Lower cost [D2S Inc]

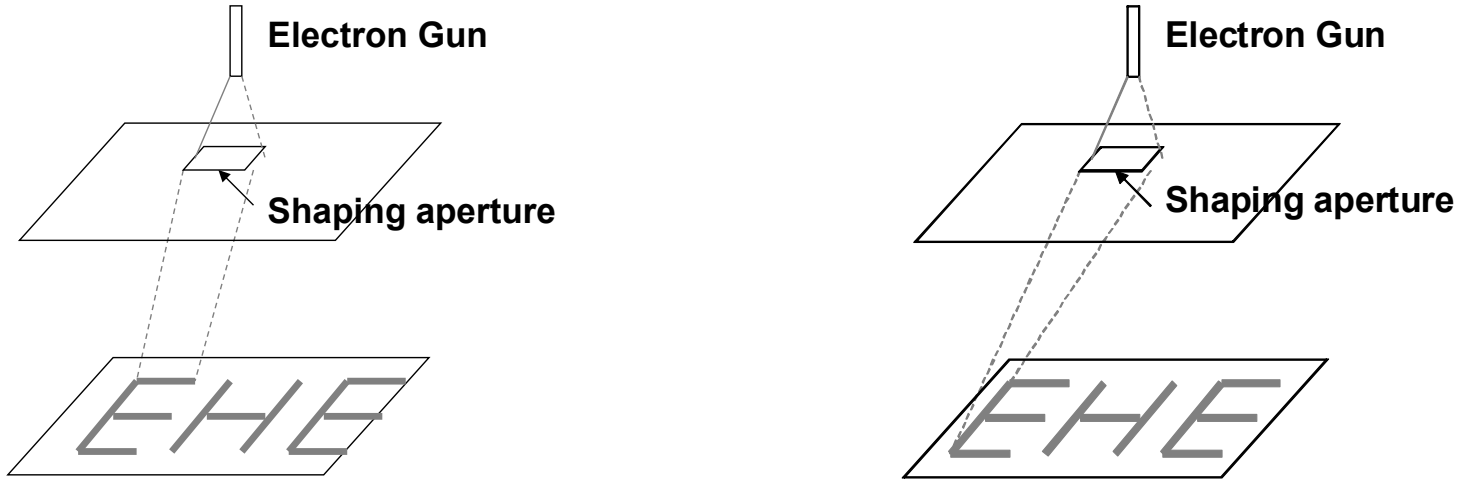


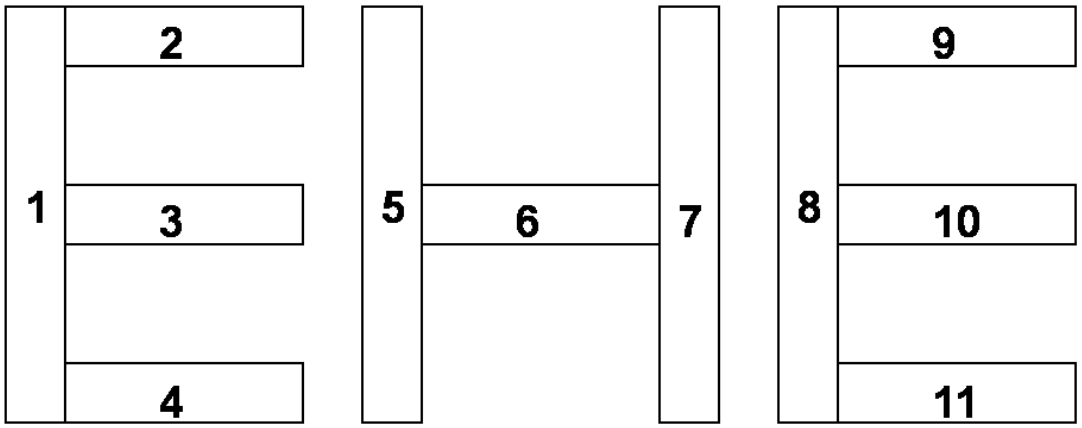
The biggest challenge:

Low throughput

Variable Shape Beam (VSB)

- One rectangle per shot

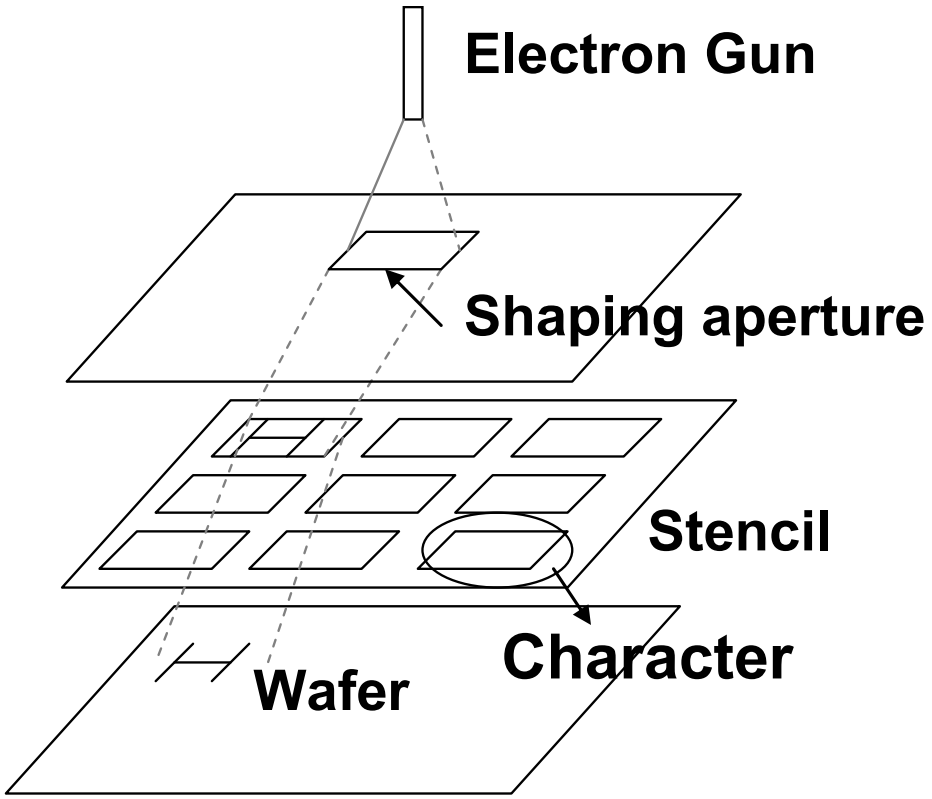




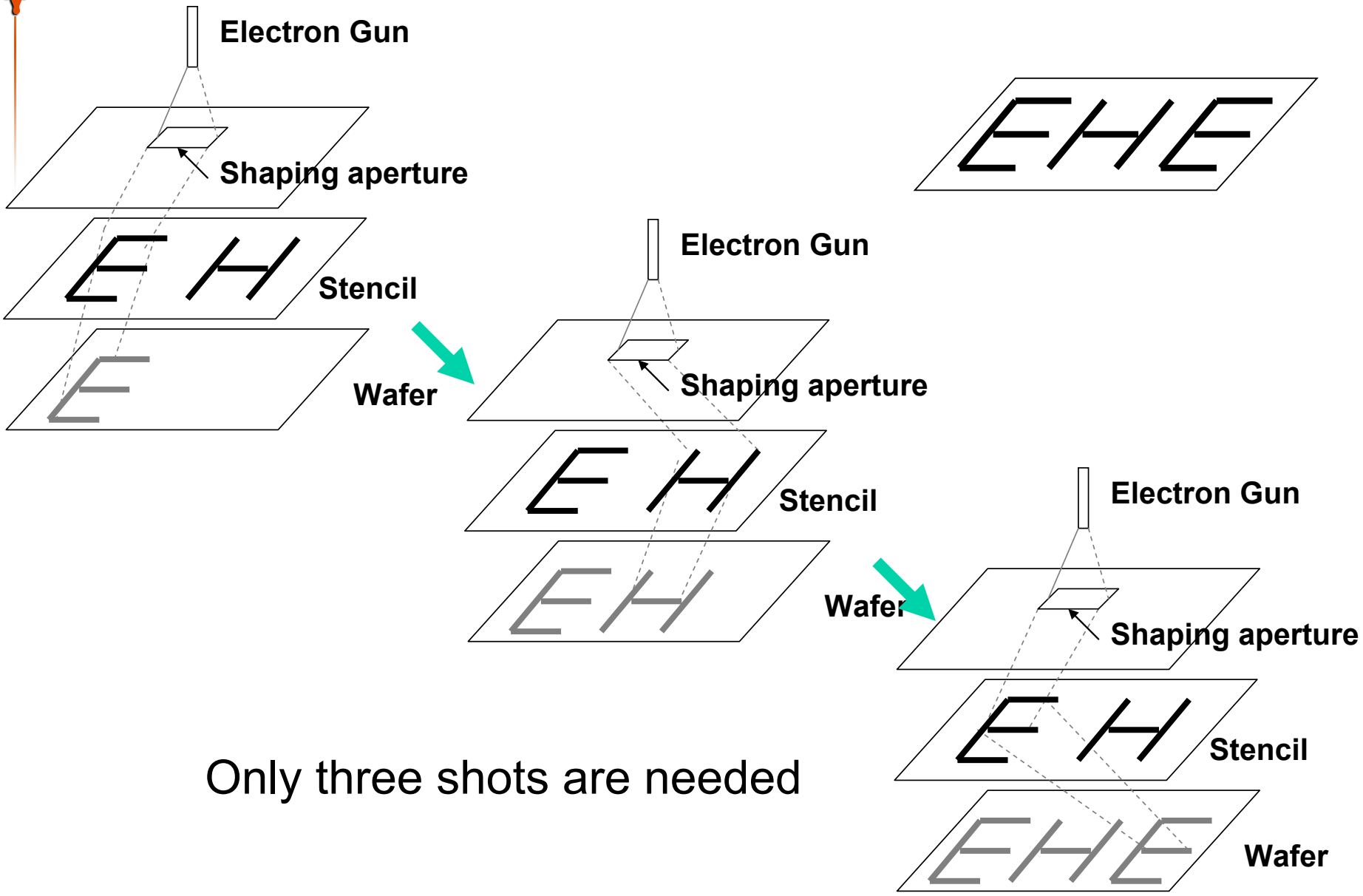
Total number of
11 shots
are needed

Character Projection (CP) Technology

- Print some complex shapes in one electronic beam shot, rather than writing multiple rectangles.



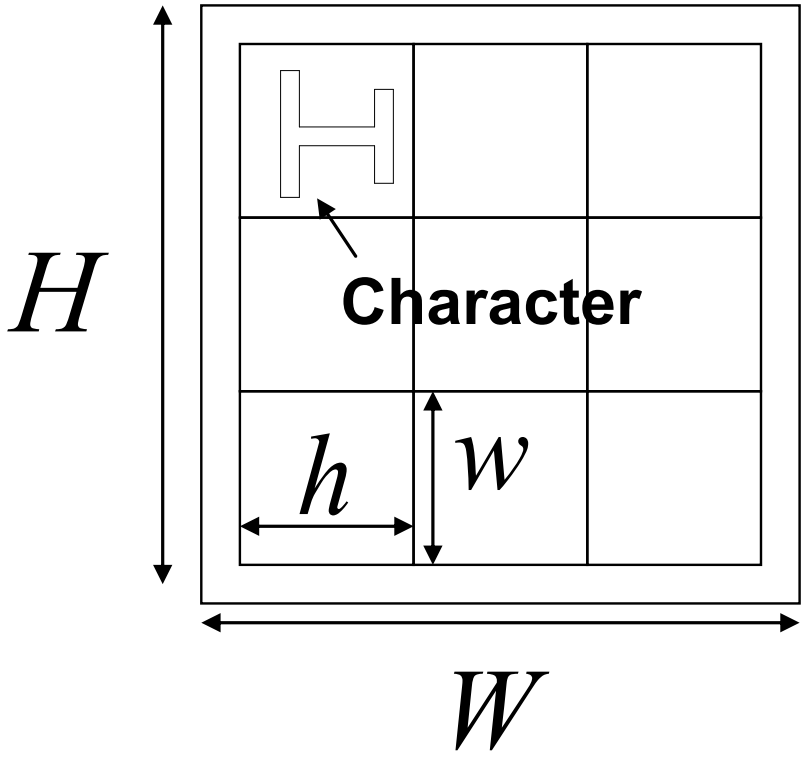
Character Projection Technology (Cont.)



Only three shots are needed

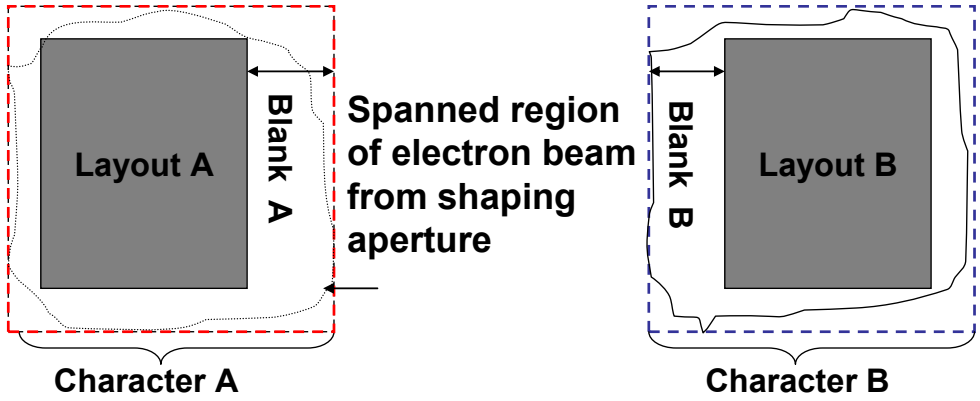
Limitation of Character Projection

- The number of characters is limited due to the area constraints of the stencil
  - Various investigations [**Makoto et al. SPIE'06, SPIE'09**] on optimization of character selection

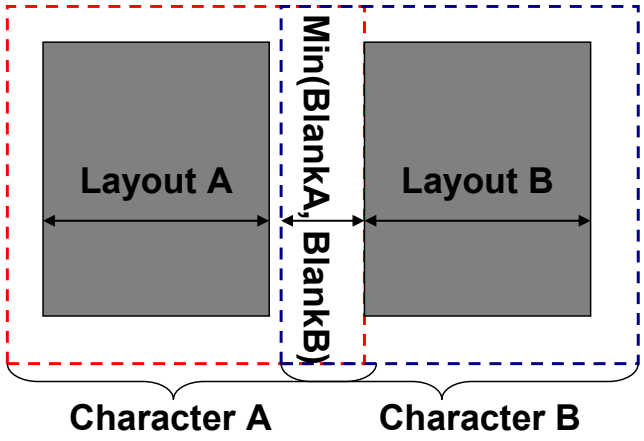


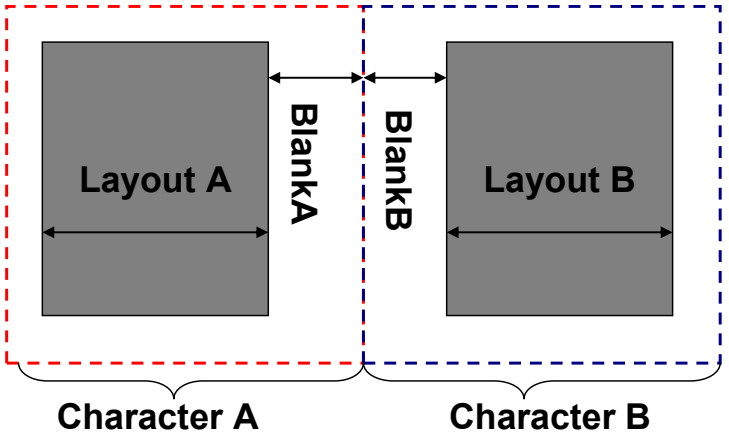
Overlapped Characters

- Blanking space is usually reserved around its enclosed rectangular circuit pattern



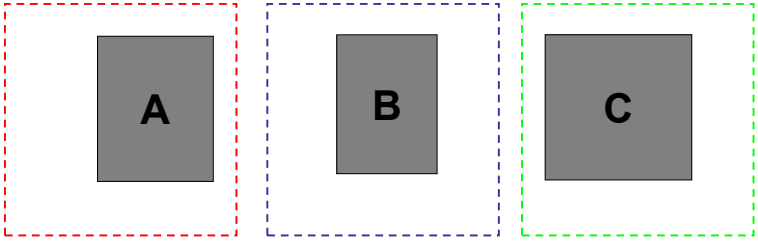
- By allowing over-lapping adjacent characters, more characters may be put on stencil [Fujimura+, 2010]





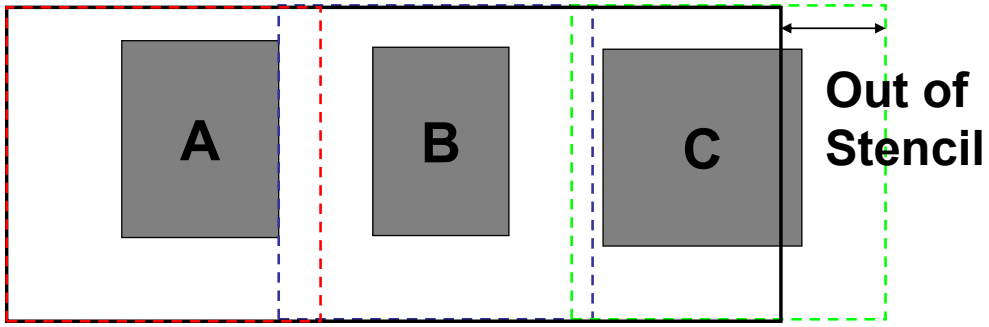
Not a Trivial Task

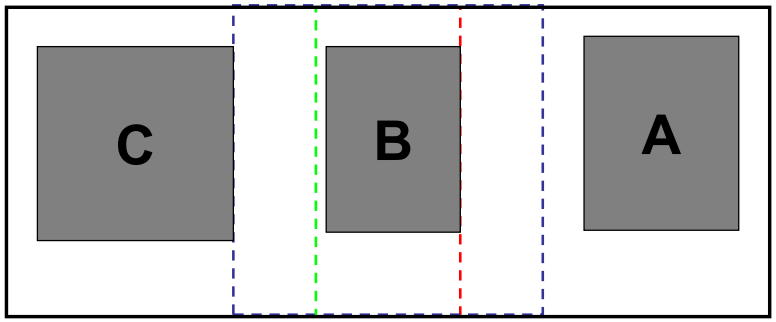
Character Candidates to be Considered



Stencil

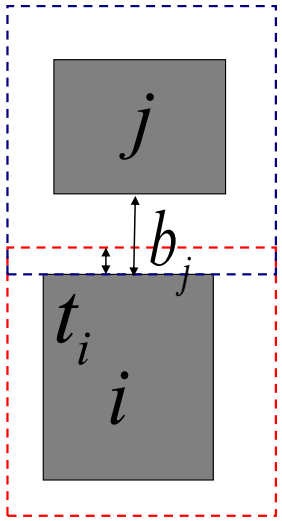
Order Matters

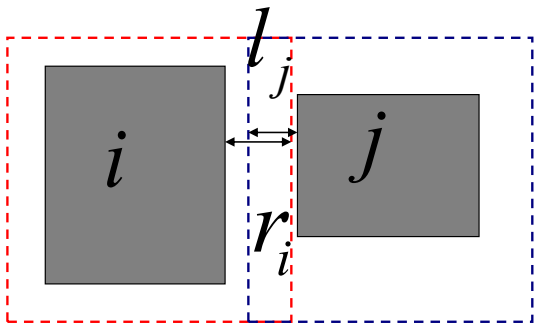




Problem Definition

- Given a set of character candidates C_C





$$o_{ij}^{V} = \min(t_i,\ b_j) \qquad o_{ij}^{H} = \min(r_i,\ l_j)$$

Each candidate C_i appears r_i in the circuit

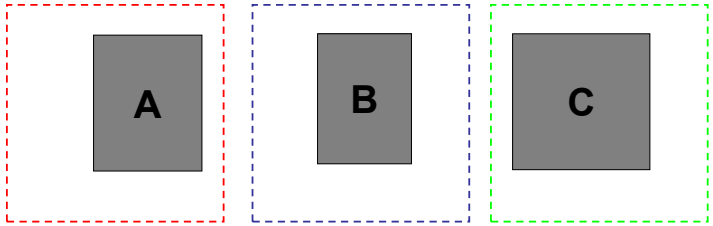
#shots by VSB: n_i^{VSB} #shots by CP: n_i^{CP}

Problem Definition (Cont.)

- Select a subset C_{CP} out of character candidates C_C, and place them on the stencil S

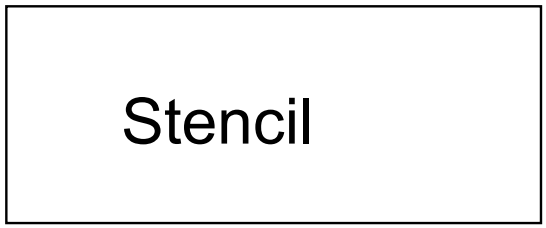
Minimize total number of shots:

$$\sum_{C_i \in C_{CP}} r_i n_i^{CP} + \sum_{C_i \in C_C \setminus C_{CP}} r_i n_i^{VSB}$$



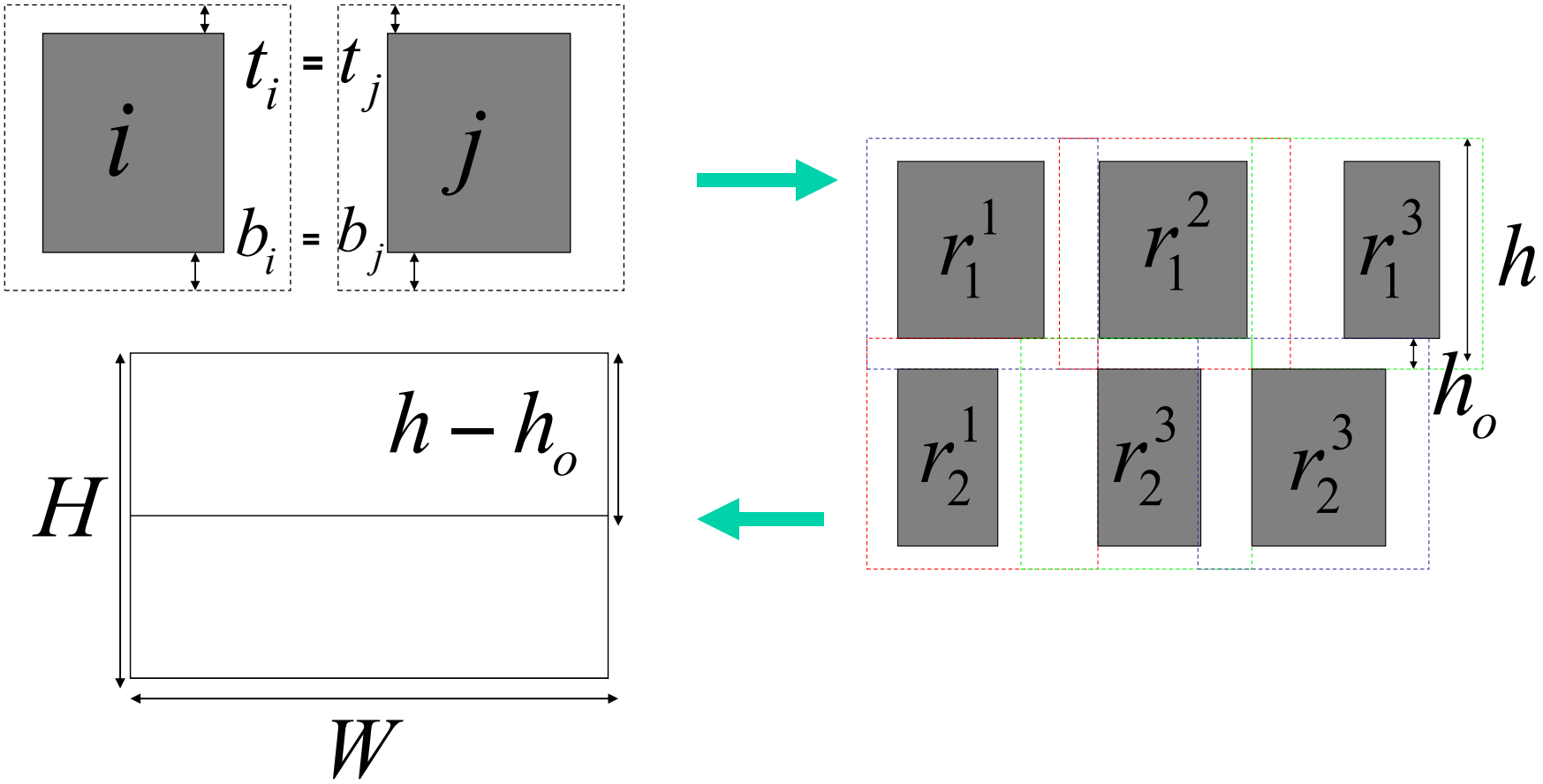
While

The placement of C_{CP} is bounded by the outline of stencil.

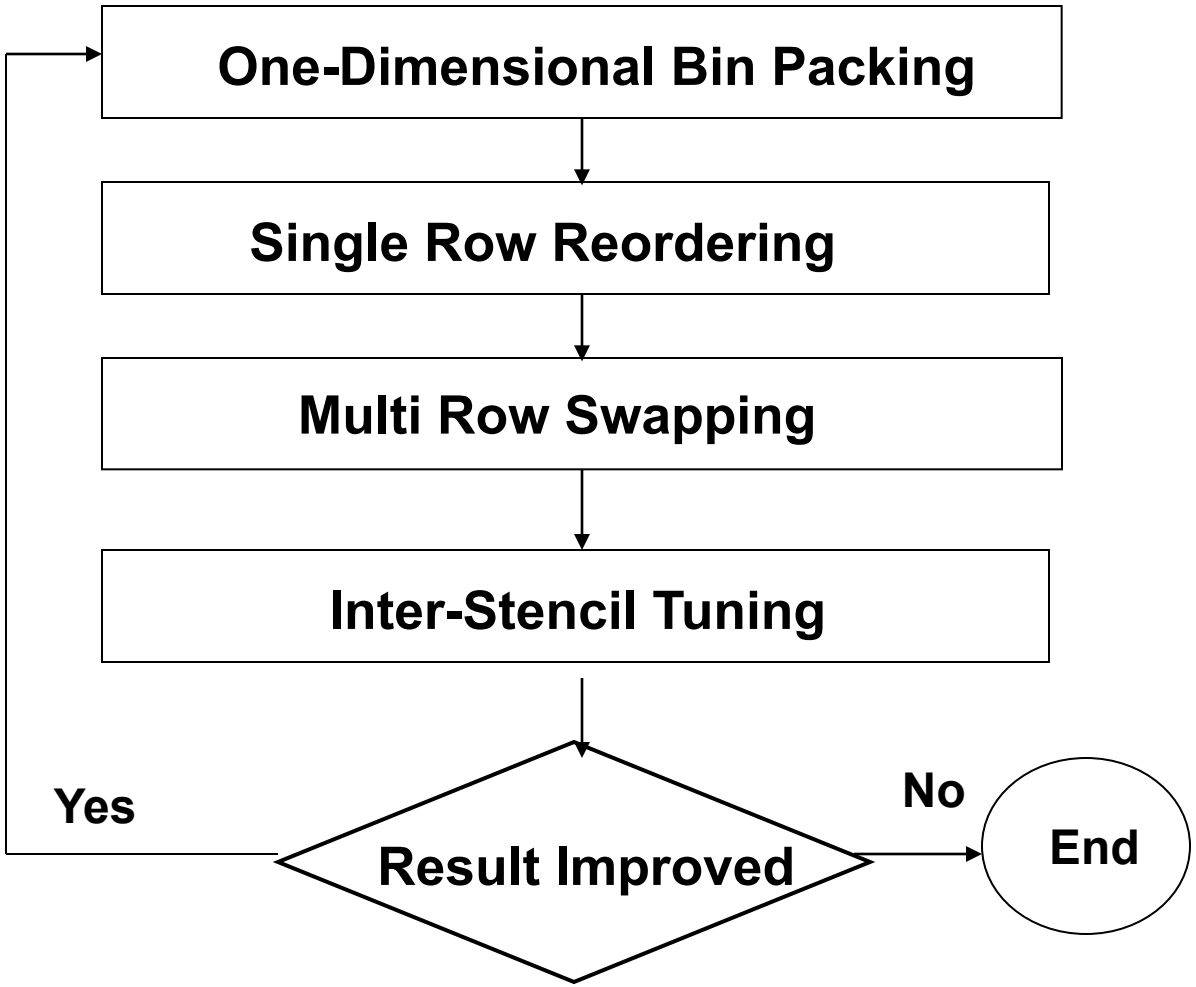


One Dimensional Problem

- The required blanking spaces on the top *t* and bottom *b* are nearly identical for all the candidates.



Optimization Flow



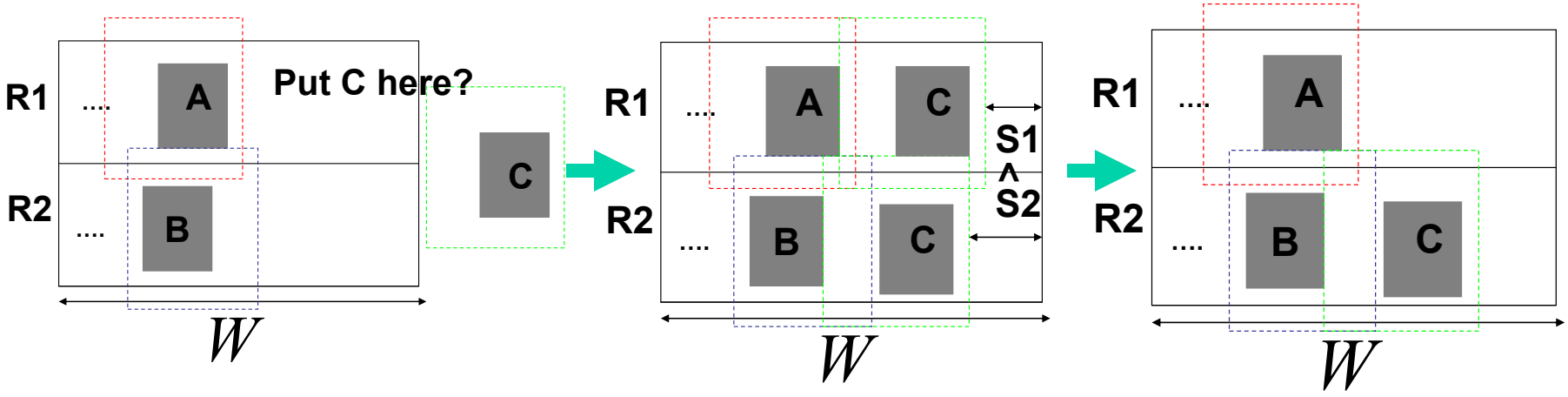
One-Dimensional Bin Packing

$$\sum_{C_i \in C_{CP}} r_i n_i^{CP} + \sum_{C_i \in C_C \setminus C_{CP}} r_i n_i^{VSB}$$ Minimize

$$= \sum_{C_i \in C_C} r_i n_i^{VSB} - \sum_{C_i \in C_{CP}} r_i (n_i^{VSB} - n_i^{CP})$$

Constant Maximize

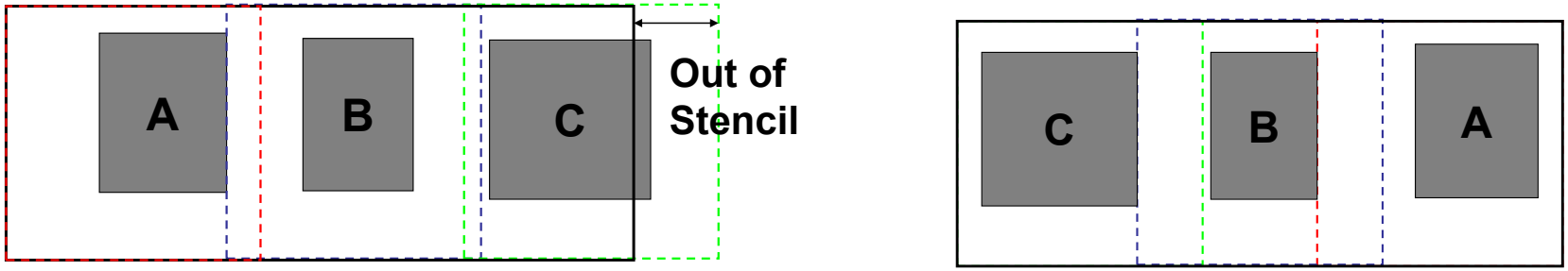
Packing by the decreasing order of $\sum_{C_i \in C_{CP}} r_i (n_i^{VSB} - n_i^{CP})$



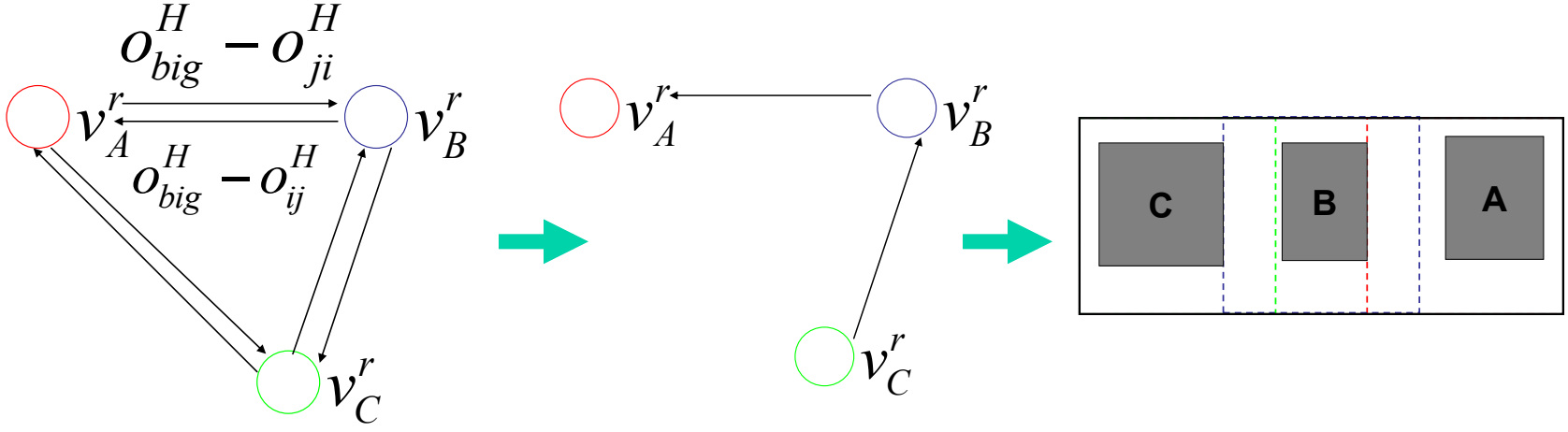
Put the candidate into the row with most blacking space left

Single Row Reordering

- Adjust the relative locations of already-placed characters in each row to shrink its occupied width and increase remaining capacity

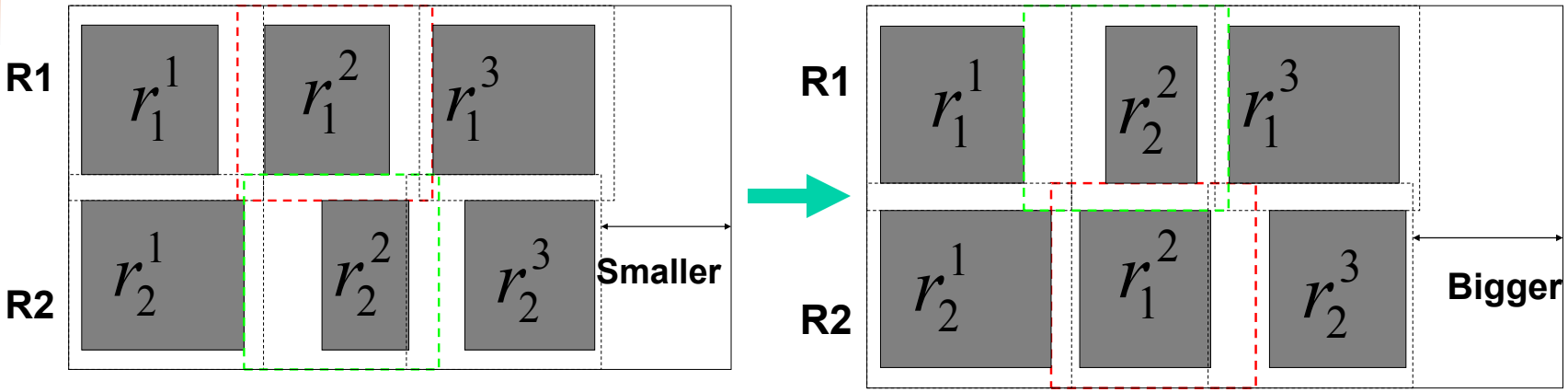


- Transform to *min-cost Hamiltonian path* problem



Multi-Row Swapping and Inter-Stencil Tuning

- Multi-Row Swapping



- Inter-Stencil Tuning
  - Exchange the placed characters with those which have not been selected

Two Dimensional Problem

- The blanking spaces of templates are non-uniform along both horizontal and vertical directions.
- Simulated Annealing Framework with Sequential Pair Representation

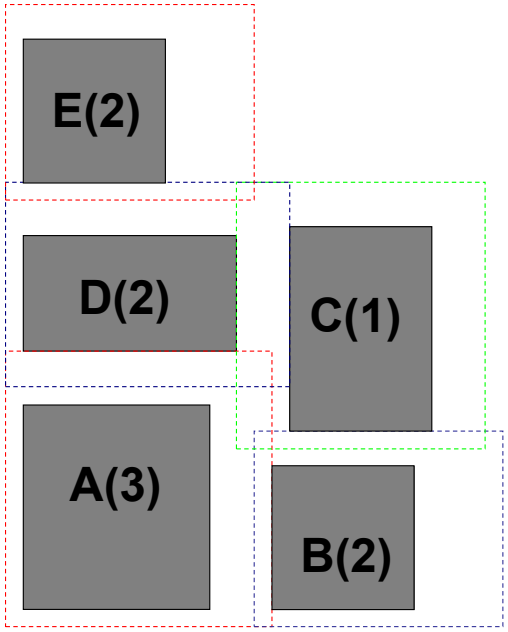
$\overline{X}, \overline{Y}$ are two permutations of characters $(c_0, c_1 \ldots c_n)$

$\overline{X} = (\ldots c_i \ldots c_j \ldots), \overline{Y} = (\ldots c_i \ldots c_j \ldots)$. c_i is left to c_j

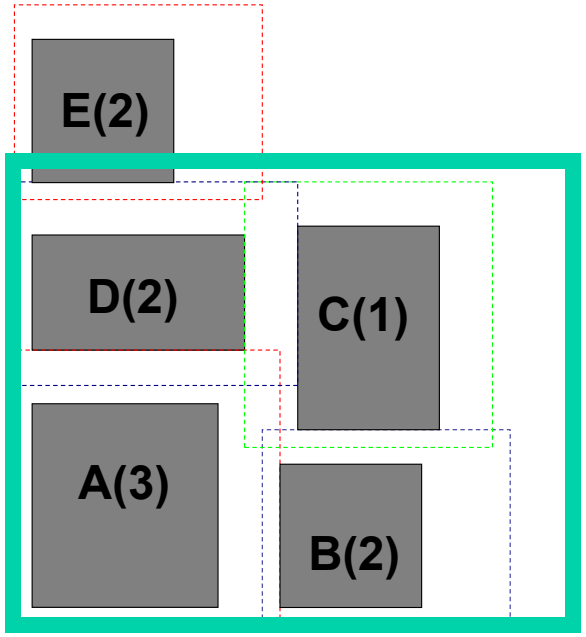
$\overline{X} = (\ldots c_j \ldots c_i \ldots), \overline{Y} = (\ldots c_i \ldots c_j \ldots)$. c_i is below c_j

Transformation from SP to Stencil

- Transform SP to a min-area packing solution
- Pick the candidates within outline of stencil as characters



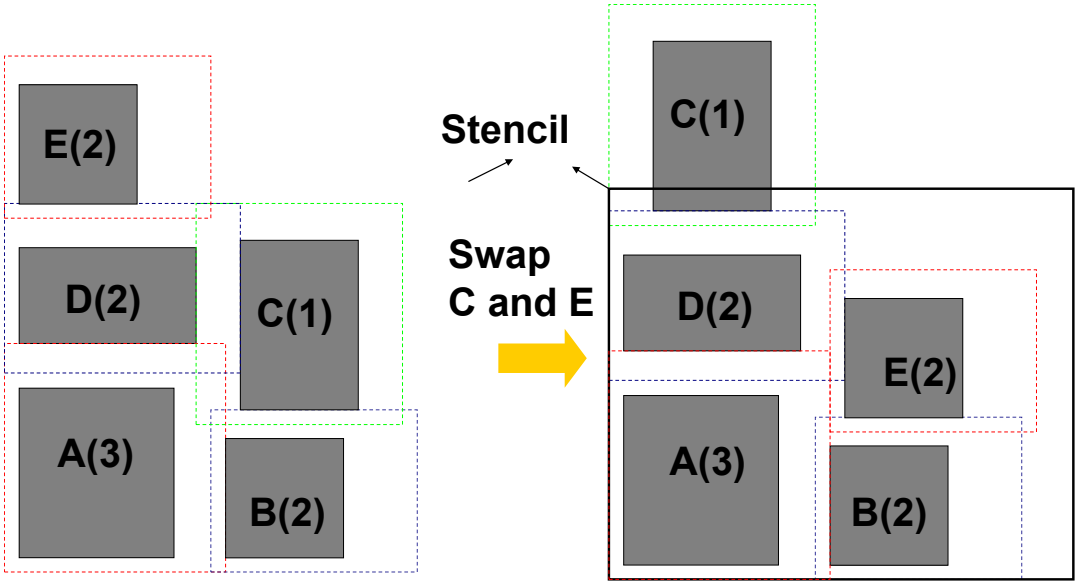
$$\overline{X} = (E\ D\ A\ C\ B)$$
$$\overline{Y} = (A\ B\ D\ E\ C)$$



$$\overline{X} = (E\ D\ A\ C\ B)$$
$$\overline{Y} = (A\ B\ D\ E\ C)$$

Throughput-Driven Swapping

- Try to reduce the projection time by swapping the positions of two candidates in the *X* & *Y* SP.



$\overline{X} = (E\ D\ A\ C\ B)$

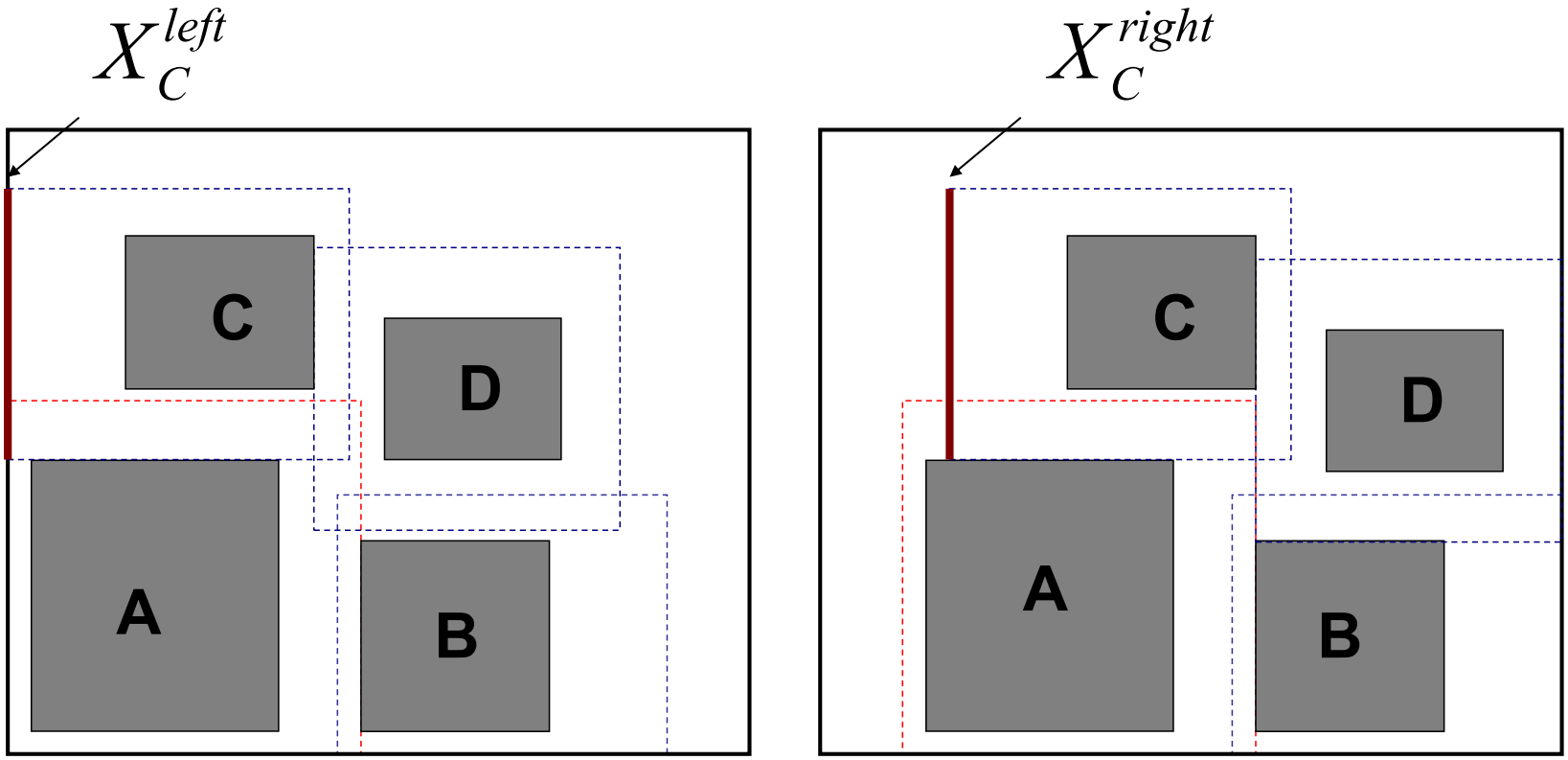
$\overline{Y} = (A\ B\ D\ E\ C)$

$\overline{X} = (C\ D\ A\ E\ B)$

$\overline{Y} = (A\ B\ D\ C\ E)$

Slack-Base Insertion

- Make use of the concept of slack to find a good position to insert extra candidate into the stencil



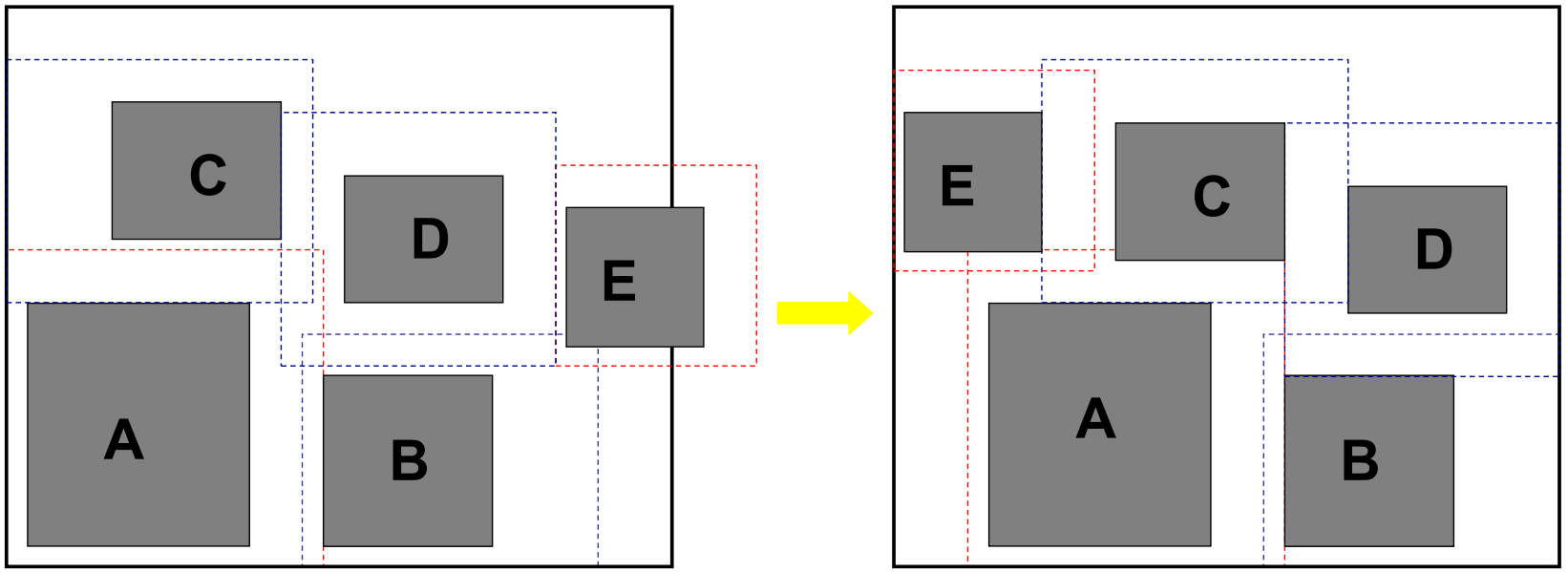
$$X_C^{slack} = X_C^{right} - X_C^{left}$$

Slack-Based Insertion

- Make use of the concept of slack to find a good position to insert extra candidate into the stencil

$$\overline{X} = (C\ A\ D\ B\ E)$$
$$\overline{Y} = (A\ C\ B\ D\ E)$$

$$\overline{X} = (E\ C\ A\ D\ B\ )$$
$$\overline{Y} = (A\ E\ C\ B\ D\ )$$



Experimental Setup

- Implemented in C++
- Intel 8 Core Linux, 3.0 Ghz, 32GB
- Parquet [TVLSI 2003] is adopted as SA framework
- Compare with two baseline methods
  - ILP-based approach without overlap characters [Sugihar, SPIE 2009]
  - Greedy bin-packing algorithm with overlap characters

Benchmark

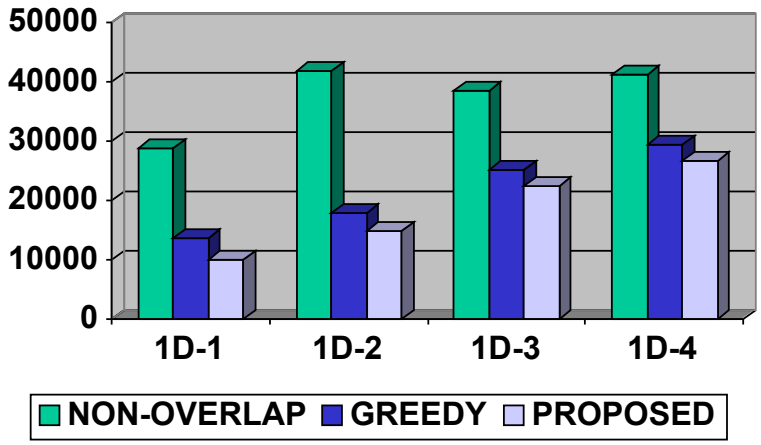
Circuit	Character Size $um \times um$	Total area $1e^4 um^2$	Total blanks $1e^4 um^2$	Optimal area $1e^4 um^2$
1D-1	3.8x3.8	1.444	0.416	1.028
1D-2	4.0x4.0	1.6	0.479	1.121
1D-3	4.2x4.2	1.764	0.514	1.25
1D-4	4.4x4.4	1.936	0.569	1.367
2D-1	3.8x3.8	1.444	0.414	1.03
2D-2	4.0x4.0	1.6	0.529	1.071
2D-3	4.2x4.2	1.764	0.662	1.102
2D-4	4.4x4.4	1.936	0.774	1.162

The area of stencil is $100um \times 100um$

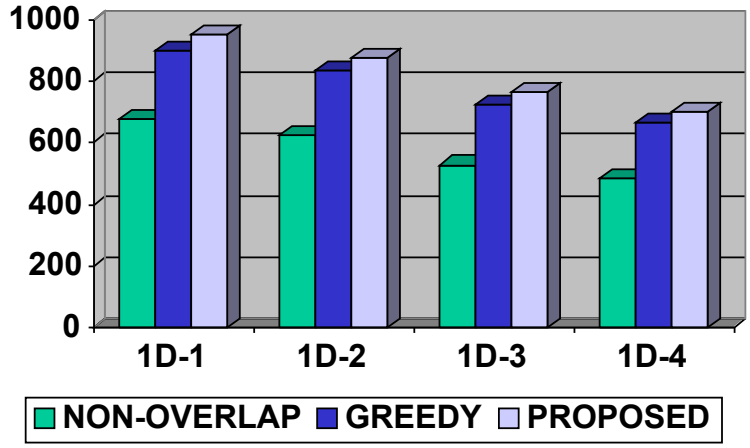
1000 character candidates

One Dimensional Stencil Design

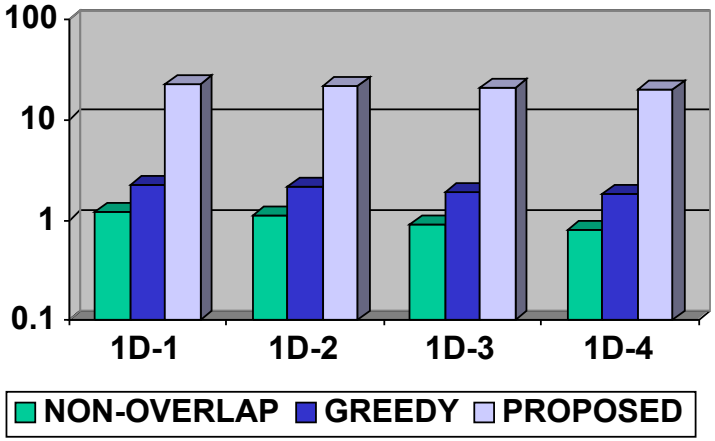
#shots (projection time)



#characters on stencil



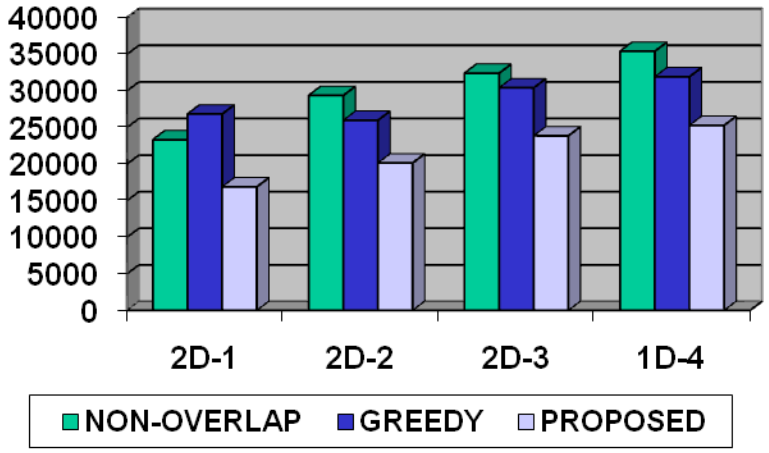
#CPU(logscale)



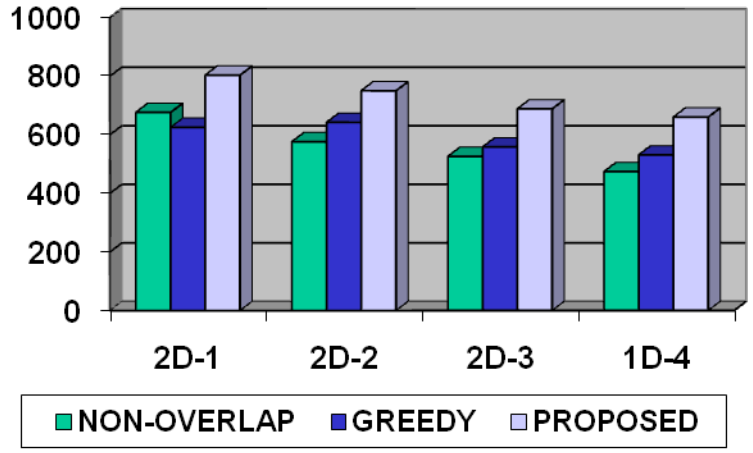
- 51%, 14% reduction on shot number over previous ILP-based approach without overlapping characters and greedy algorithm.

Two Dimensional Stencil Design

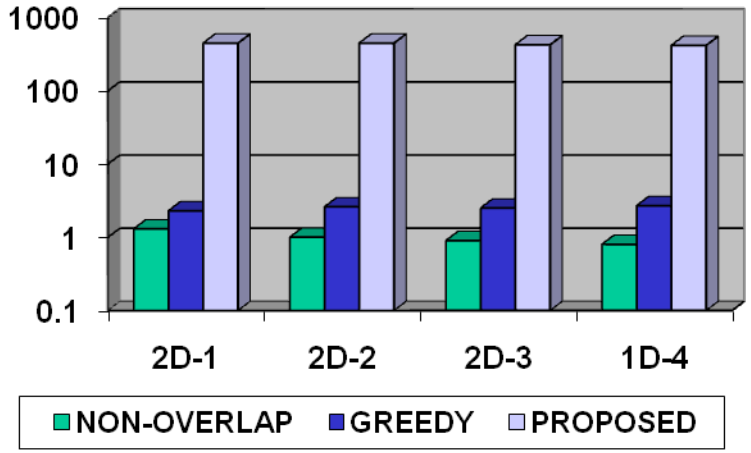
#shots (projection time)



#characters on stencil



#CPU(logscale)



- 31%, 25% reduction on shot number over previous ILP-based approach without overlapping characters and greedy algorithm.

Conclusion

- E-Beam Lithography is a promising emerging technology for better resolution and lower cost
- Low throughput is its key hurdle
- E-beam lithography stencil planning and optimization with overlapped characters
- Lots of future research opportunities on physical design and emerging lithography
  - E-beam multi-stencil optimization problems
  - Massive parallel e-beams/characters
  - Double/triple patterning lithography
  - EUV, ……

Acknowledgment

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- Dr. Gi-Joon Nam at IBM Austin Research Lab for helpful discussions.

Thank you!