Litho and Design: Moore Close Than Ever

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Gasp!

Outline

- The frenetic pace of Moore's Law, and why we put up with it!
- How the co-optimization of design and lithography have enabled Moore
- How computational lithography is squeezing more juice out of steppers

The Economics of Moore's Law

The Benefit: $

Source: STS/Gartner/Intel

The Cost:

FAB	$4 B
PILOT LINE	$1-2 B
R&D PROCESS TEAM	$0.5-1 B

Source: Intel

Investment & co-optimized execution required to maximize the benefit

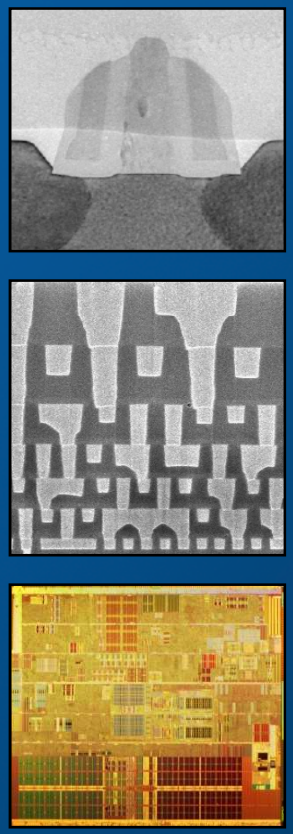
Intel's Silicon R&D Pipeline

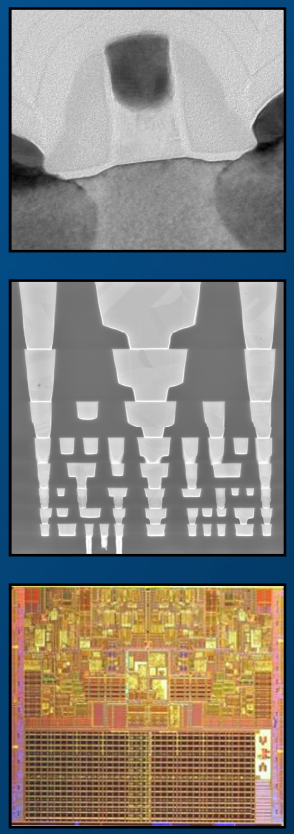
Research Pathfinding Development Manufacturing

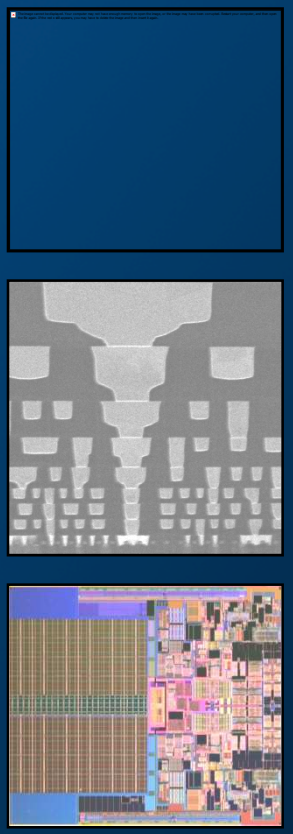
Continuous flow of new technologies from research to development to manufacturing

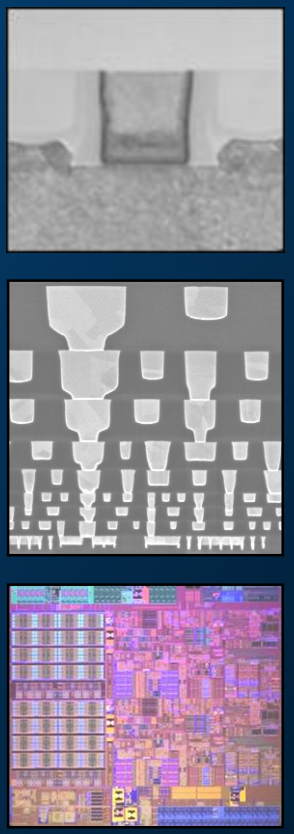
On-time 2 Year Cycles

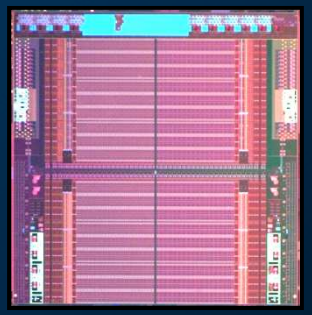
90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011





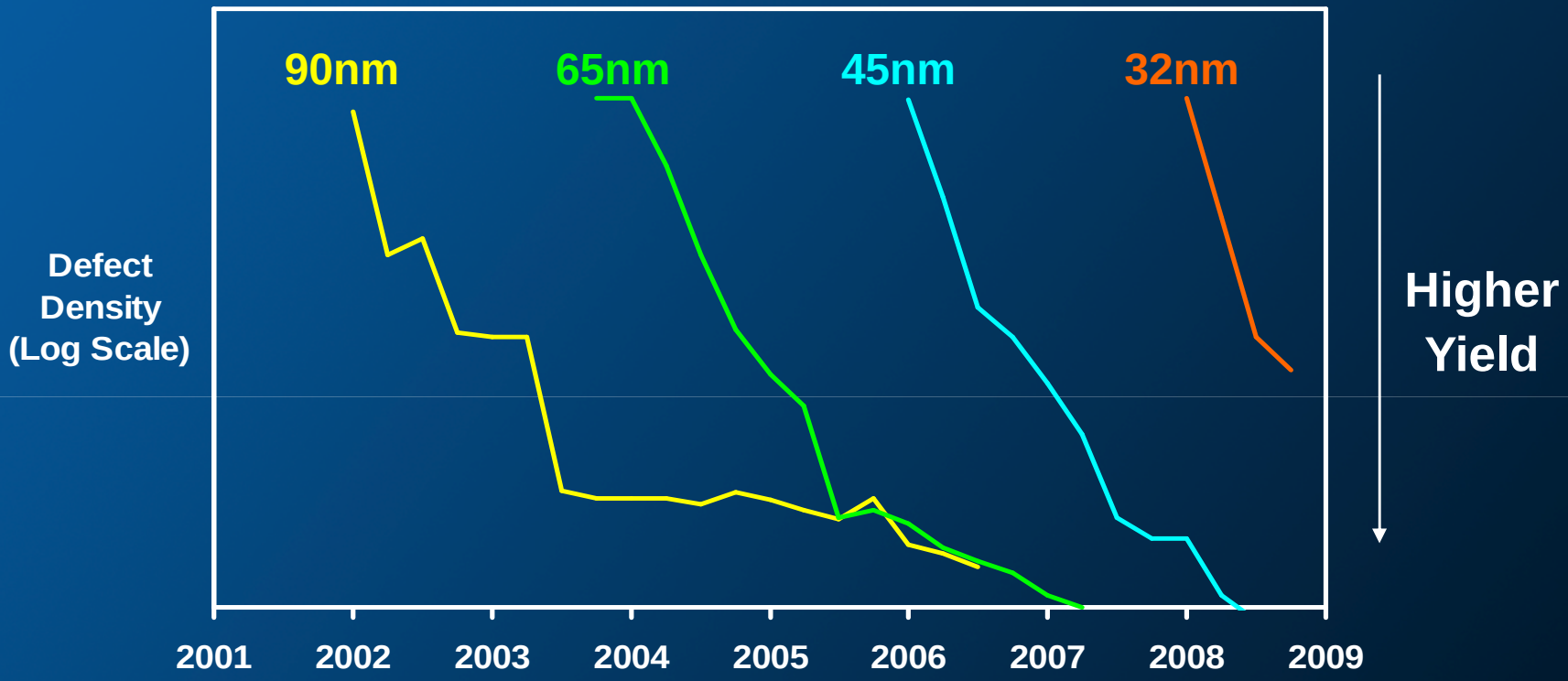






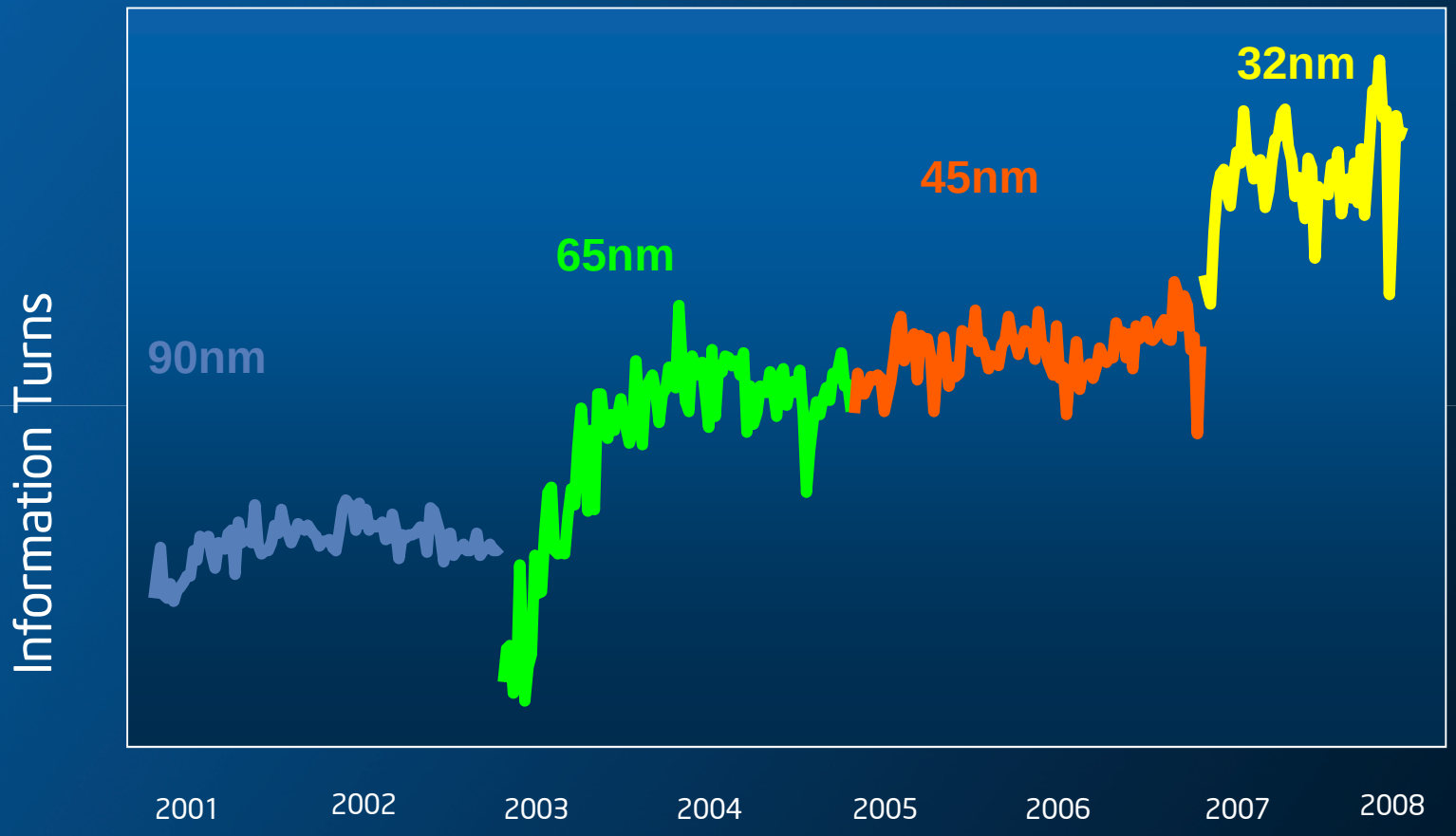
In development

Defect Density Trends



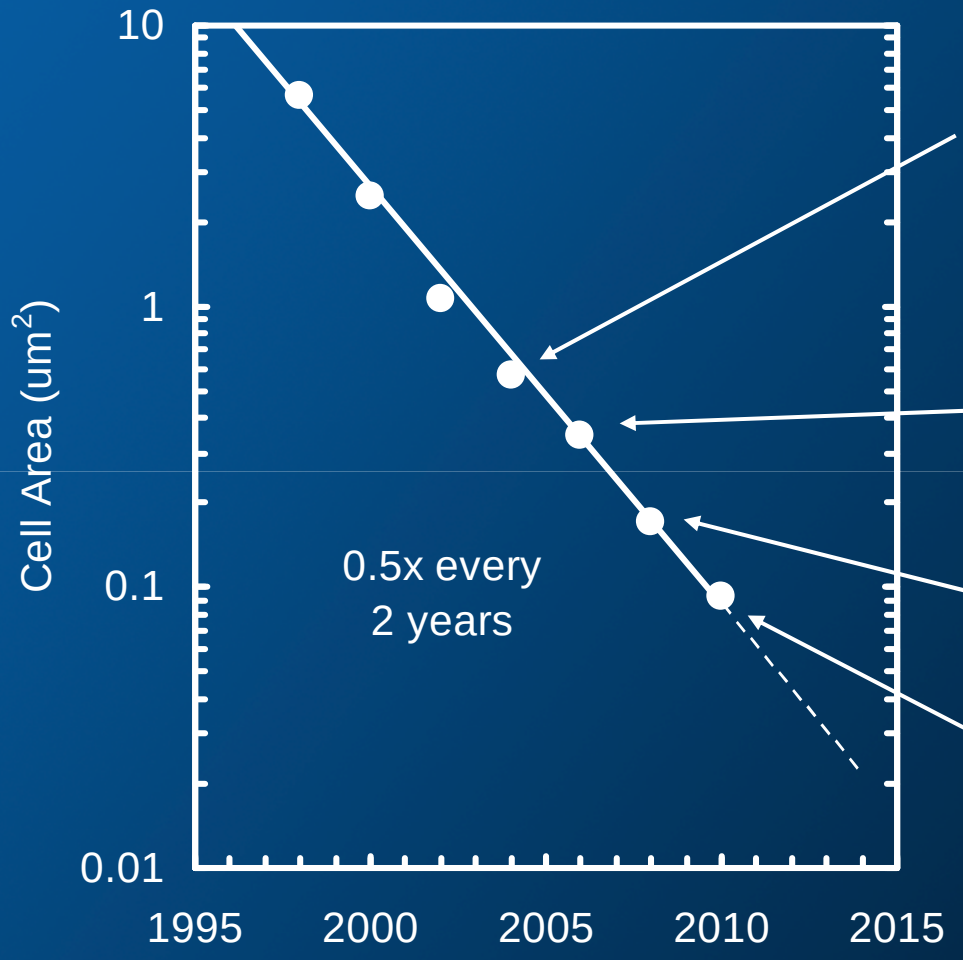
Continuing to improve wafer defect density is crucial to achieving historical yield trends

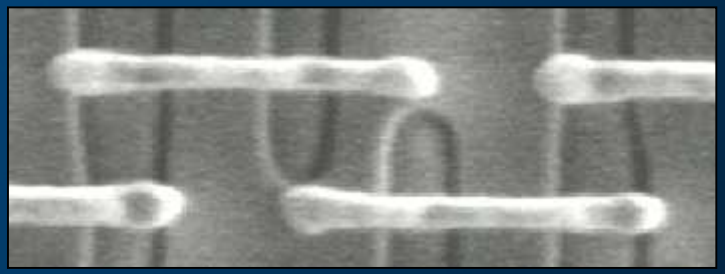
Breakthroughs in Technology Information Turns



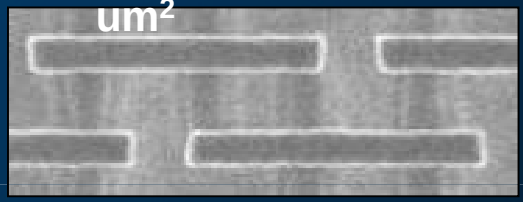
1.7 X improvement in Information turns
Faster information back to process development and design teams

SRAM Cell Size Scaling

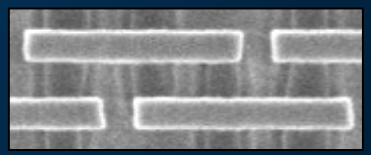




65 nm, 0.570 um²



45 nm, 0.346 um²

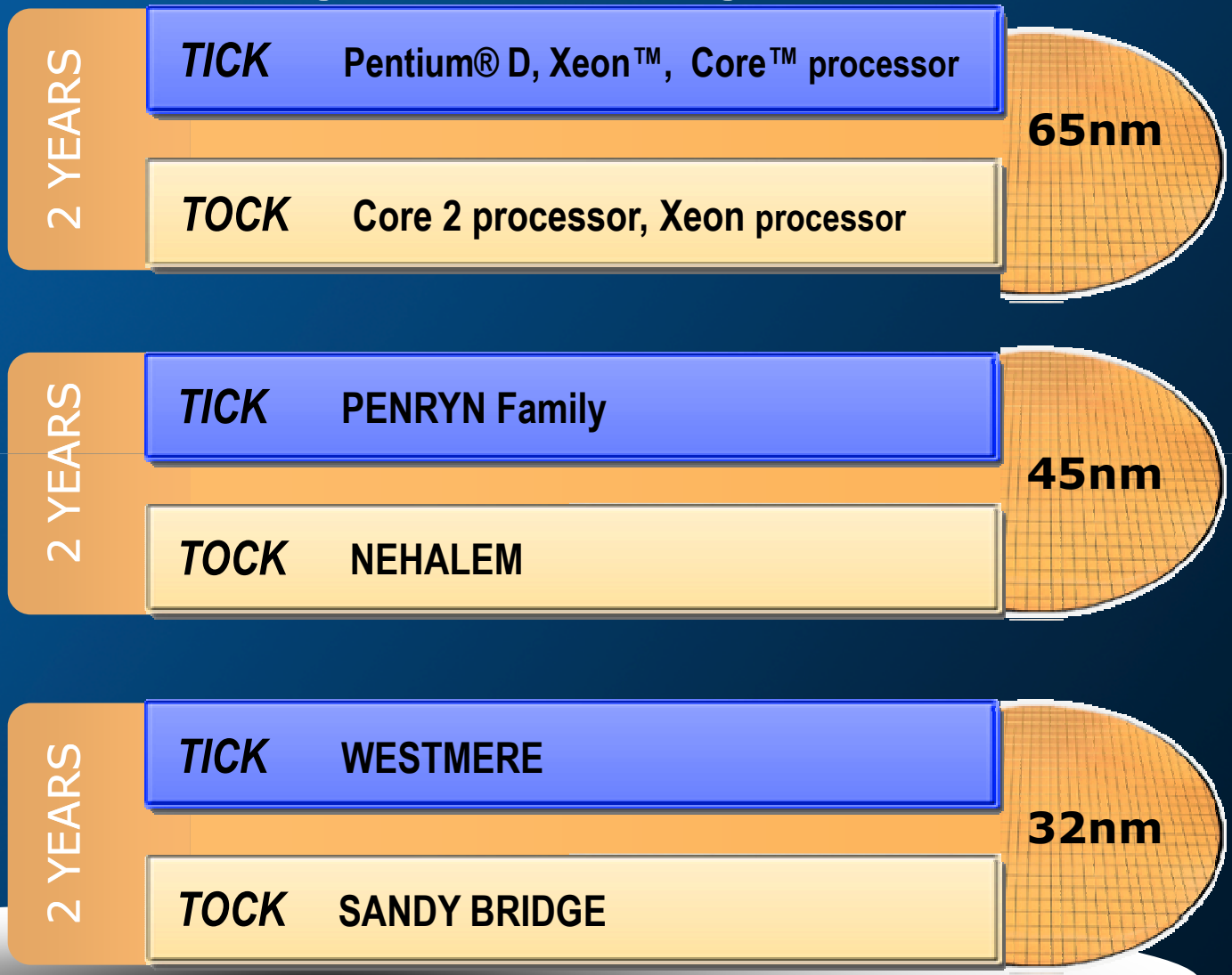


32 nm, 0.171 um²

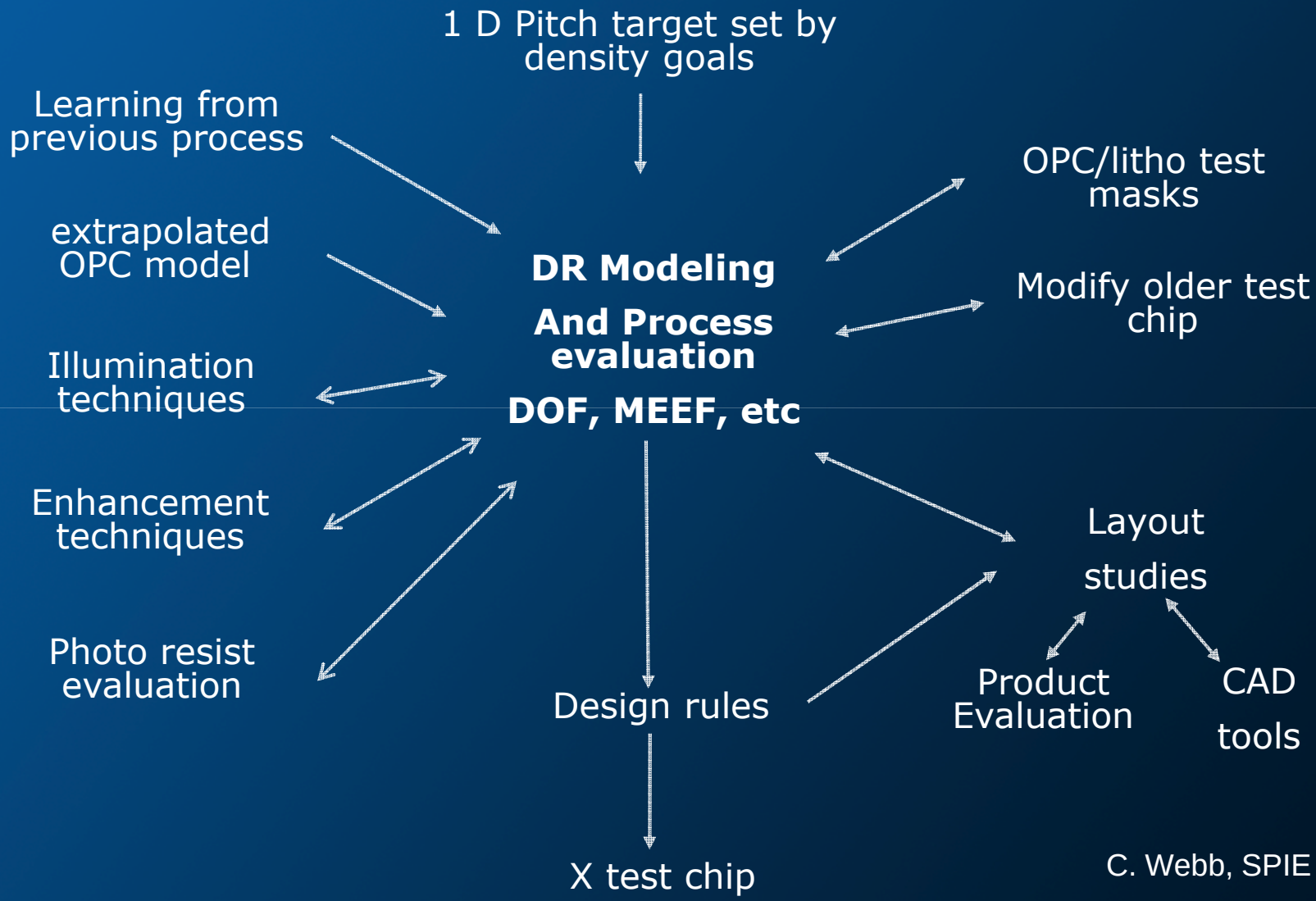
22 nm, 0.092 um²

All Patterned with 193nm!!

Tick-tock: an example from Intel of process and design marching in cadence

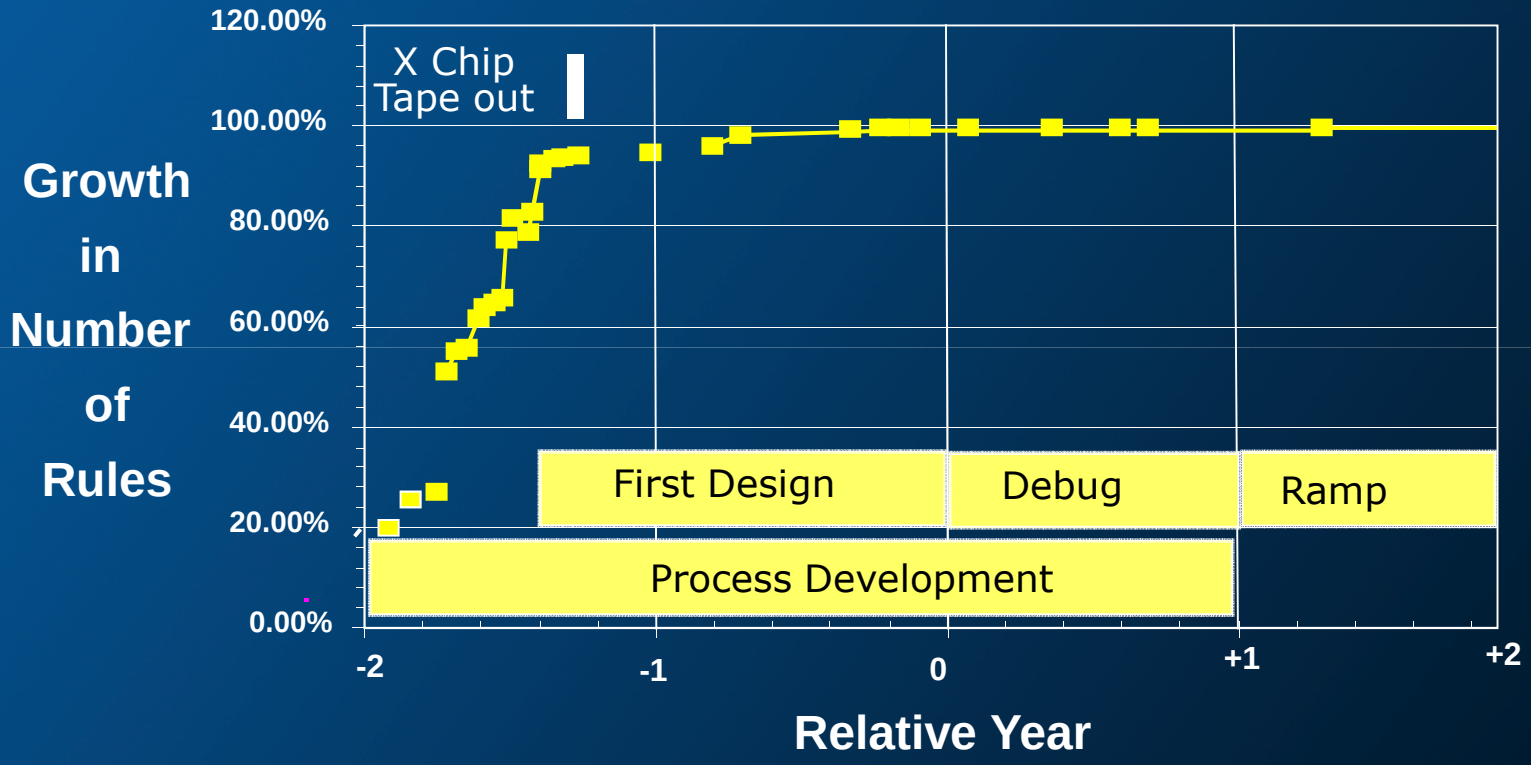


Design Rule Definition Process: How Litho and Design are connected



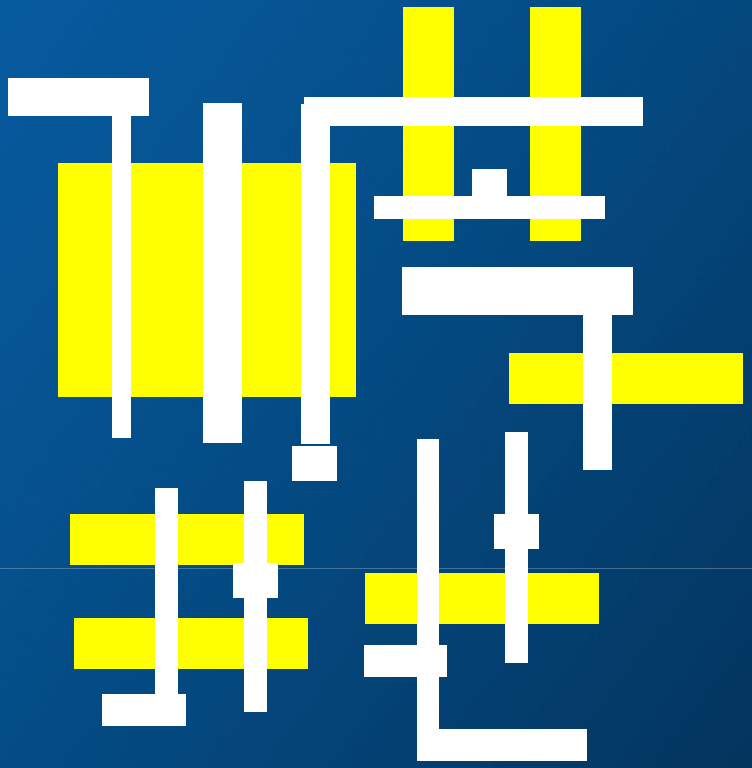
C. Webb, SPIE 2007

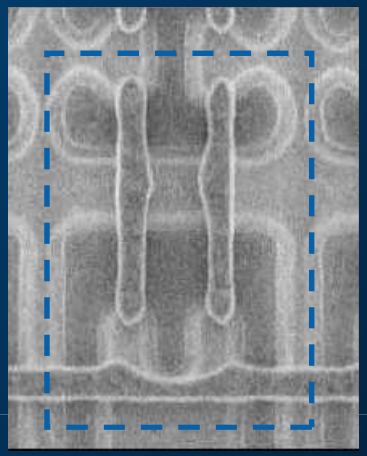
Rule Stability



C. Webb, SPIE 2007

130nm



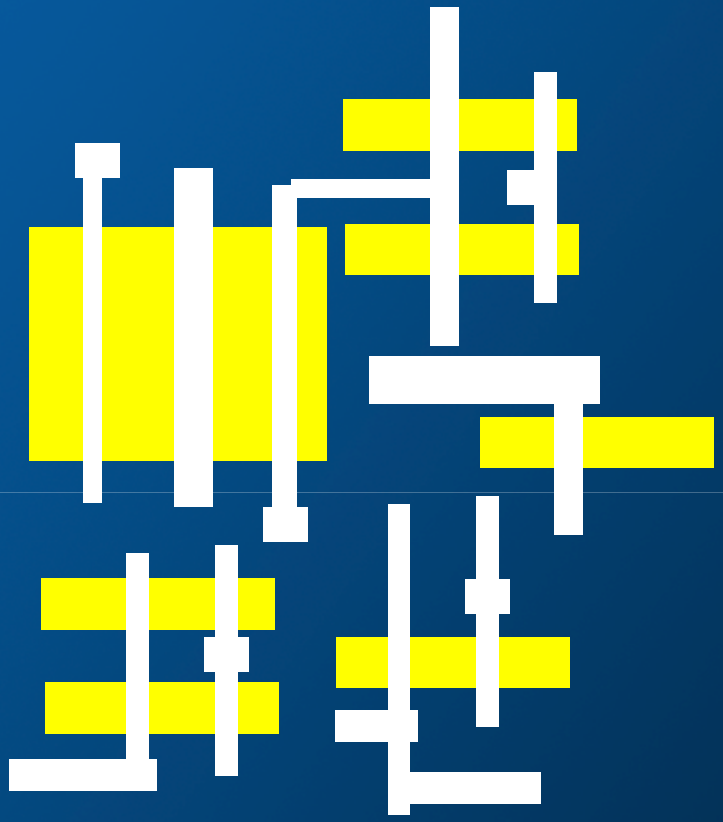


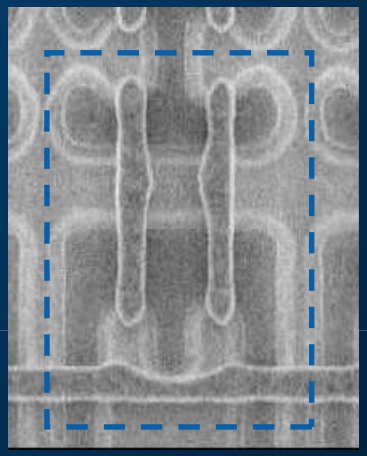
SRAM Bit

- **Variable poly pitch and line widths**
- **X and Y transistor orientation**
- **Design rule definition was primarily done through simple scaling of rules from previous generation**
- **Limited modeling of layout and design rules**

C. Webb, SPIE 2007

90nm
47% increase in number of poly rules





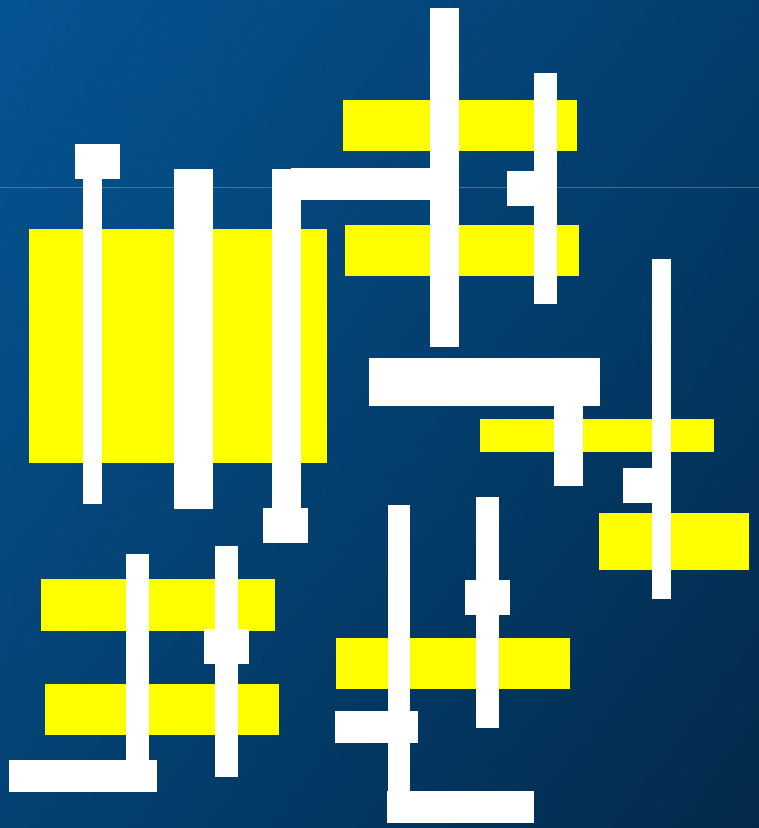
SRAM Bit

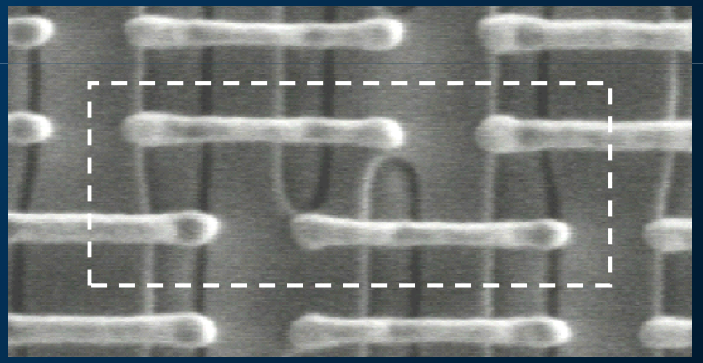
- **All Devices in one orientation except SRAM**
- **Complex rules did not impact transistor density**
  - **Modeling and layout study effort increased from 130nm generation**

C. Webb, SPIE 2007

65nm
65% increase in number of rules

- **All Devices in one orientation including SRAM**
- **Rules to enable phase shift masks**
- **Different rules for minimum pitch, larger poly pitch and poly routing**
- **Layout more difficult but no significant density impact**

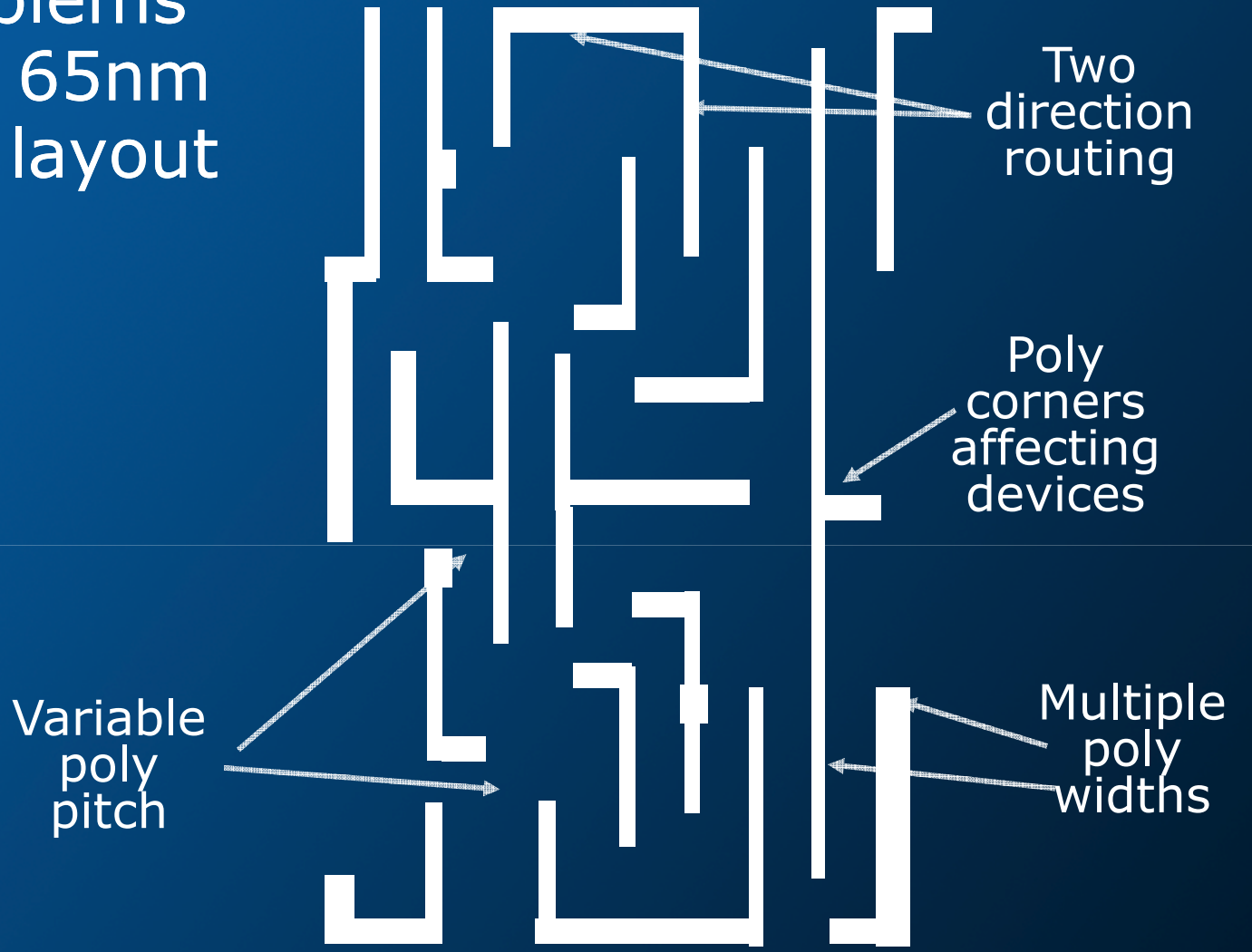




SRAM

C. Webb, SPIE 2007

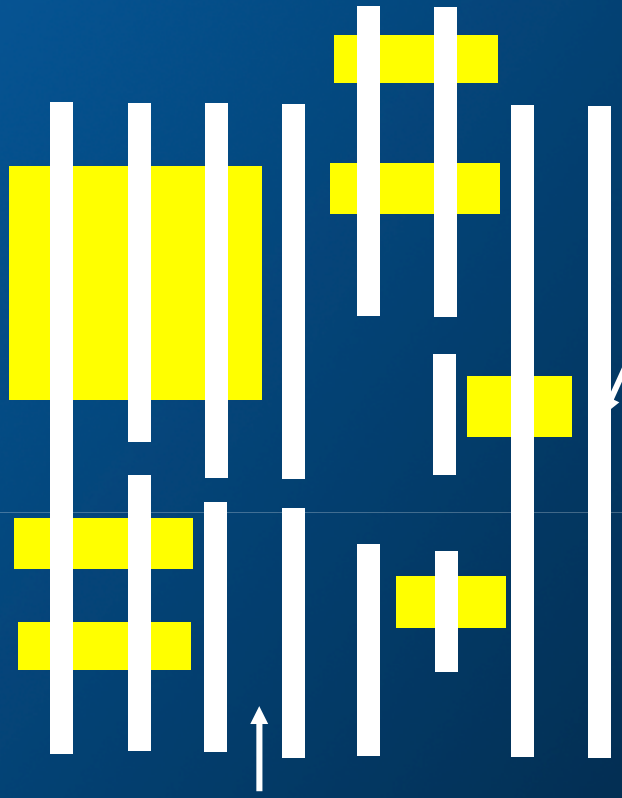
Problems with 65nm poly layout



Could all logic poly layout be simple like the SRAM bit?

C. Webb, SPIE 2007

45nm Logic Layout
37% reduction in number of rules

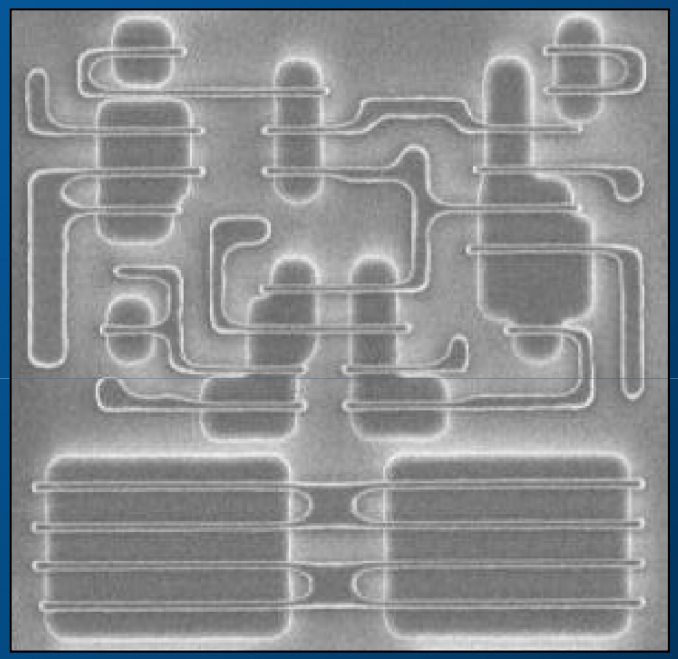


- **No significant density impact**
- **Design had to adapt to limited channel length choices and new layout style**

C. Webb, SPIE 2007

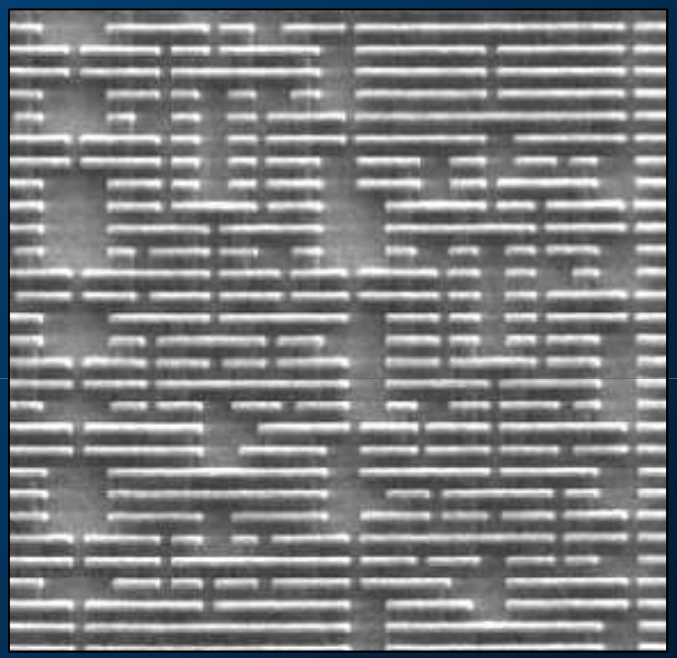
Layout has adapted to litho constraints, without affecting Moore's march

65 nm Layout Style



- **Bi-directional features**
- **Varied gate dimensions**
- **Varied pitches**

32 nm Layout Style

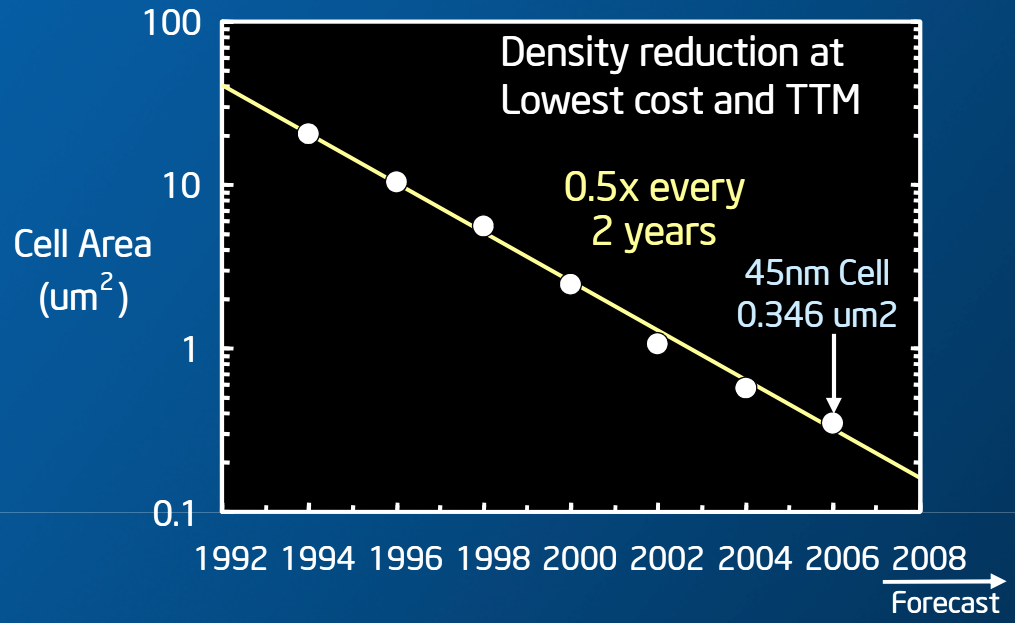


- **Uni-directional features**
- **Uniform gate dimension**
- **Gridded layout**

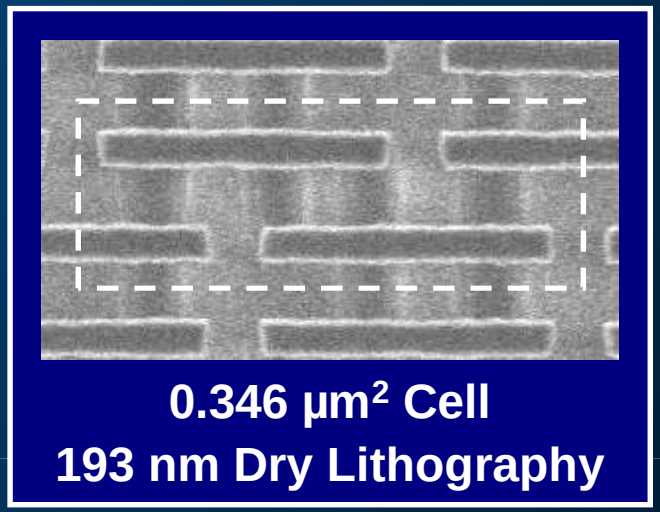
M. Bohr, ISCC, 2009

What matters is Best Total Cost

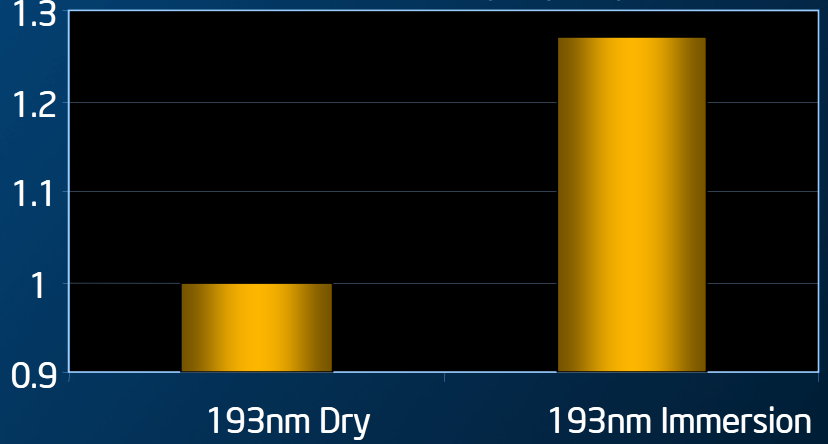
SRAM Cell Size



SRAM - Functional silicon in Jan '06

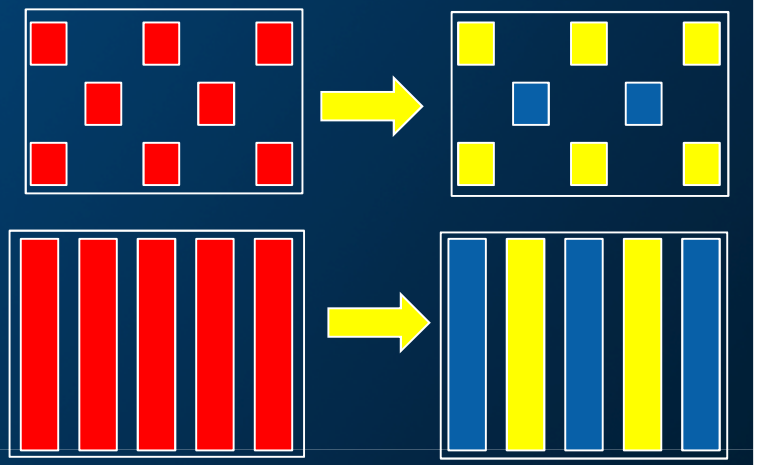


Critical Layer Lithography Cost Comparison
45nm Node assuming equal yield

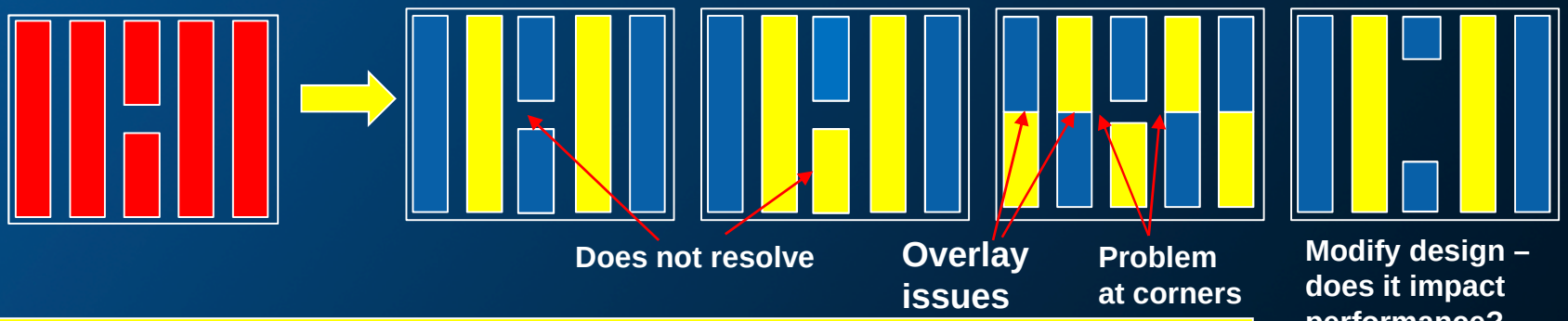


Multi-mask patterning – a friend in need

- As wafer dimensions reach optical limits, multi-mask patterning came to rescue
- Works well for simple repeated patterns

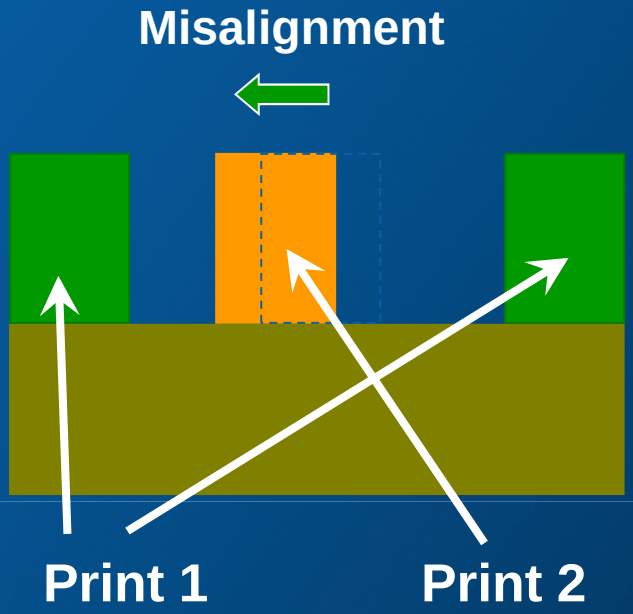


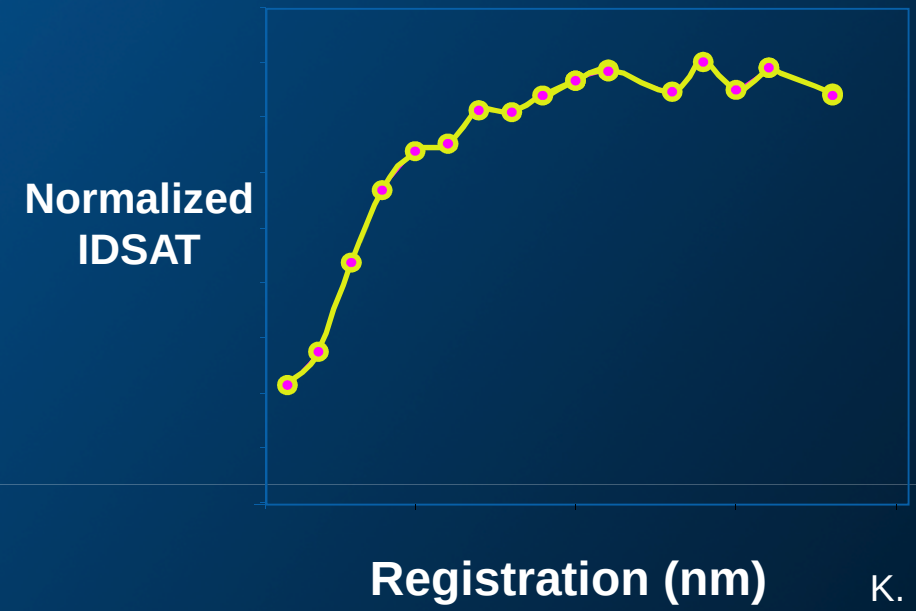
- Not so well with general patterns



- **Need complex design rules to capture multi-mask conflicts**
- **Design tools need to be multi-mask aware to minimize impact**

One implication of Double-patterning



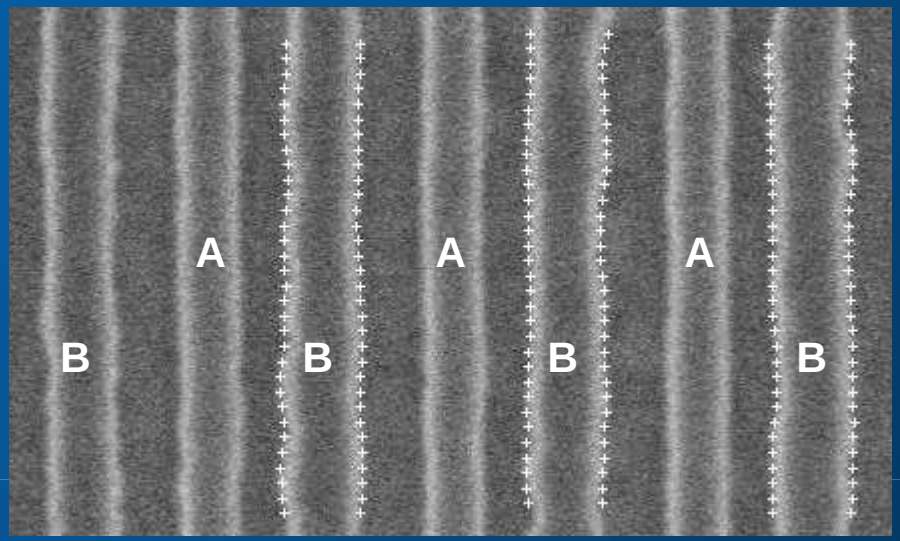


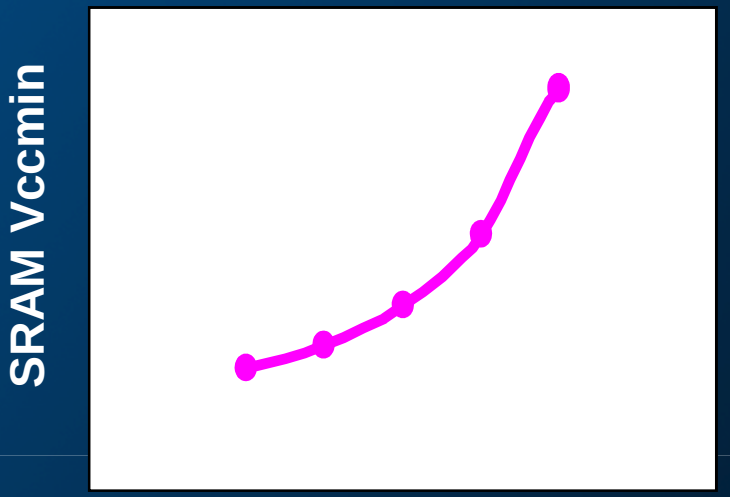
K. Kuhn, ICVC, 2009

Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability

Transistor parameters can be affected by asymmetry between the source and drain regions

Pitch doubling and gate CD matching



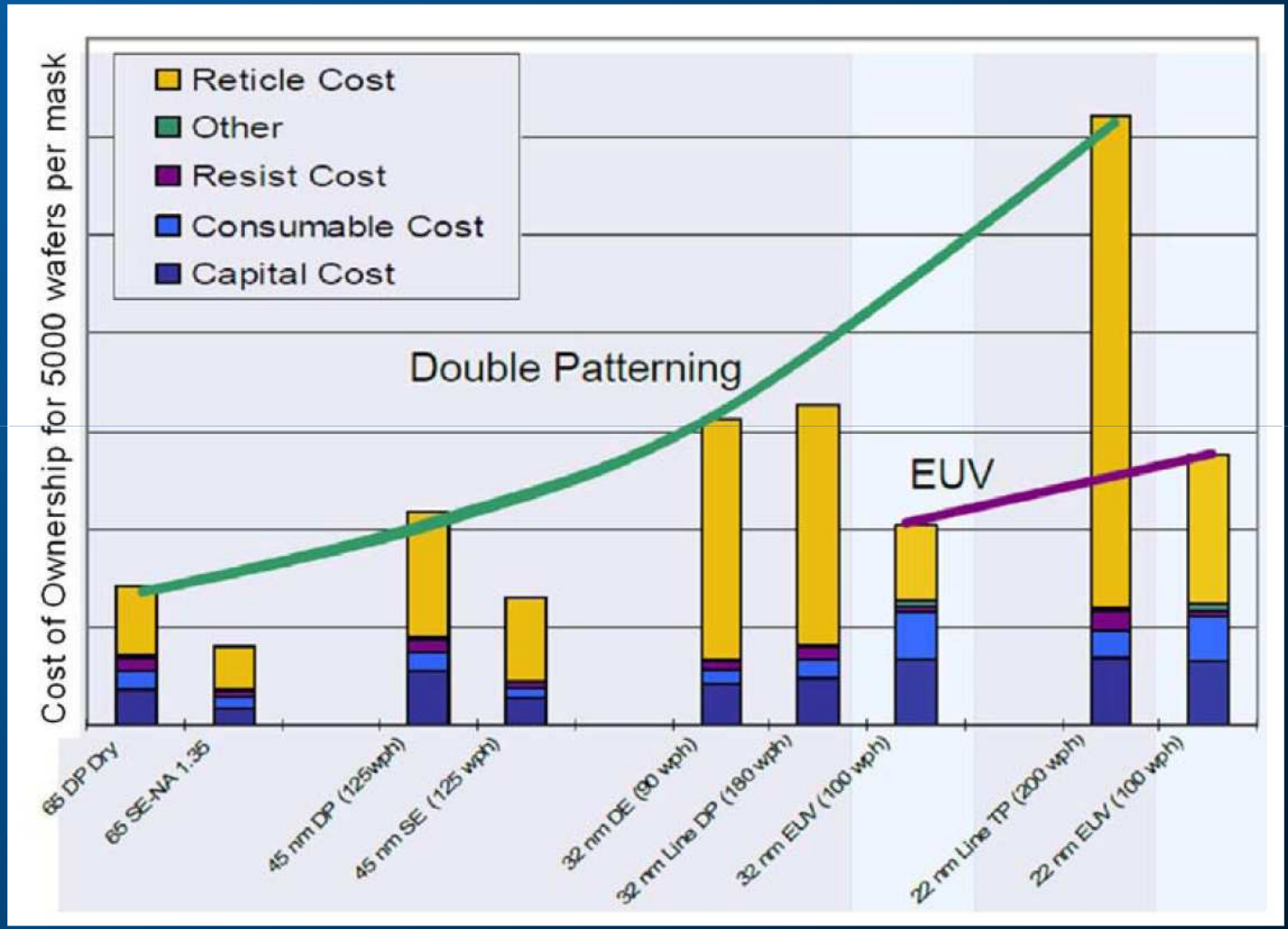


C. Kenyon, TOK conf., Dec. 2008

Pitch doubling eliminates the close correlation which currently exists between the CDs of adjacent gates

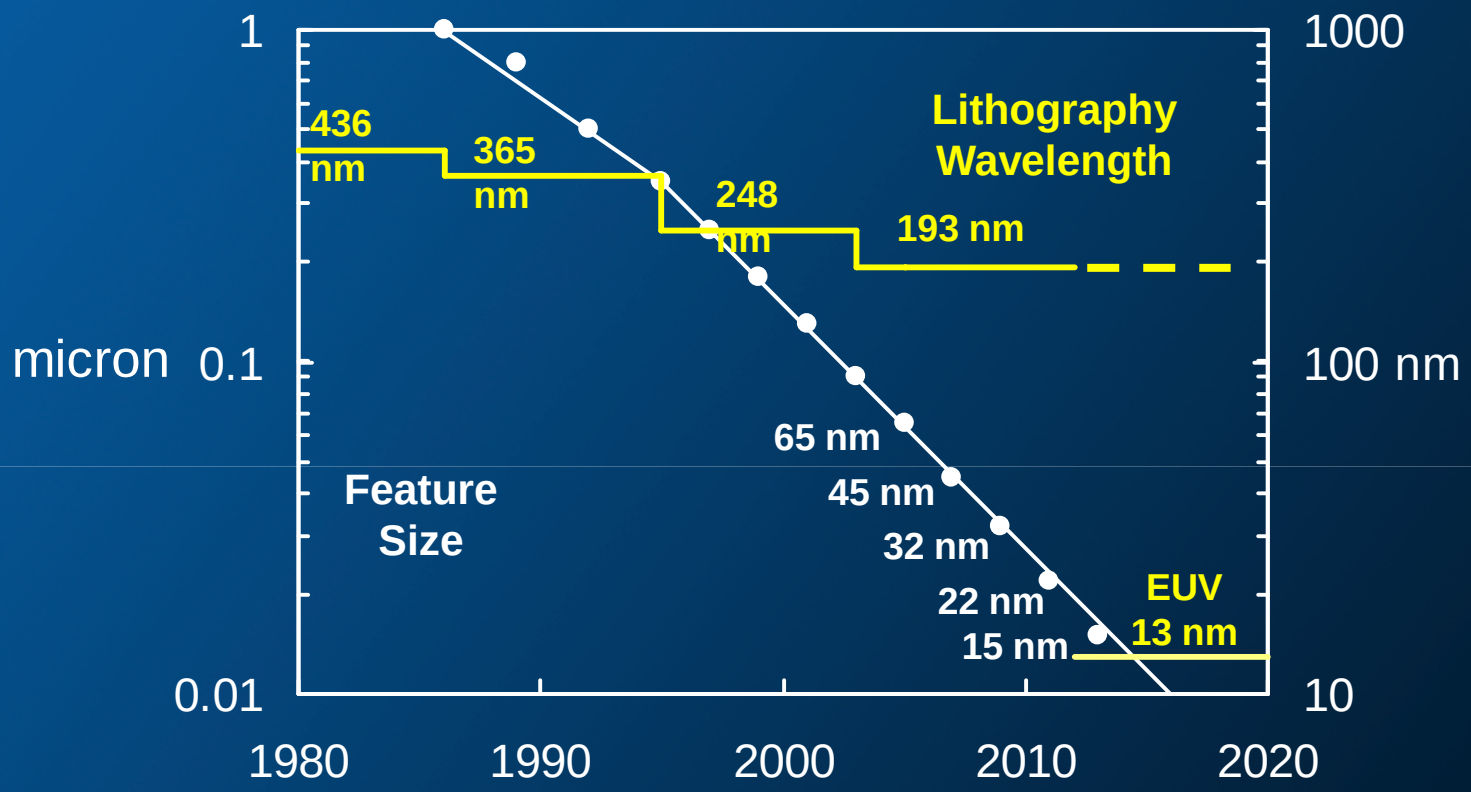
This has implications for memory cells and other circuits which depend upon this CD matching

NGL solutions can help contain rising cost of double patterning



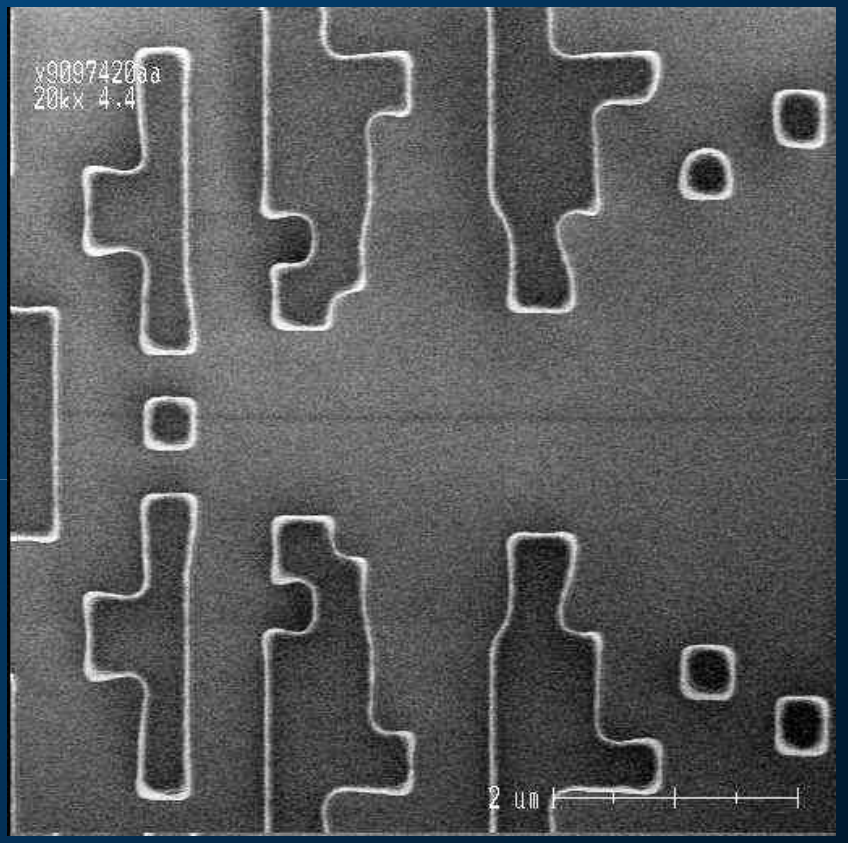
Source: ITRS 2009

Computational lithography – enabling Moore



Computational lithography innovations and co-optimization with design necessary to bridge this gap

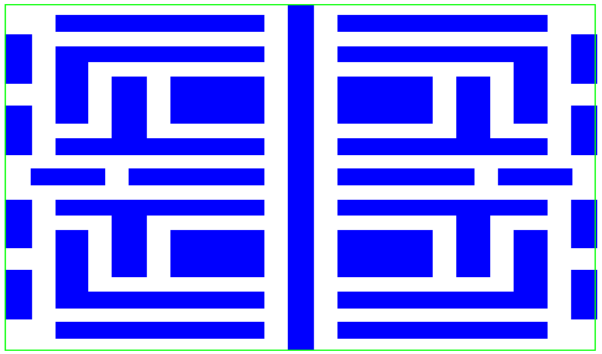
2D Effects Become Important



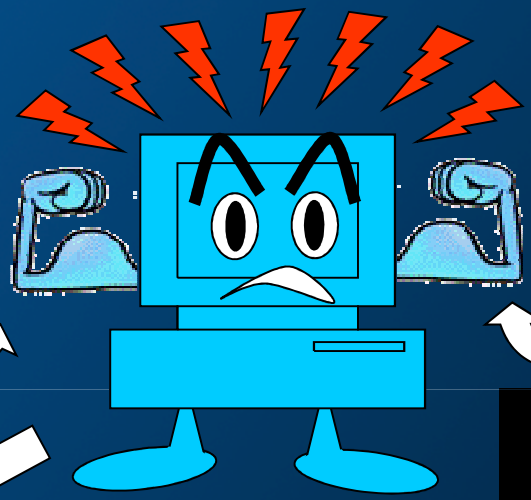
Rule-based serif placement were first instance of on-mask pattern manipulation to deliver design intent

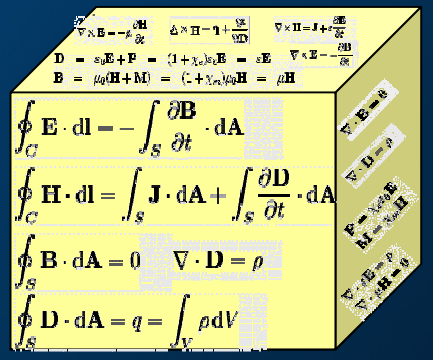
S. Sivakumar, SPIE, 2011

One CL product: pixelated masks

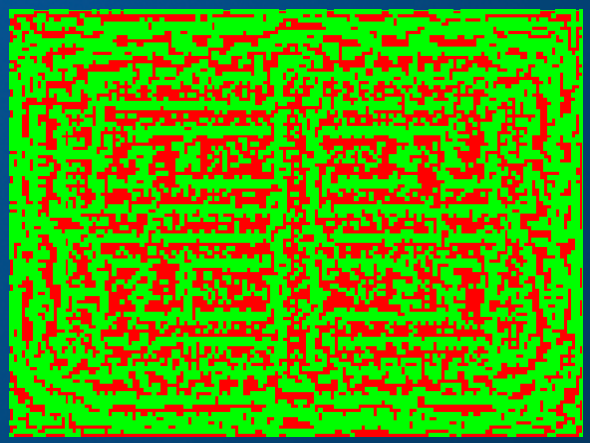


Design Pattern

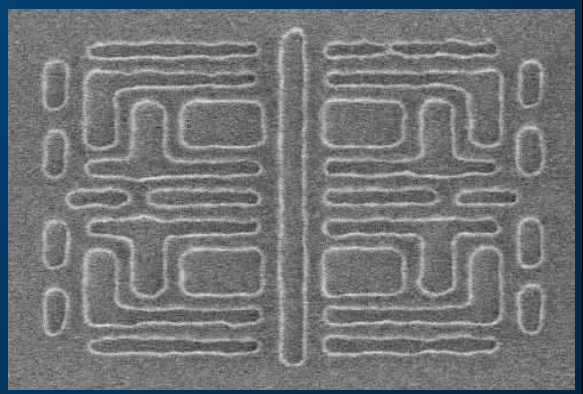




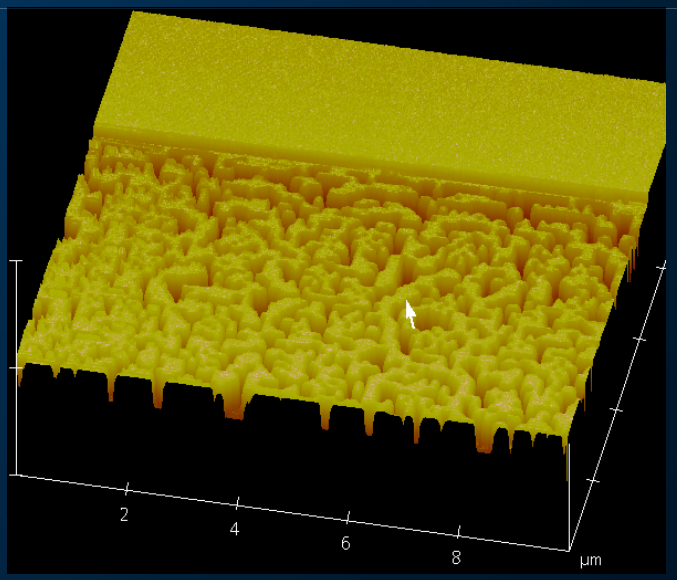
Model black-box



Pixelated mask

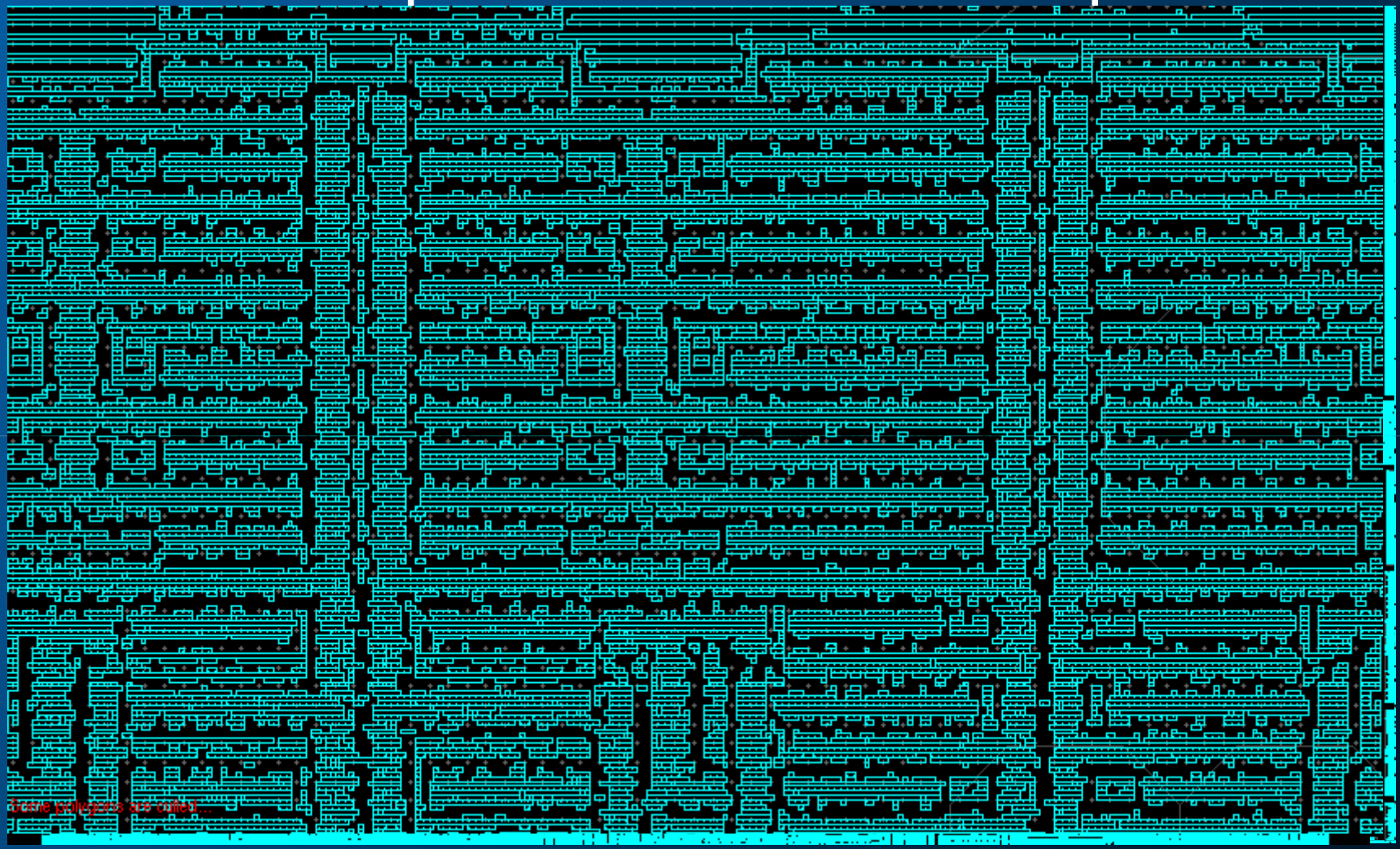


SEM image of wafer



Atomic Force Microscope Picture of the mask

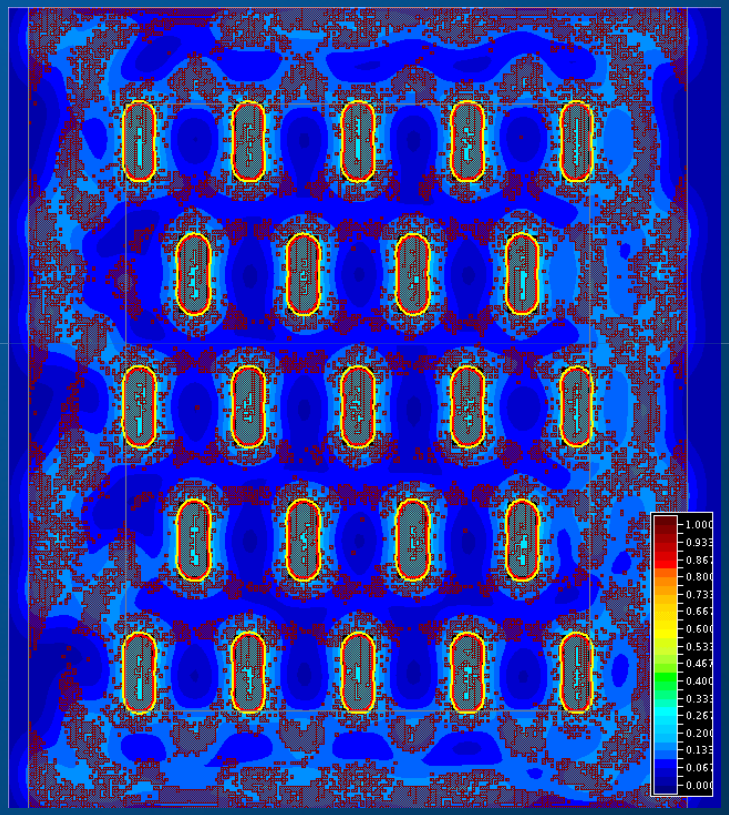
A Full-Chip View is worth a trillion pixels



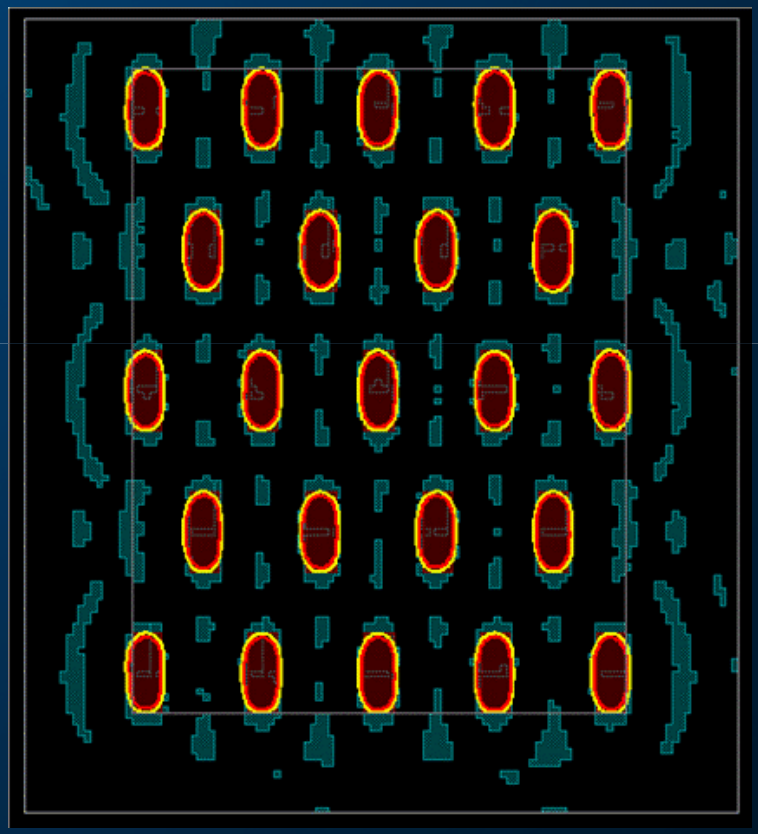
Note: some cells are not visible due to graphics culling
Top-cell pixels are not displayed
Only 0-deg pixels are displayed

Convert pixelated mask to more manufacturable mask, while preserving performance

pixelated mask

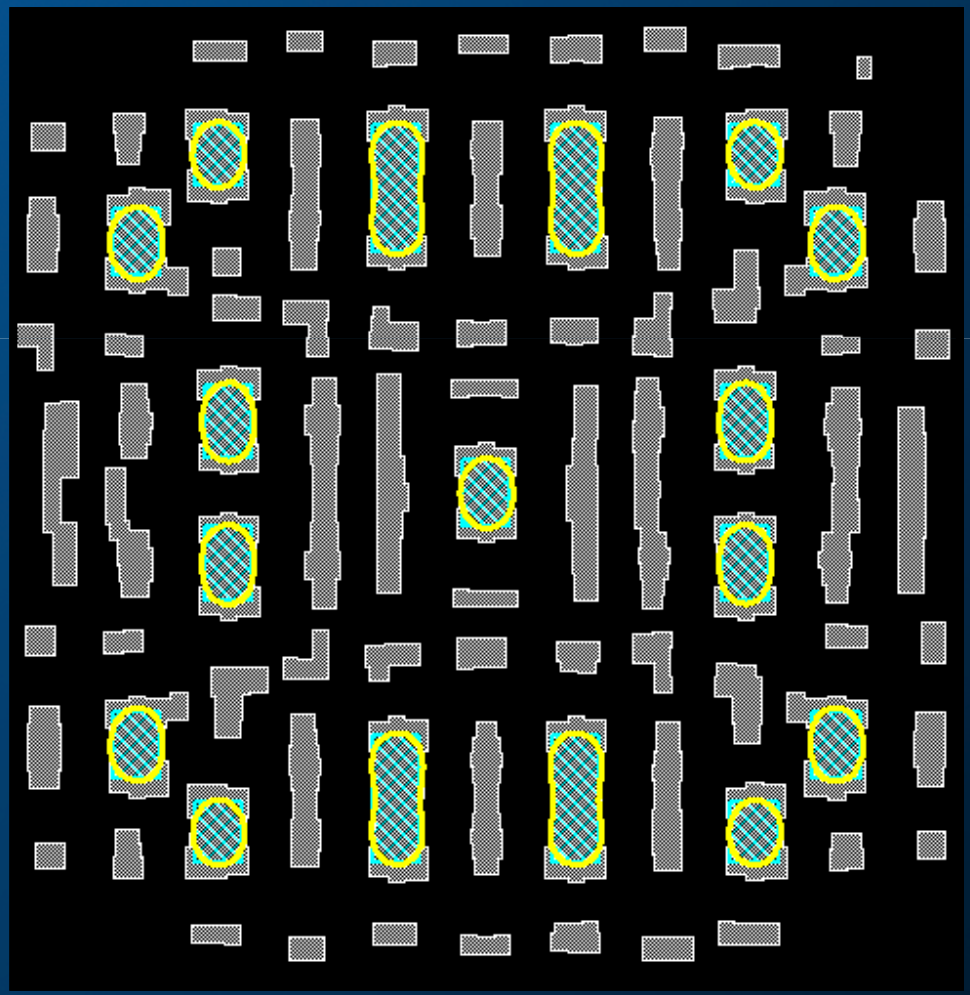


More manufacturable mask



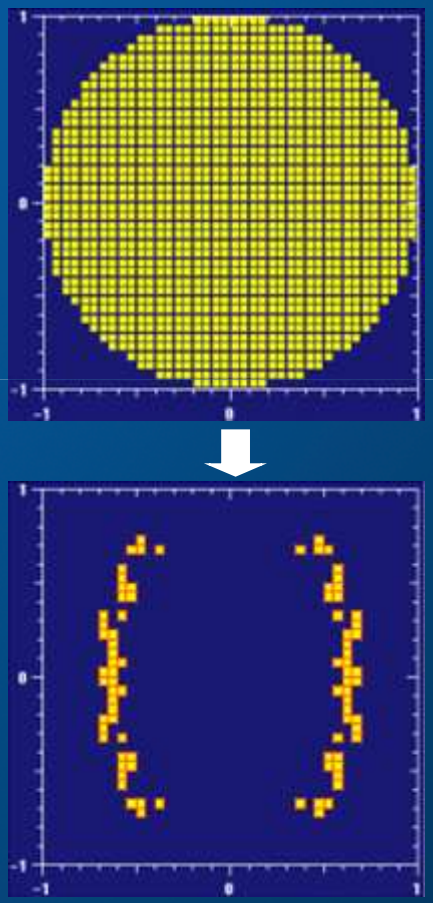
Two pronged approach:

simplify inverse masks
improve mask shop capabilities

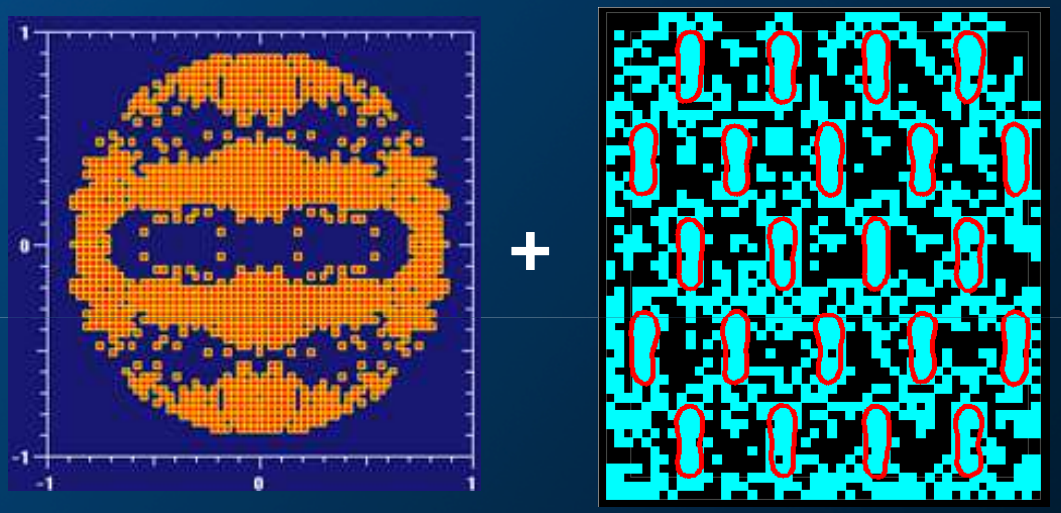


Optimizing Source and Mask

Source Optimization



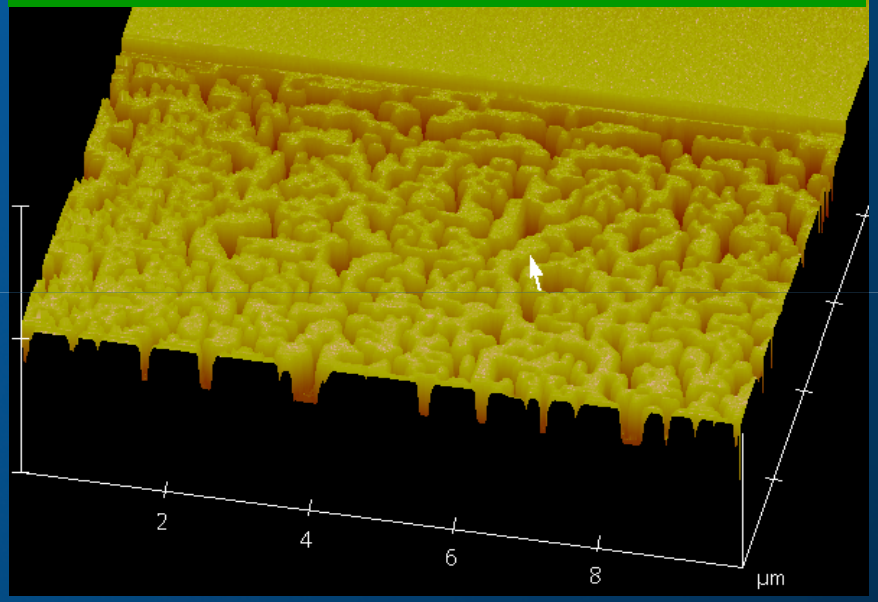
Source Mask Optimization



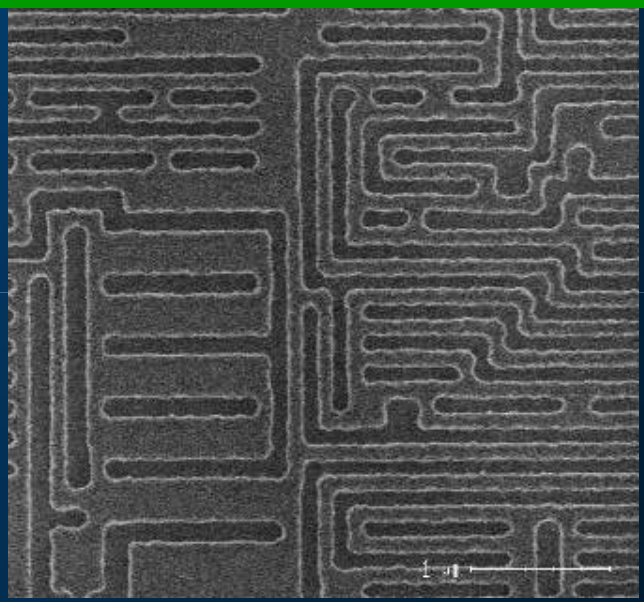
Computational Lithography is a key enabler for extracting maximum resolution from existing technology

Ultimately, the proof is in the pudding. Exotic techniques need to be viable for production.

Atomic Force Microscope Picture of Pixelated Phase Mask



SEM Picture of 65nm MT1 resist Pattern from Pixelated Phase Mask



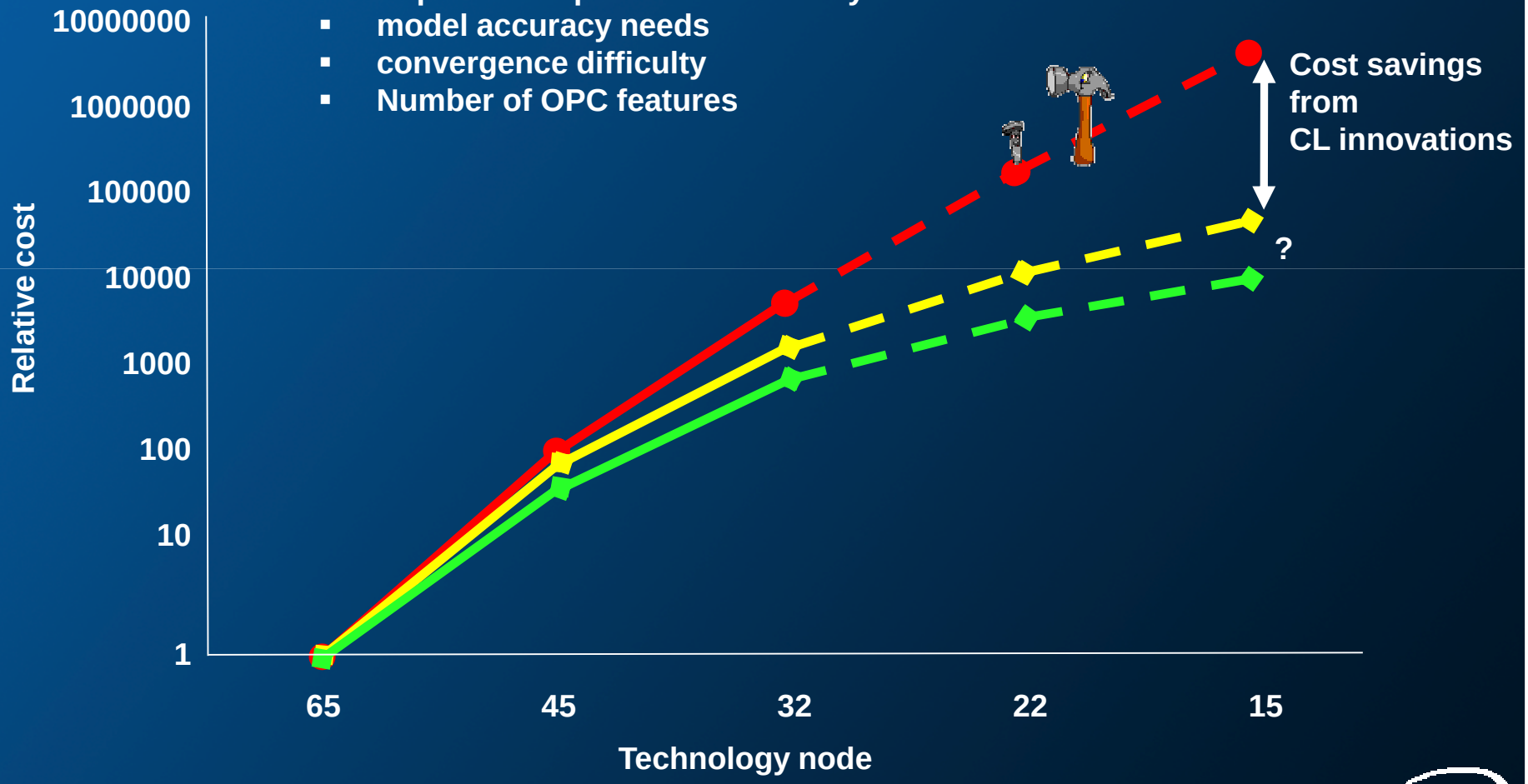
Defect free Pixelated Phase Masks produced, Leading 65nm node Microprocessor patterned at MT1 with Pixelated Phase Mask yielded close to manufacturing baseline

Computational lithography is helping extract more resolution from existing technology

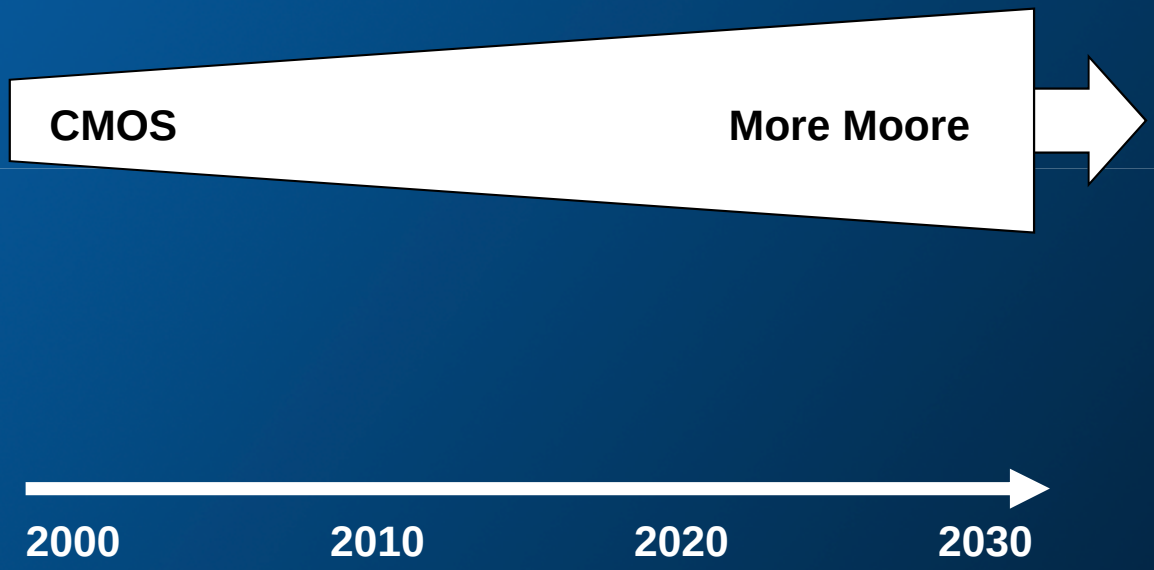
Other things being equal, you can measure CL innovation through compute cost

A new node increases compute cost due to increase in:

- number of OPC layers
- density
- required computational accuracy
- model accuracy needs
- convergence difficulty
- Number of OPC features



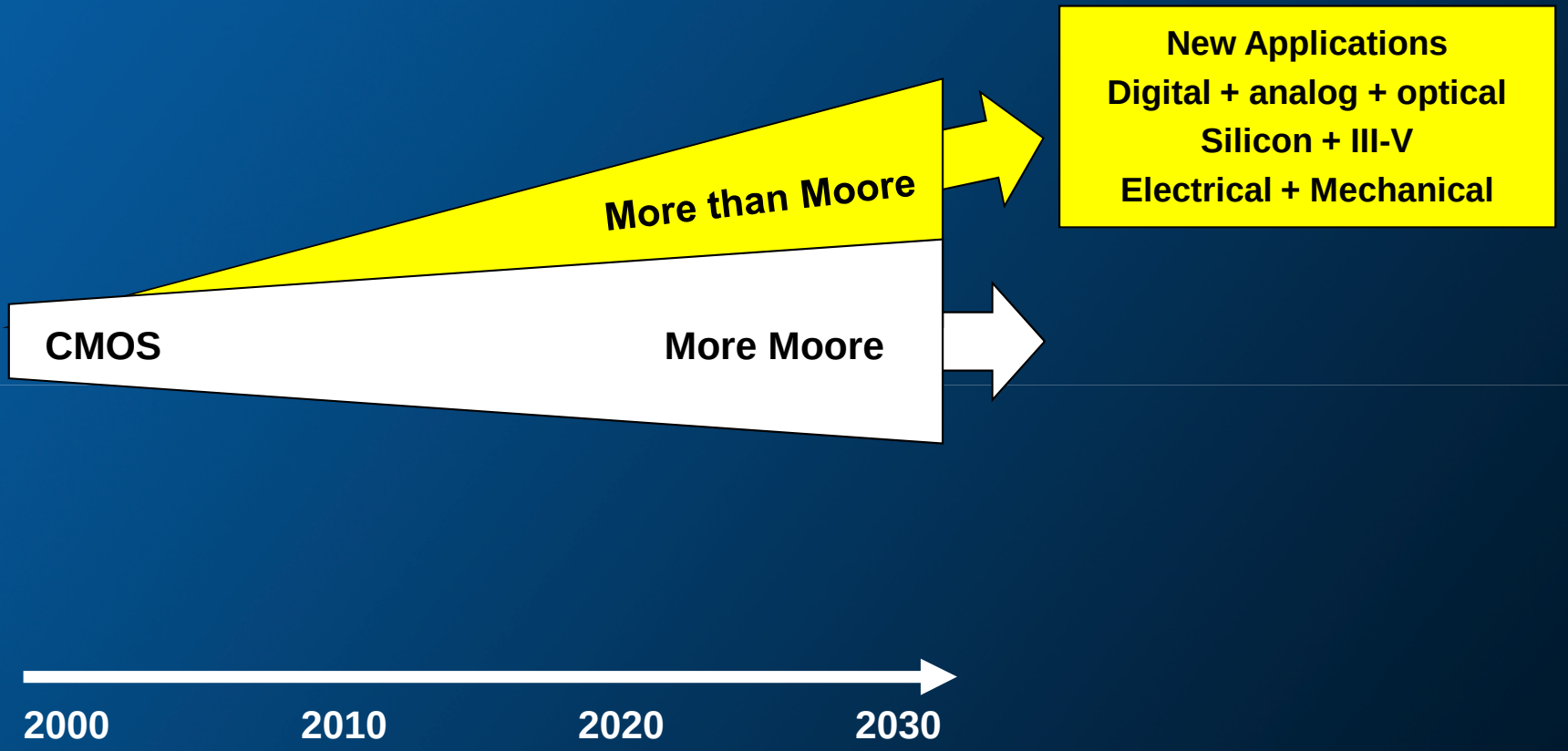
Future Technology Directions



New device technology will be needed by 2020

M. Bohr, SPIE, 2011

Future Technology Directions



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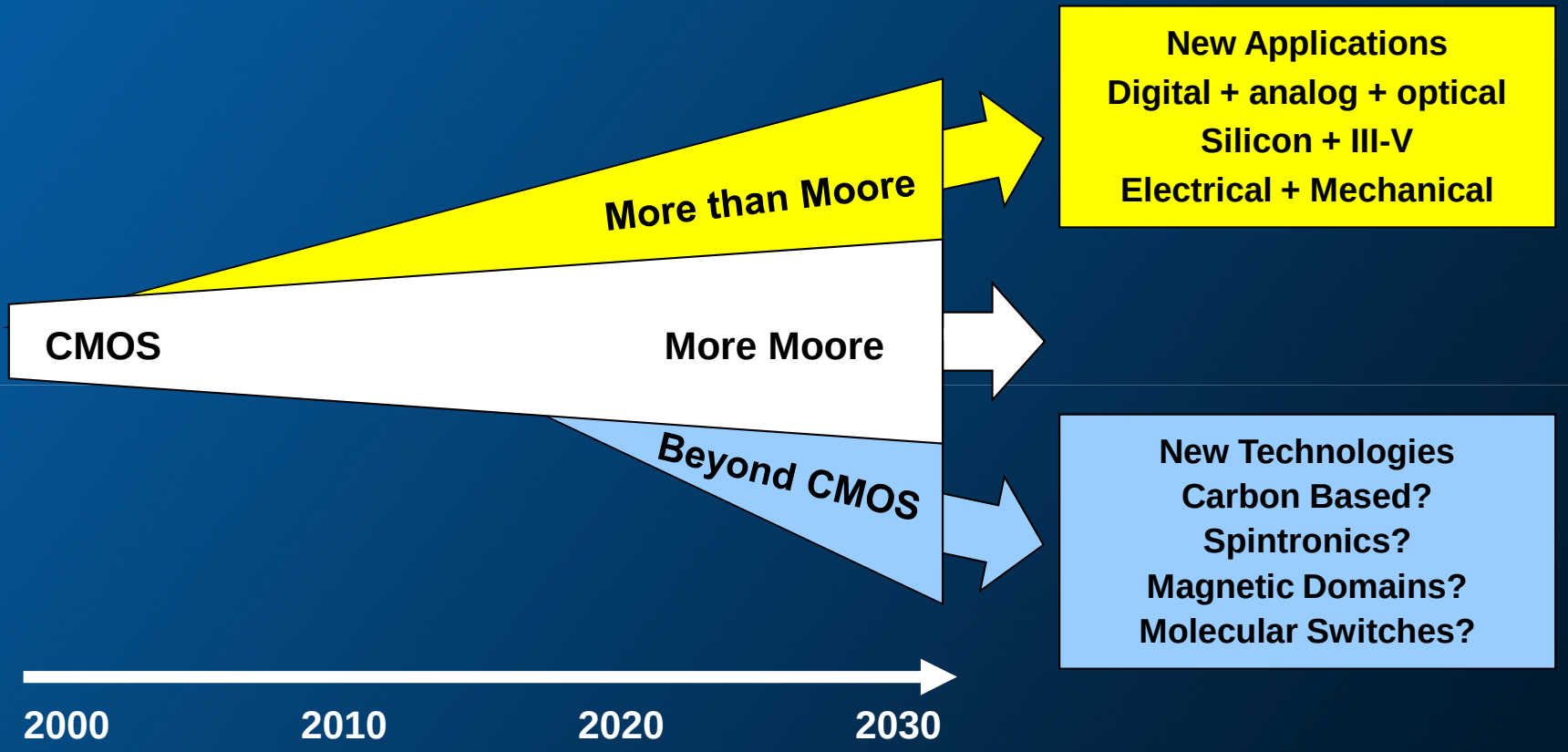
M. Bohr, SPIE, 2011

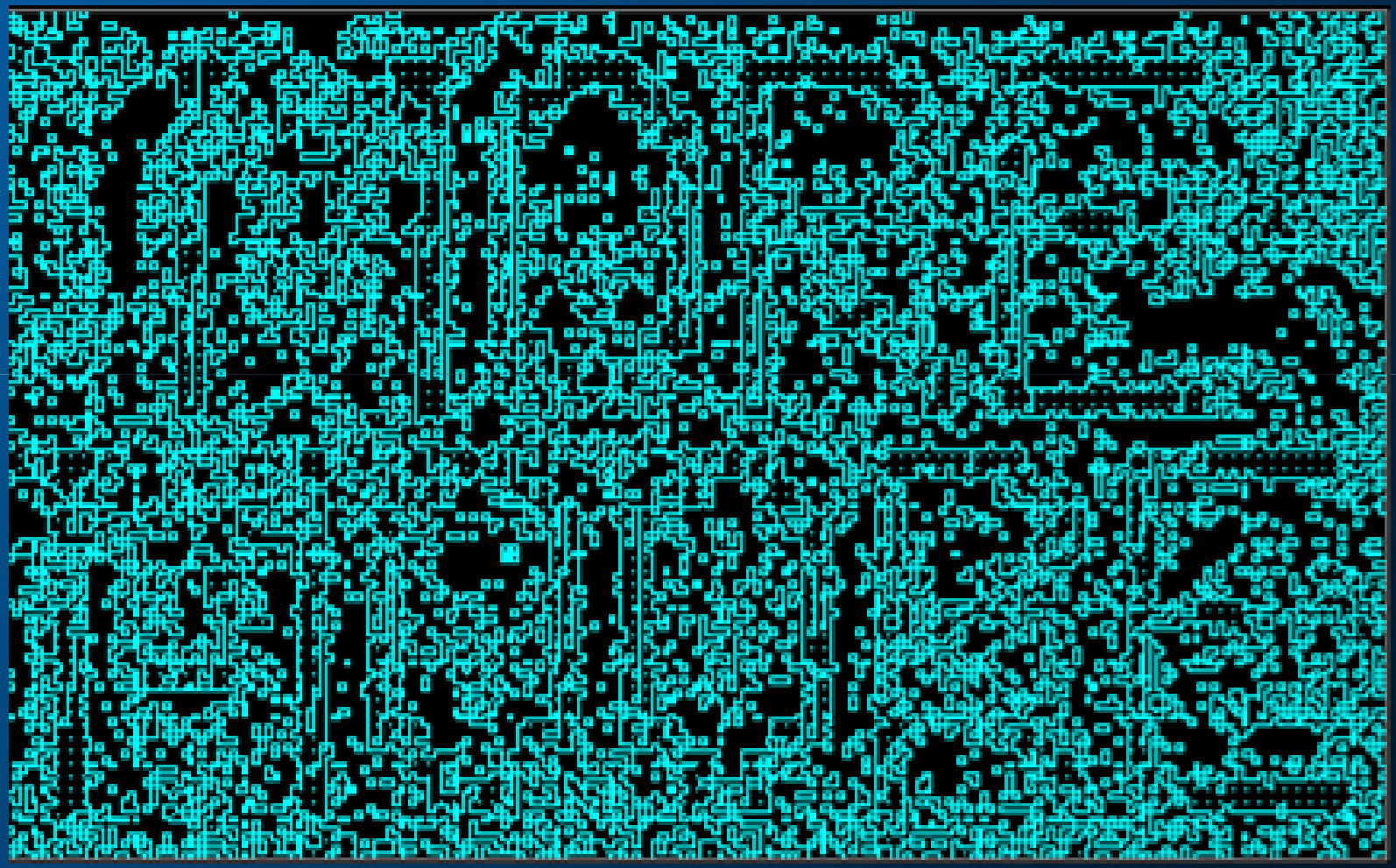
Future Technology Directions



New device technology will be needed by 2020

M. Bohr, SPIE, 2011

What will be printed?




MORE
MOORE

Conclusion

"No exponential is forever … but we can delay 'forever'."

Gordon Moore
ISSCC
2003