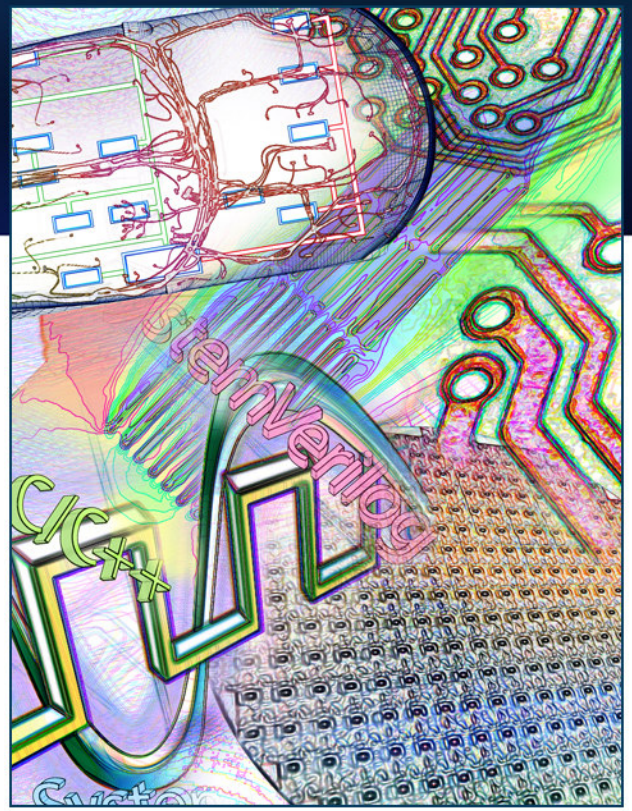
Impact of Manufacturing on Routing Methodology at 32/22 nm



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Outline

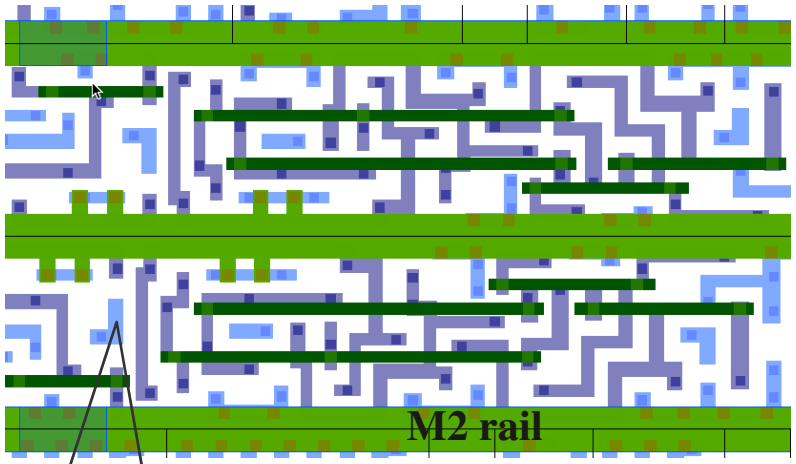
- ASIC detail router challenges at 32/22nm
  - Library density and design size
  - Complexity of DRC rules
  - DFM consideration
  - Double Pattern (DP) methodology
- Methodology Impact
  - Accuracy
  - Pre-calculation
  - Prevention

Density

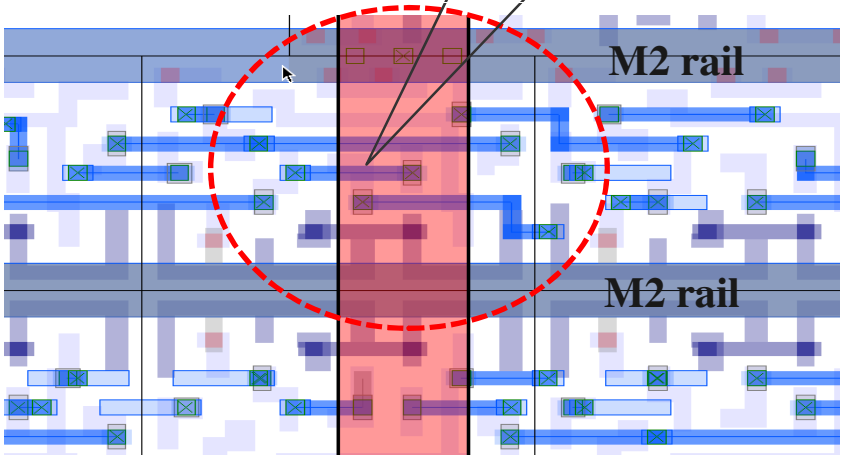
- High density libraries at 32nm
  - M2 PG rails
  - M1 M2 pins
  - Dense library cells cause routing problems
- Aggressive rules
  - Modeling vias and short connections in Global Route
- Size of designs exceeds > 10M instances
  - Geographic database
  - NlogN is not enough

Density: M2 Library

- M2 PG rails and M2 pins:
  - Reduced routing resources
  - Limits possibility for pin connection
  - M3 stripe can cause a trap

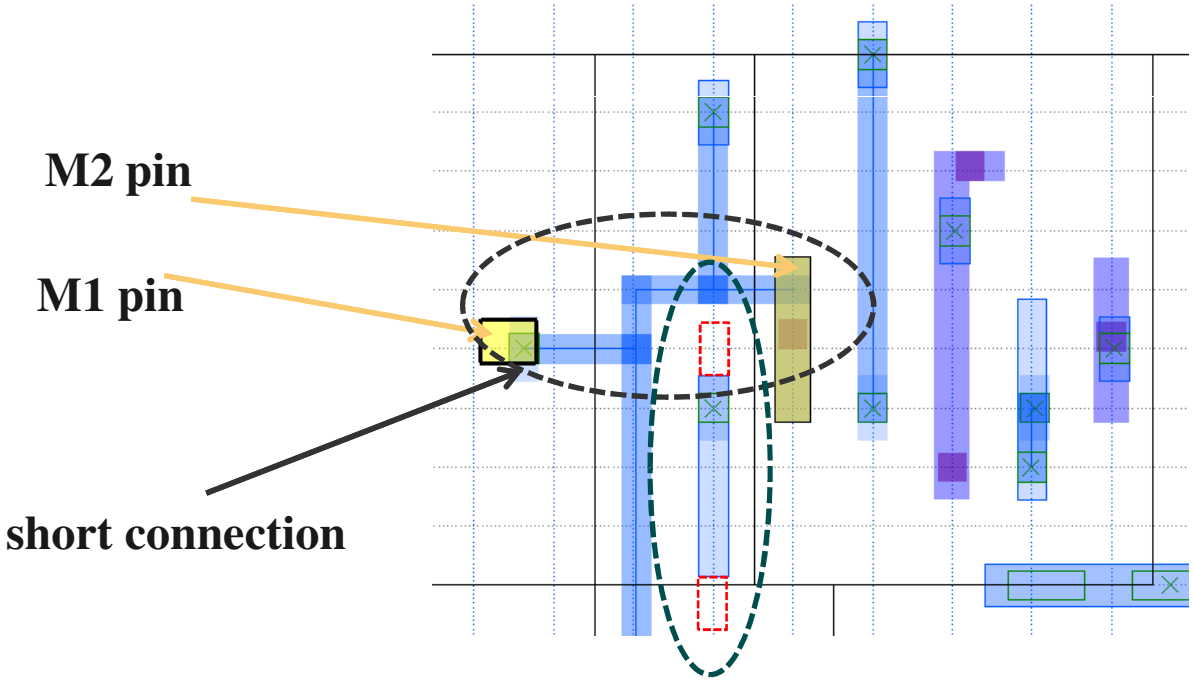


M1 pin surrounded by M1/M2 shapes



Density: Aggressive Rules

- Global router requires precise modeling
  - Via is not a point anymore
  - Need to consider min area and EOL rules
  - Small connections in gcell affects M2/M3 resources



min area via and EOL areas

Density: Size of Designs

- Design size is a challenge
  - 30M design → 1 Billion of wires and vias
  - Geographic database after 1M
- N*log(N) can be expensive for N – need n*log(n)

```
LargeData {};
vector<LargeData> data;

sort(data);
  { … swap(N1, N2); …}
```

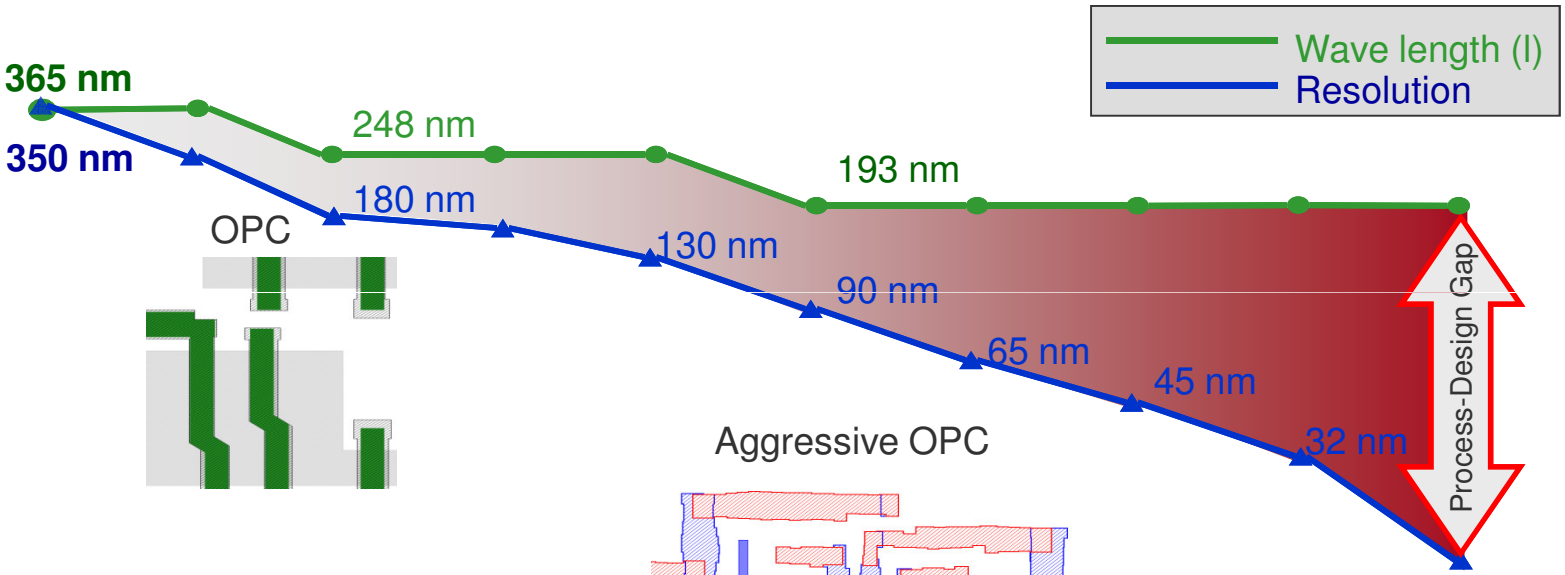
```
LargeData {};
vector<LargeData*> data;

sort(data);
  { … swap(n1*, n2*); …}
```

DRC Complexity

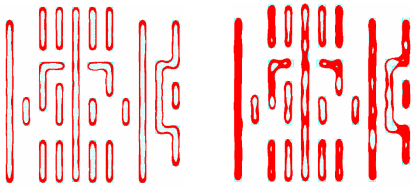
- DRC rule count
  - Increase in number of rules
  - Increase in number of ranges per rule
- Complexity
  - Actual polygon processing
  - Multiple objects result in a violation
  - Pessimistic and simple models do not work anymore
- Various approaches
  - Post processing of layout
  - Integration of DRC engine with router

DRC: Number of Rules and Complexity

- Manufacture uses 193nm light to print 32nm feature



What you see is not what you get



150nm 45nm

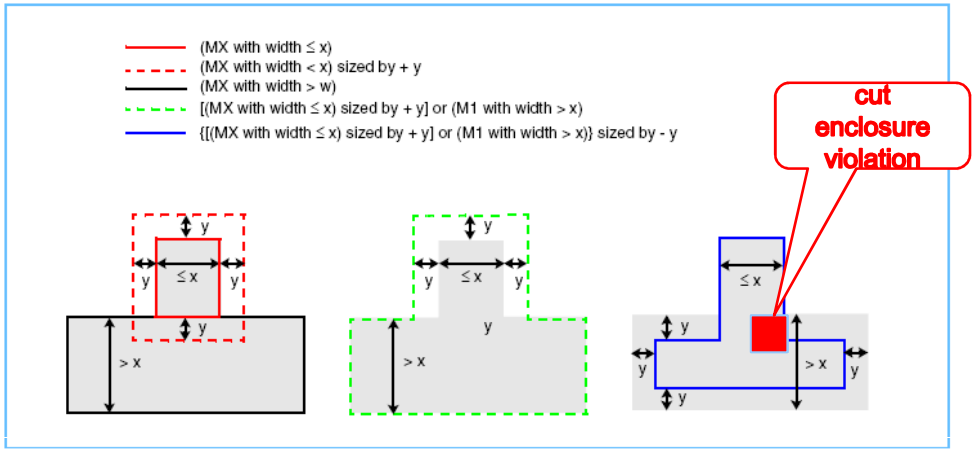
DRC: Number of Rules and Complexity

- Increase in DRC rules to address printability issues

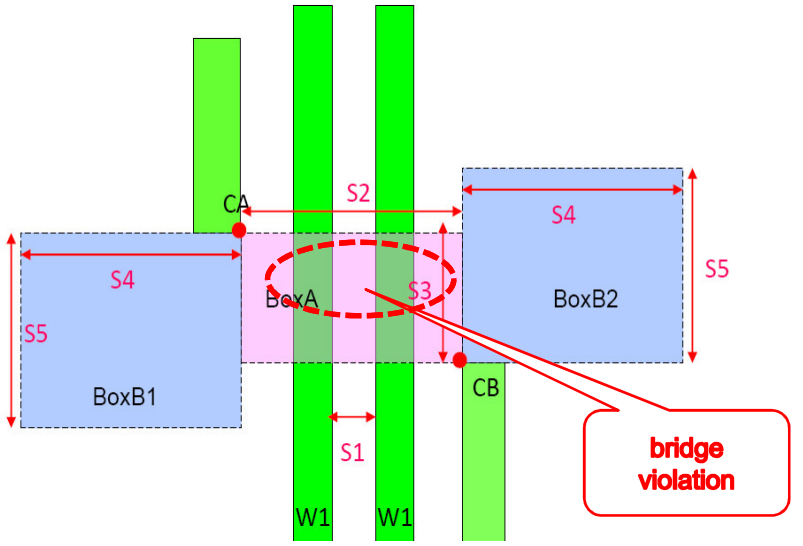
Rule	130nm	90nm	65nm	45nm	32nm	22nm
Width-based spacing	1-2	2-3	3-4	4-5	7+	7+
Min-Area	1 pitch	1.5 pitch	1.5 pitch	2 pitch	2.5 pitch	3 pitch
Min-Step (OPC)	-	1	1	2	2	3+
End-of-Line (OPC)	-	-	1	1-2	2-3	2-3
Pinch (OPC)	-	-	-	-	4	4+
Fat Jog (OPC)	-	-	-	-	5	5+
Cut Number (Via)	-	1-2	3-4	5-6	6+	6+
Bar Via spacing	-	-	-	-	Cut-to-Cut	Cut-to-Met
Direction Rules	-	-	-	-	-	Yes
Discrete width	-	-	-	-	-	Yes
Double Patterns	-	-	-	-	-	Yes

DRC: Complexity of Verification

- Complex polygon operations
  - build polygon for shape
  - perform 5 reshape operations
  - check via enclosure vs. resulted blue contour

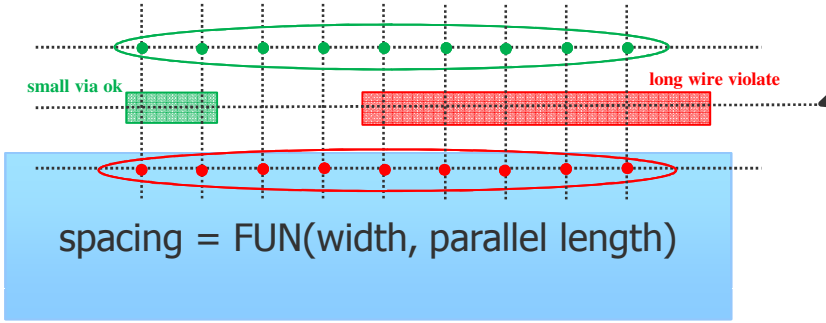


- Multiple objects in a violation
  - two wires (green) with W1 and S1 between two other wire corners (CA CB)
  - if no any objects in BoxB1 BoxB2 then OPC will create bridge violation



DRC: Complexity for Router

- Complex shape-dependent rules is a challenge

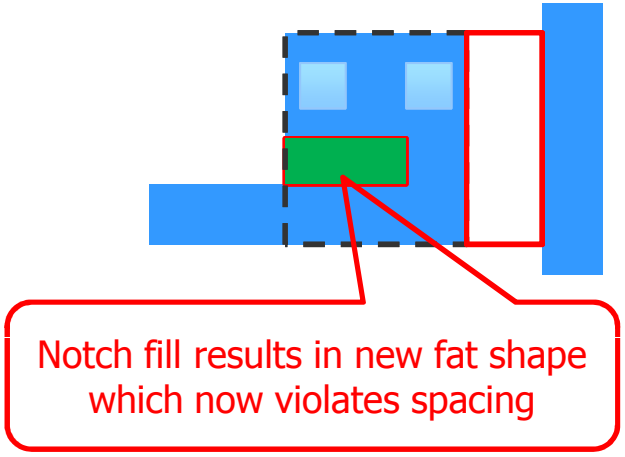


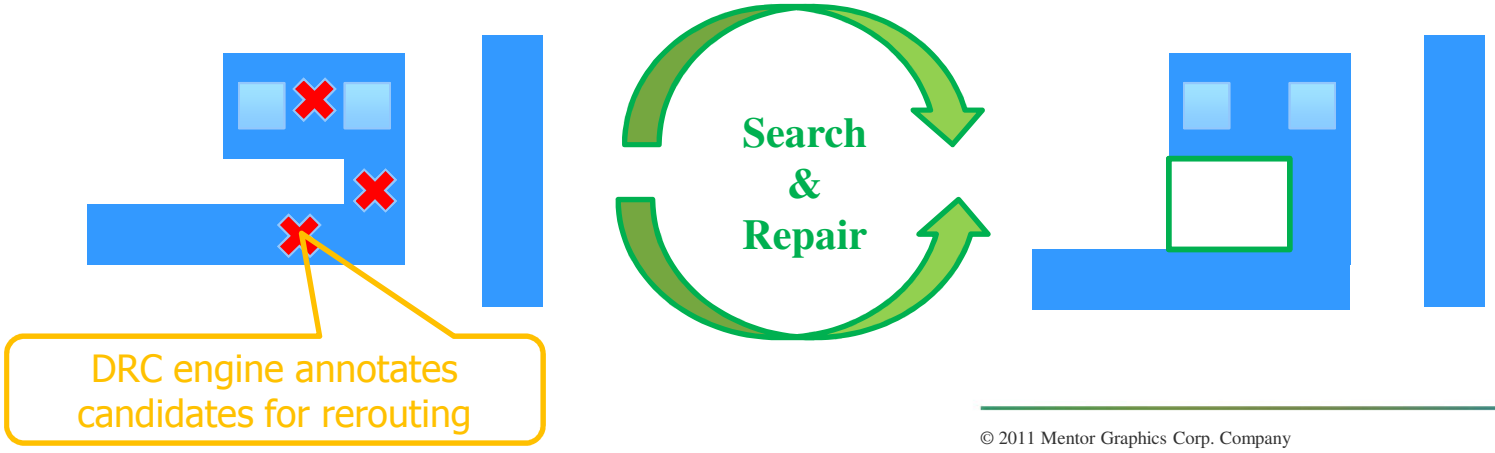
How to consider the track?
pessimistic – loose via
optimistic – bad long wire

- "Shadowing" grid points do not work
  - There are many "gray" areas around shapes where router should be accurate
  - Router should understand length dependent rules
  - Router should dynamically change solution from "history"

DRC: Complexity for Router

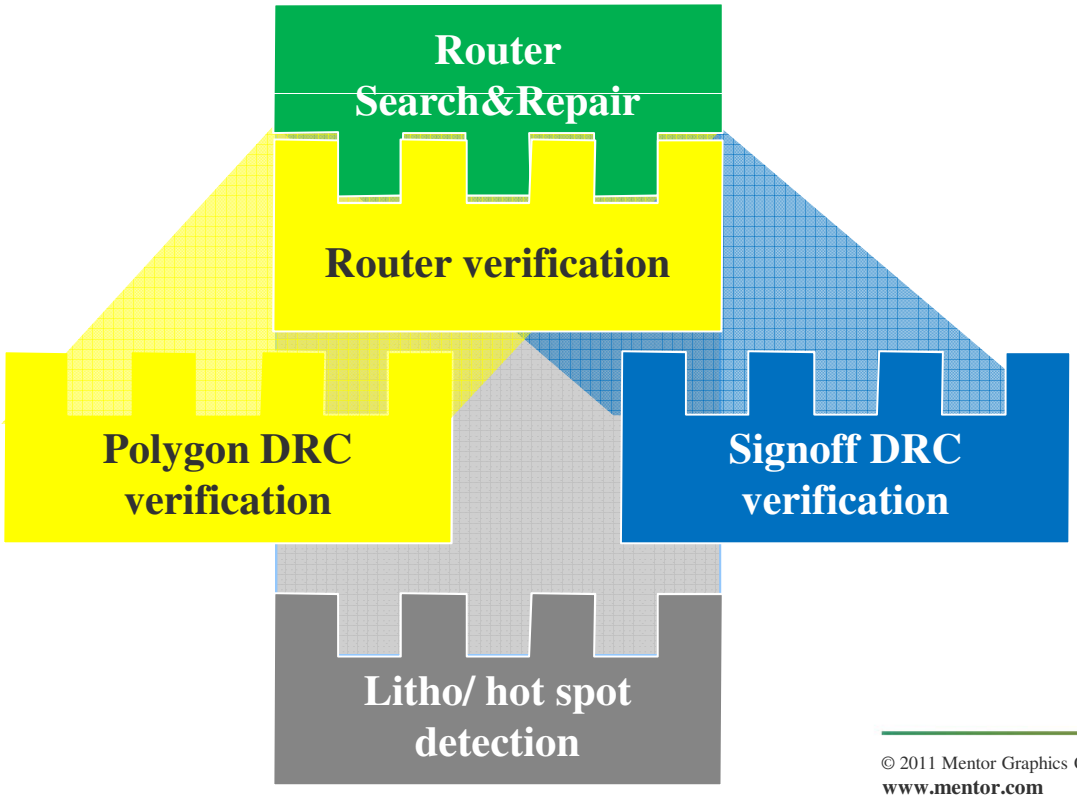
- Addressing complex violations
- Post processing fixing
  - Easy to implement
  - Not guaranteed
- Integration with DRC engine
  - Difficult to implement
  - Best approach





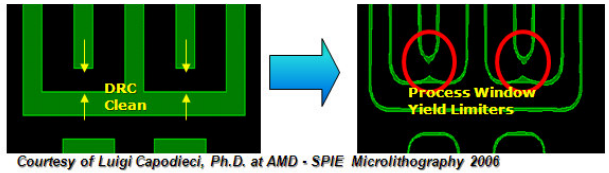
DRC: Router Integration

- Requirement for DRC/DFM closure at 32m/22nm
  - — Decouple verification from core router
  - — Use polygon based DRC engine
  - — Integrate core router with various signoff tools

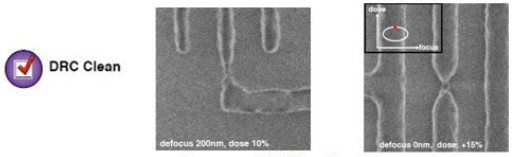


DFM Requirements

- DRC clean does not mean good yield
  - Any angle is the problem for manufacturing
  - Any via is object for failure
- Preferred routing style
  - Enclose via in pin – library pre-calculation
  - Minimize fat shapes – wire/via relations
  - Minimize non-preferred direction
- Various DFM approaches
  - Post processing
  - Concurrent routing with reservation of room
  - Pins pre-calculation for DFM vias



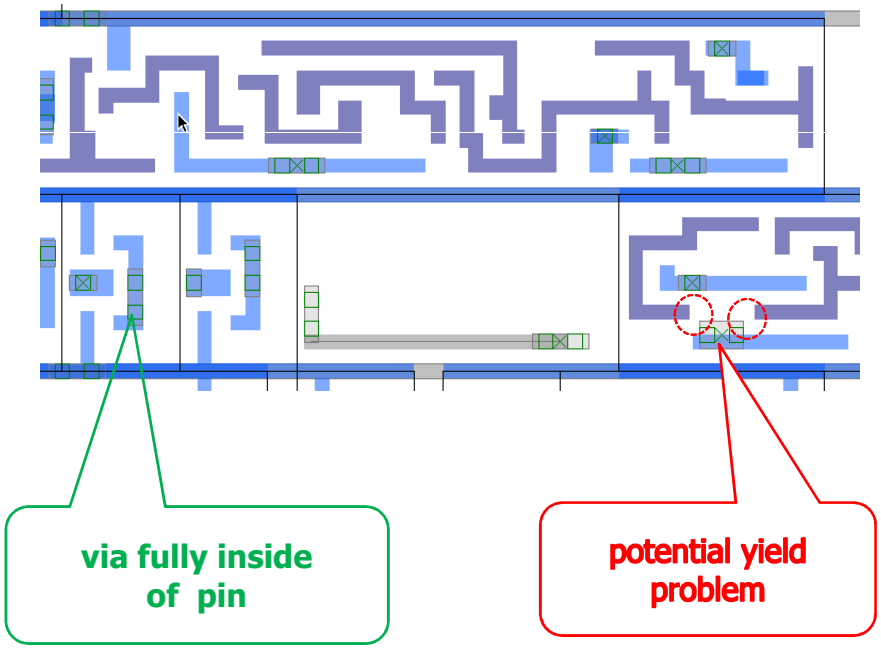
Courtesy of Luigi Capodieci, Ph.D. at AMD - SPIE Microlithography 2006

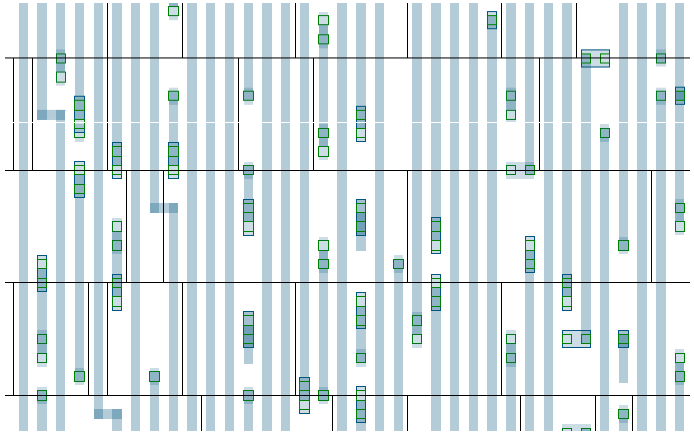


Courtesy of ST Microelectronics

DFM: Preferred Routing Style

- Via inside of pin, short M1 connections
- Minimize fat shapes and jogs on top layers

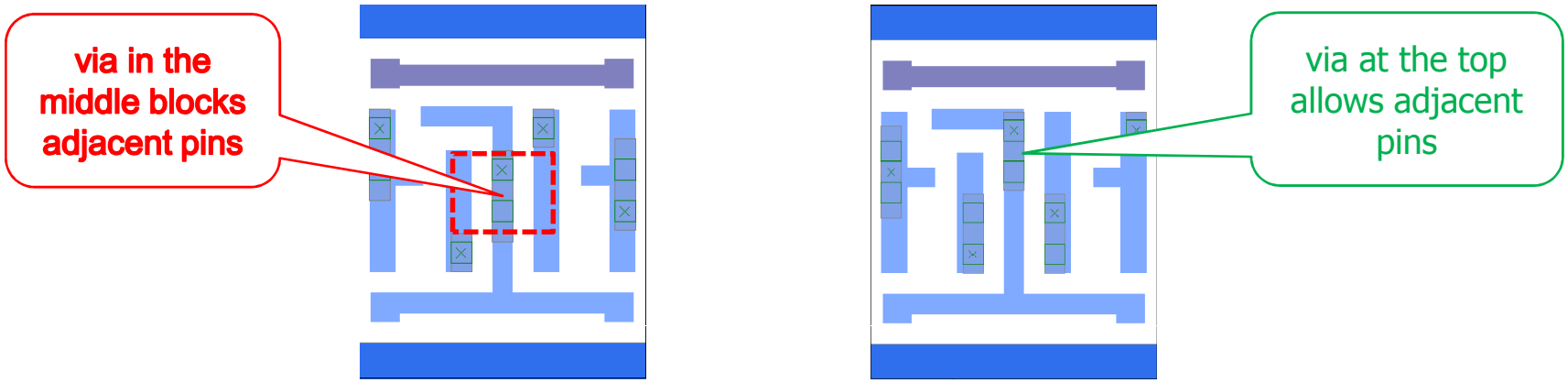




ideal routing picture

DFM: DFM Via Approaches

- Pre-calculate library for DFM



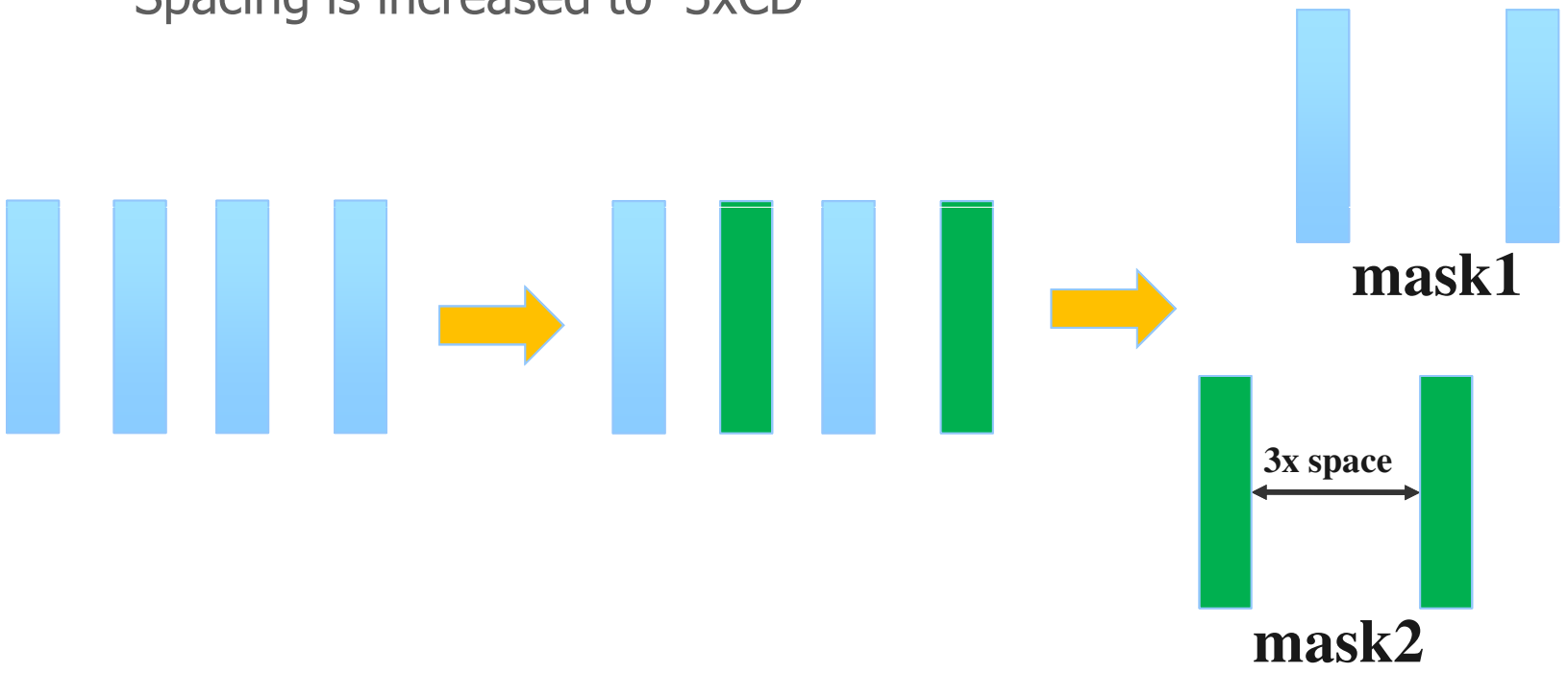
- Concurrent DFM via usage in routing
  - Many vias leads to excessive runtime
  - Aggressive via insertion leads to unrecoverable violations
  - Space reservation

Double Patterning at 20nm – Another Magnitude Increase in Complexity

- New dimension for routing tasks
  - Multiple schemes of DP
  - Non-formalized rules because DP is a synthesis process
  - Coloring is the core for DP process
  - Global conflict vs. local marker
- Various manufacturing solutions
  - Conservative to flexible
- Routing solutions
  - DRC prevention rules
  - Integration with signoff tools
  - Own coloring algorithm

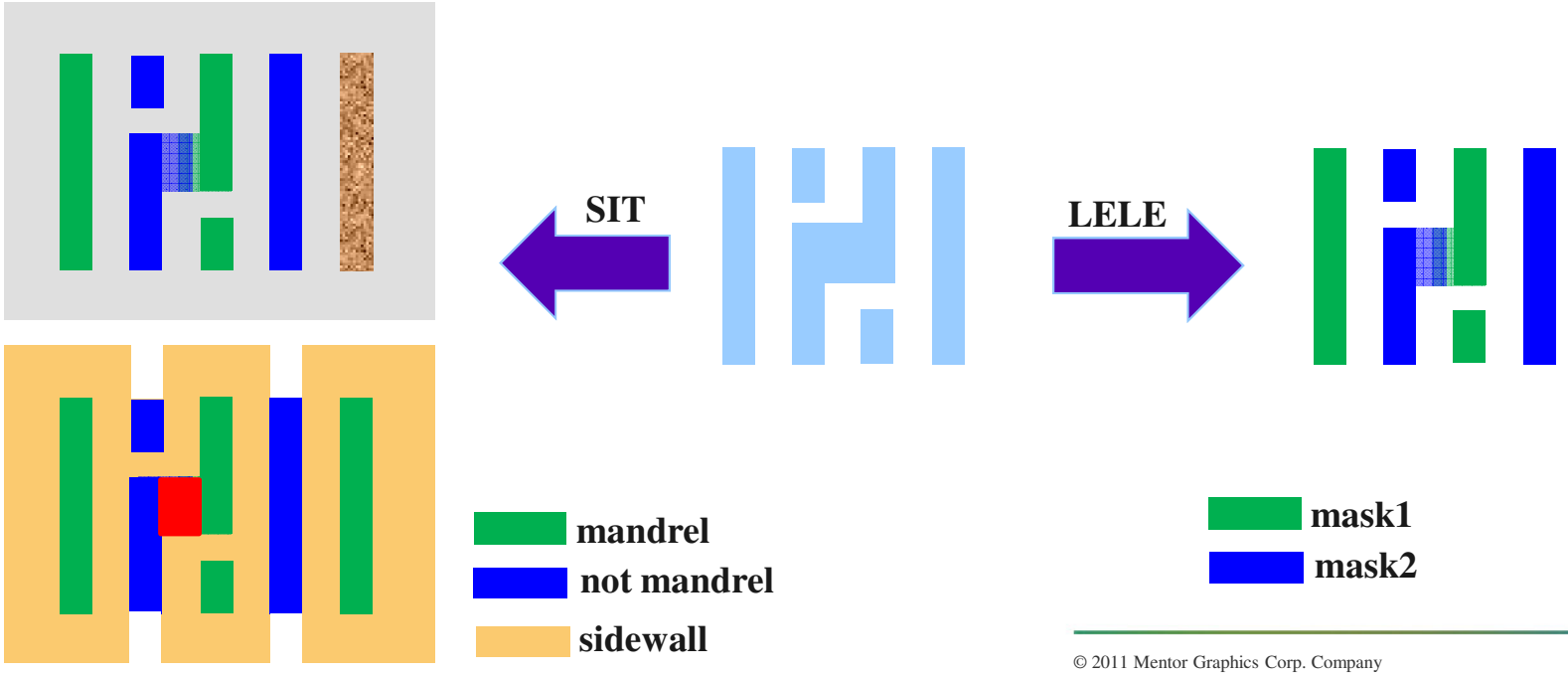
DP: Problem Statement

- Create two or more masks
  - Metal line stays as CD
  - Spacing is increased to 3xCD



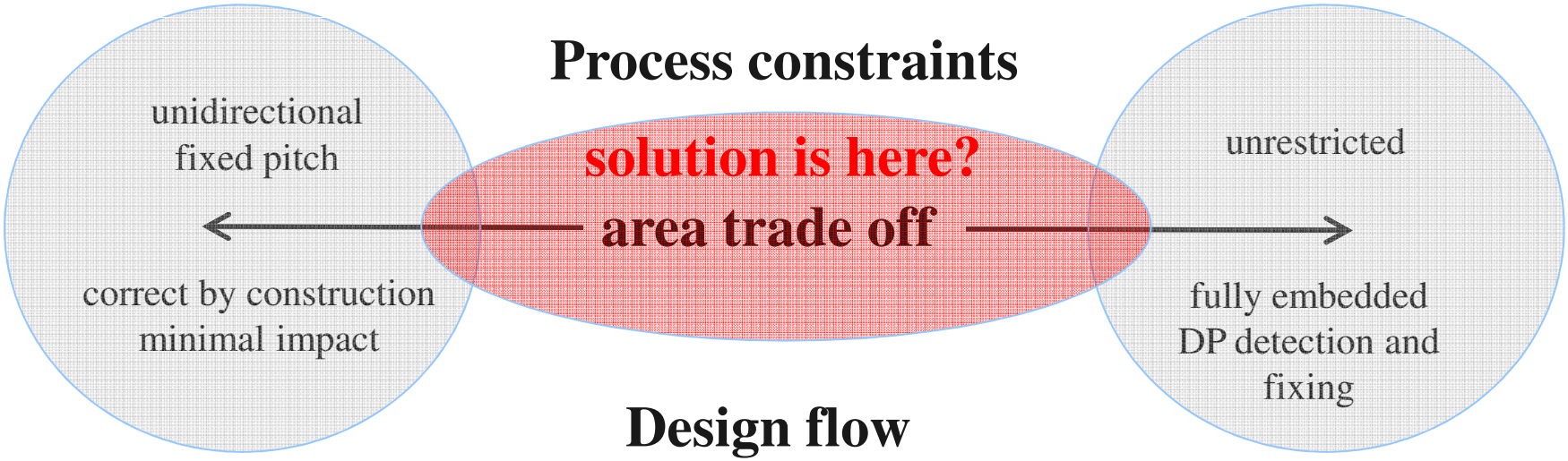
DP: Problem Statement

- Different DP Methodologies
  - SIT (SADP): Sidewall Image Transfer (Self Align DP)
  - LELE: litho-etch, litho-etch
  - Can be mixed in the process
  - Every Fab have their own methodology



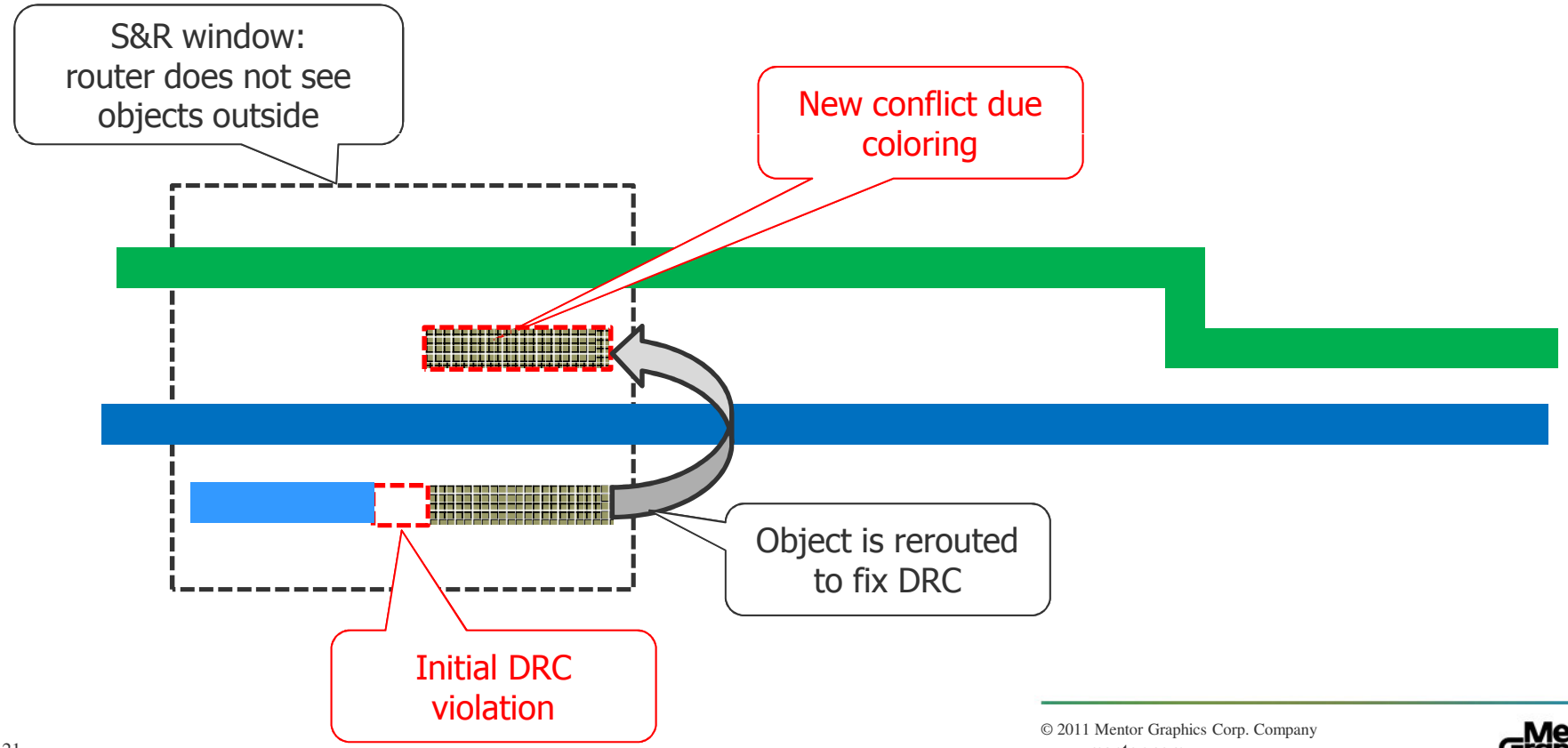
DP: Manufacturing Dilemma

- DP methodology is still evolving
  - No experience on design side for DP conflict resolution
  - Unknown manufacturing cost and design impact
  - No agreement on the best approach



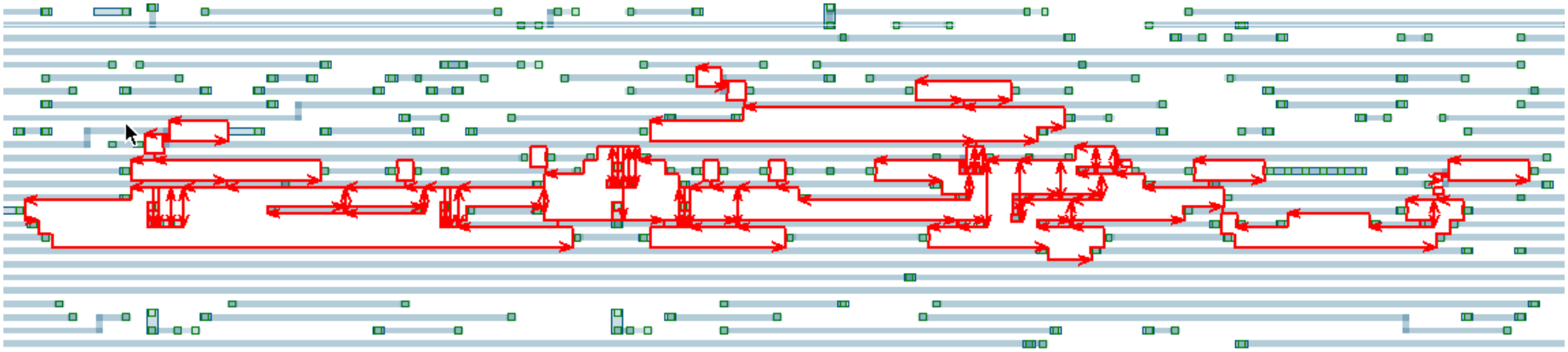
DP: Global Conflict in Routing

- DP problem is not localized as regular DRCs
  - Reroute can result in violation on another portion of the chip
  - Incremental approach is broken



DP: Global Conflict in Routing

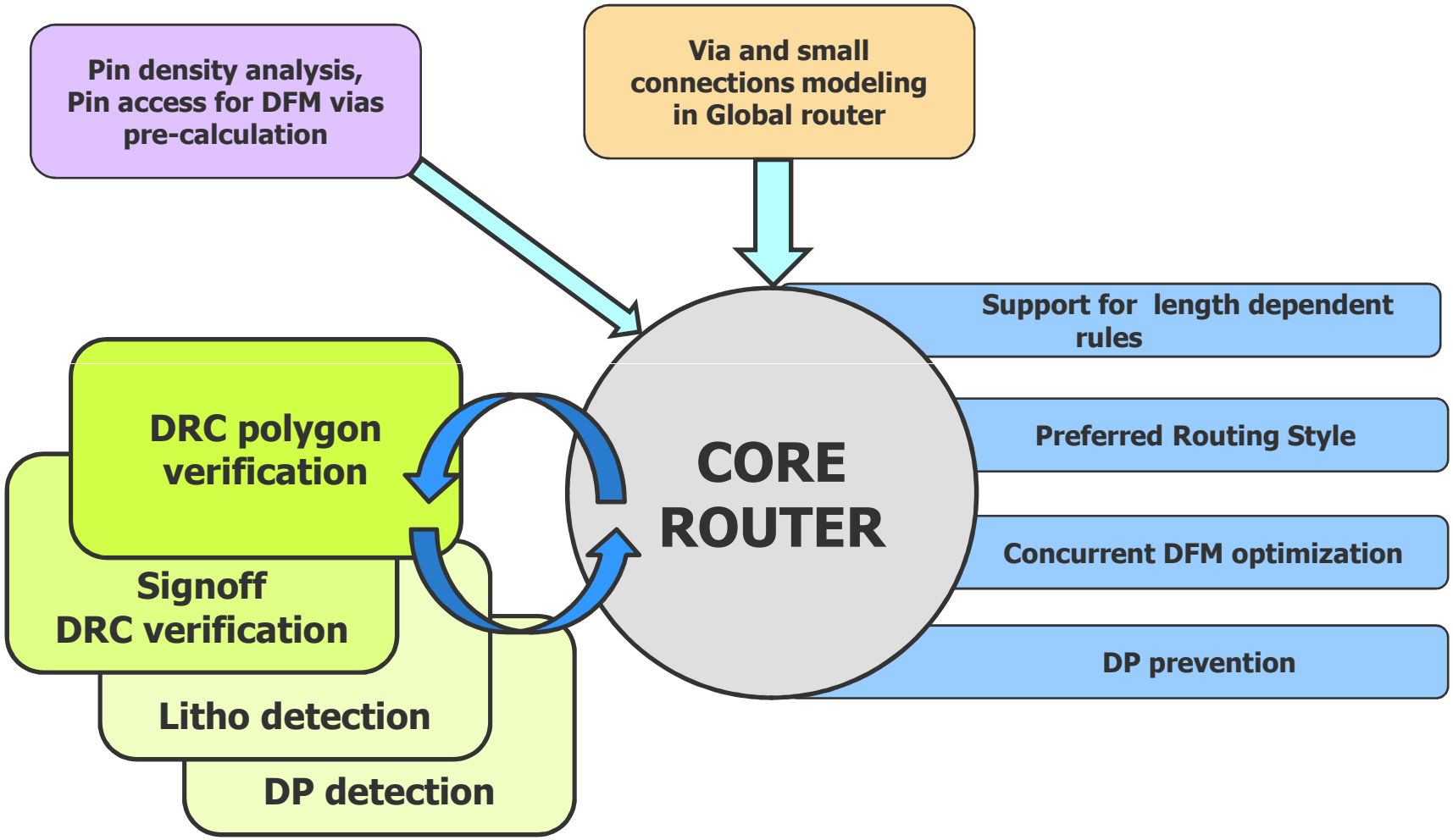
- Conflict contour can include too many objects
  - DP detection does not tell who is the reason of violation
  - Several objects can be the reason in a big countour



DP: Routing Approach

- Prevention by DRC rules
  - Restrictions for non-preferred direction
  - Spacing depending on direction
  - Track routing only
- DP verification
  - Own coloring engine
  - Integration with signoff
- Repair of DP conflicts is still an open question

Modern Detail Router architecture



Summary

- 32/22nm technology complexity stressing traditional models, methodologies and algorithms
  - Advanced DRC
  - DFM
  - DP
- A new routing architecture is needed for predictable and efficient manufacturing closure
  - Adaptable to evolving methodologies vis-à-vis cost vs. benefit
  - Concurrent verification and design
  - Signoff driven prevention and repair

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