Obstacle-aware Clock-tree Shaping during Placement

Dong-Jin Lee and Igor L. Markov

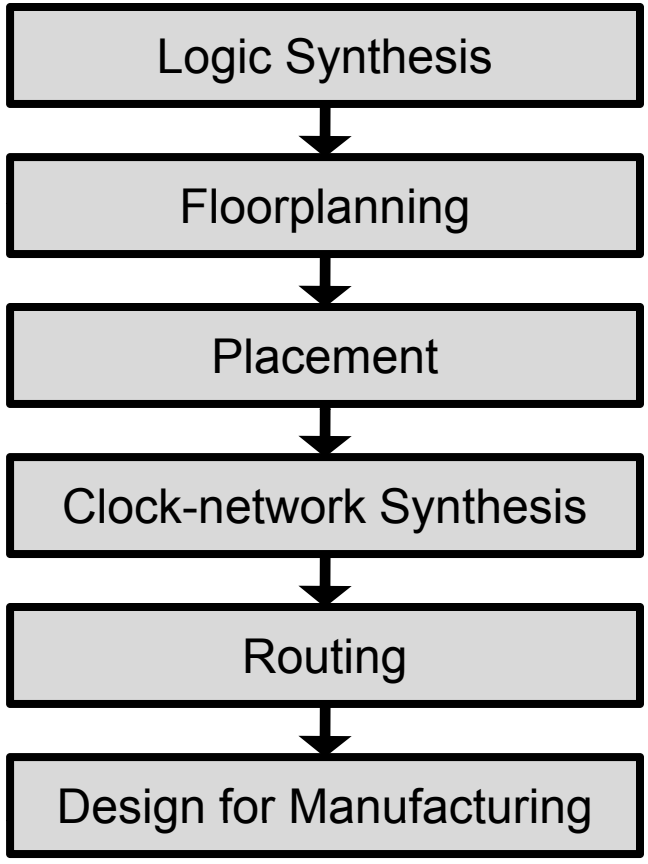
Dept. of EECS, University of Michigan

Outline

- **Motivation and challenges**
- **Limitations of existing techniques**
- **Optimization objective**
- **Proposed techniques and methodology**
  - Obstacle-aware virtual clock trees
  - Arboreal clock-net contraction force
  - Obstacle-avoidance force
  - The Lopper flow
- **Empirical validation**
- **Conclusion**

Physical Design Flow

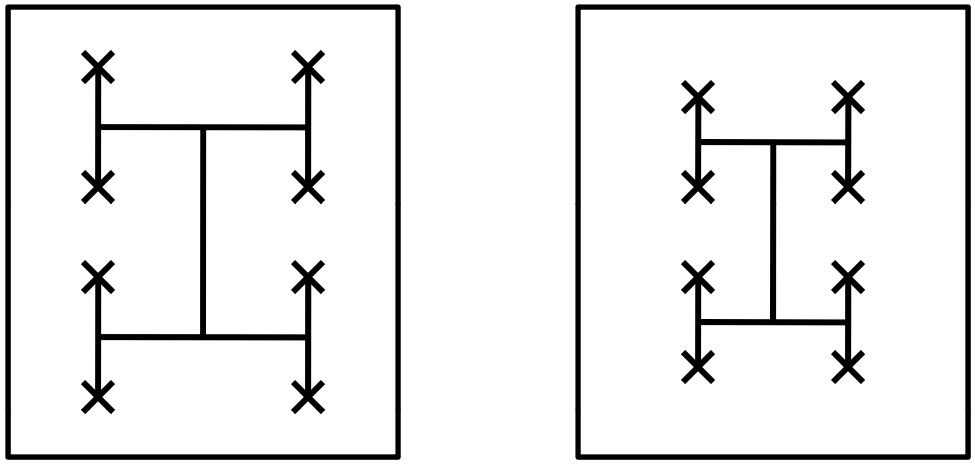
- **Synchronous systems** consist of sequential registers (latches, flip-flops) and combinational logic



- Physical locations of **registers** are determined during **placement**
- **Clock networks** are built based on the physical locations of registers during **Clock-network synthesis**
- **Placement-level optimization techniques for high-quality clock networks**

Register Placement

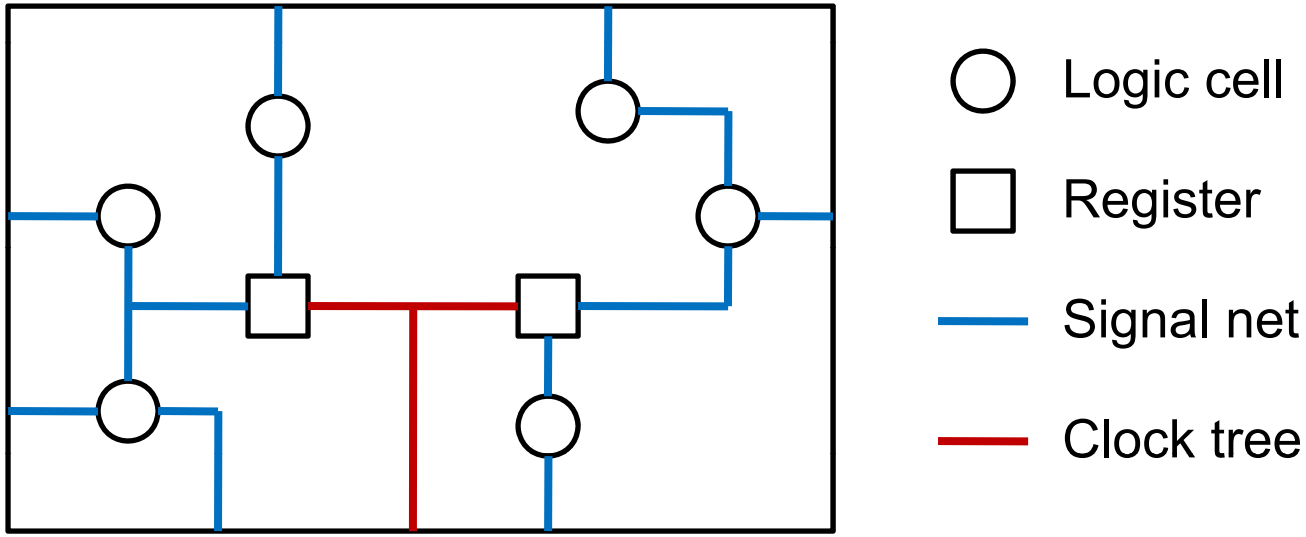
- **Quality of clock networks is greatly affected by register placement**



- **High-quality register placement cannot be achieved by easy pre- or post-processing**
- **Mainstream literature on placement focuses on wirelength of only signal nets**

Challenges

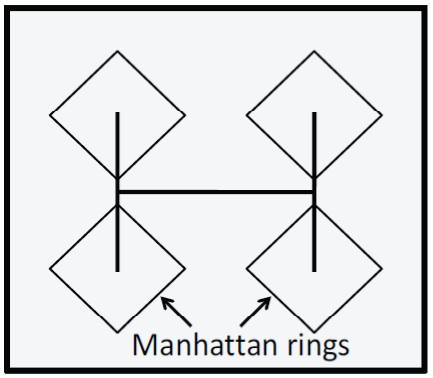
- **Trade-off between clock network minimization and total signal-net wirelength**

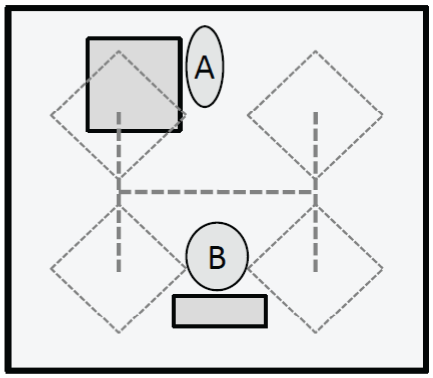


- **Both signal-net and clock-tree wirelength must be considered in primary placement objective**
- **Difficult to estimate the topology of the final clock tree during placement**

Limitations of Existing Techniques

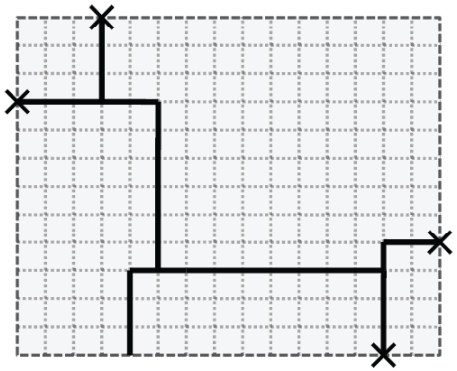
- **Manhattan-ring guidance method***

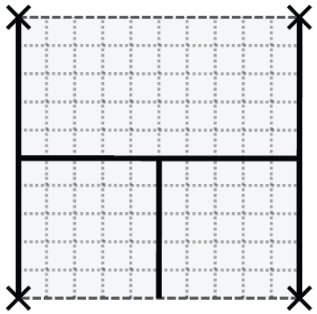




  - Inaccurate
  - Poor in the presence of obstacles (macro blocks)

- **Intermediate simple clock-network estimates****, *****





  - Unrealistically simplified clock networks
  - Bounding box based representation (HPWL)

** : Y. Lu et al, "Navigating Registers in Placement for Clock Network Minimization," DAC`05*

*** : Y. Cheon et al, "Power-Aware Placement," DAC`05*

**** : Y. Wang et al, "Clock-Tree Aware Placement Based on Dynamic Clock-Tree Building," ISCAS`07*

Our Contribution

- **Optimization objective which captures total net-switching power**
- **Obstacle-aware virtual clock trees**
- **Arboreal clock-net contraction force**
  - Switching-power minimization problem solved by wirelength-driven placer capable of net weighting
- **Obstacle-avoidance force**
- **The Lopper flow**
  - Quality control
  - Gated clocks and multiple clock domains
  - Flexible integration
- **Experimental results on practical benchmarks derived from industrial circuits**
  - 30% clock wirelength, 6.8% power reduction

Optimization Objective

- $\mathcal{N}$: Set of signal nets, $\mathcal{E}$: Set of clock-tree edges
- **Total switching power**

$$P_{sw} = P_{\mathcal{N}} + P_{\mathcal{E}}$$

- α_{n_i} , α_{e_i} : Signal-net and clock-edge activity factors
- C_n , C_e : per-unit capacitance of signal and clock wires
- **Total signal-net switching power**

$$P_{\mathcal{N}} = \sum_{n_i \in \mathcal{N}} \alpha_{n_i} HPW L_{n_i} C_n V^2 f$$

- **Total clock-net switching power**

$$P_{\mathcal{E}} = \sum_{e_i \in \mathcal{E}} \alpha_{e_i} L_{e_i} C_e V^2 f$$

L_{e_i} : Manhattan length

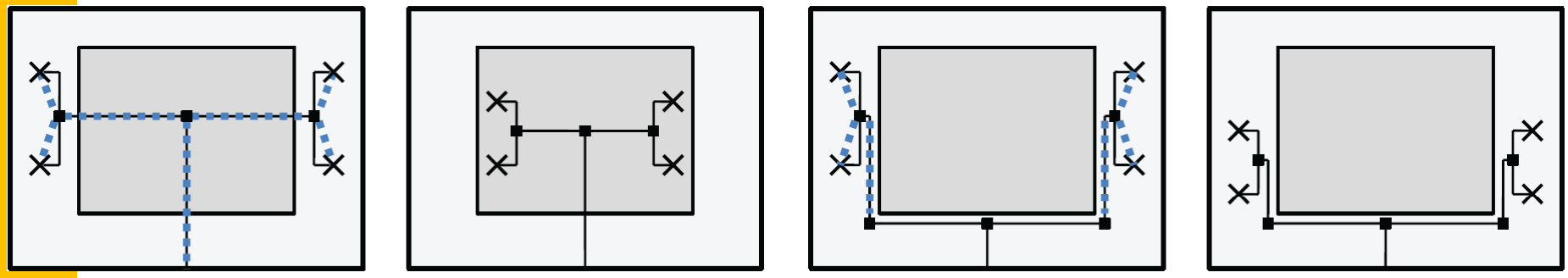
Activity Factor

- **Activity factors of signal nets are commonly not available at placement stage**
- **Clock-power ratio β**
  - Clock-net switching power divided by total switching power
  - Target design constraint or user-control variable
  - Affects how much a placer emphasizes clock-network reduction
- **Average activity factor of signal nets based on clock-power ratio β**

$$\alpha_{avg} = \frac{(1-\beta)\sum_{e_i \in \mathcal{E}} L_{e_i} C_e}{\beta \sum_{n_i \in \mathcal{N}} HPWL_{n_i} C_n}$$

Obstacle-aware Virtual Clock Trees

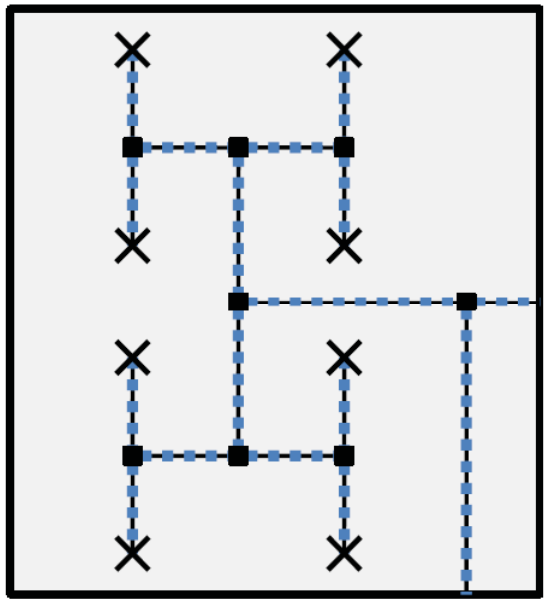
- **Challenges in clock-net optimization without obstacle handling**



- **Obstacle-aware virtual clock-tree**
  - Traditional DME-based zero-skew clock-tree synthesis with Elmore delay model
  - Incrementally repair the clock tree to avoid obstacles
  - Represents realistic modern clock networks (Avg. 2.2% differences in capacitance on the ISPD`10 CNS benchmarks)

Arboreal Clock-net Contraction Force

- **Structurally-defined forces**
  - To reduce individual edges of the virtual clock tree
  - Virtual nodes represent branching nodes and split the clock tree into individual edges
  - Create forces between clock-tree nodes and structurally transfer the forces down to registers



Arboreal Clock-net Contraction Force

- **Two-pin net representing clock-net contraction force**

$$w_{e_i} = \frac{C_e \alpha_{e_i}}{C_n \alpha_{avg}}$$

- **Total switching power ($L_{e_i} = HPWL_{e_i}$)**

$$\Big(\sum_{n_i \in \mathcal{N}} \alpha_{avg} HPWL_{n_i} C_n + \sum_{e_i \in \mathcal{E}} \alpha_{e_i} HPWL_{e_i} C_e \Big) V^2 f$$

- **By substituting α_{e_i} in terms of w_{e_i}**

$$\Big(\sum_{n_i \in \mathcal{N}} \alpha_{avg} HPWL_{n_i} C_n + \sum_{e_i \in \mathcal{E}} \alpha_{avg} w_{e_i} HPWL_{e_i} C_n \Big) V^2 f$$

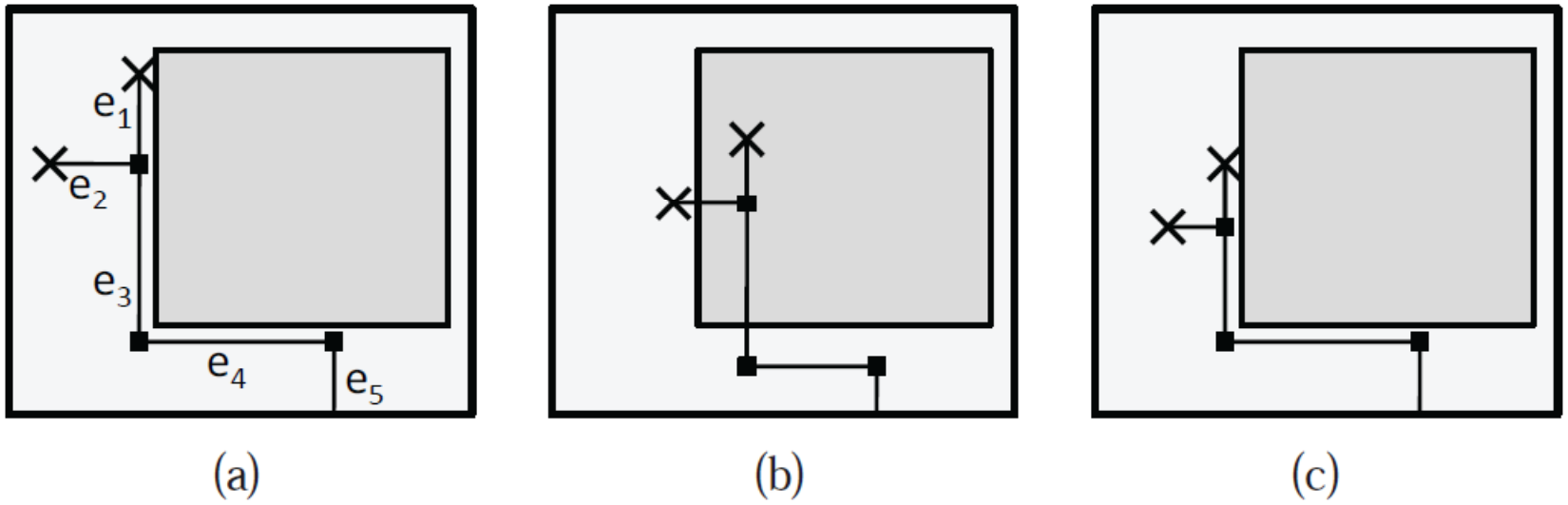
- **From switching power minimization problem to weighted HPWL minimization problem**

$$P_{sw} = P_{\mathcal{N}} + P_{\mathcal{E}} = K \sum_{m_i \in \mathcal{M}} w_{m_i} HPWL_{m_i}$$

$$K = \alpha_{avg} C_n V^2 f$$
$$w_{n_i} = 1$$
$$\mathcal{M} = \mathcal{N} \cup \mathcal{E}$$

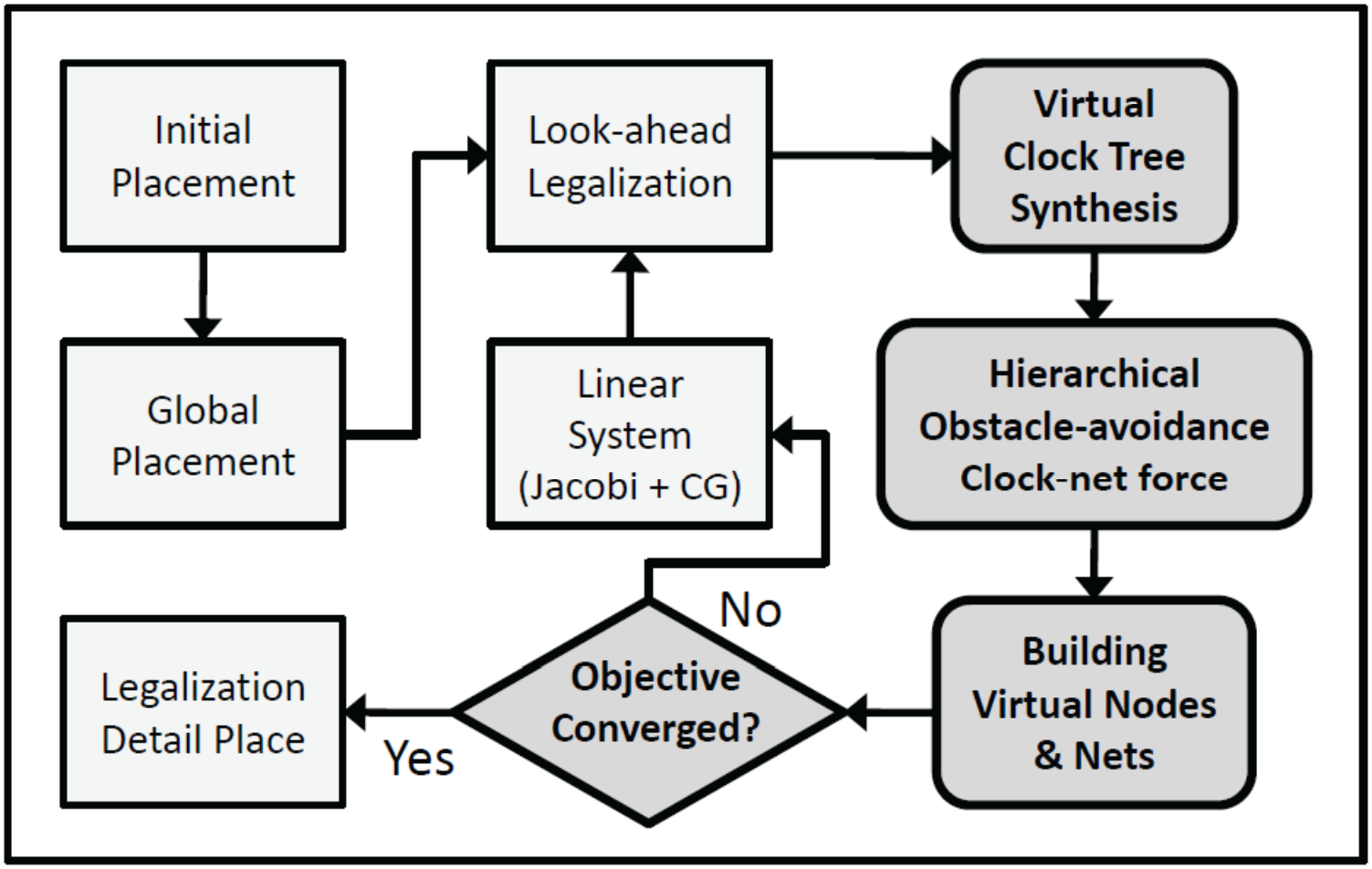
Obstacle-avoidance Force

- **Force-modification for obstacle avoidance**
  - Modify clock-net contraction forces around obstacles
  - Eliminate the contraction forces of obstacle-detouring edges (e_4, e_5)



The Lopper Flow

- **Our techniques are integrated into SimPL***



* : M.-C. Kim et al, "SimPL: An Effective Placement Algorithm," ICCAD`10, pp.649-656

Trade-offs and Additional Features

- **Quality control**
  - Trade-off between clock-net and signal-net switching power can be easily controlled with β
  - Achieve intended design target without changing the algorithms or internal parameters
- **Gated clocks and multiple clock domains**
  - Activity factors of registers are propagated to clock edges and used for clock-net contraction forces
- **Flexible integration**
  - Clock-net contraction forces are represented in placement instances by virtual nodes and nets
  - Lopper can integrate any obstacle-aware clock-tree synthesis technique into any iterative wirelength-driven placer capable of net weighting

Empirical Validation

- **Problems of the benchmarks used in prior work**
  - Inaccessible
  - Unrealistically small placement instances
  - No macro blocks
  - Reference placement tools are outdated or self-implemented
- **New benchmark set (CLKISPD05)**
  - ISPD 2005 Placement Benchmark
  - Directly derived from industrial ASIC designs (IBM)
  - Used extensively in placement research
  - 15% of cells are selected to be registers
  - Largest benchmark : 2.1M cells, 327K registers
  - http://vlsicad.eecs.umich.edu/BK/CLKISPD05bench

Experimental Setup

- Benchmarks are mapped to Nangate 45nm open library*
- Clock-power ratio β is set to 0.3 in the experiments based on clock power ratio of industrial circuits
- Wire specifications are derived from ISPD`10 contest** and Nangate 45nm library
- Supply voltage : 1.0V
- Clock frequency : 2GHz
- Clock source : bottom left corner of core area
- Quality of clock networks is evaluated by Contango 2.0***

** : Nangate Inc. Open Cell Library v2009 07, http://www.nangate.com/openlibrary*

*** : C. N. Sze, "ISPD 2010 High-Performance Clock Network Synthesis Contest: Benchmark Suite and Results," ISPD`10, pp. 143.*

**** : D.-J. Lee et al, "Low-Power Clock Trees for CPUs," ICCAD`10, pp.444-451.*

Empirical Results

	SimPL 101			SimPL+Lopper			
Bench	ClkWL (mm)	HPWL (m)	Pwr (mW)	ClkWL (mm)	HPWL (m)	Pwr (mW)	⏲ (min)
clkad1	209.1	8.968	279.9	**152.3**	9.233	**263.0**	4.30
clkad2	223.1	10.54	297.6	**161.0**	10.83	**278.4**	7.11
clkad3	468.5	24.08	624.7	**326.9**	24.90	**583.0**	13.4
clkad4	519.4	21.70	692.6	**354.4**	22.32	**640.4**	14.1
clkbb1	238.2	11.18	317.6	**166.3**	11.53	**295.7**	6.32
clkbb2	533.2	16.75	710.9	**371.2**	17.26	**661.4**	31.9
clkbb3	866.3	39.22	1155	**602.2**	40.97	**1085**	35.3
clkbb4	1855	92.96	2473	**1266**	95.21	**2279**	110
Avg	1.00×	1.00×	1.00×	**0.70×**	1.03×	**0.93×**	

- **30% clock-tree wirelength reduction**
- **3.1% signal-net wirelength increase**
- **6.8% total wire-switching power reduction**
- **2.5X slower than SimPL**

Empirical Results

- **Compared to mPL6***

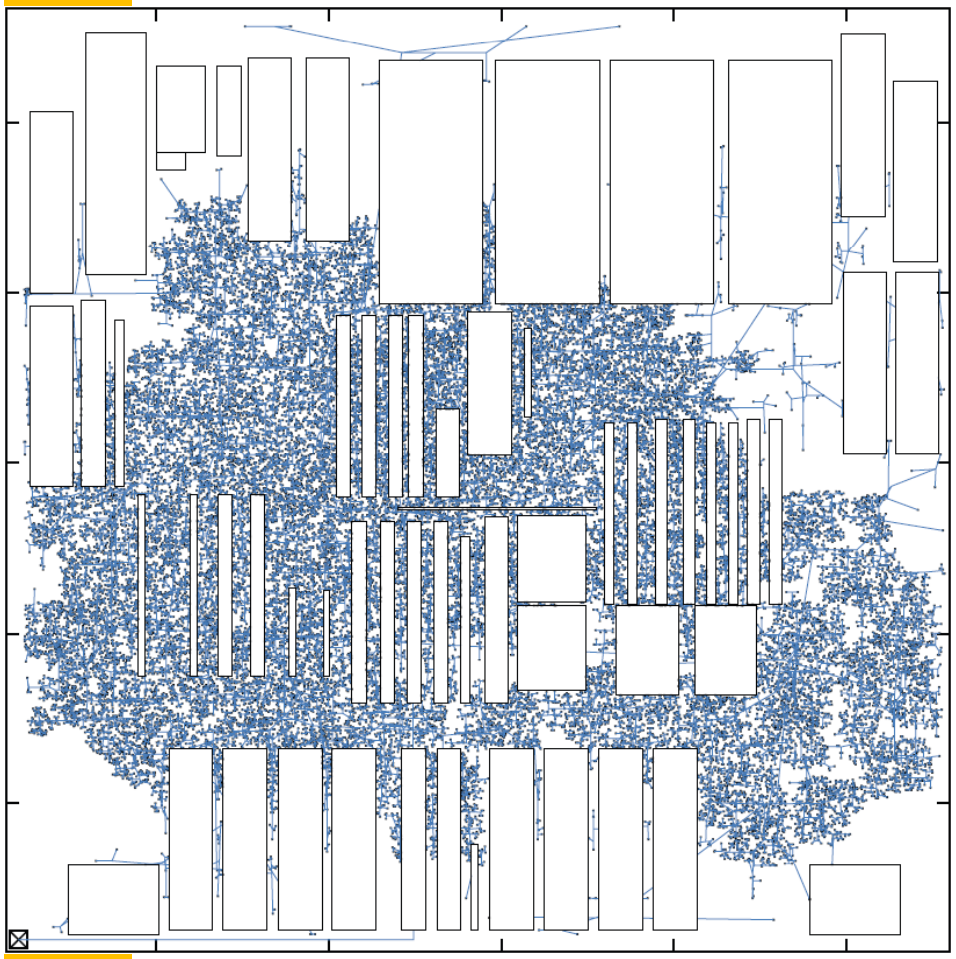
	mPL6			SimPL+Lopper			
Bench	ClkWL (mm)	HPWL (m)	Pwr (mW)	ClkWL (mm)	HPWL (m)	Pwr (mW)	⏲ (min)
clkad1	248.2	9.092	298.3	**152.3**	9.233	**263.0**	4.30
clkad2	267.0	10.74	318.9	**161.0**	10.83	**278.4**	7.11
clkad3	467.6	24.99	640.8	**326.9**	24.90	**583.0**	13.4
clkad4	615.6	22.62	751.6	**354.4**	22.32	**640.4**	14.1
clkbb1	245.1	11.29	322.5	**166.3**	11.53	**295.7**	6.32
clkbb2	514.1	17.77	733.6	**371.2**	17.26	**661.4**	31.9
clkbb3	1032	40.15	1240	**602.2**	40.97	**1085**	35.3
clkbb4	2119	96.77	2650	**1266**	95.21	**2279**	110
Avg	1.11×	1.03×	1.06×	**0.70×**	1.03×	**0.93×**	

- **Our techniques produce 36.6% less ClkWL while the total signal-net HPWL is very similar**
- **2.57X faster than mPL6**

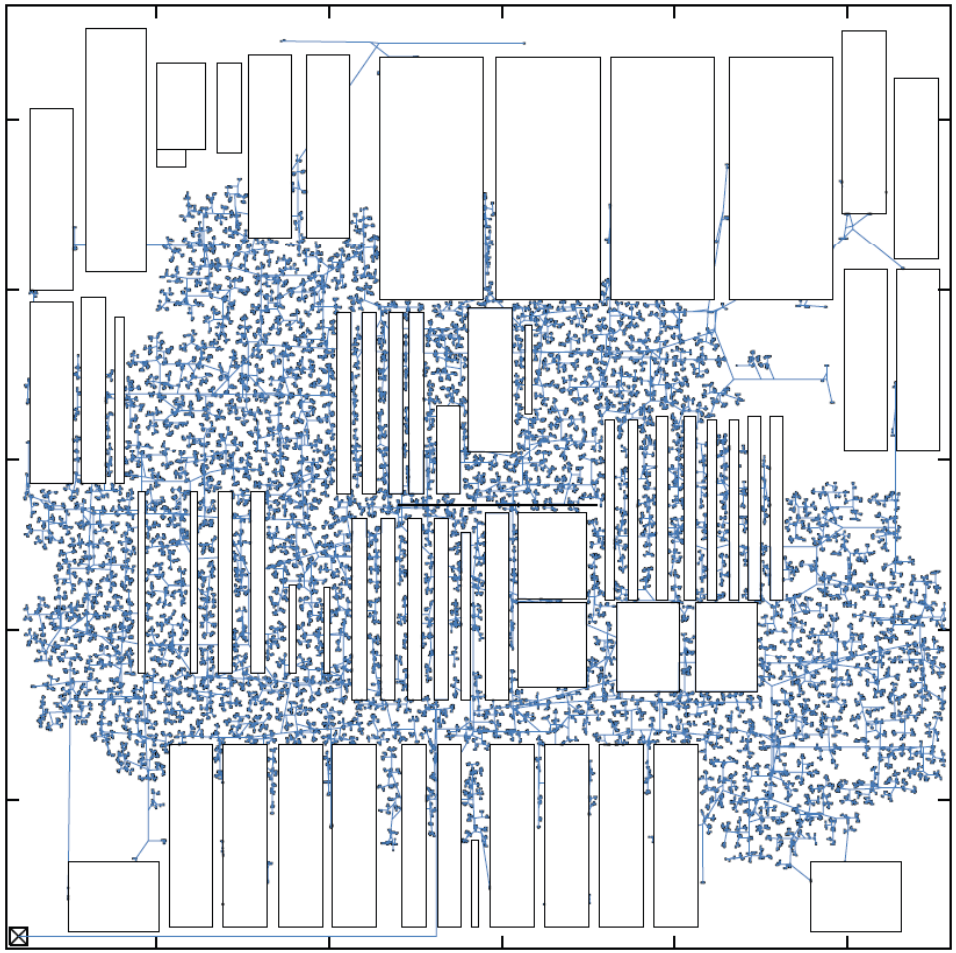
* : T. F. Chan et al, "mPL6: Enhanced Multilevel Mixed-Size Placement," ISPD`06

Example

- **Clock trees for clkad1, based on a SimPL register placement (left) and produced by our method (right)**



209.13*mm*



152.27*mm* (-27%)

Other Experiments

- **Impact of excluding obstacle-aware virtual clock trees (OAVCT), obstacle avoidance forces (OAF)**

	Orig. Flow		w/o OAVCT		w/o OAF	
Bench	ClkWL (*mm*)	Pwr (*mW*)	ClkWL (*mm*)	Pwr (*mW*)	ClkWL (*mm*)	Pwr (*mW*)
clkad1	152.27	263.0	165.86	267.8	158.52	265.3
clkad2	161.03	278.4	170.90	285.5	163.69	278.7
clkad3	326.94	583.0	362.11	595.1	340.78	587.4
clkad4	354.44	640.4	403.05	657.2	379.78	649.4
clkbb1	166.33	295.7	172.58	297.4	169.12	296.4
clkbb2	371.18	661.4	411.24	673.8	389.92	666.7
clkbb3	602.22	1085	663.10	1104	627.19	1093
clkbb4	1265.5	2279	1411.8	2331	1328.1	2102
Avg	**1.0**×	**1.0**×	+**9.5**%	+**1.8**%	+**4.1**%	+**0.7**%

- **Handling obstacles is important for virtual clock trees and force generation**

Other Experiments

- **Comparison to multi-level attractive force (MLAF)***

	SIMPL+MLAF		
Bench	ClkWL (*mm*)	HPWL (*m*)	Pwr (*mW*)
clkad1	182.44 (46.9%)	9.194 (85.3%)	274.2 (33.7%)
clkad2	200.91 (35.8%)	10.764 (76.2%)	293.0 (24.0%)
clkad3	402.46 (46.6%)	24.713 (76.9%)	609.8 (35.7%)
clkad4	449.48 (42.4%)	22.238 (86.9%)	676.6 (30.7%)
clkbb1	203.79 (47.9%)	11.476 (84.9%)	309.7 (36.1%)
clkbb2	473.77 (36.7%)	17.161 (80.0%)	699.3 (23.4%)
clkbb3	743.53 (46.5%)	40.813 (91.0%)	1139 (22.9%)
clkbb4	1586.5 (45.5%)	94.765 (80.2%)	2399 (38.1%)
Avg	**(43.5%)**	**(82.7%)**	**(30.6%)**

- When MLAF is utilized, the amount of reduction in ClkWL is reduced to 43.5% compared to our techniques (100%)
- Only 30.6% of power reduction by our techniques can be obtained by MLAF

* : *Y. Wang et al, "Clock-Tree Aware Placement Based on Dynamic Clock-Tree Building," ISCAS`07*

Conclusion

- **New techniques and a methodology to optimize total dynamic power during placement**
  - For large IC designs with numerous macro blocks
  - Obstacle-aware virtual clock-tree synthesis
  - Arboreal clock-net contraction force with virtual nodes that can handle gated clocks
  - Obstacle-avoidance force modification
  - Integrated into the SimPL placer
  - A new set of 45nm benchmarks
- **Our method lowers the overall dynamic power by significantly reducing clock-net switching power**

Questions and Answers

Thank you!!

Questions?