Automated Placement for Custom Digital Designs

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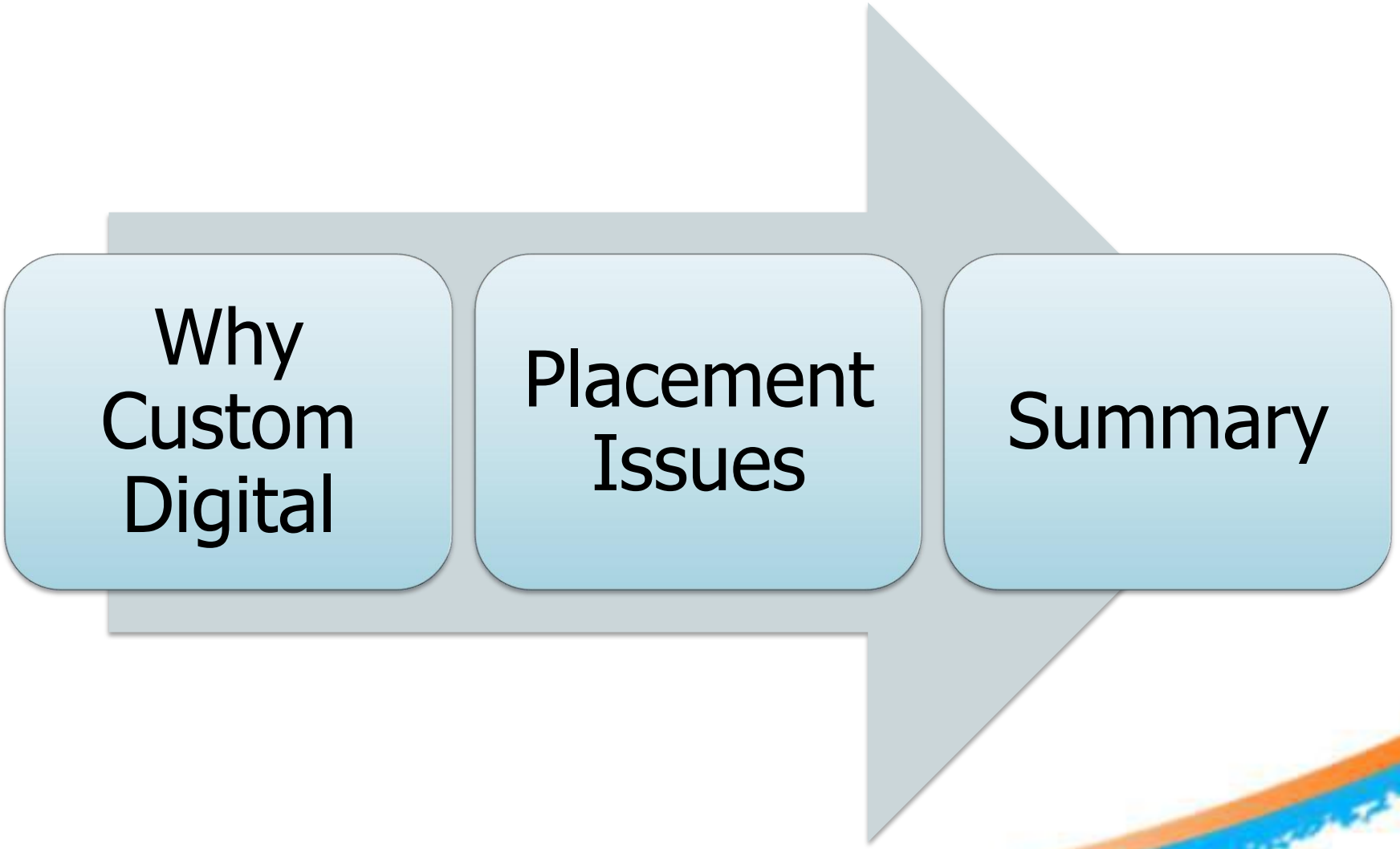
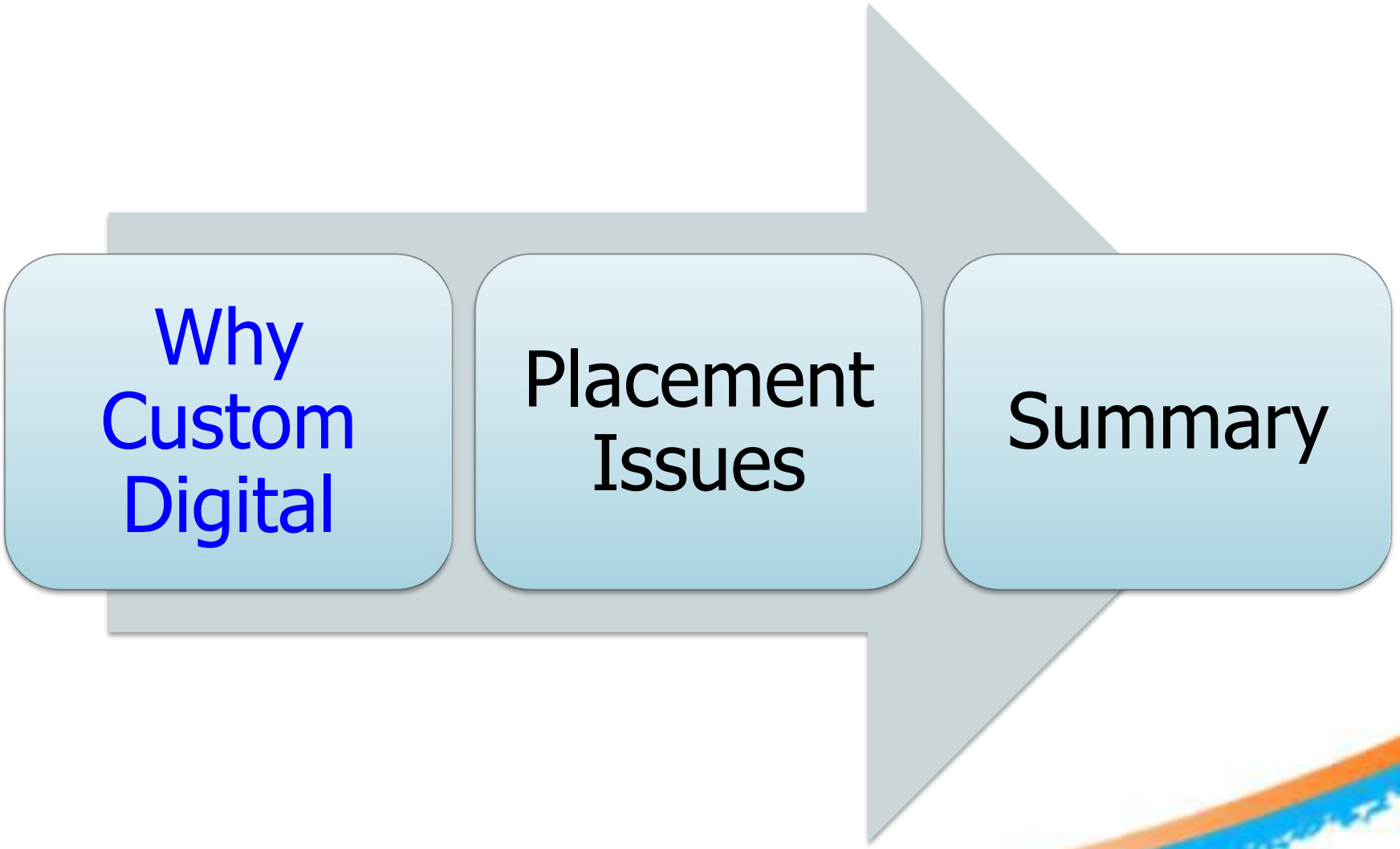
Mar 29 2011 (ISPD-2011)

Outline



Outline



Why Custom Digital

- Allow precise custom design of digital blocks often used in mixed-signal environment
- Meet the critical performance requirements that often cannot be achieved by standard digital design flow

Properties for Custom Digital Designs

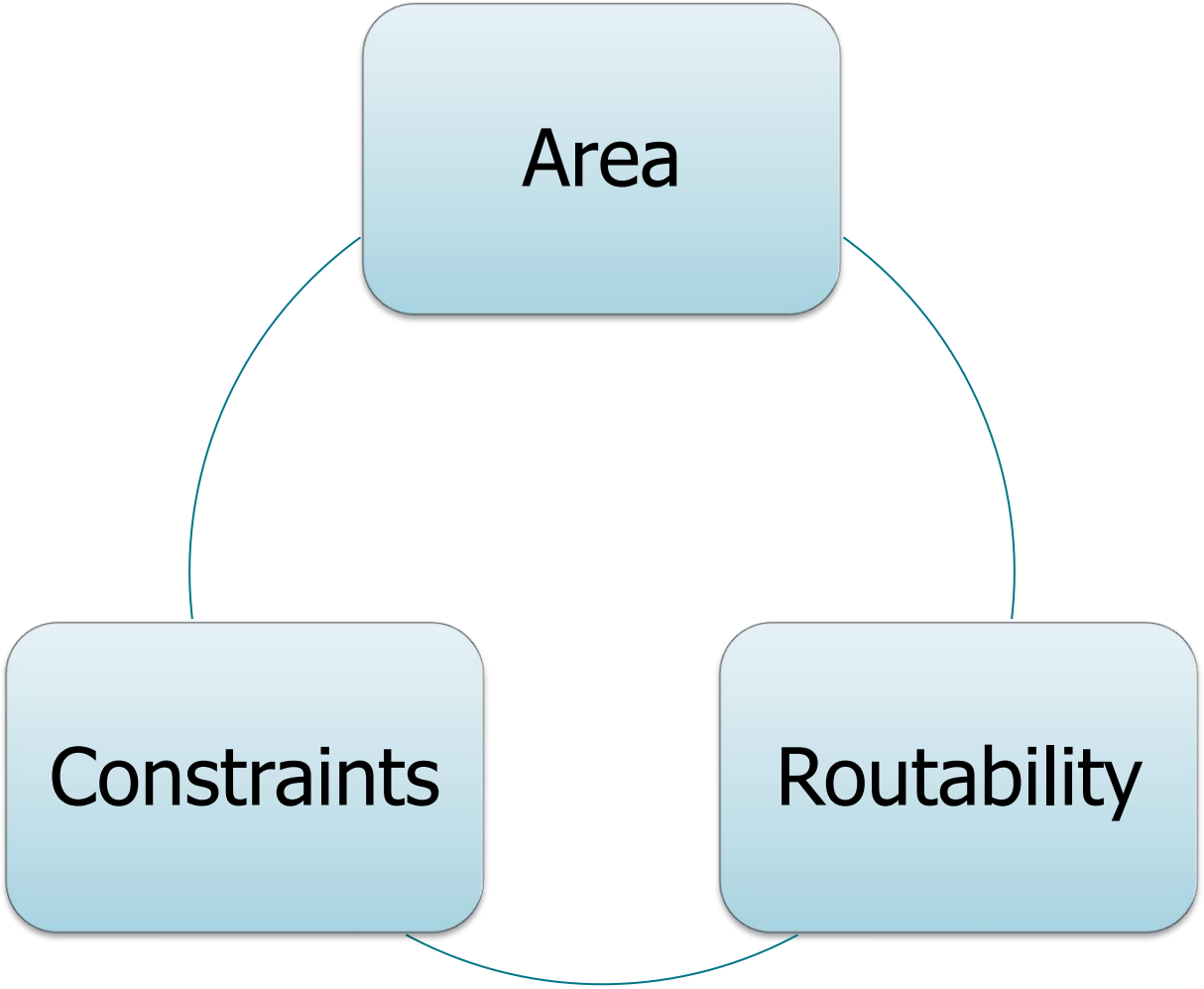
Tight Utilization

Limited Metal Layers

Various Placement Constraints

Need unique automation techniques to solve issues in custom digital placement

Placement Issues



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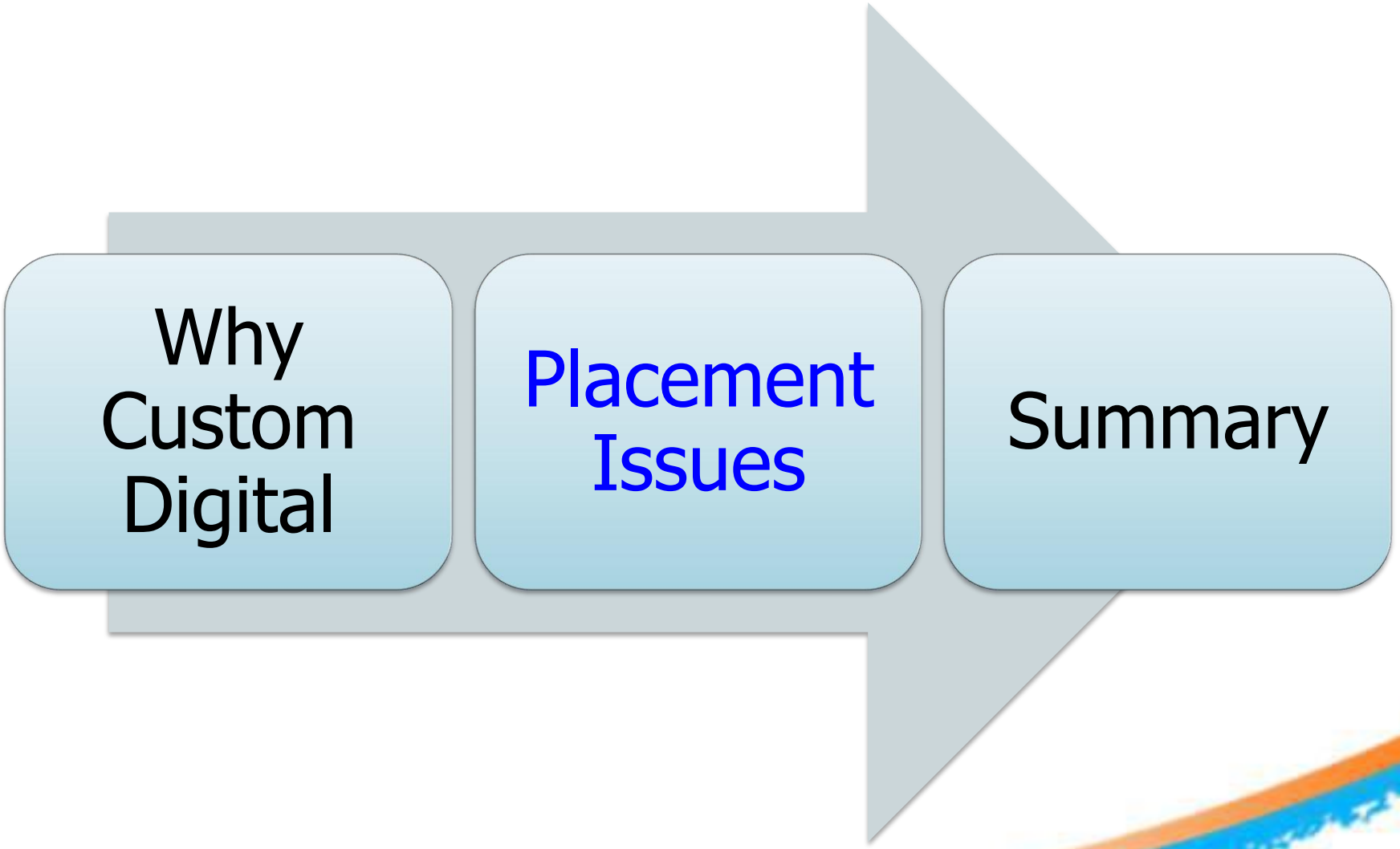
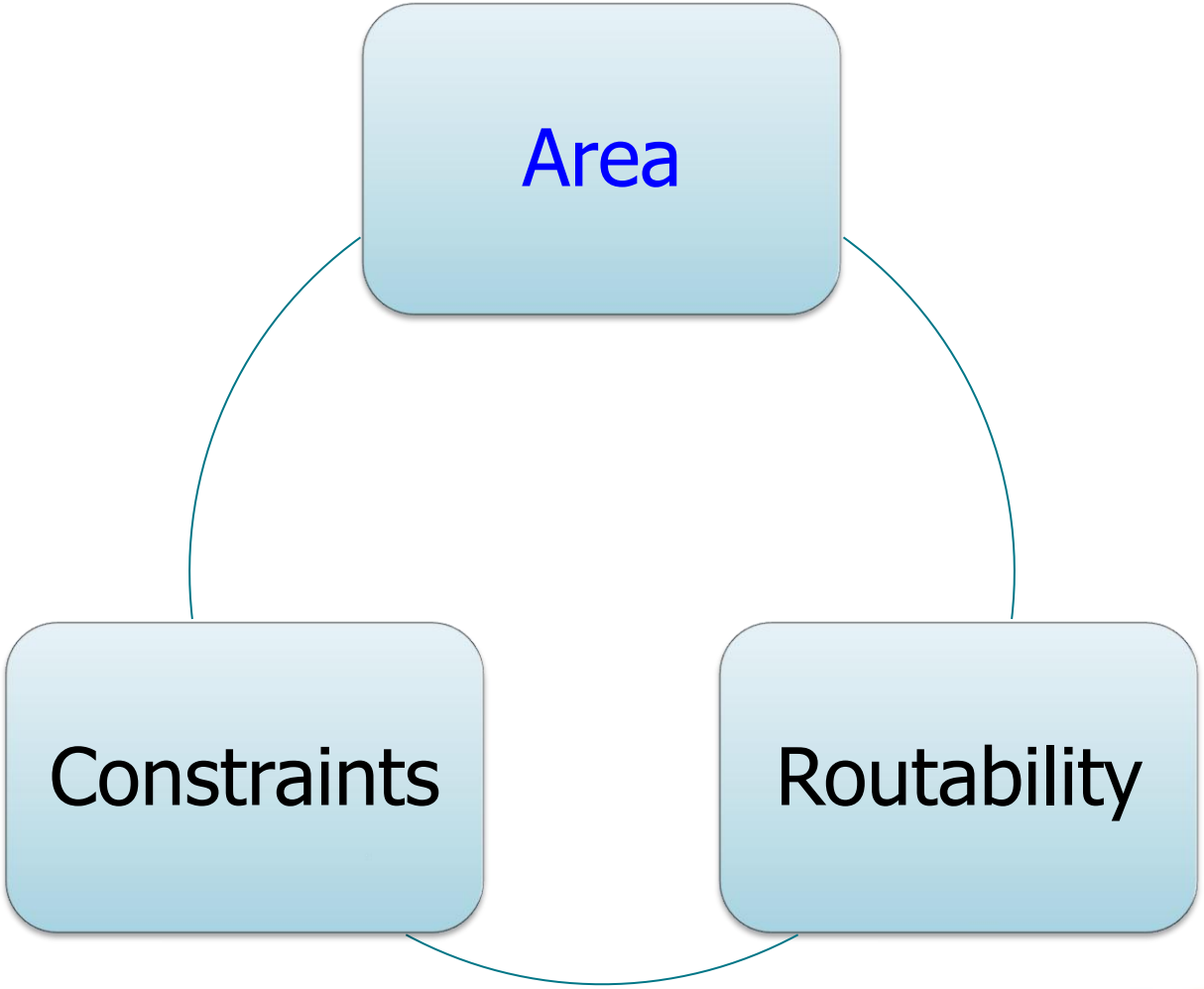


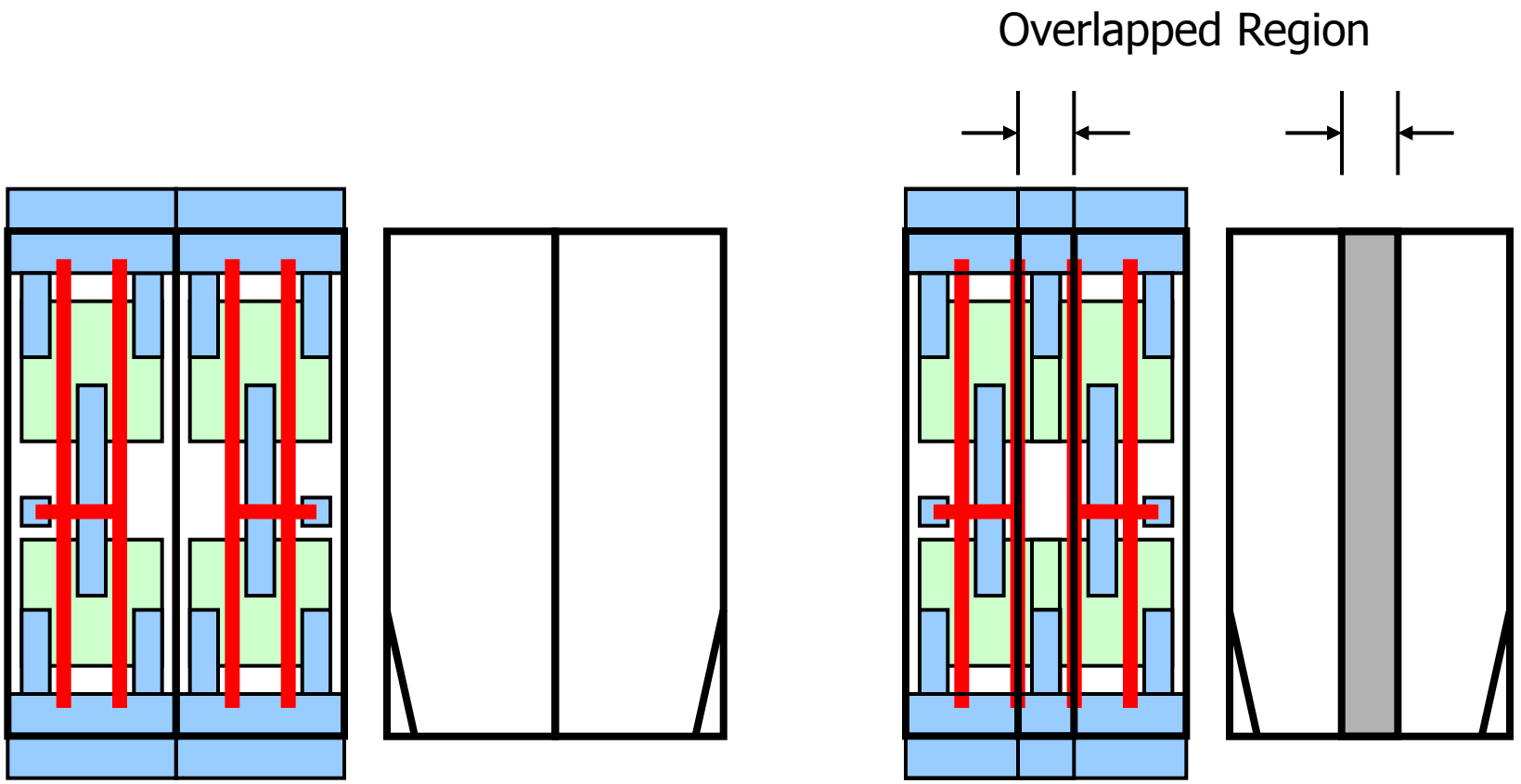
Placement Issues



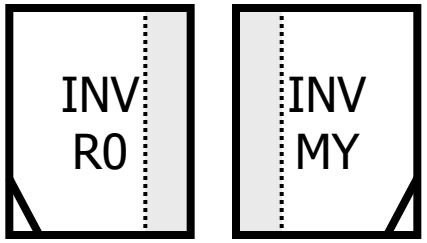
Area Minimization

- How to minimize placement area?
  - Reduce whitespace by increasing cell utilization
  - Overlap cells
- Cell overlapping by oxide diffusion sharing
  - A common technique used in transistor-level placement but not in cell-level placement
  - Cells with common power/ground portion can be overlapped to reduce area

Cell Overlapping Example



Cell Overlapping Problem



- Input
  - A cell placement
  - A list of allowable cell overlap combinations
    - For example, INV-Right and INV-Right means an INV (R0) can be overlapped with an INV (MirrorY)

- Decide the new orientation of each cell so that the number of cell overlaps for adjacent cells can be maximized

Cell Overlapping Study

- 1p3m
- Area reduction is around 6% to 13%

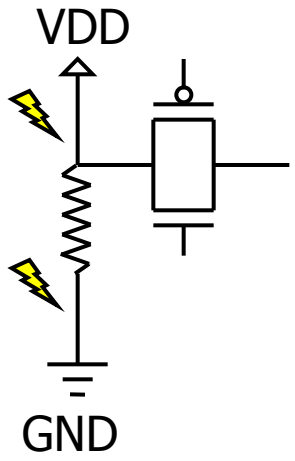
	Cell #	CellArea / RowArea		Reduced Area
		Without overlapping	With Overlapping	
Case1	85	99.9%	106.7%	6.8%
Case2	87	95.1%	106.3%	11.8%
Case3	113	98.1%	110.8%	13.0%
Case4	362	99.6%	106.1%	6.5%

Problem of Squeezing Cells…

- Routability
  - Need a better routing plan (topology) to utilize the routing resources
- Electrostatic discharge (ESD) path
  - Prevent a direct power-to-ground current path with small resistance

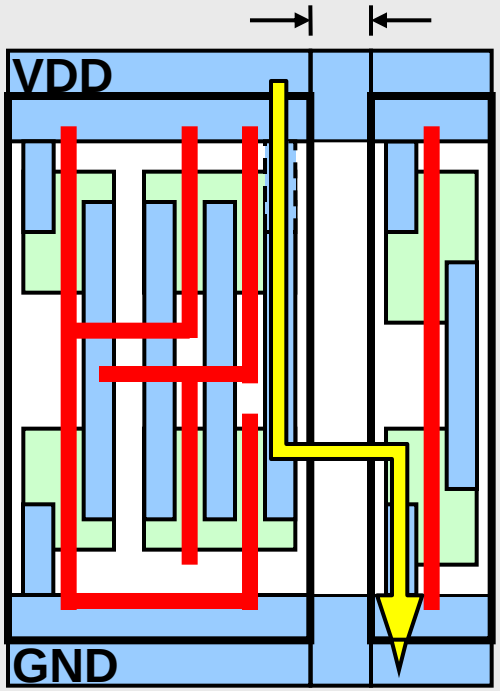
Electrostatic Discharge (ESD) Path

- Direct connection of power-to-ground rails without tie cells can be used to compact size in a high utilization design
- A larger spacing rule is used to avoid direct power ground path due to small resistance

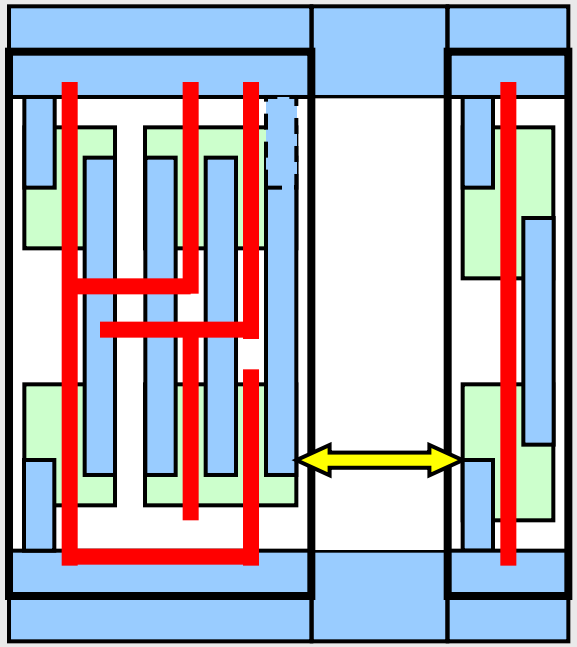


Solving ESD Spacing Rule

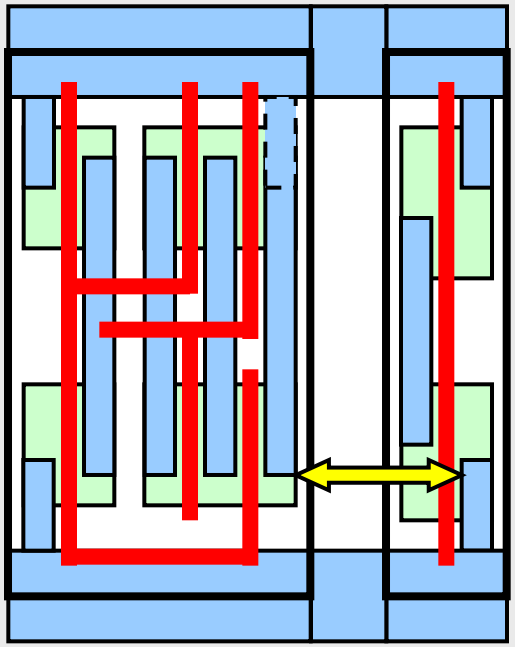
Need larger spacing to increase resistance from power to ground



Increase cell spacing to prevent the violation



Flip the cell to reduce cell spacing while keeping the same ESD space rule

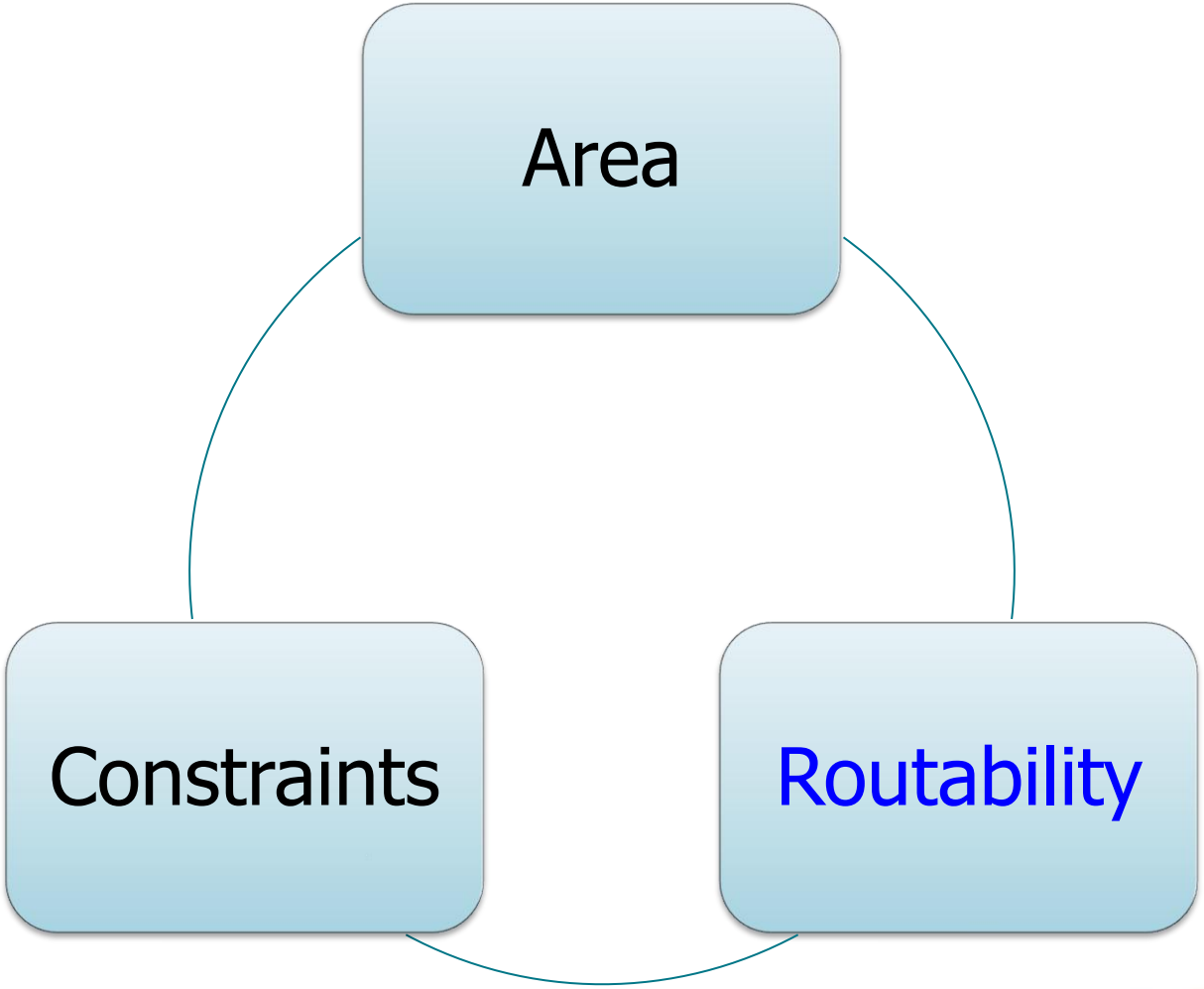


ESD-Violation-Fixing Problem

- Input
  - A cell placement
  - ESD spacing rule
  - Direct tie-high/low pins

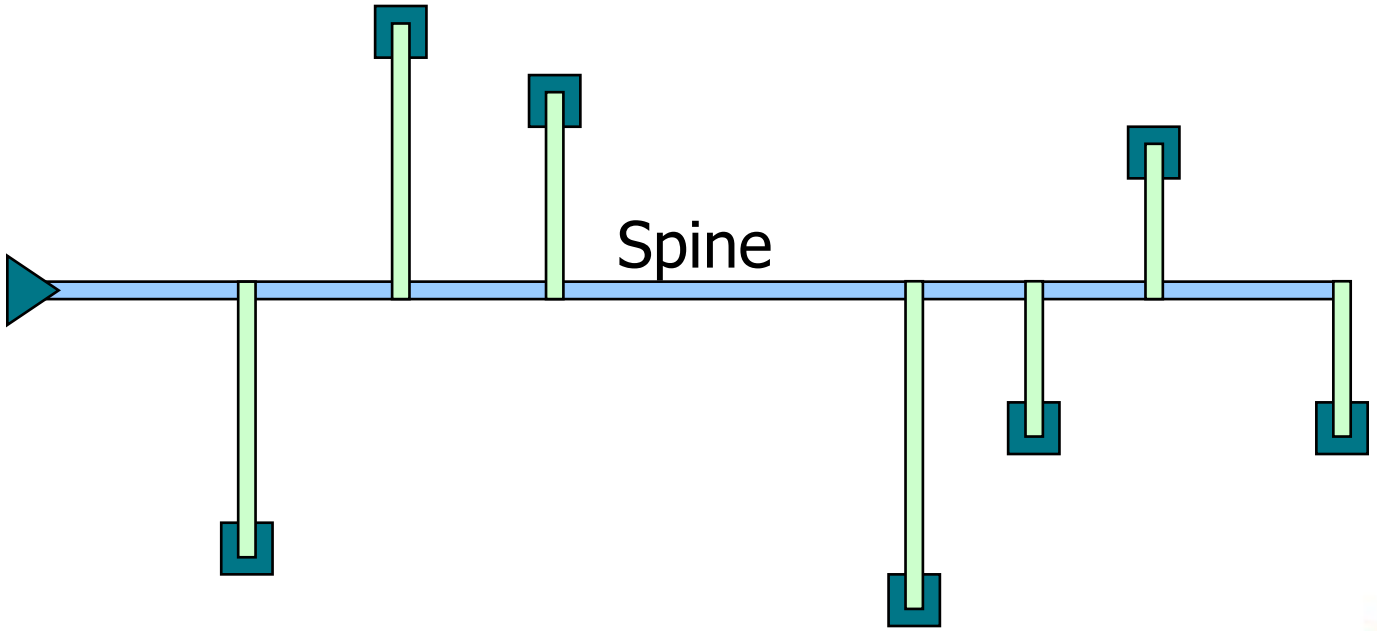
- Decide new cell positions and orientations so that all ESD spacing violations are resolved and the change of cell positions and orientations are minimized

Placement Issues



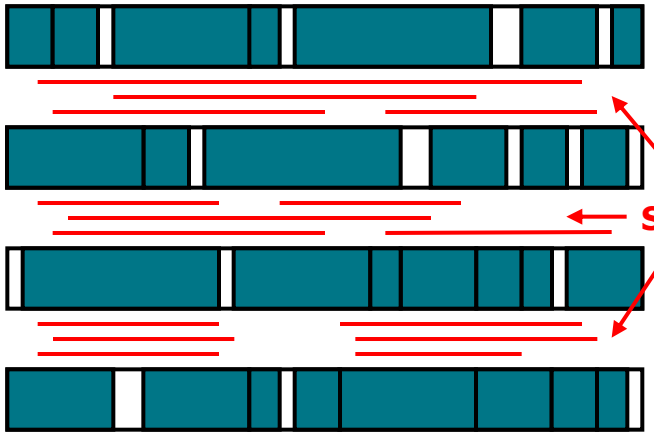
Improving Routability

- Spine Routing Topology
  - More predictable for resource usage, wire length, source-to-sink path, etc.



Floorplan for Spine Routing

Channel Floorplan

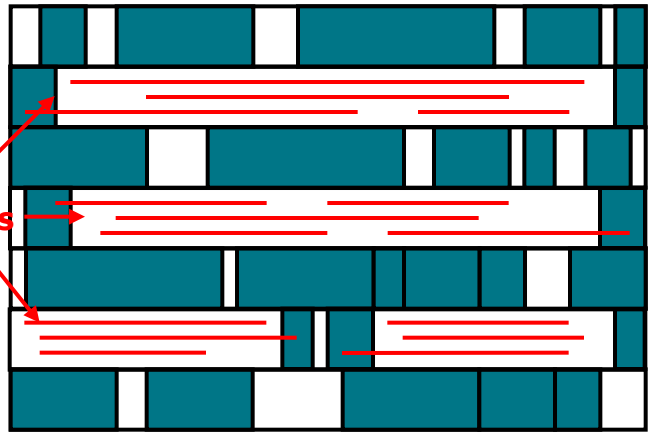


Channels are pre-defined before cell placement

Pro:

* Channel sizes can be different

Pseudo-Channel Floorplan



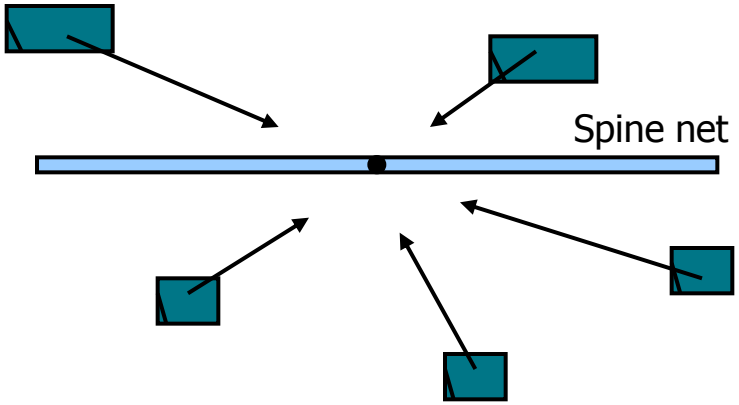
Channels are automatically created during placement

Pro:

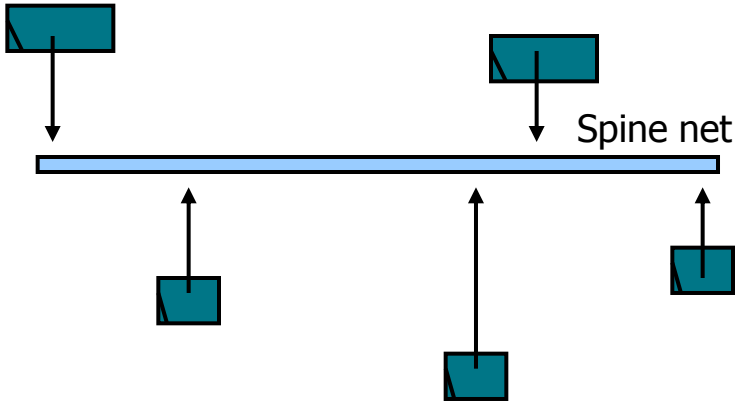
* No need to define channels before placement
* Cell positions are more flexible

Need an Accurate Net Model for Spine Nets

- A pin is usually modeled by using a point
  → NOT accurate for a large pin (spine)



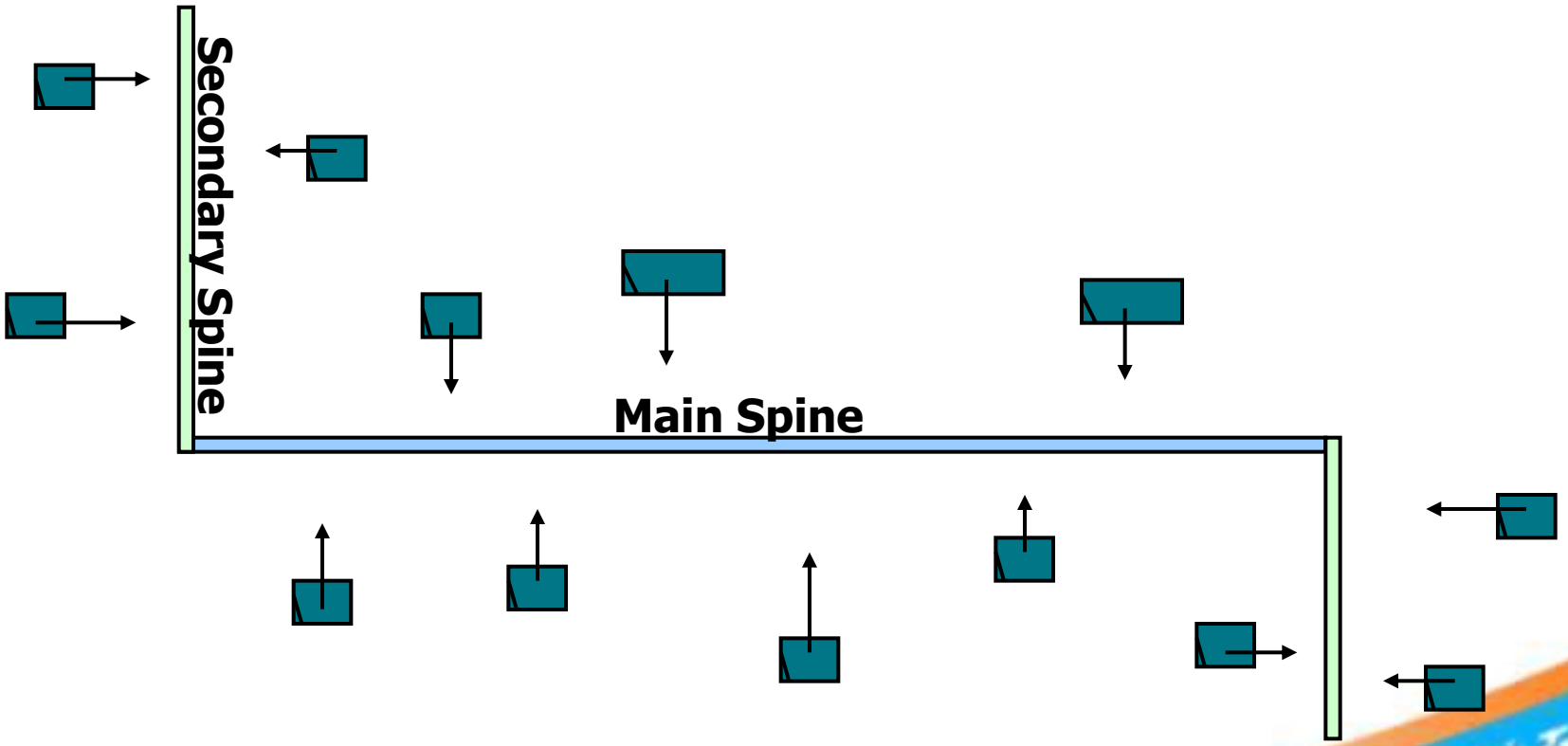
Using an inaccurate net model for a spine net may cause cells collapsed to a point



The desired cell moving directions

Complex Spine Topology

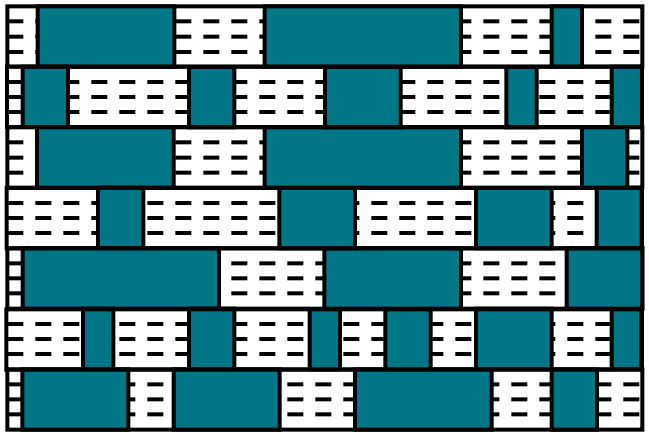
- Placement becomes harder when spine topology becomes complicated



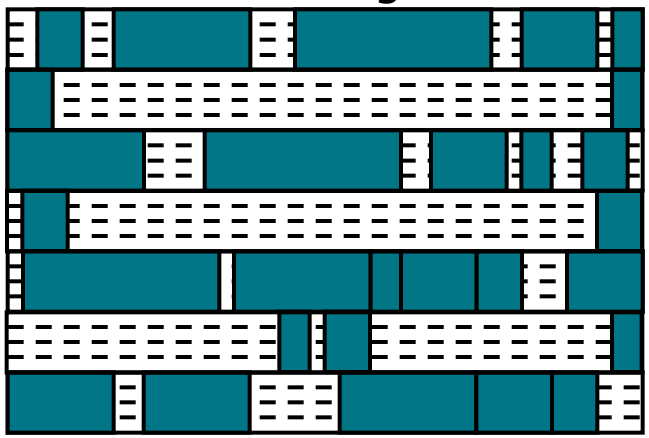
Pseudo-Channel Placement

- F.-Y. Chang et al., "Cut-Demand Based Routing Resource Allocation and Consolidation for Routability Enhancement," ASP-DAC 2010
- How to create "useful routing tracks"?

"useless routing tracks"

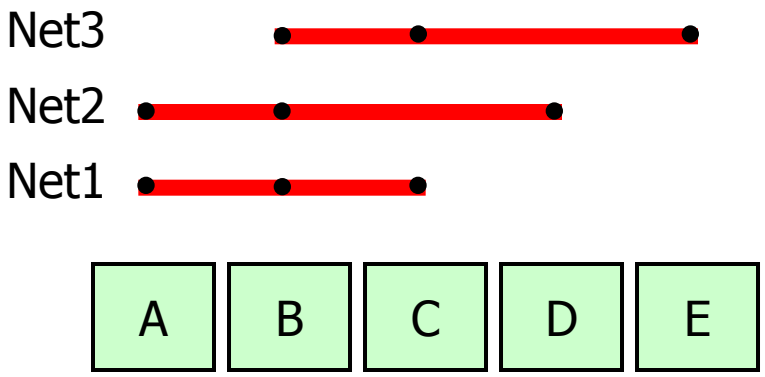


"useful routing tracks"

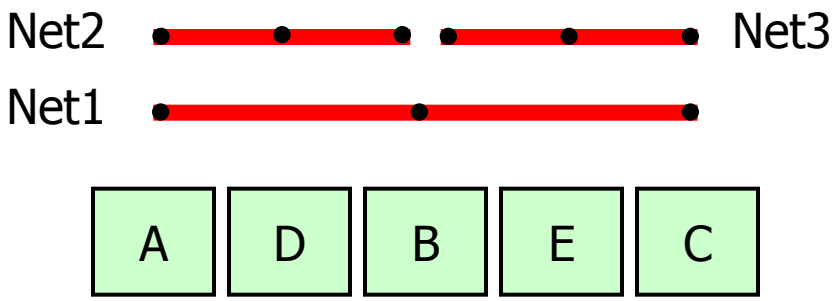


Wire Length vs. Routing Track Number

- Routing track may not be reduced when minimizing wire length

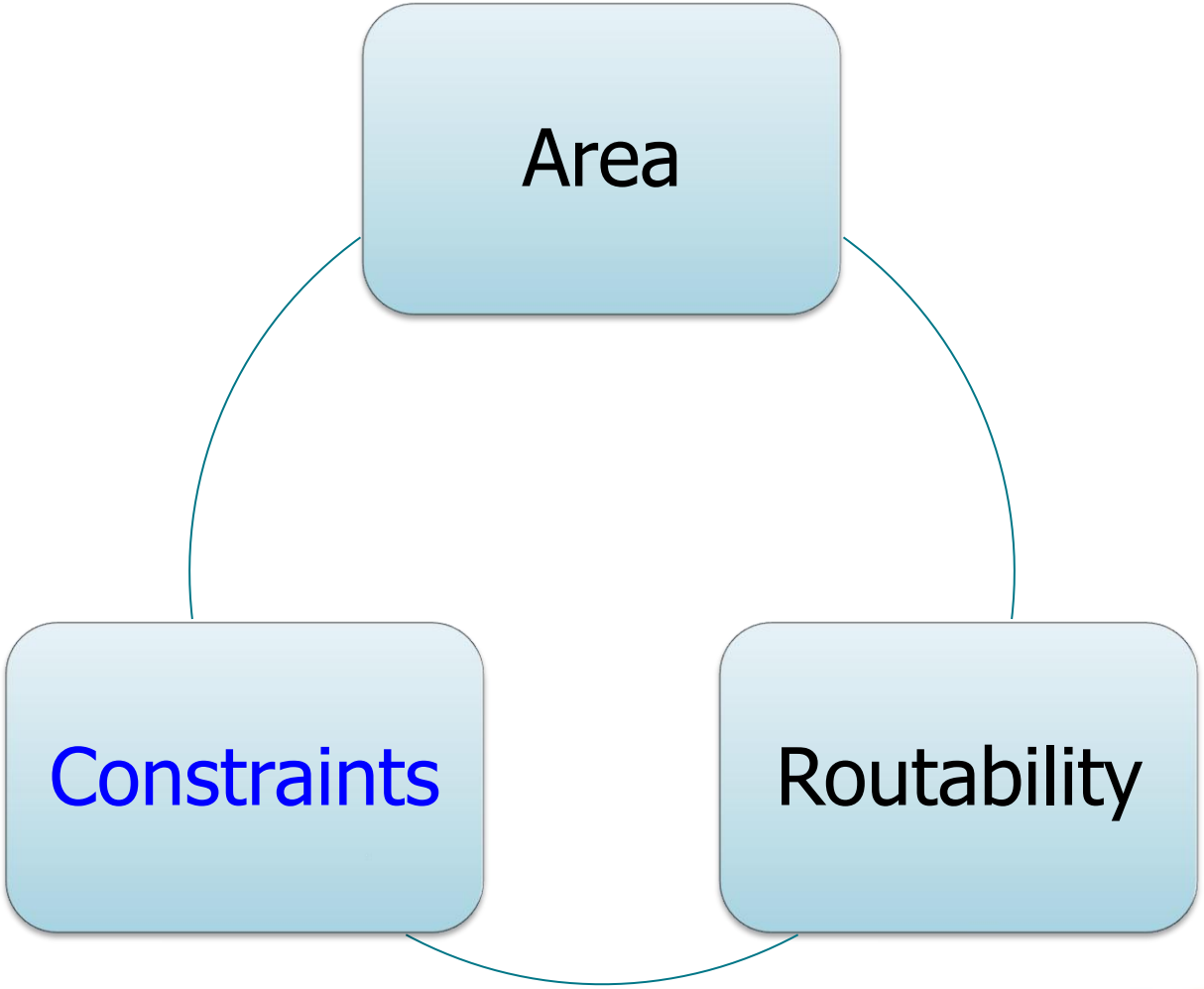


Wirelength = 8
Track = **3**



Wirelength = 8
Track = **2**

Placement Issues



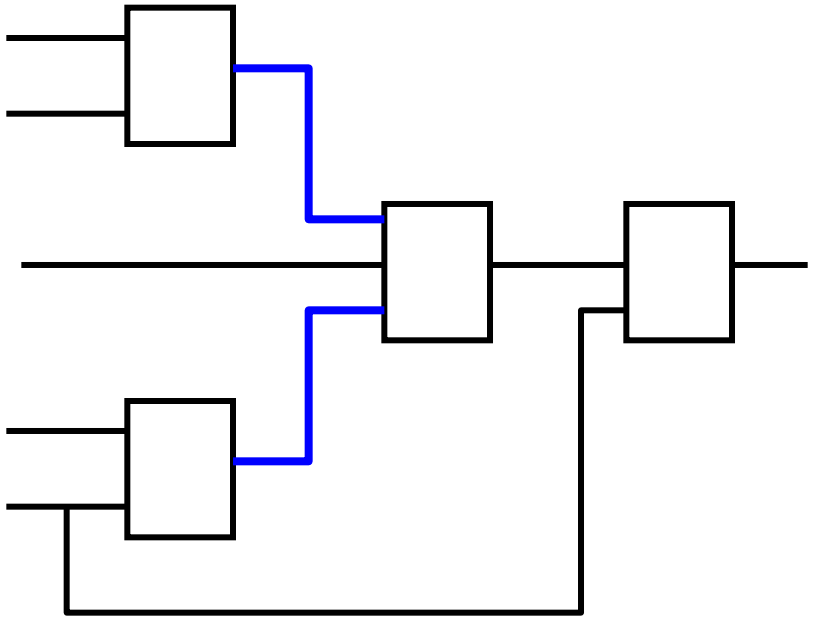
Placement Constraints

- Symmetry constraints
- Relative placement constraints
- Hierarchy constraint

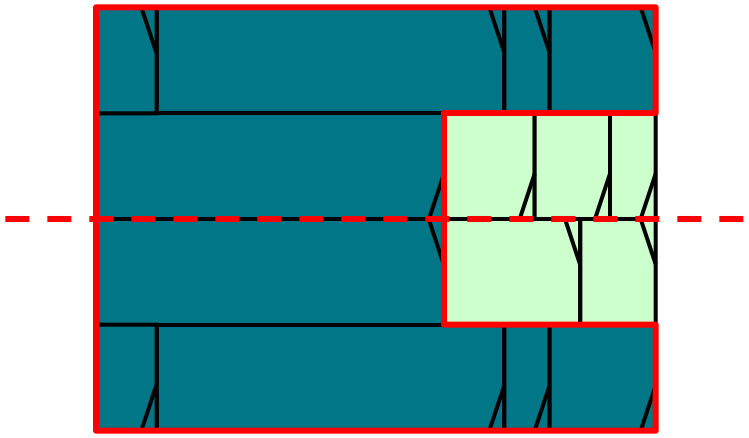
- All constraints should be followed at any stage of automatic placement

Symmetry Constraint

- Symmetric placement for device/net matching

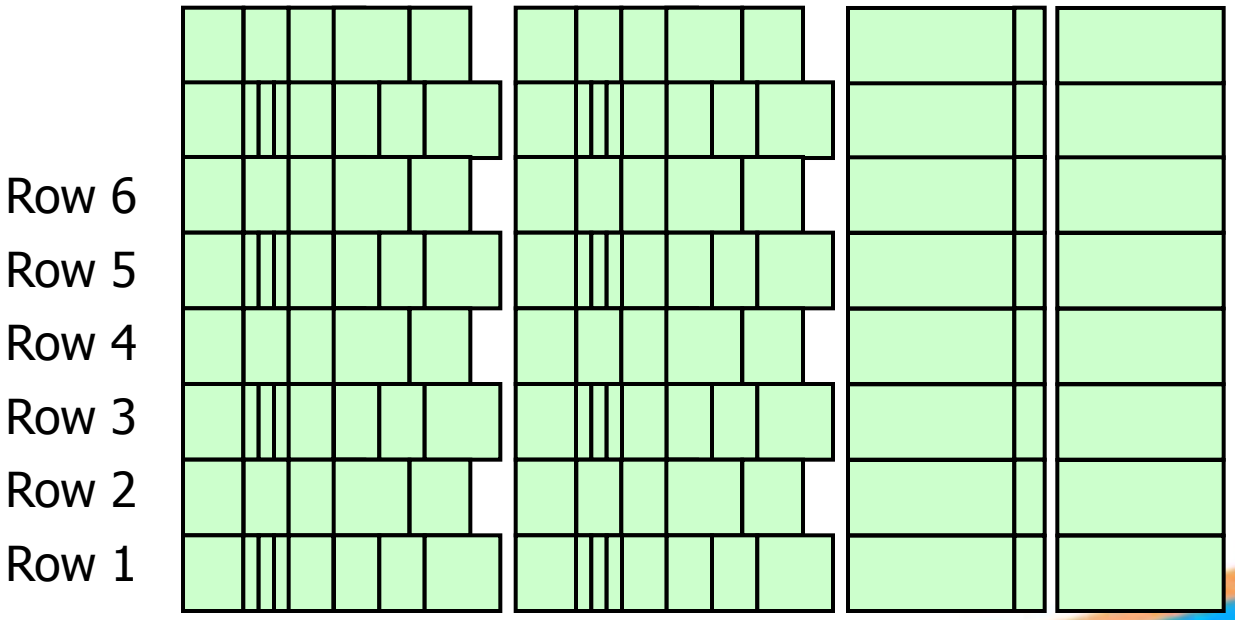


symmetry placement about x-axis



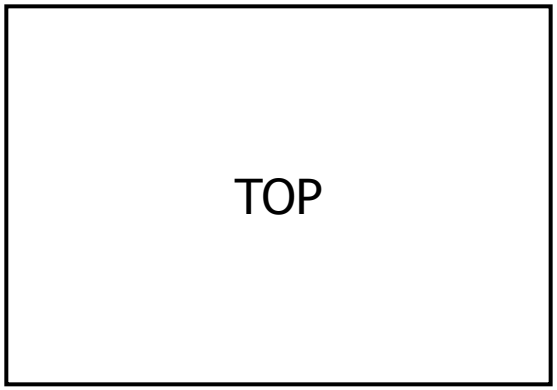
Relative Placement Constraint

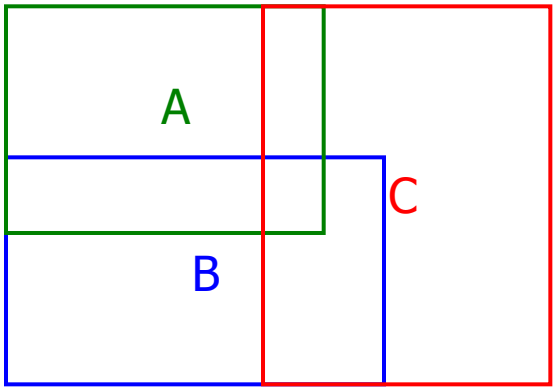
- Also known as structure/matrix placement
- Good for data-path designs
- Constraints can be defined in a matrix style (col/row)



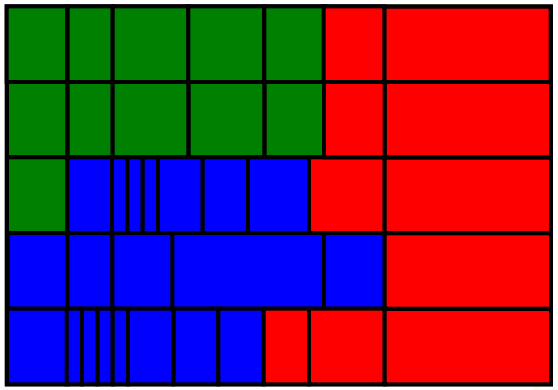
Hierarchy Constraint

- Placement while keeping cells in the same hierarchy block
- No overlap between cells in different hierarchy blocks (cellviews)



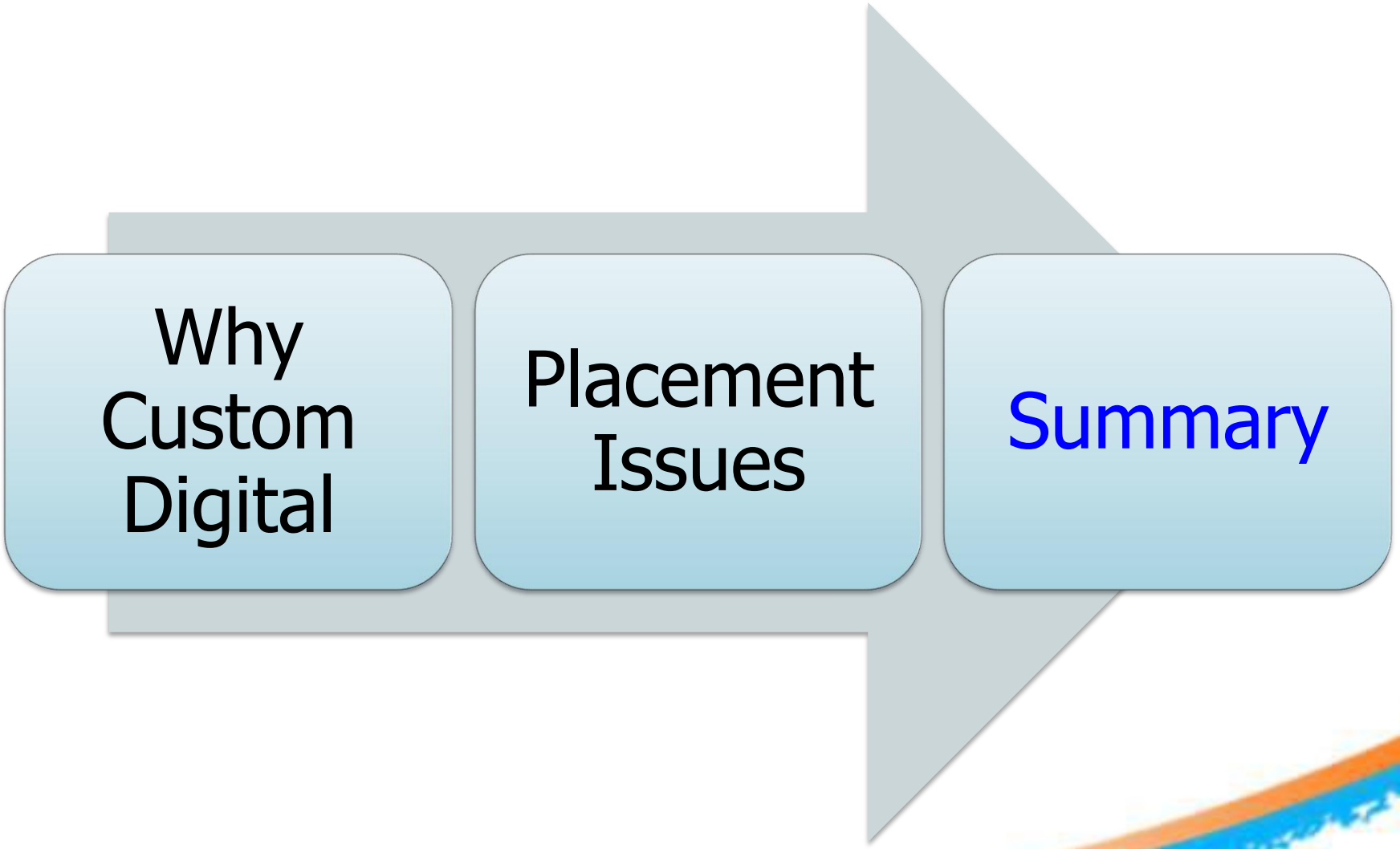


block level



cell level

Outline



Summary

Issues in automated custom digital placement

Area	• Cell overlapping • ESD rule spacing
Routability	• Spine routing topology • Pseudo-channel floorplan • Track number vs. wire length
Constraints	• Symmetry • Relative placement • Hierarchy

Thank You for Your Attention!

Any Question?