On Old and New Routing Problems

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A Short History of Interconnect Routing

Time Period	Advances in Routing
1800 s	Geometric Steiner problem, Hamiltonian path (traveling salesman) formulated.
1960 -1969	Point-to-point routing algorithms (Lee's maze and Hightower's line search).
1965 -1975	Layout tools first developed for printed circuit boards. First abstract multi-net optimization problems formulated.
1975 -1985	Planar routing, more sophisticated graph models, VLSI layout styles and various abstract routing problems formulated.
1985 -1990	First performance-driven tools , clock routing, power and ground routing; graph theory, computational geometry, algorithm complexity techniques/concepts applied to routing problems.
1990 -2000	Over-the-cell routing, 3D and multilayer placement and routing techniques developed. Routability driven design. Routing + electrical constraints = physical synthesis introduced.
2000 - now	DFM driven routing; dramatic algorithmic improvements.

Kuh's Group Contributions

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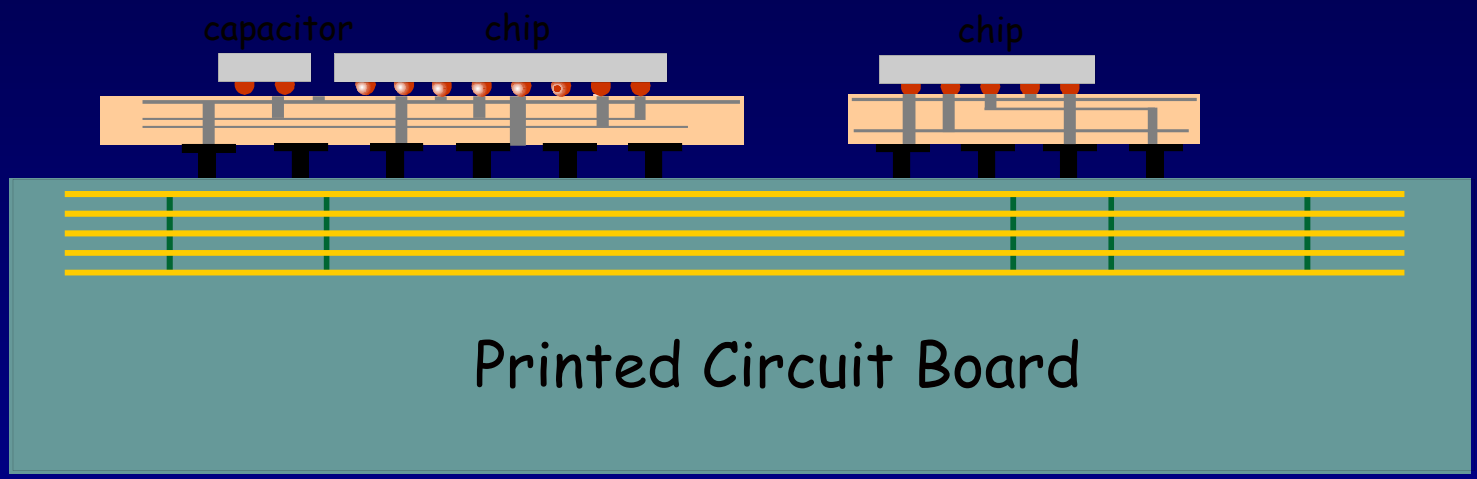
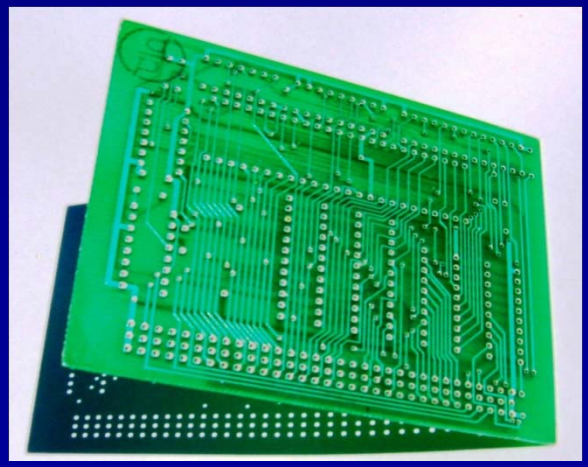
Overview

- **Interconnect Routing Automation in Kuh's Group**
  - PCB Wiring and Single Row Routing
  - Building Block style layout
  - Wire Coupling Minimization
  - Post-routing Topology Optimization for Clock and Power Networks
- **Research Problems**

PCB Routing



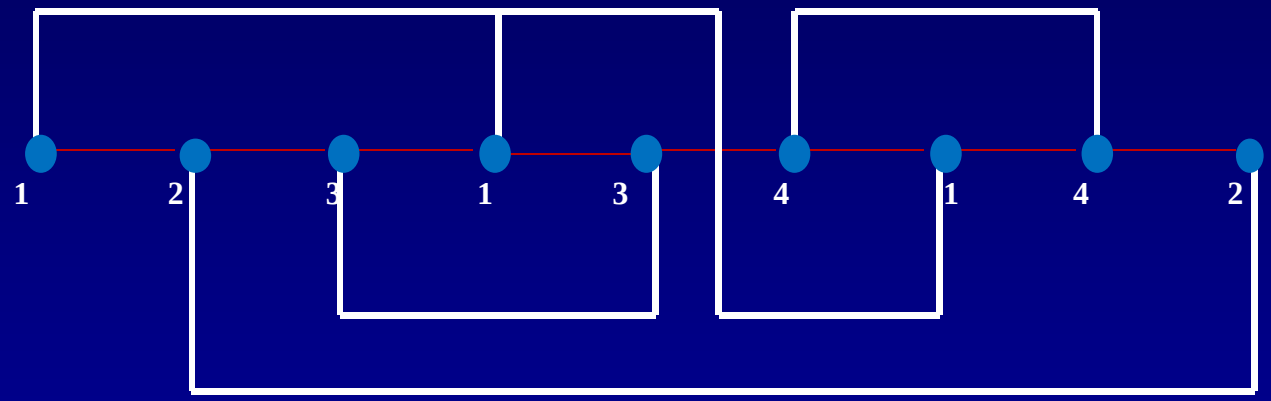
- Many layers
- Relatively large area
- Low performance
- Modern designs:
  - High-density fine-pitch packages
  - Large pin counts



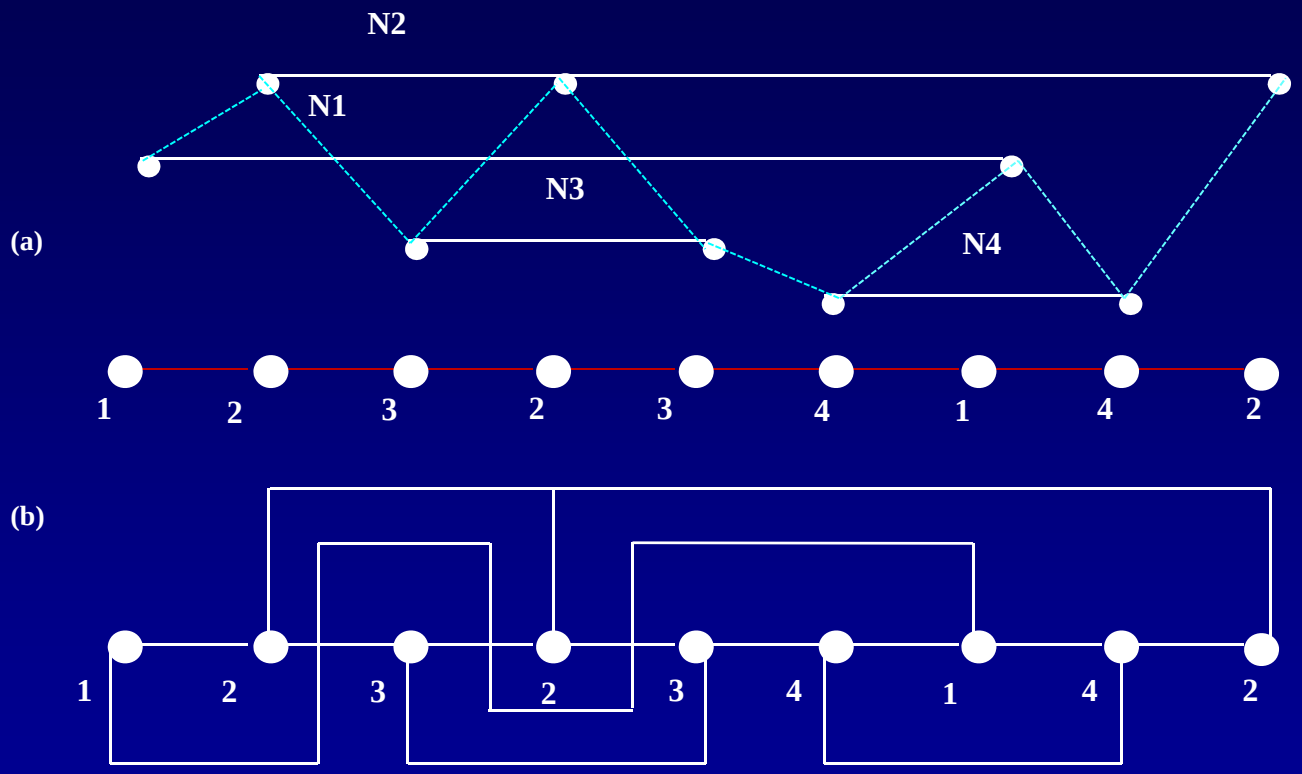
PCB Routing Formulation

- **The model:**
  - The board has a fixed geometry and many layers
  - Each layer has fixed platted through holes uniformly spaced on grid
  - Every other column of holes consists either of conductor pins reaching all layers, or vias
- **Problem: Connect the module terminals using wires, pins and vias.**
- **Key abstraction: single row routing problem.**

Single Row Routing Problem



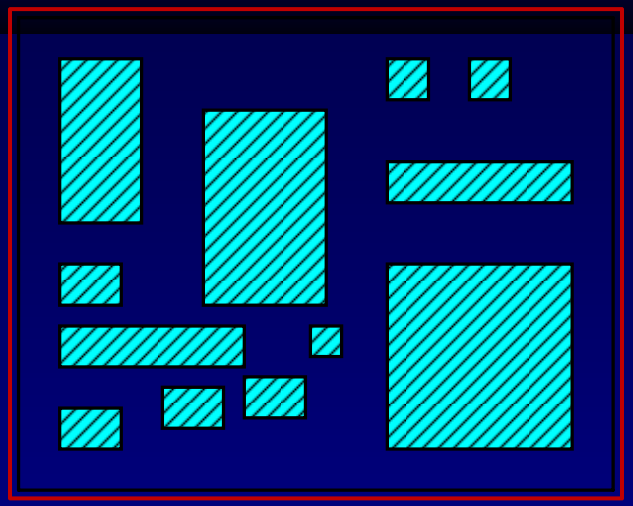
Single Row Routing Problem



What is special about Single Row?

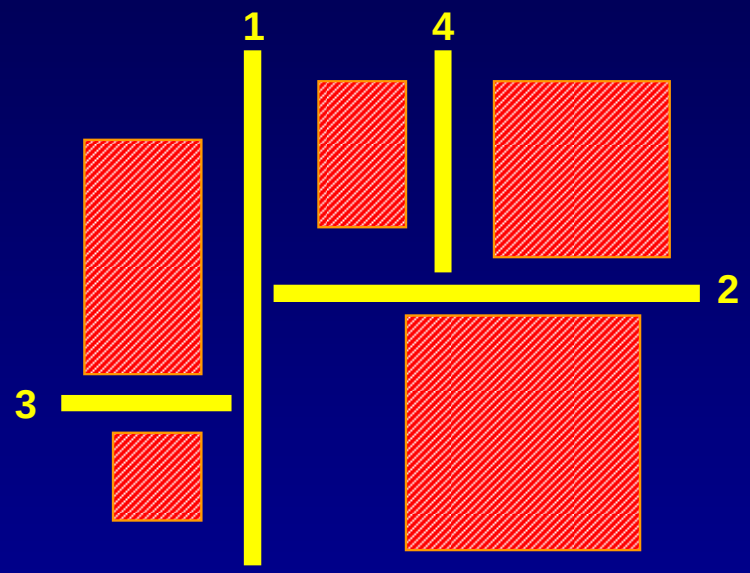
- Key properties of the single row routing representation
  - Interval ordering determines completely the routing solution
  - Defines a topological to geometric mapping
- First time routing of many nets was addressed simultaneously
- Inspired topological routing research
- Recently, the model has been used for wireless cellular network channel assignment

Building Block Layout

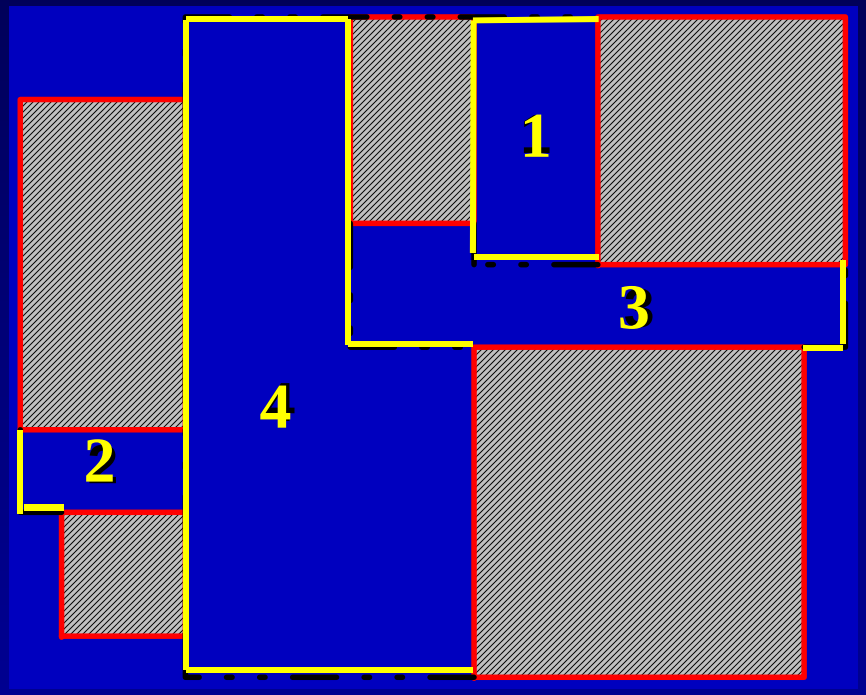


- **Blocks differ in size and shape**
- **Difficult to automate**
  - Irregular routing area
  - Blocks can move
- **Two approaches to routing:**
  - Fracture the routing region; route the sub-regions and adjust block placement.
  - Fix the block positions and make all connections (routing may be too loose or design rules violated); apply compaction/decompaction.

Channel Definition and Ordering

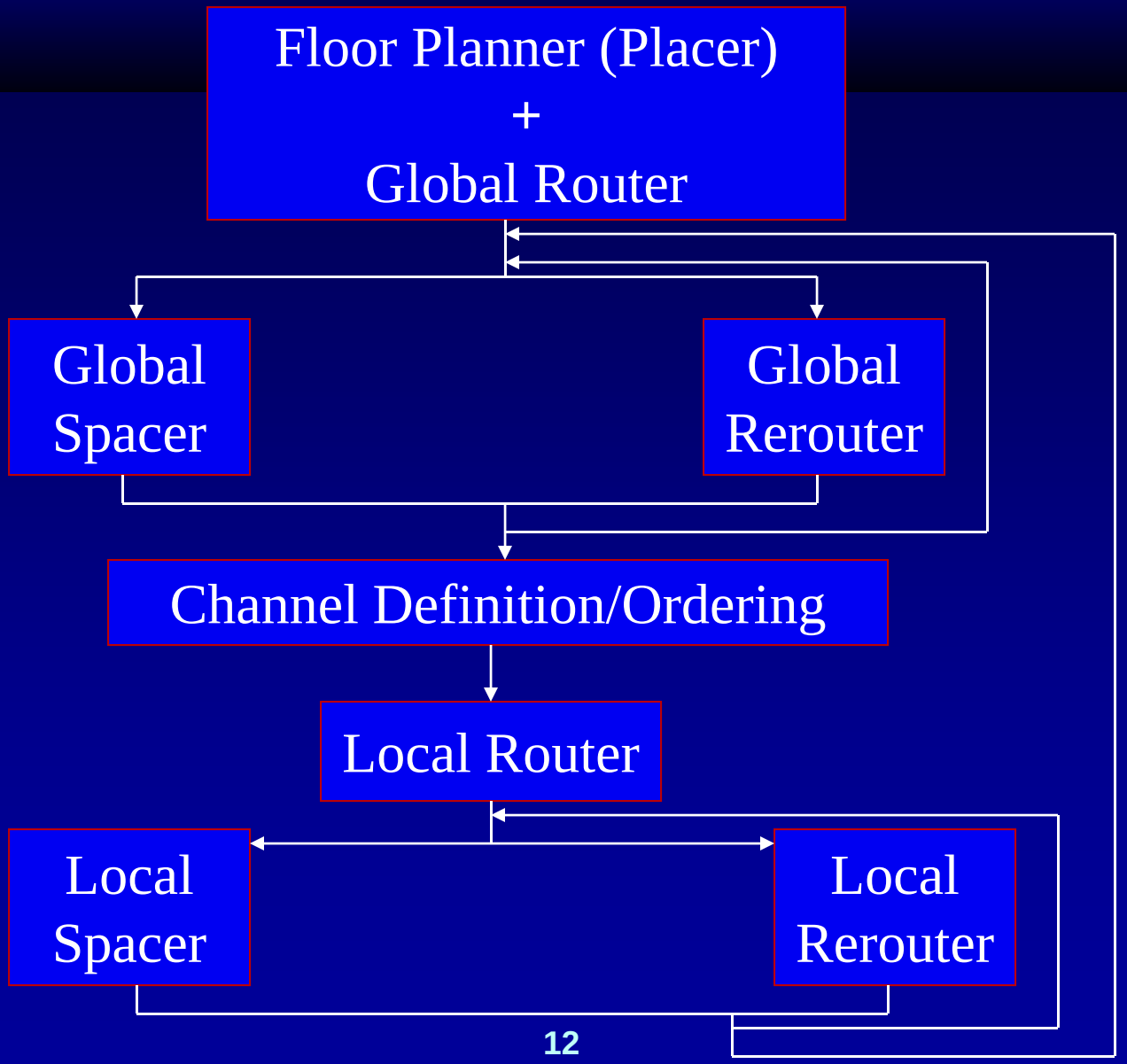


Topological channels

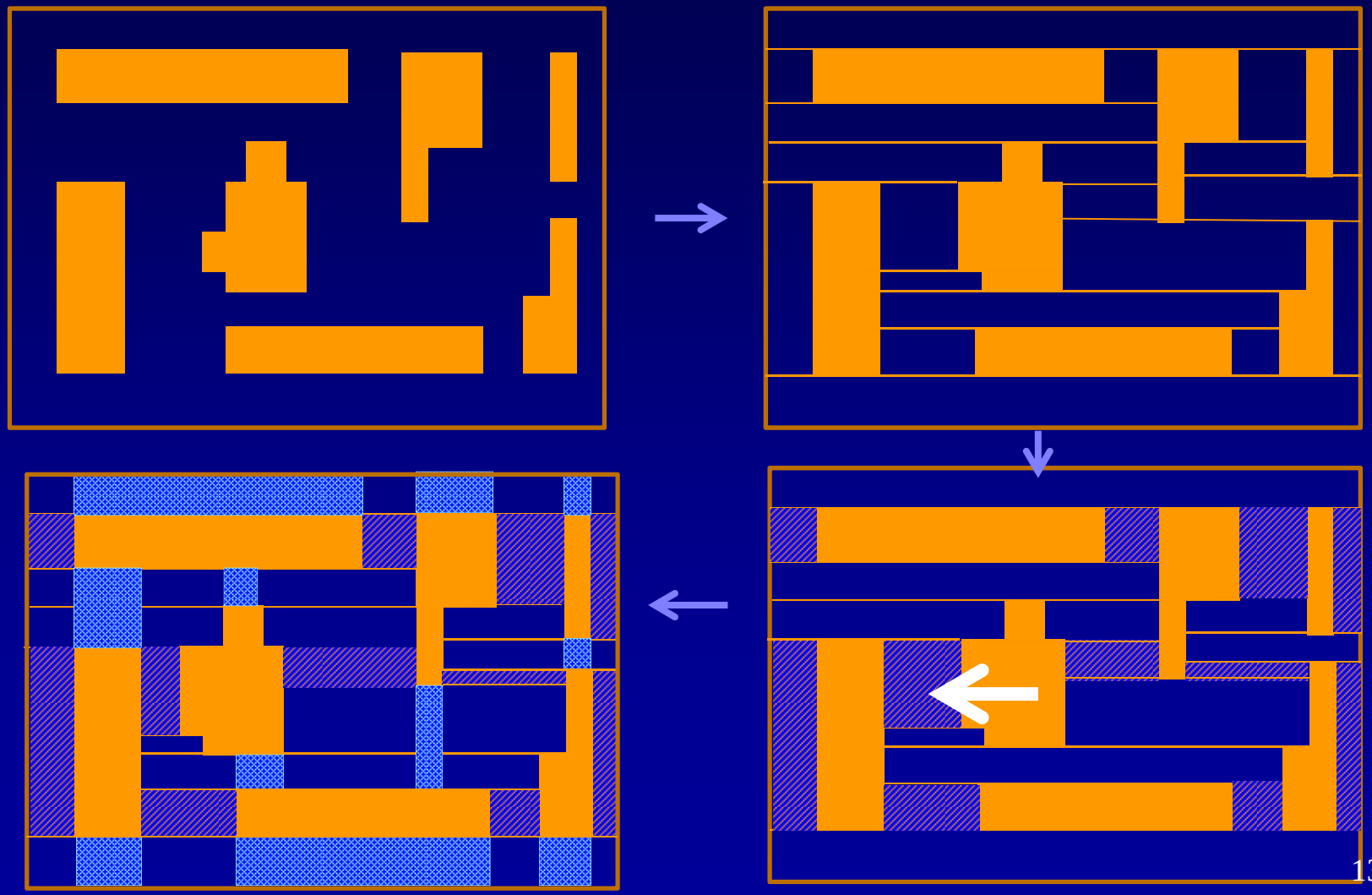


Geometric channels

Building Block Routing



Dynamic routing update

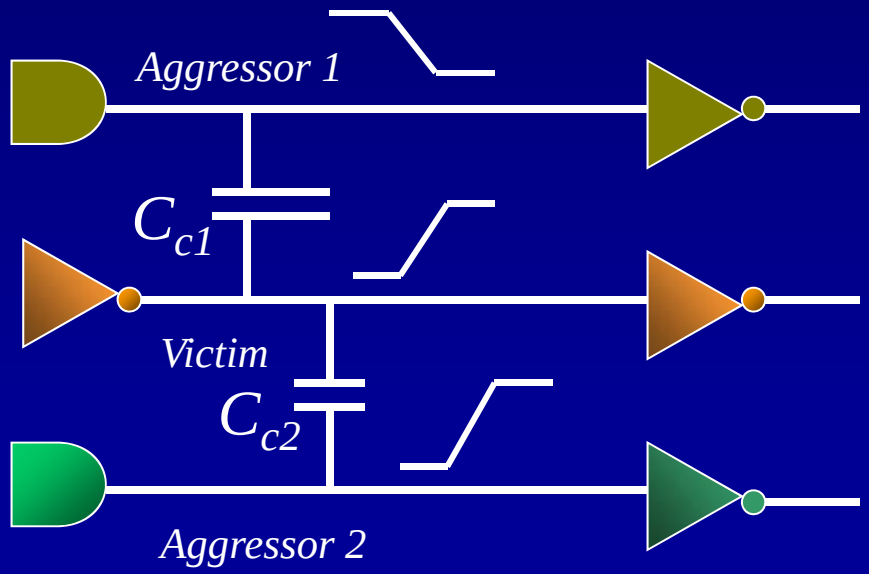


Building Block Layout – Contributions

- **Channel router (Yoshimura and Kuh)**
- **Prototype system developed**
- **Computational geometry and graph theory techniques applied to formulate and solve**
  - Channel definition and ordering
  - L-channel count minimization
  - Dynamic updating of global routing
  - Gridless router
- **Follow up**
  - Rubber-band routing
  - MCM routing

Interconnect Optimization
Wire Coupling and Crosstalk

- **Delay Noise: Increases/Decreases Delay**
- Can be controlled (mitigated) by
  - Spacing (detailed routing)
  - Global routing modification

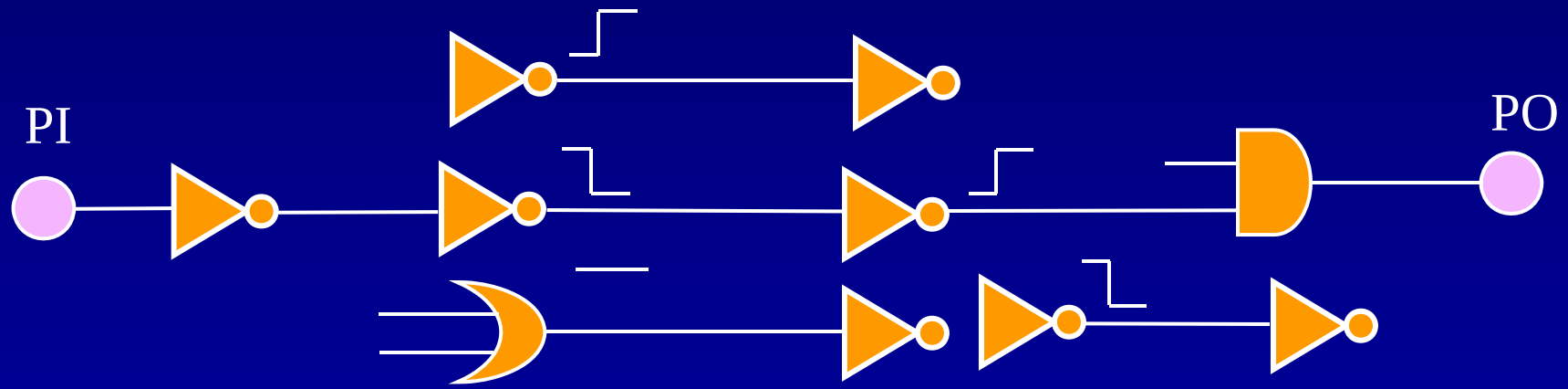


Spacing

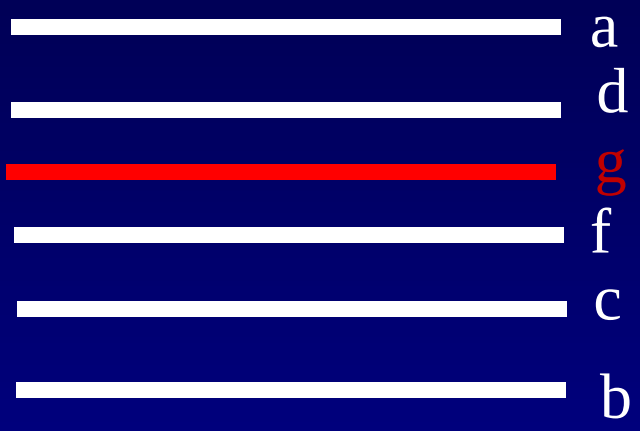
Net ordering

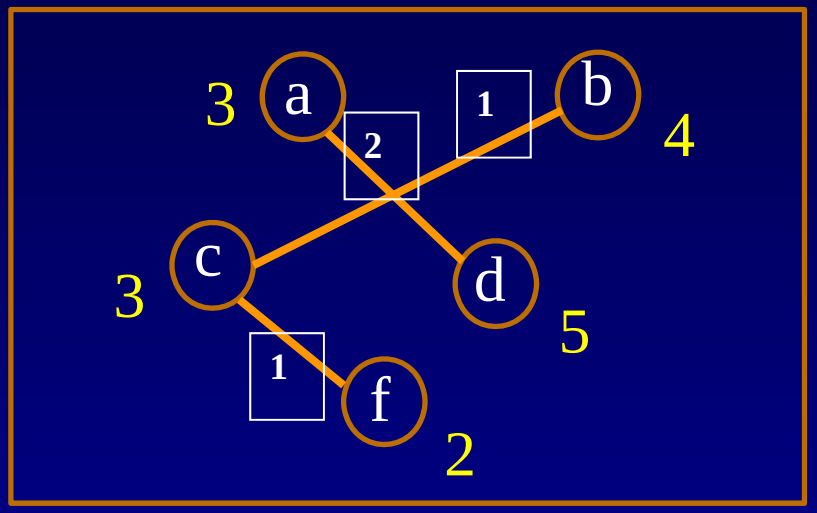
Static Timing Analysis

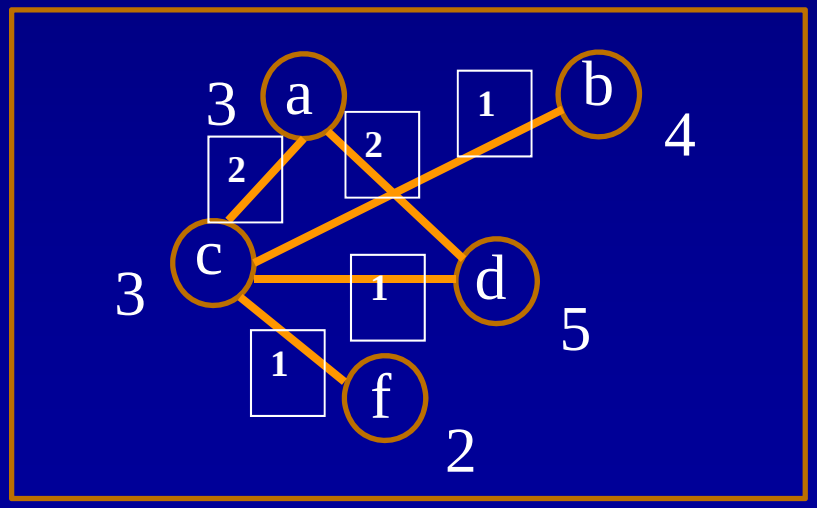
- Determines net sensitivity to coupling
  - Not all nets are sensitive to crosstalk
  - Region-based crosstalk risk bounds

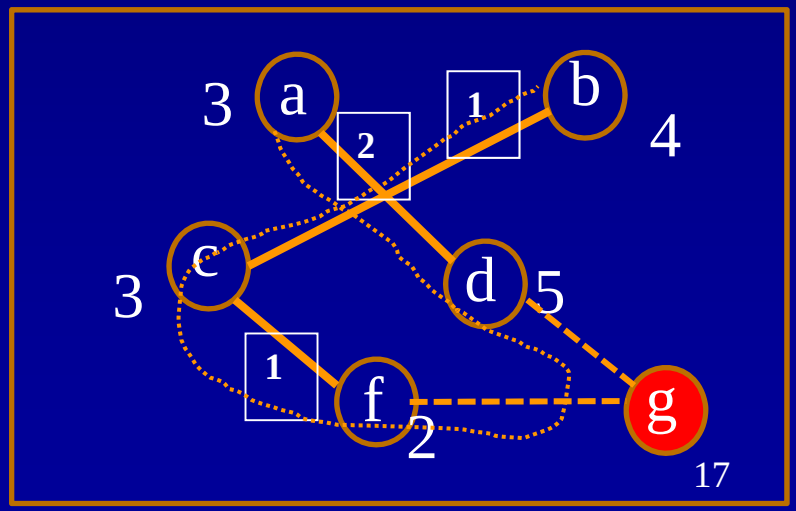


Coupling constraints within a region



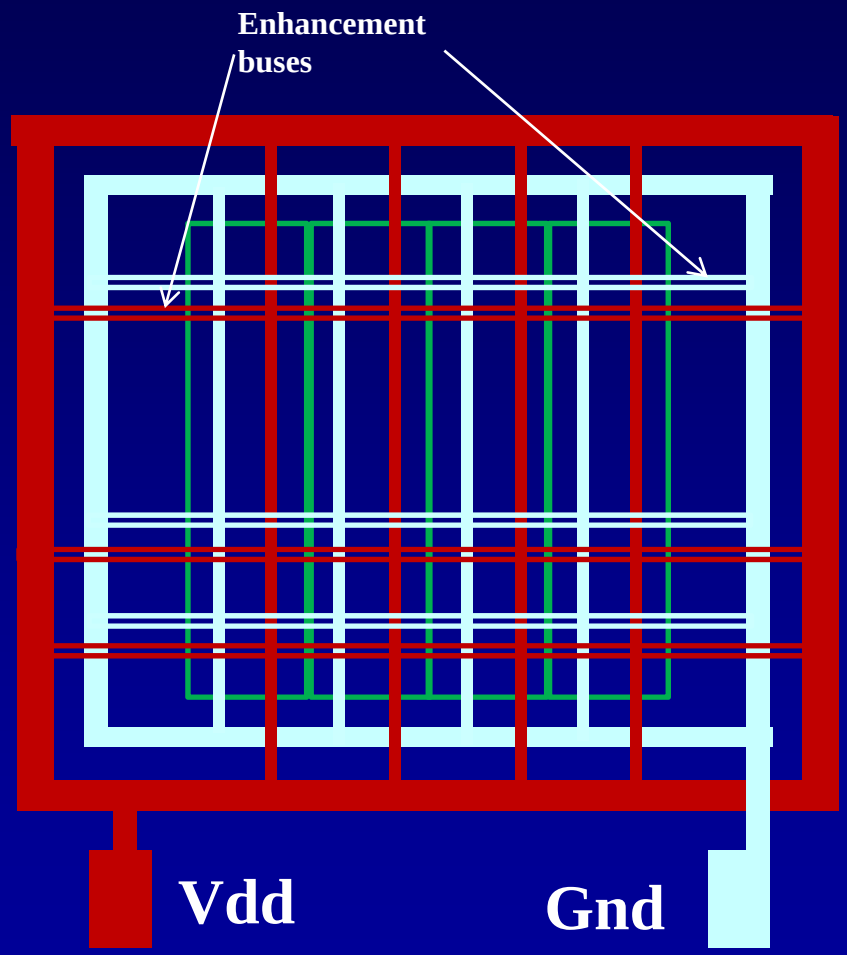






Interconnect Optimization
Power and Ground Nets

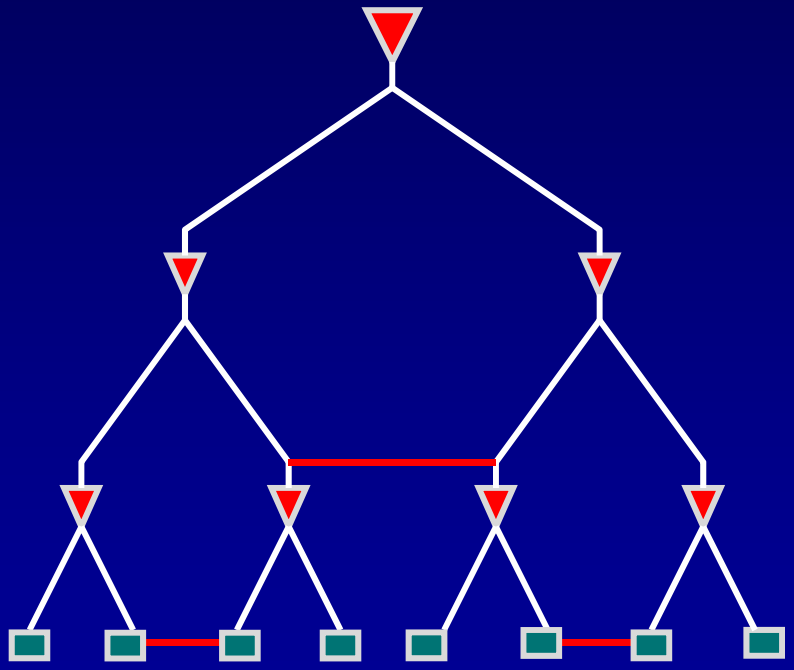
- **Formulation of an enhancement bus selection and sizing problem.**
- **Observation that adding a bus may cause local current crowding**
  - This problem has not been fully explained yet.



Clock Optimization

Multi-link insertion and wire sizing

- Performance improvement of an existing net topology after global routing.
- Detail analysis of the link insertion impact on maximum delay and skew of any arbitrary topology
- A link insertion and wire sizing algorithm that can achieve the best performance improvement.



Post-Routing Optimization: Contributions

- **Deep analysis of practical interconnect optimization problems including**
  - Cross talk reduction
  - Clock and power network topology optimization
- **Efficient optimization approaches proposed**
- **Many follow up works on**
  - Crosstalk reduction
  - Clock link insertion

Some (Still Open) Research Problems

- Routing Complexity/ Technology Scaling Implied Problems
  - Global Routing
- Routing for Manufacturability
- Routing for ECO and Debugging
- Power Grid Topology Optimization
- Routing for New Transistor Technologies