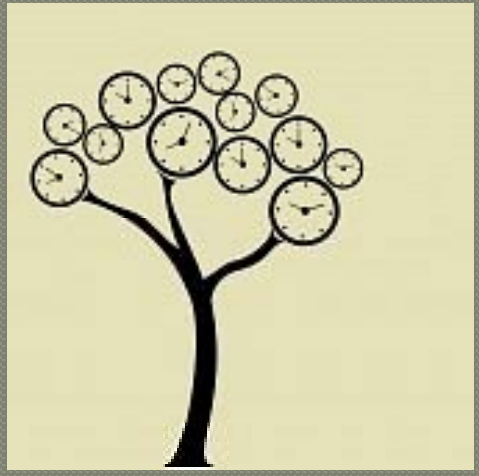
From Academic Ideas to Practical Physical Design Tools

Ren-Song Tsay

ISPD, March 2011

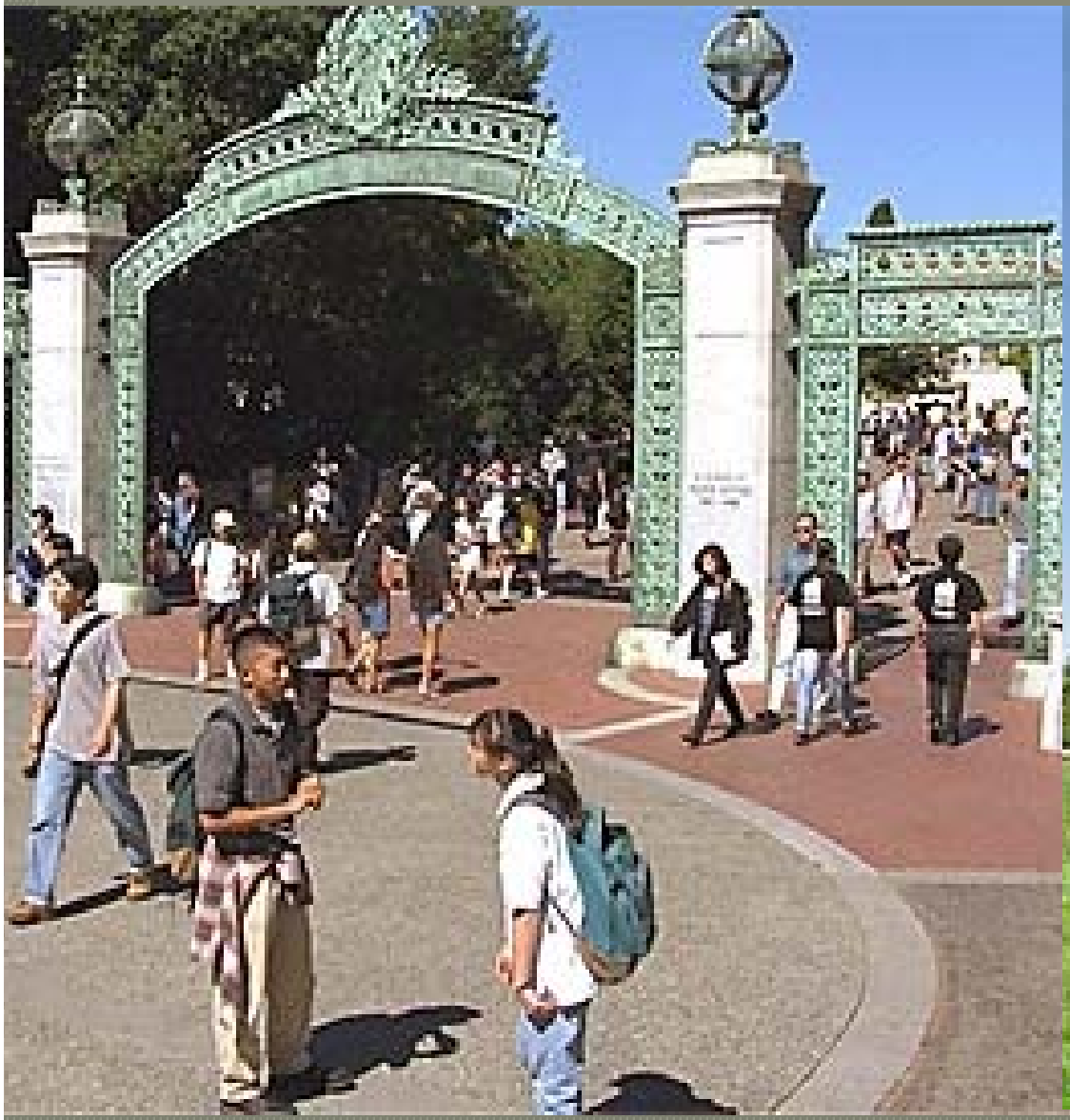


My Family

Logos Embedded System Design Automation Lab

National Tsing-Hua University, Taiwan

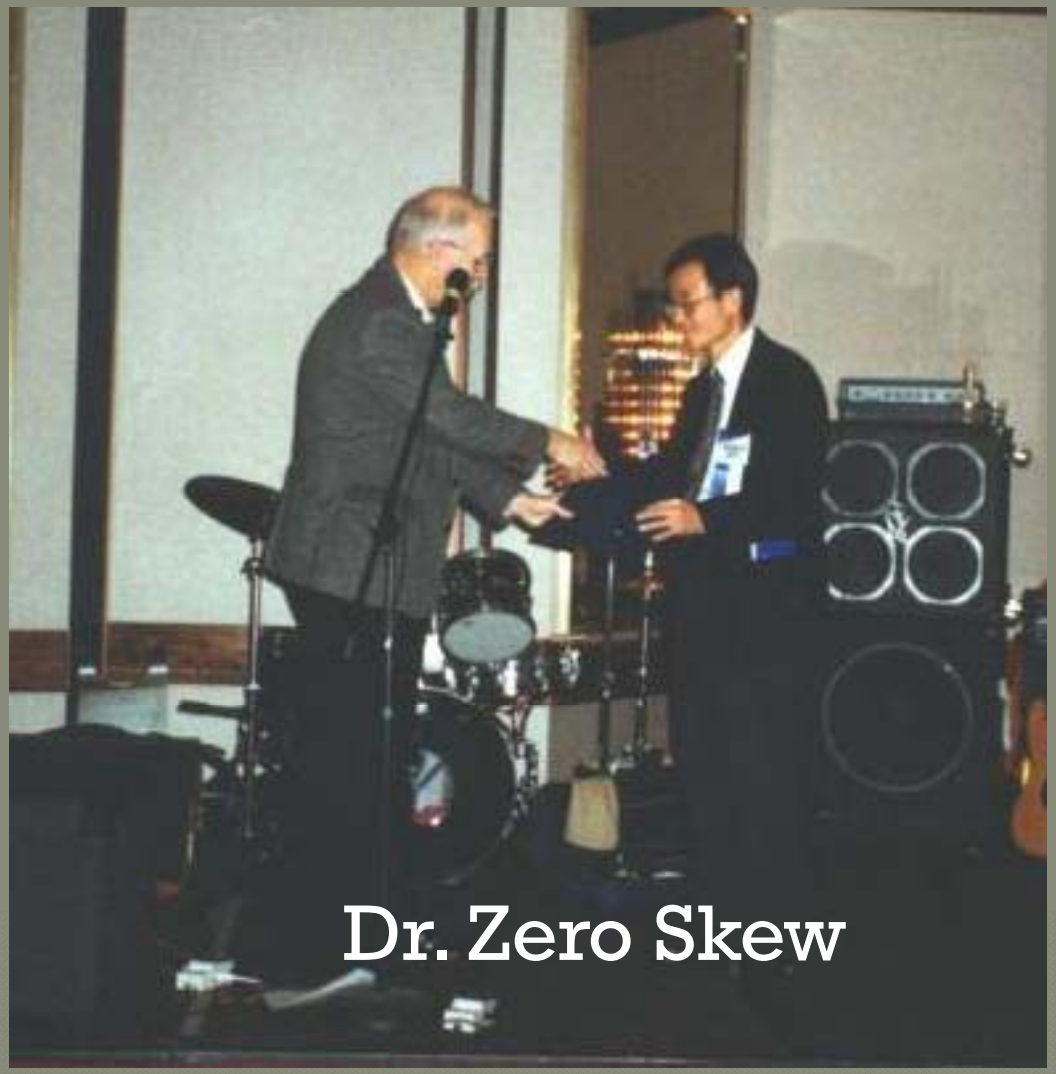
UC Berkeley

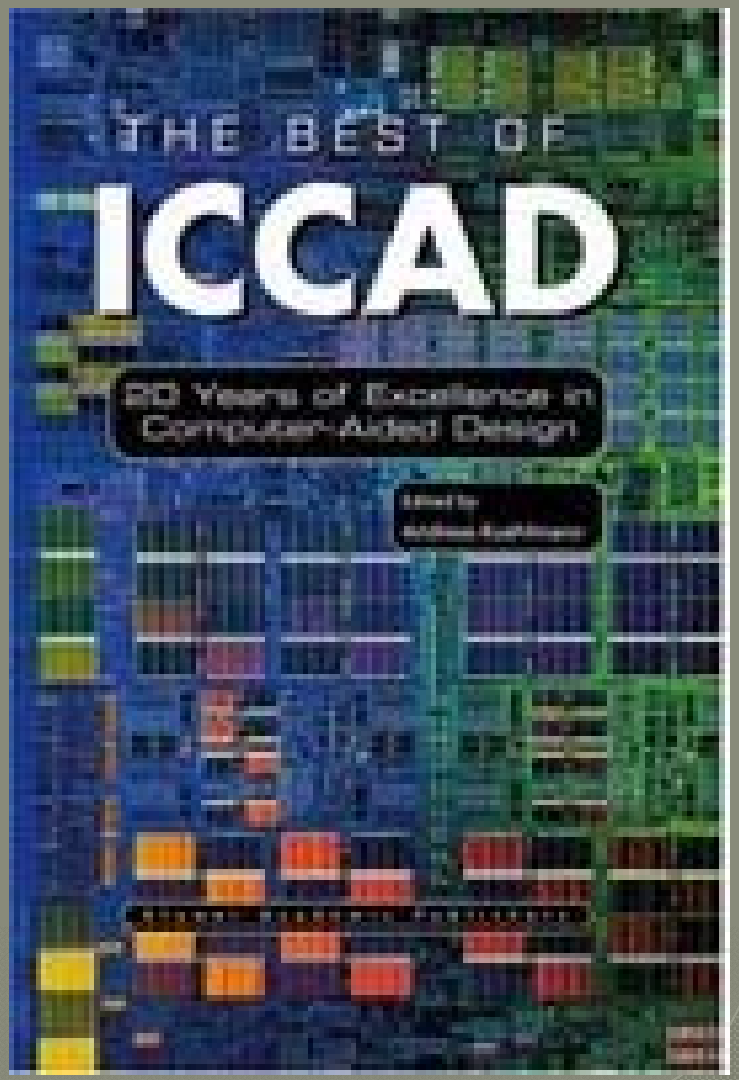


IBM T.J. Watson Research Center

- Zero Skew Clock Routing
- PRIDE: Placement and Routing Integrated Design Environment

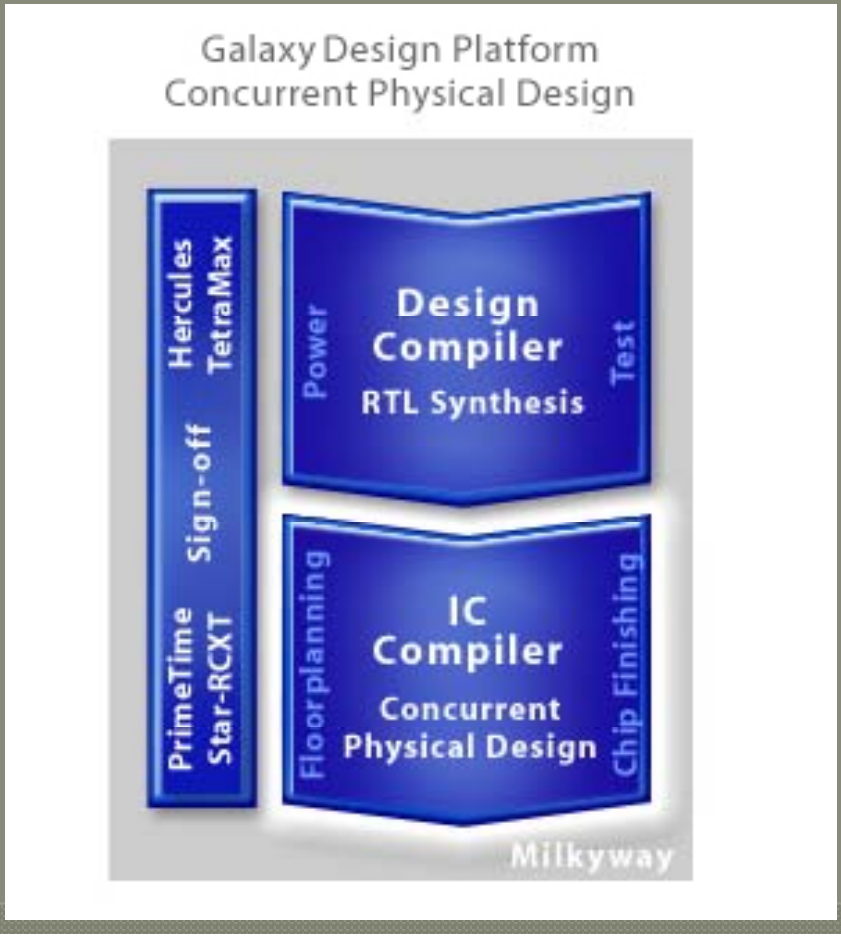
1994 IEEE Transaction CAD Best Paper Award

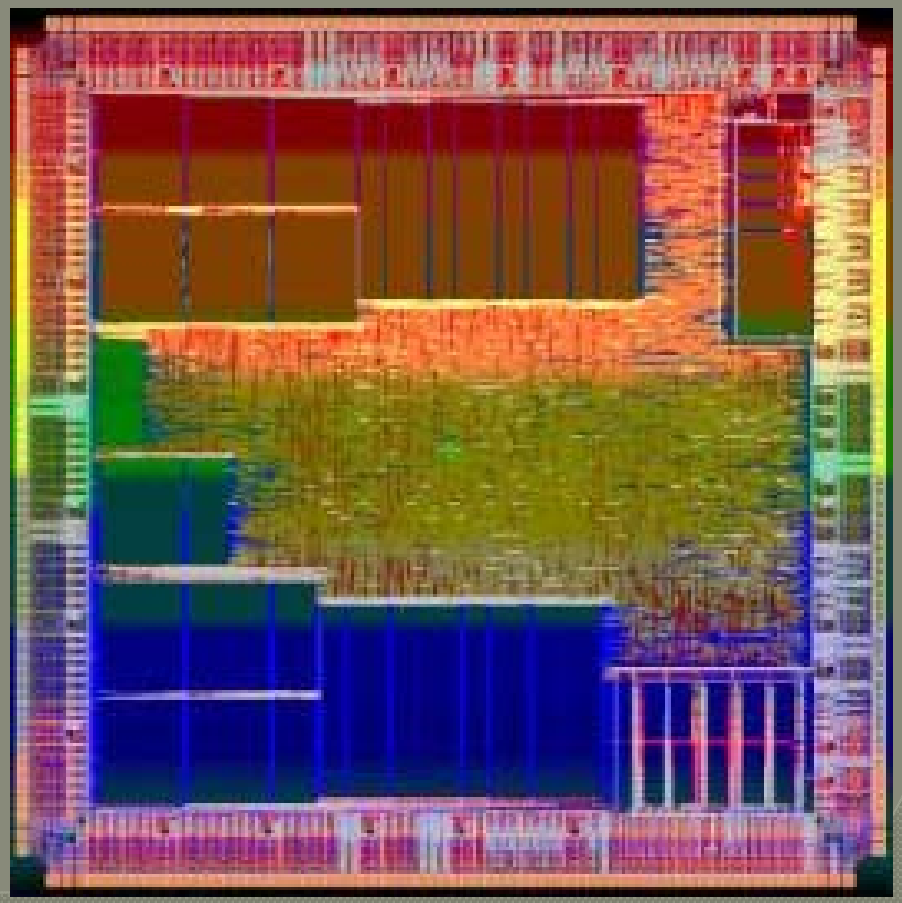




Physical Design System

- ArcGate – Astro: the first commercially successful performance optimization physical design system





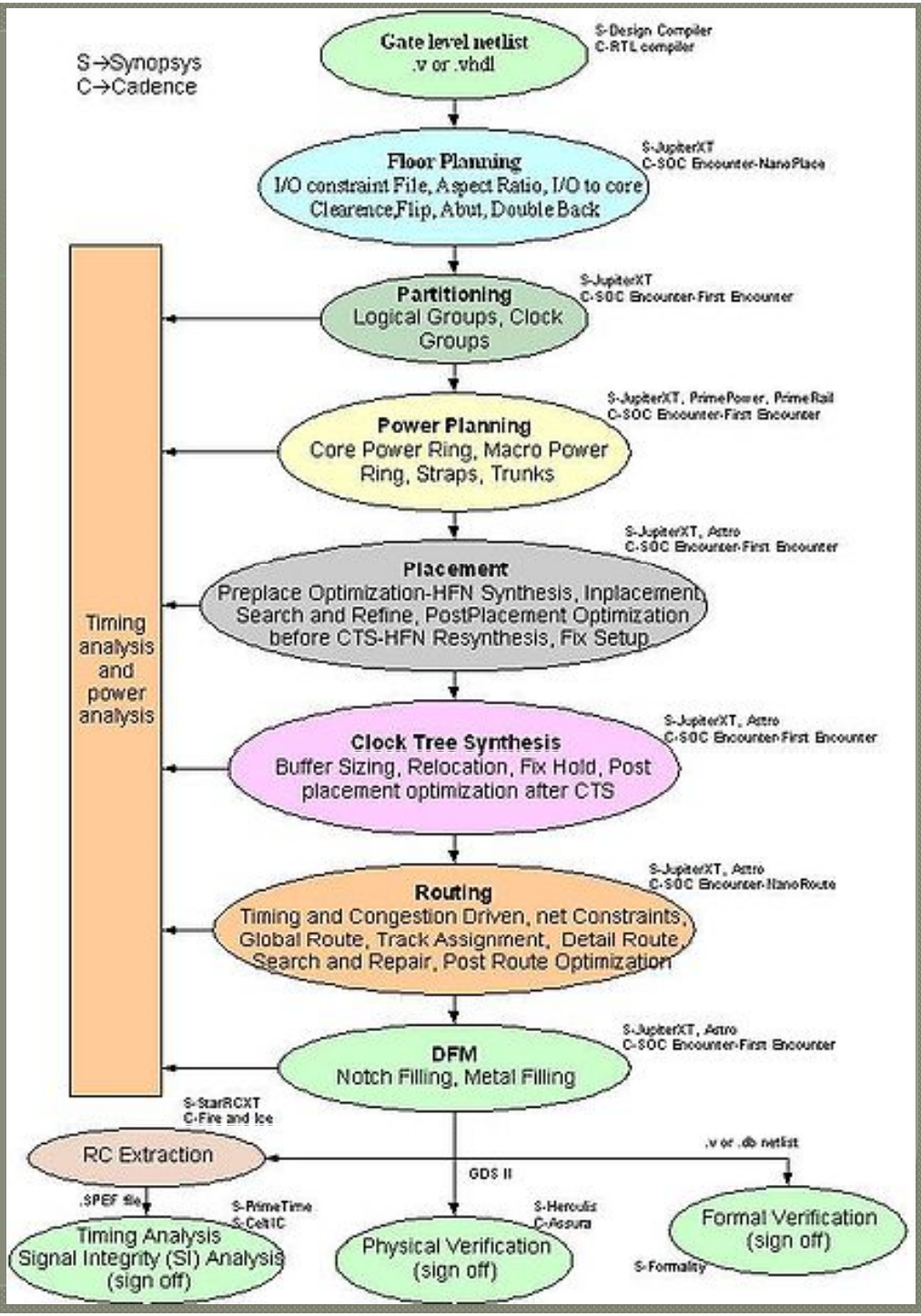
Reconfigurable Computer for Semulation

- a breakthrough logic verifications (Simulation/Emulation) system

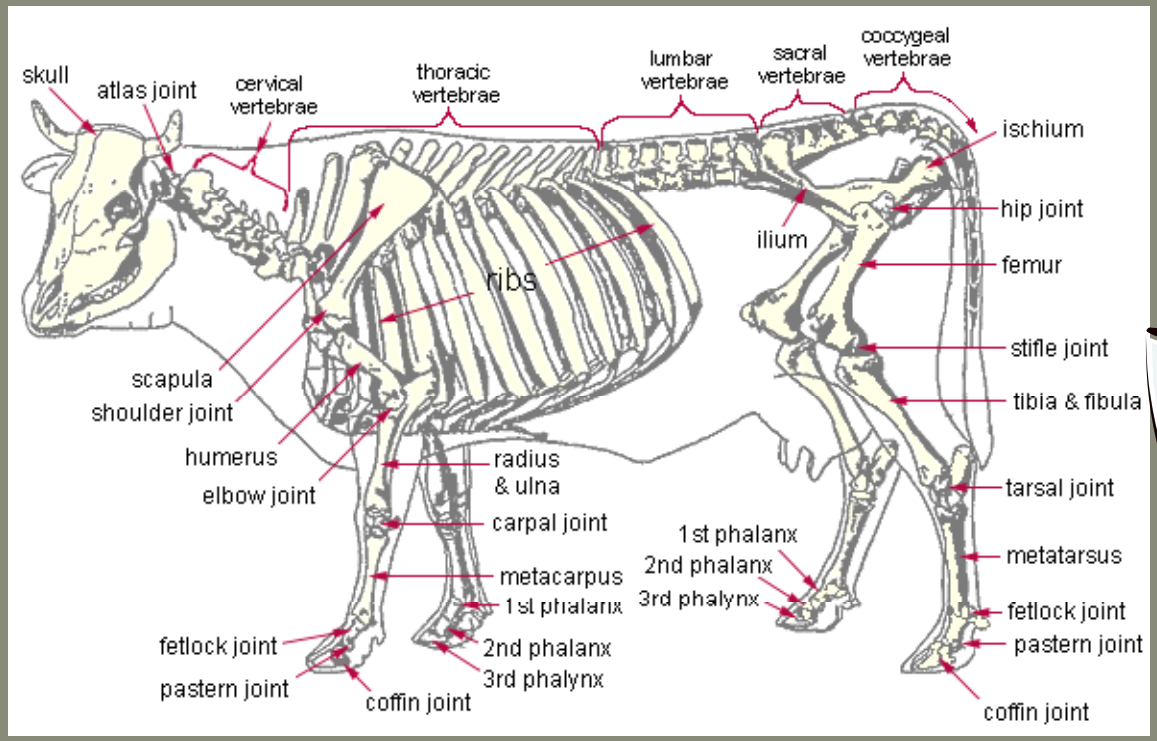
Axis systems

Cadence Incisive Xtreme series

Wiki Physical Design Flow



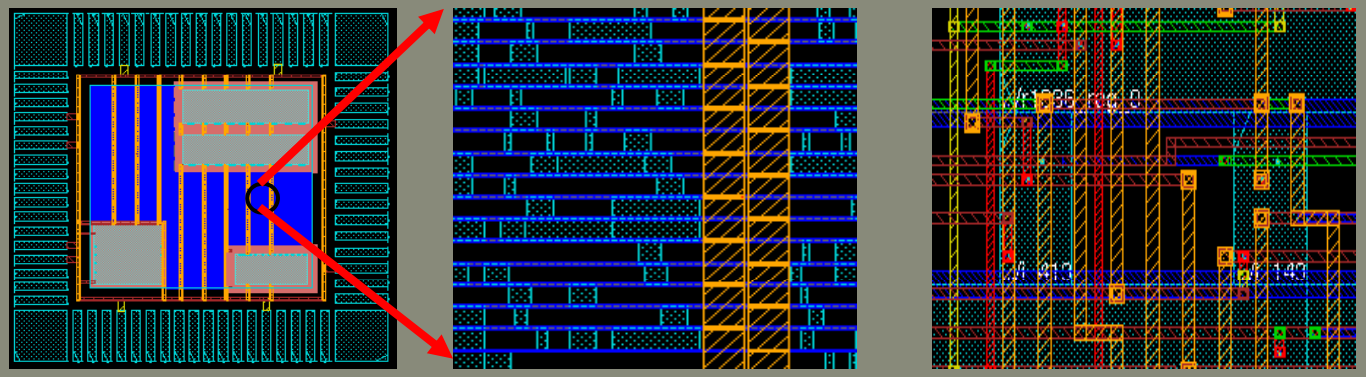
Pao-Ding


skull
atlas joint
cervical vertebrae
thoracic vertebrae
lumbar vertebrae
sacral vertebrae
coccygeal vertebrae
ischium
hip joint
femur
stifle joint
tibia & fibula
tarsal joint
metatarsus
fetlock joint
pastern joint
coffin joint
ilium
ribs
scapula
shoulder joint
humerus
elbow joint
radius & ulna
carpal joint
metacarpus
1st phalanx
2nd phalanx
3rd phalynx
1st phalanx
2nd phalanx
3rd phalynx
fetlock joint
pastern joint
coffin joint

Physical Design Optimization

Physical Design Optimization

- Routability
  - No design rule violations
- Performance
  - clock period
  - Low power



Floorplan Placement Routing

A Progressive Design Methodology

Conventional Approach:

Placement **Global Routing**

Detailed Routing

ArcGate Approach:

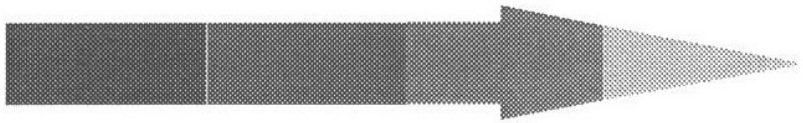
Placement

Global Routing

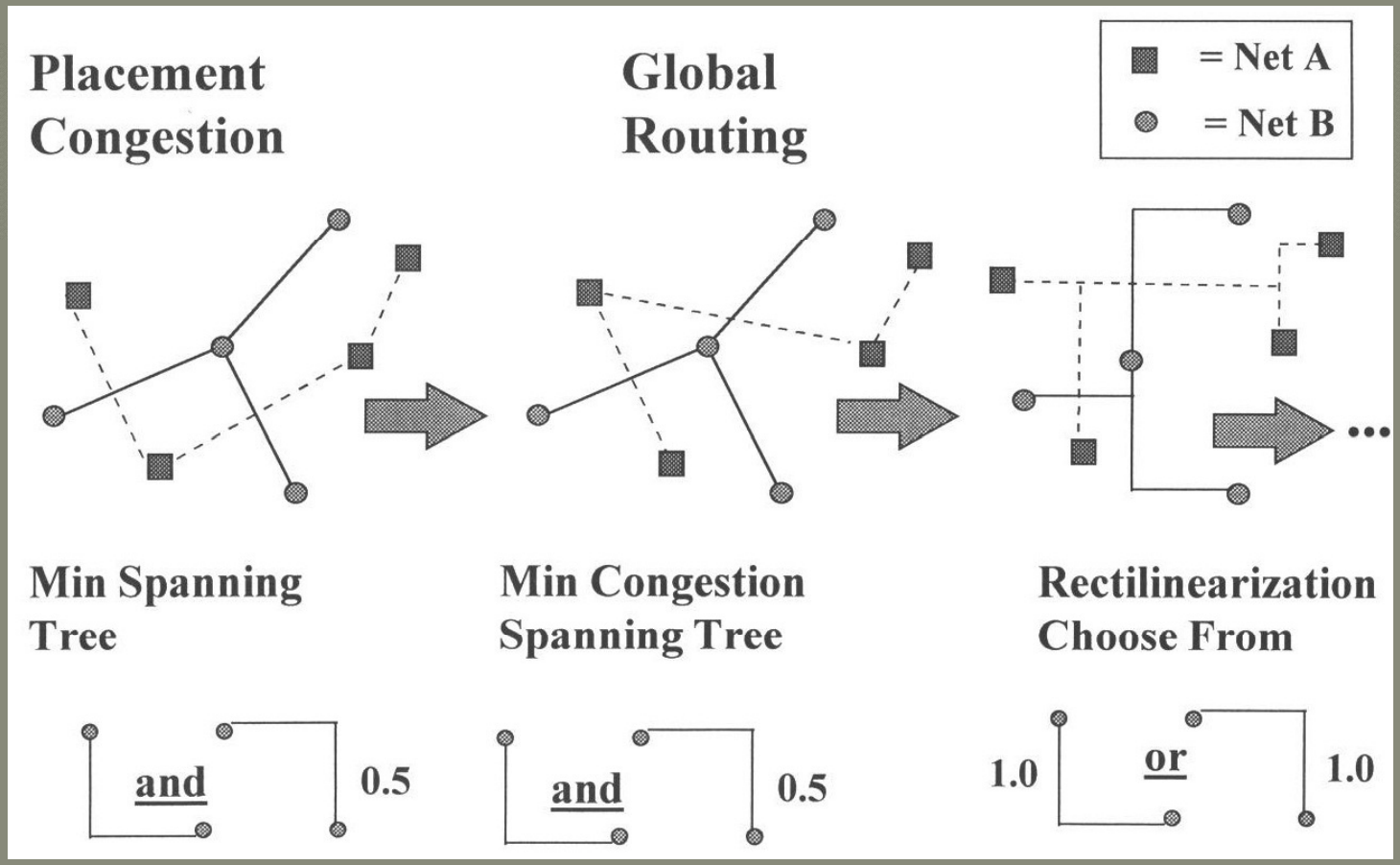
Intermediate Routing

Detailed Routing

- **Lookahead**
- **Feedback**



A Progressive Optimization Example



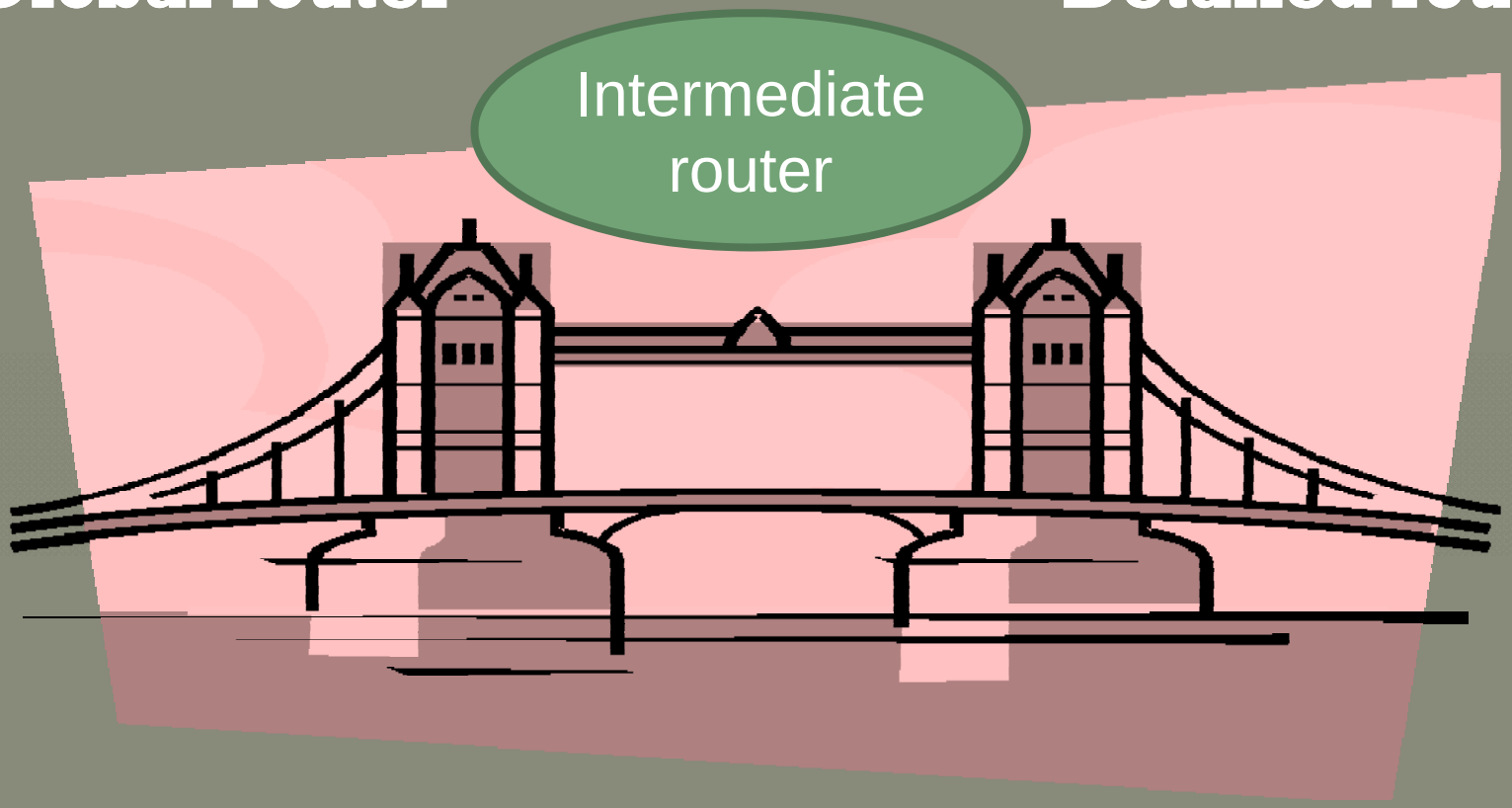
PROUD Quadratic Placement

$$\min\{L = \frac{1}{2}\sum_{i,\,j} c_{ij}(x_i - x_j)^2 \mid \forall n_{ij} \in N\}$$

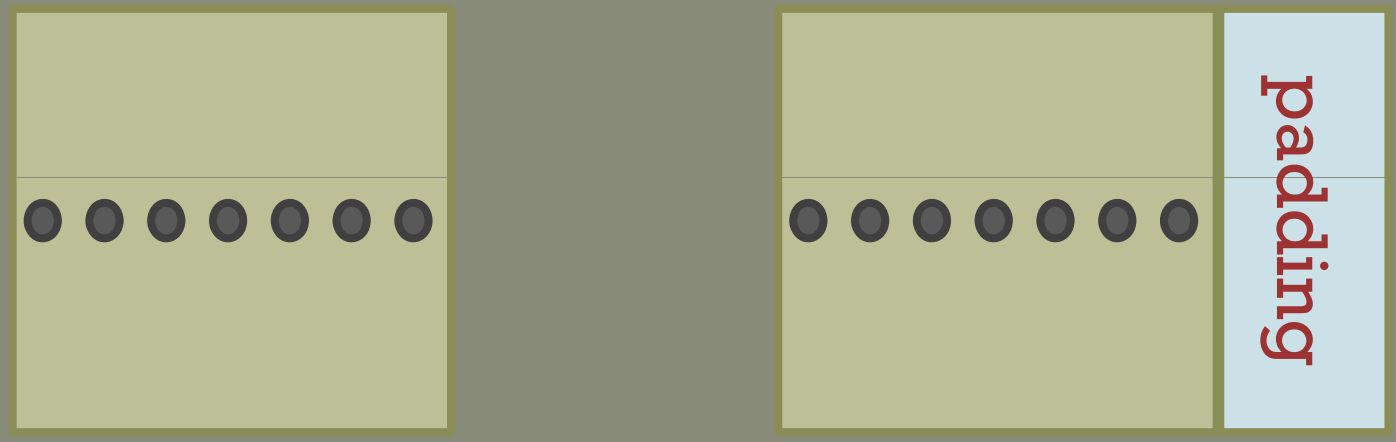
- Convex contour of the cost function
- Recursive partitioning
- Min-cut improvement
- First-order constraint
- Detailed placement improvement
  - Pair-wise interchange
  - Single cell movement
  - Rotation/flipping

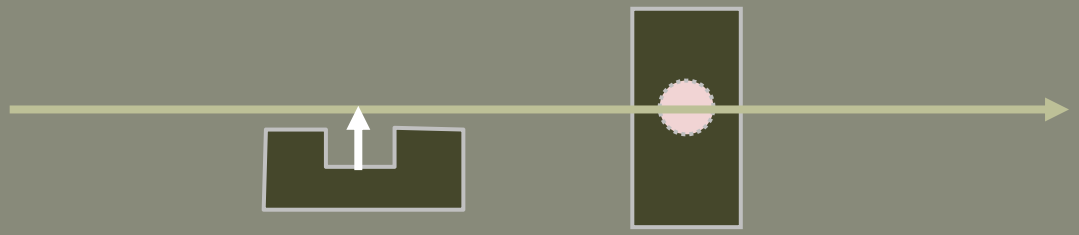
Progressive optimization

Global router **Detailed router**



Cell Porosity & Pin Access





Estimate Chip Height and Width

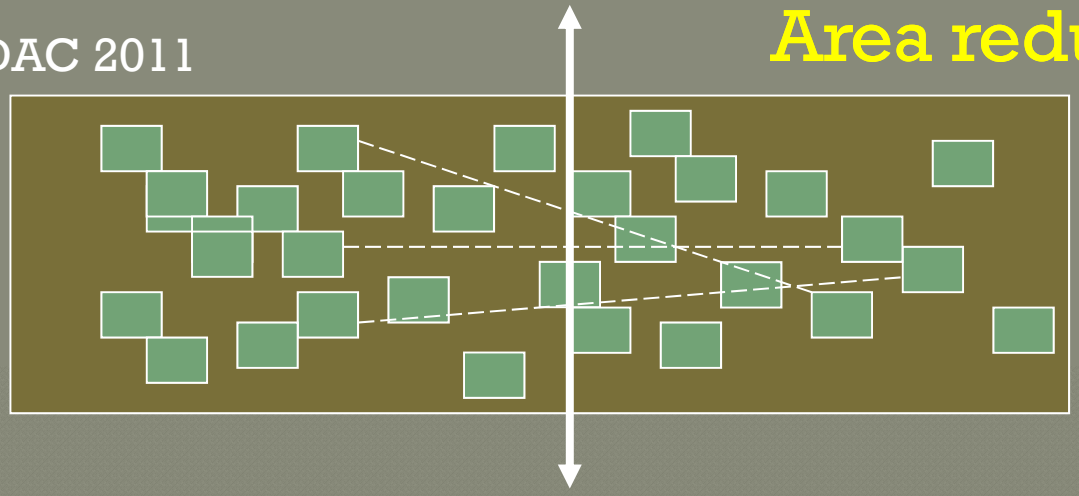
- The number of required routing tracks should satisfy H/V cut-demands
  - Height = D_h/L_h

The H demand on V cut

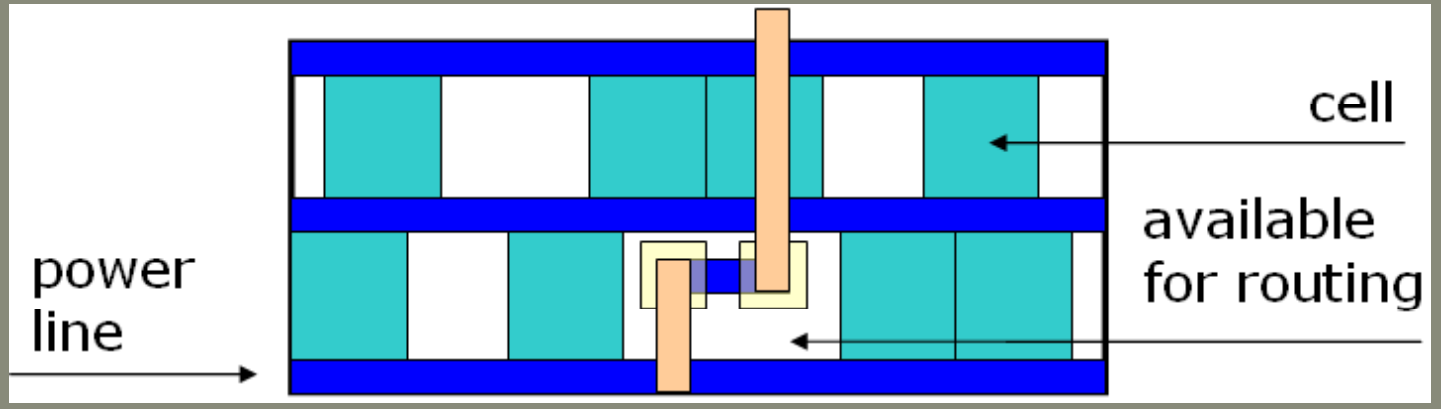
Number of H layers

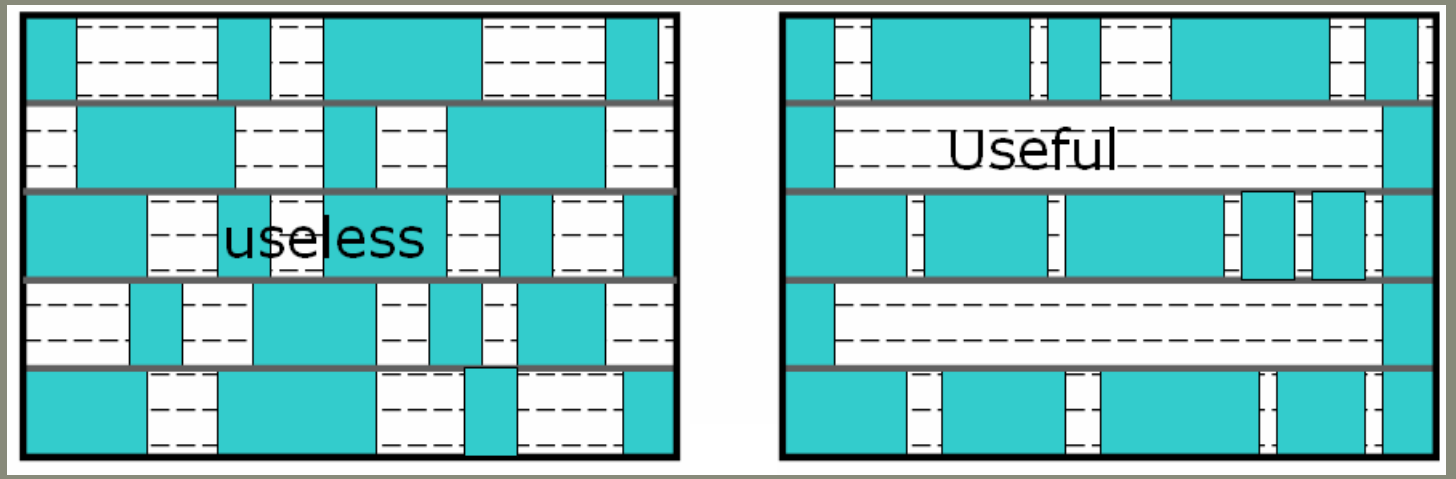
Chang, ASPDAC 2011

Area reduced 2~15%



Align Useful M1 Routing Tracks





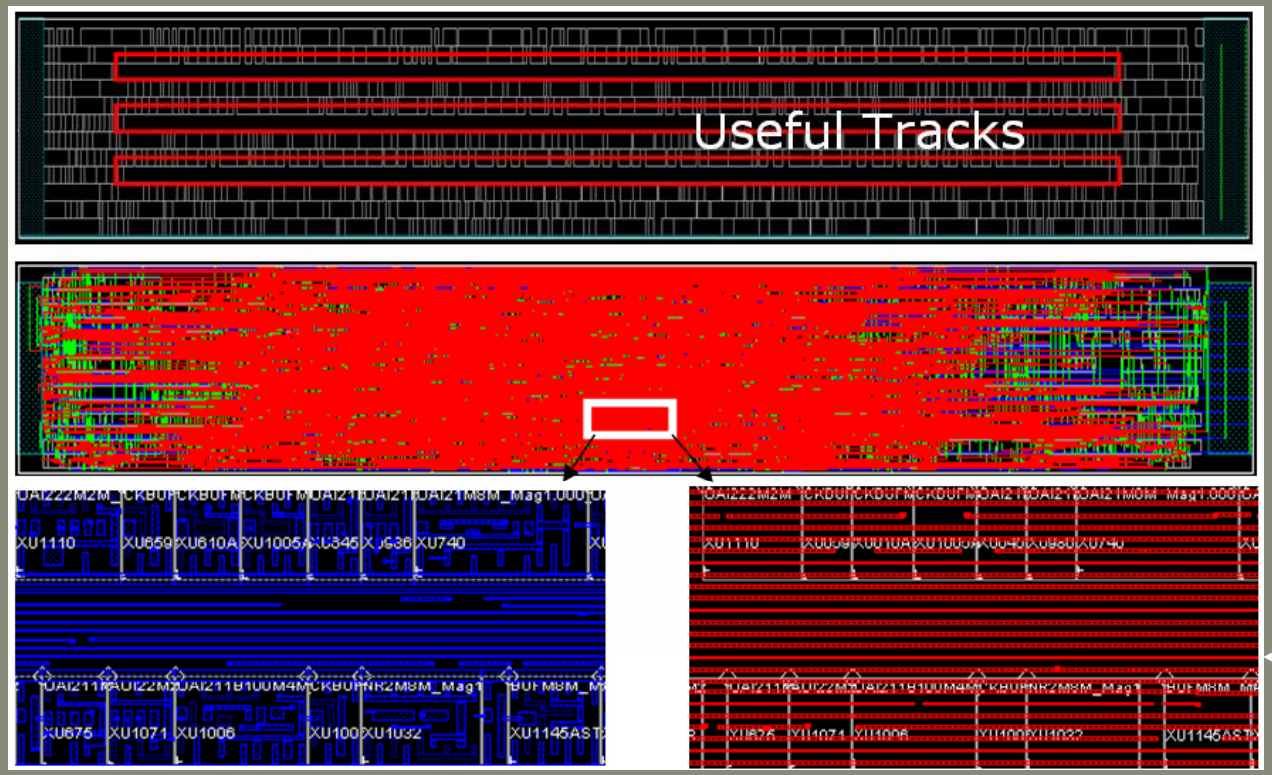
Runtime 5.3 x faster

A Test Result of M1 Alignment

"Useful" routing tracks →

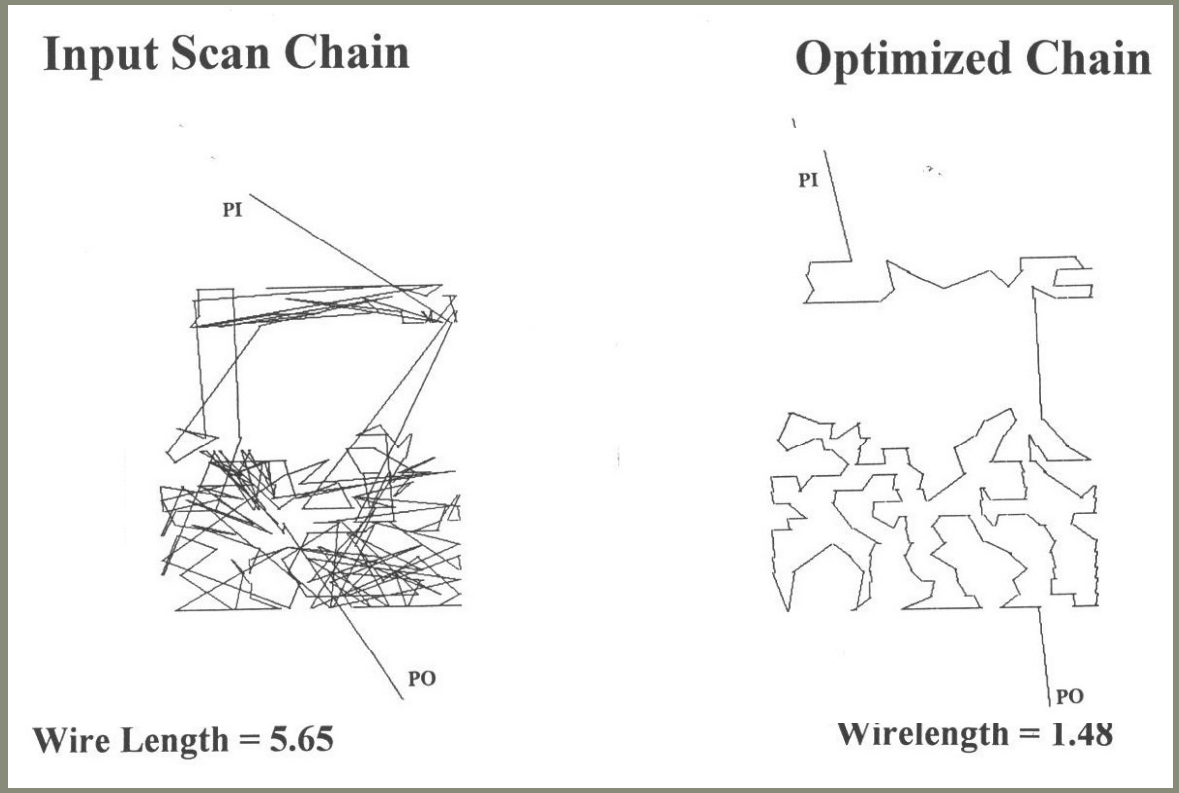
Layout results →

M1 →



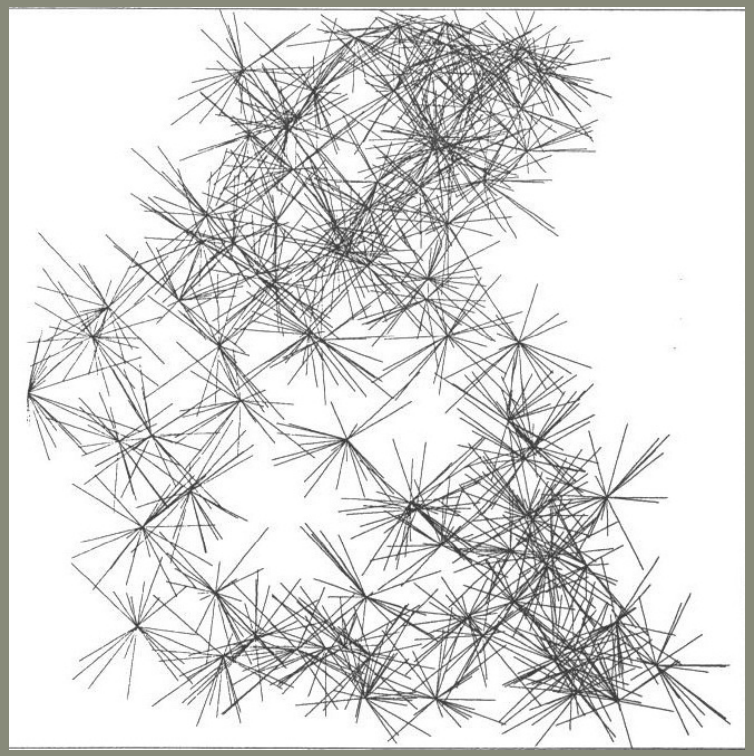
Scan Chain Optimization

- Greatly improve wirability and timing performance

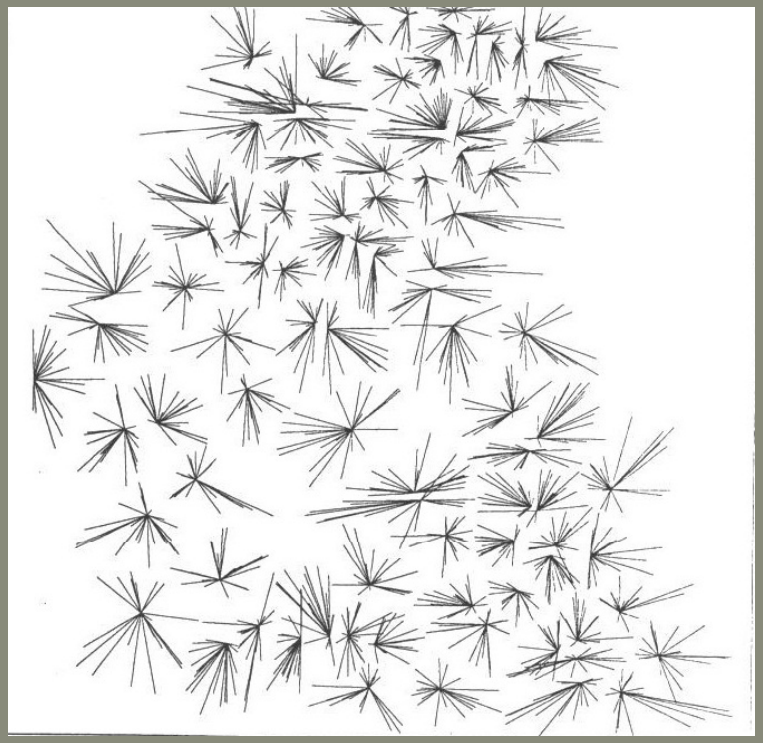


Optimal Clock Tree Synthesis

- Balance wire, load and phase delays (of macros)



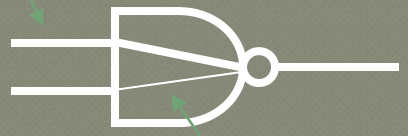
Before optimization



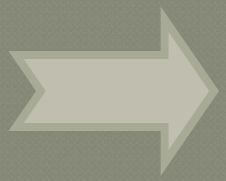
After optimization

LEQ Port Optimization

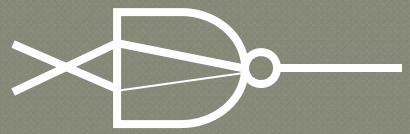
Critical path



Faster edge

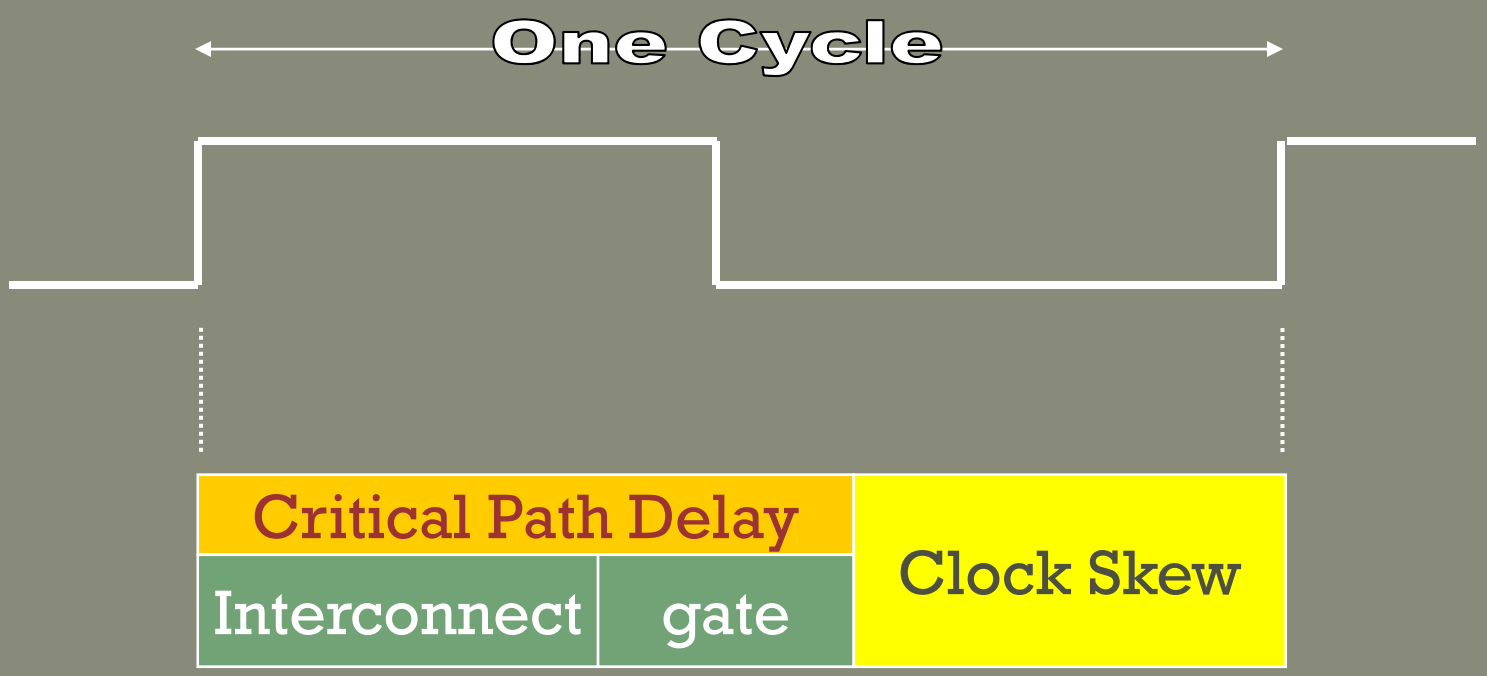


Switch to faster internal edge



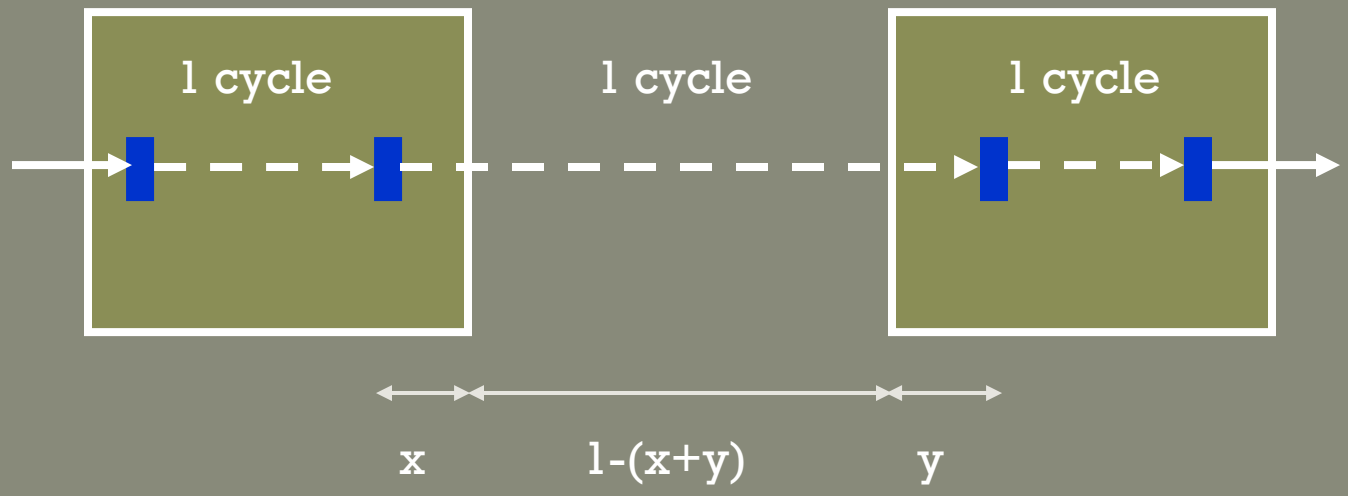
Timing Optimization

Timing-Driven: Min Cycle Time



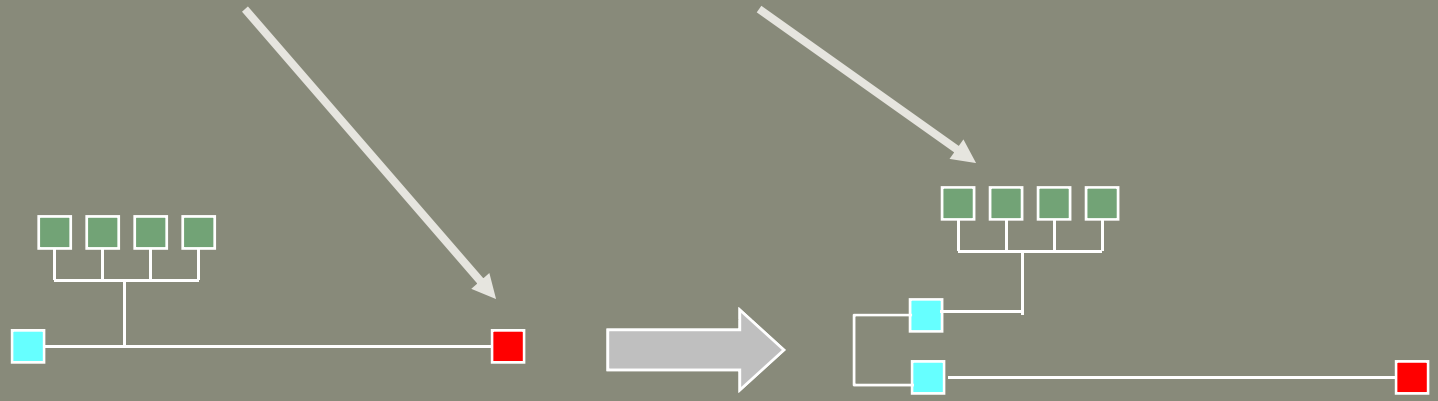
Design Plan Timing Budgeting

- Main issue: cross-macro timing paths

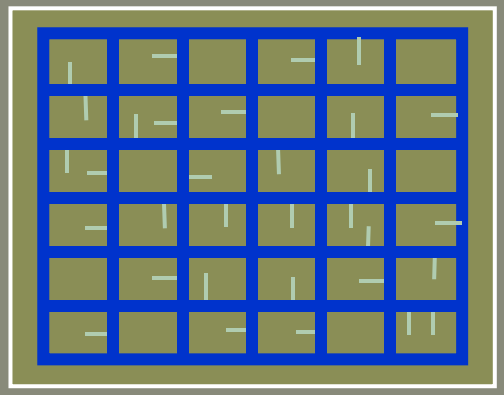


Net Splitting

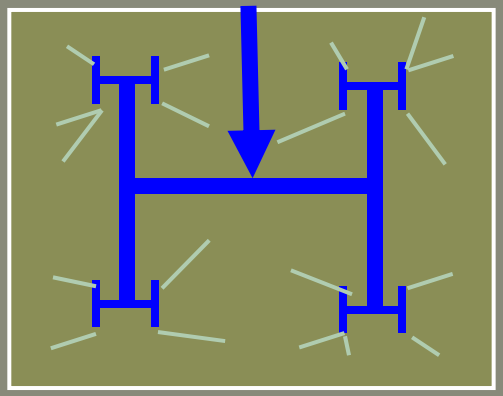
- Separate critical from non-critical group



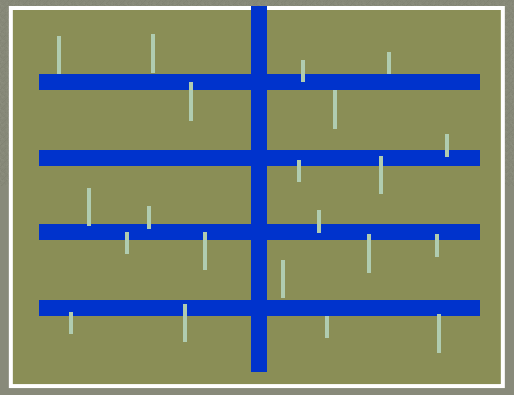
Clock Network Styles



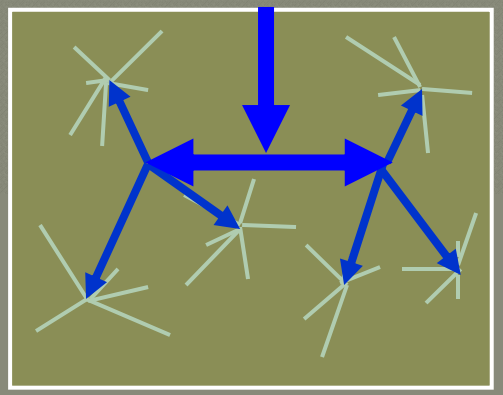
Mesh



H-Tree



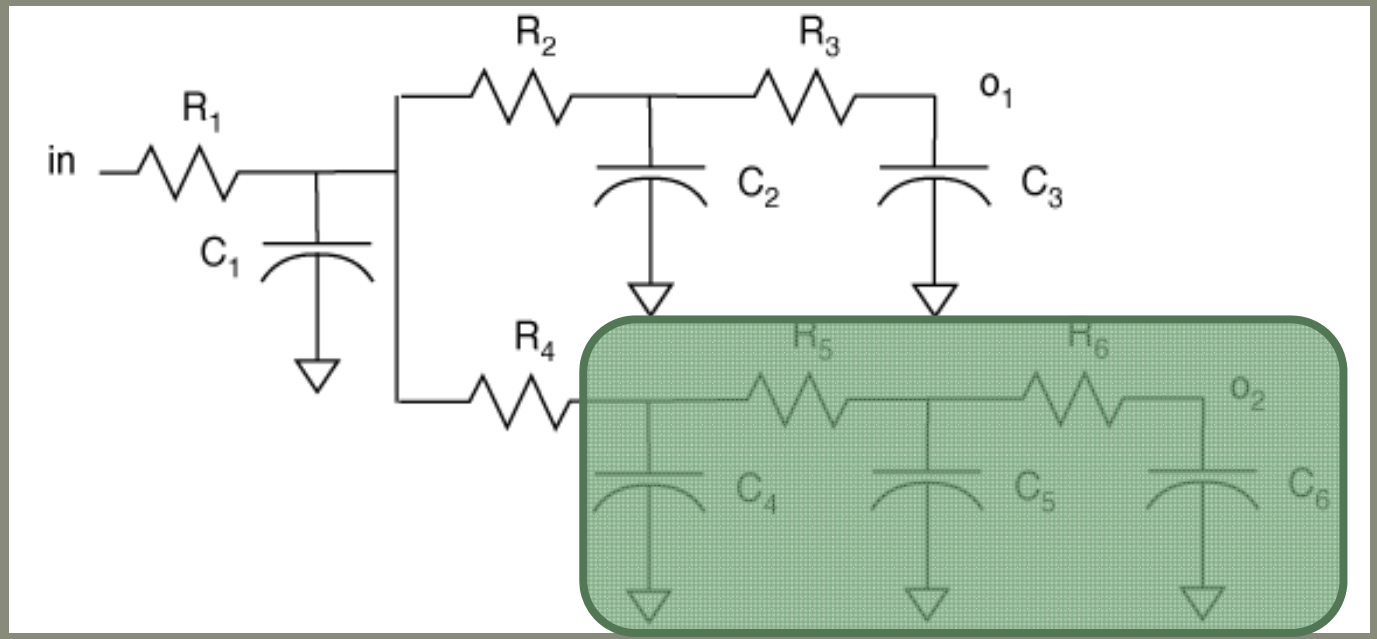
Trunk



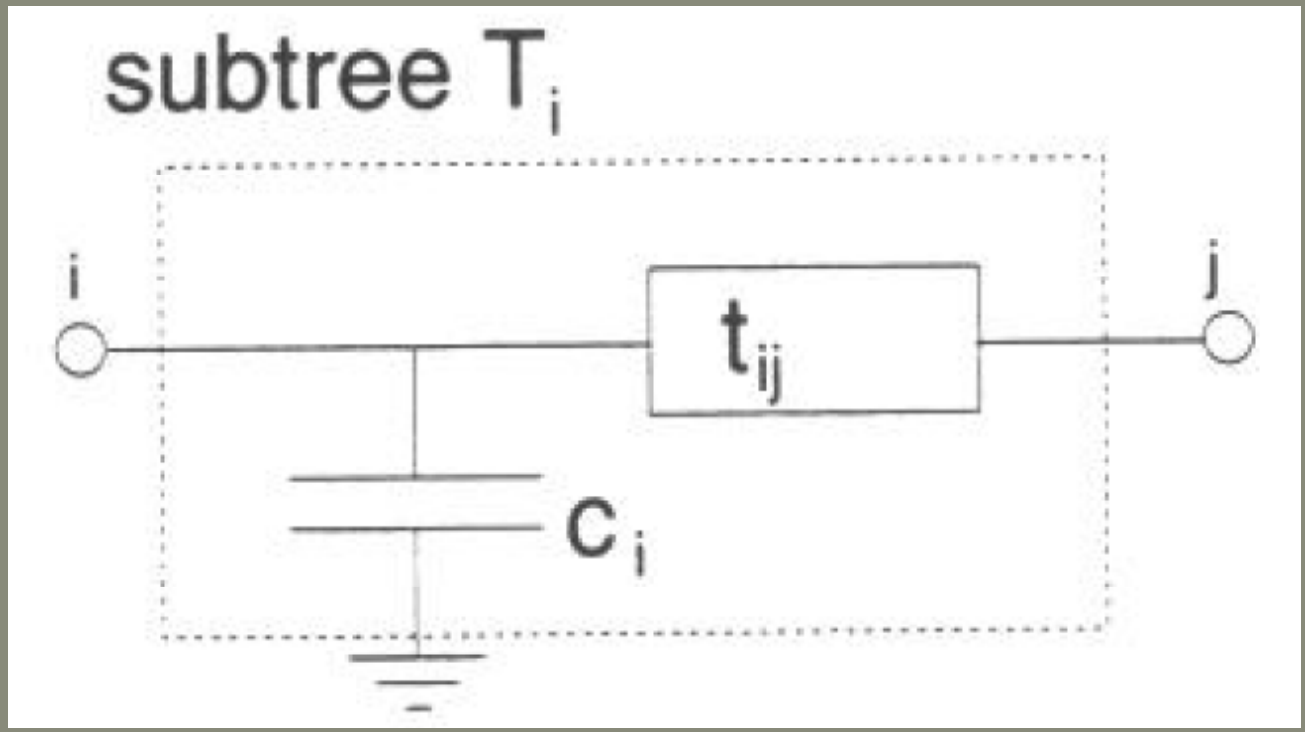
C-Tree

Elmore delay

- $t_4 = R_4(C_4 + C_5 + C_6)$
- $C_{eq} = C_4 + C_5 + C_6$



An equivalent lumped delay model of a clock subtree



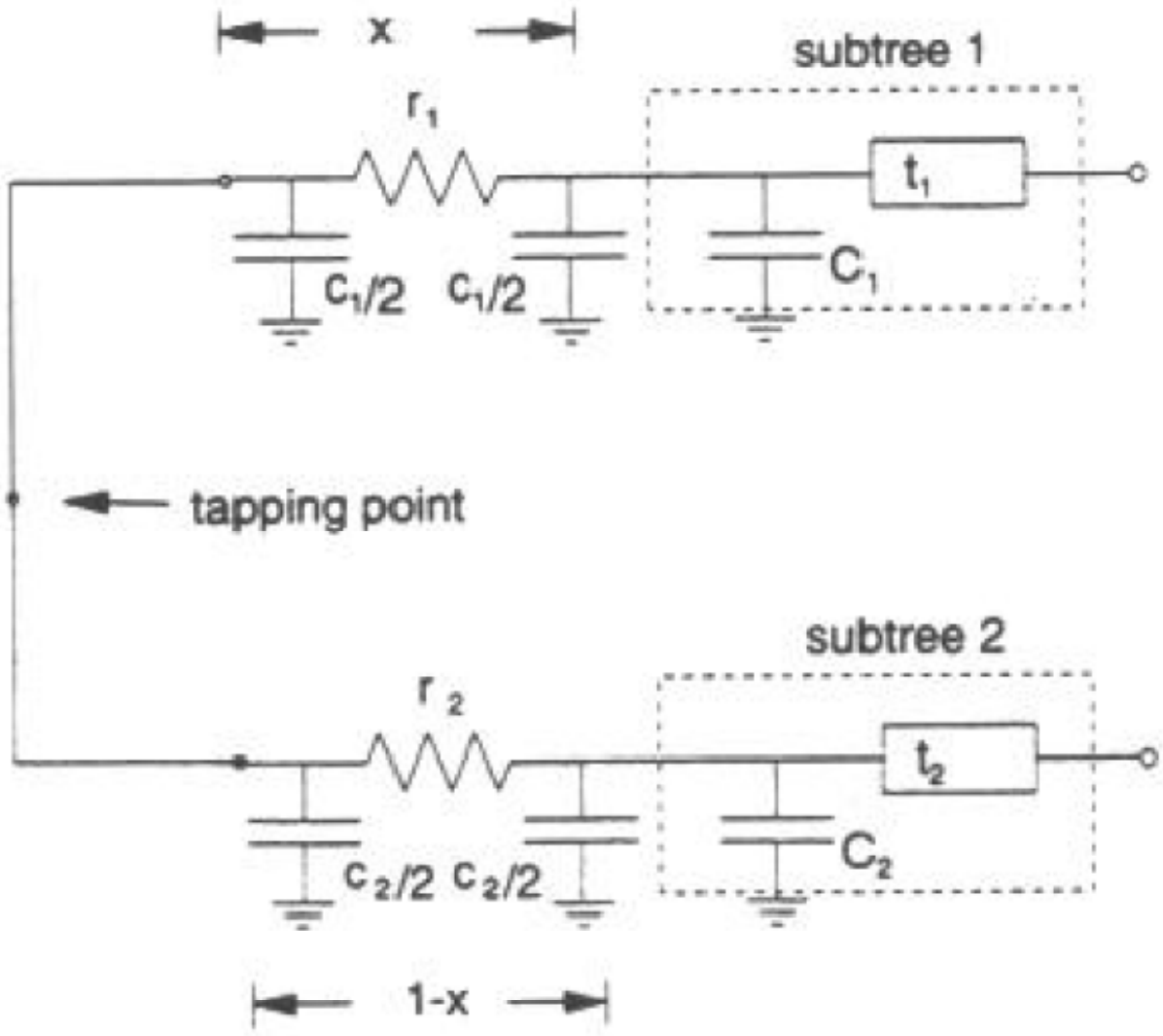


Fig. 5. *Zero-Skew Merge* of two subtrees.

Find Zero Skew Point

- Solve [r1=xl, r2 = (1-x)l]

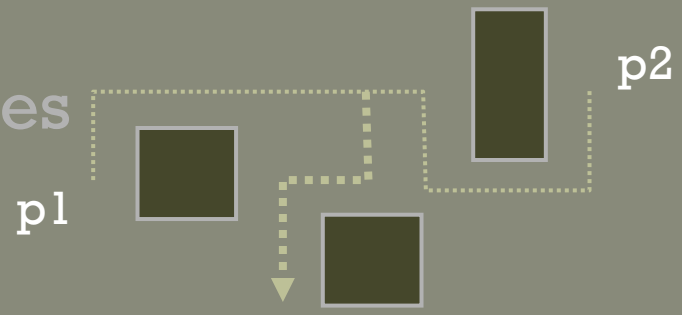
$$r_1(c_1/2 + C_1) + t_1 = r_2(c_2/2 + C_2) + t_2)$$

Get

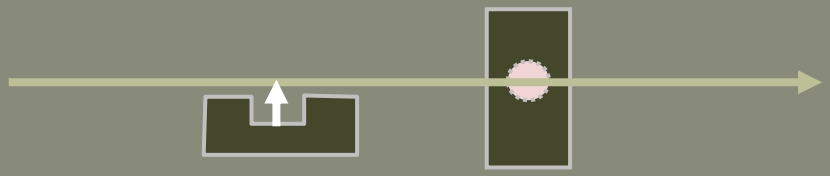
$$x = \frac{(t_2 - t_1) + \alpha l\left(C_2 + \frac{\beta l}{2}\right)}{\alpha l(\beta l + C_1 + C_2)}.$$

Practical Clock Route Consideration

- Routing Blockages
  - Instead of DME,
    generate a few routing choices



- Avoid Pin Access Blocking



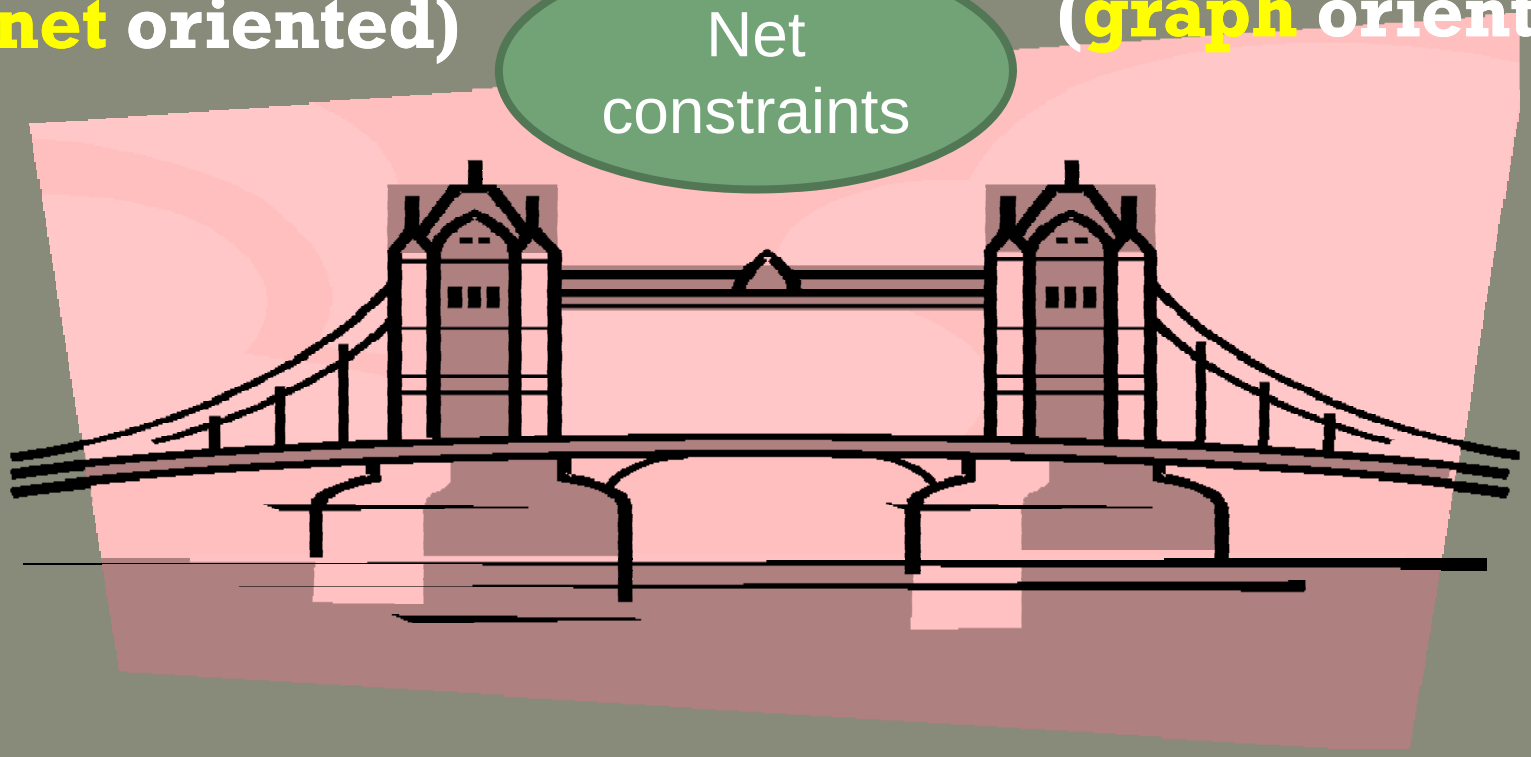
Timing Optimization

Bridging

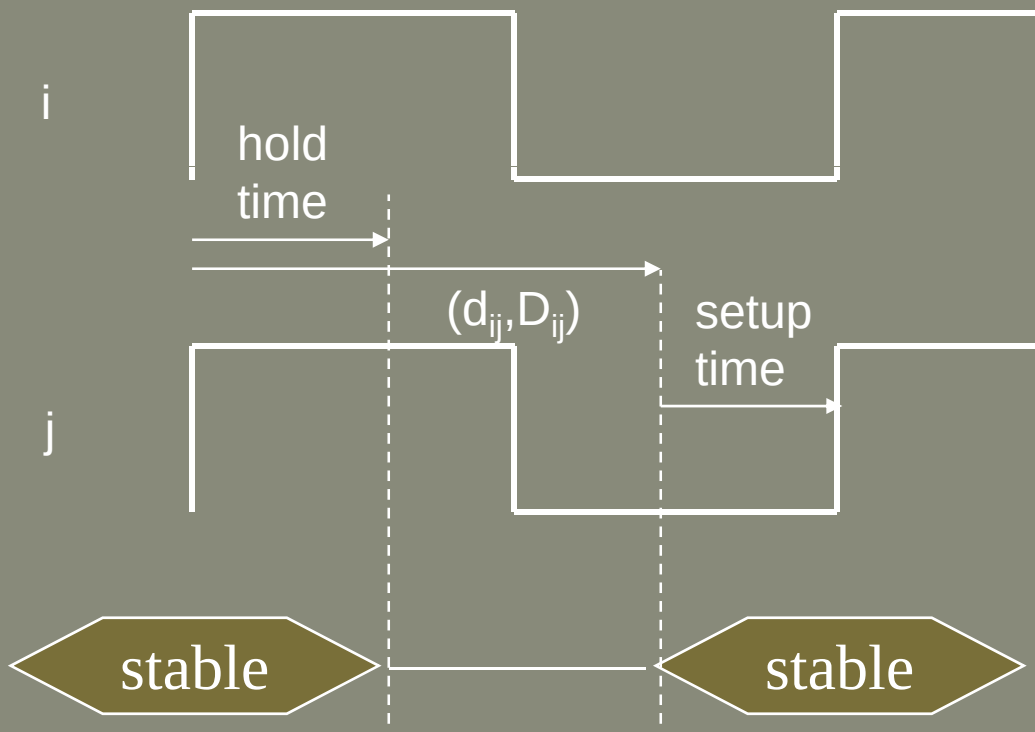
Physical Design (net oriented)

Timing Verification (graph oriented)

Net constraints



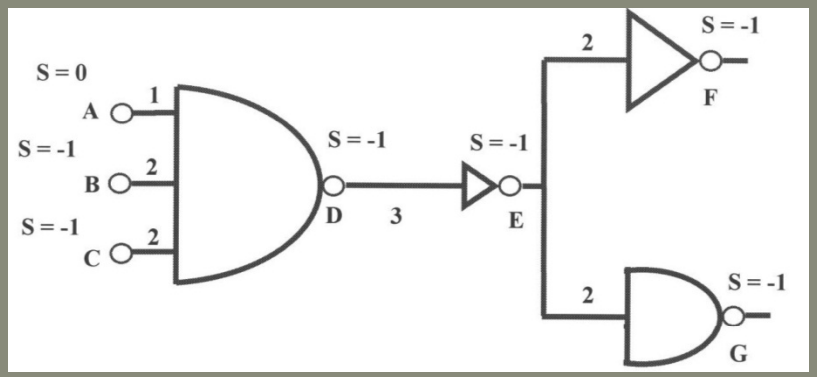
Timing Constraints

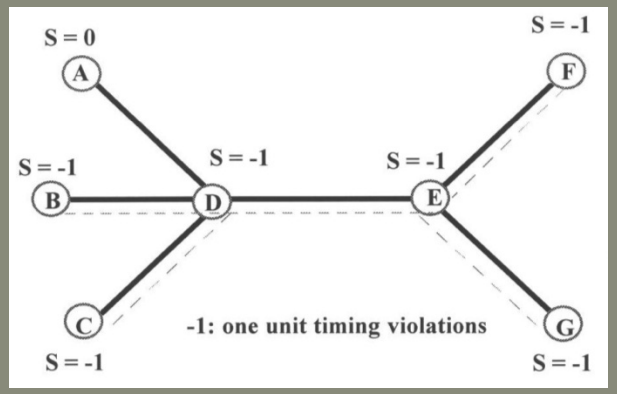


- EMTC
  d_{ij} > hold
- LMTC
  D_{ij} < T - setup

Timing Slack Graph

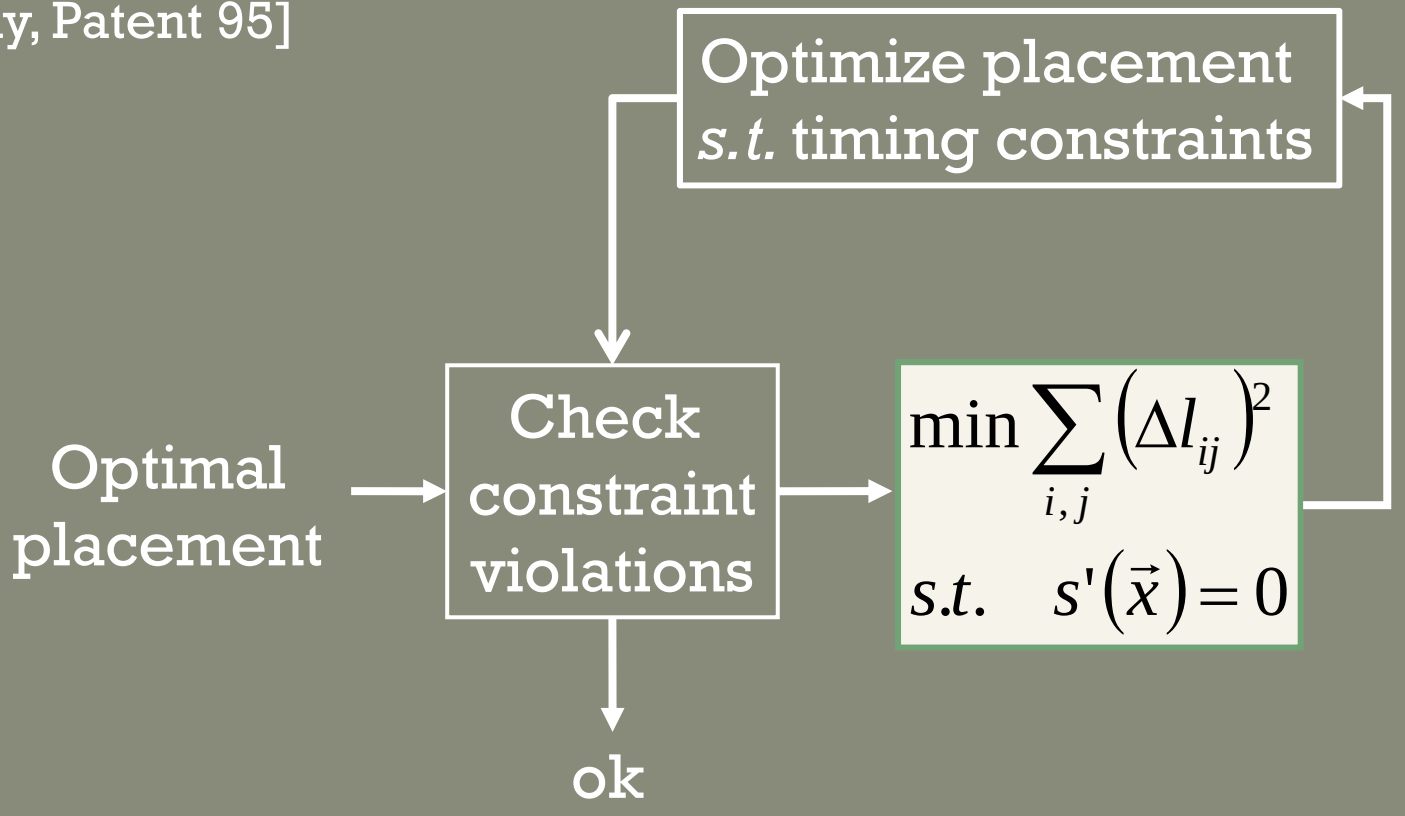
- A snap shot of the timing verification result in terms of a slack number on each pin and edge.
- It actually contains both timing and connectivity information.





TDP by Minimum Perturbation

[Tsay, Patent 95]



Slack and Delta Improvement

$$s_i = t_{ri} - t_{ai} \quad \ldots \quad \text{nodal slack}$$

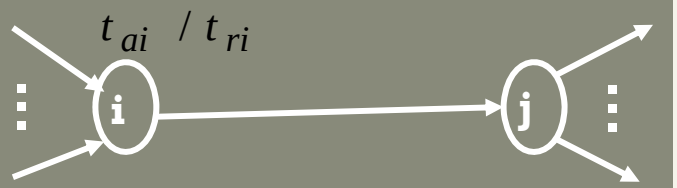
$$\mathrm{H_{ij}} = t_{rj} - \left(t_{ai} + d_{ij}\right) \quad \ldots \quad \text{edge slack, where } d_{ij} = \text{edge delay}$$

Define :

$$x_i = t_{ai} - t'_{ai} \quad \ldots \quad \text{arrival time improvement at node i}$$

$$y_j = t'_{rj} - t_{rj} \quad \ldots \quad \text{required arrival time improvement at node j}$$

Incremental Slack Calculation



$$s_i' = t_{ri}' - t_{ai}' = (t_{ri} + y_i) - (t_{ai} - x_i)$$
$$= (t_{ri} - t_{ai}) + (x_i + y_i) = s_i + (x_i + y_i)$$

similarly,

$$H_{ij}' = H_{ij} + x_i + y_j - \Delta d_{ij}$$

where,

$$d_{ij}' = d_{ij} + \Delta d_{ij}$$

Zero-Slack on Active Constraints

- At node i:

$$x_i + y_i + s_i = 0 \quad \Rightarrow \quad y_i = -\left(x_i + s_i\right)$$

- At edge ij:

$$x_i + y_j - \Delta d_{ij} + H_{ij} = 0 \quad \Rightarrow \quad \Delta d_{ij} = \left(x_i + H_{ij}\right) - \left(x_j + s_j\right)$$

Minimum Placement Perturbation

- Assume local placement change

$$\Delta l_{ij} = \Delta d_{ij} / \left(R_i c + r C_j \right)$$

- Hence

$$\min \sum_{i,j} \left(\Delta l_{ij} \right)^2 = \min \sum_{i,j} \left(\Delta d_{ij} / \left(R_i c + r C_j \right) \right)^2$$

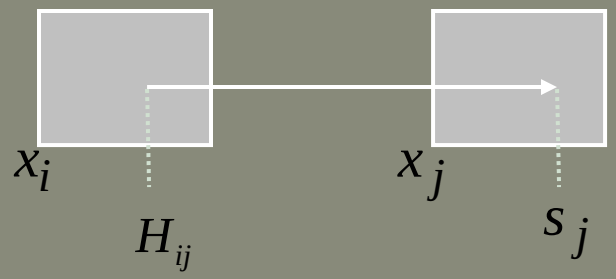
$$= \min \sum_{i,j} \frac{1}{\left(R_i c + r C_j \right)^2} \left[\left(x_j + s_j \right) - \left(x_i + H_{ij} \right) \right]^2$$

Equivalent to Quadratic Placement

$$min \sum_{i,j} (\Delta l_{ij})^2 = min \sum_{i,j} \frac{1}{D_{ij}^2} [(x_j + s_j) - (x_i + H_{ij})]^2$$

connectivity

Pin offset



* Then take $(l_{ij} + \Delta l_{ij})$ as the upper bound constraint

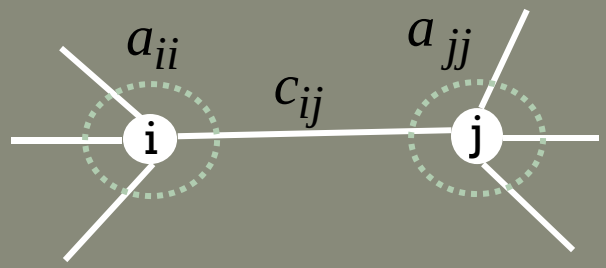
Net Weighting Placement Approach

$$\min\{L = \frac{1}{2}\sum_{i,j} c_{ij} x_{ij}^2 \mid x_{ij}^2 \le u_{ij}^2, \forall n_{ij} \in N\}$$

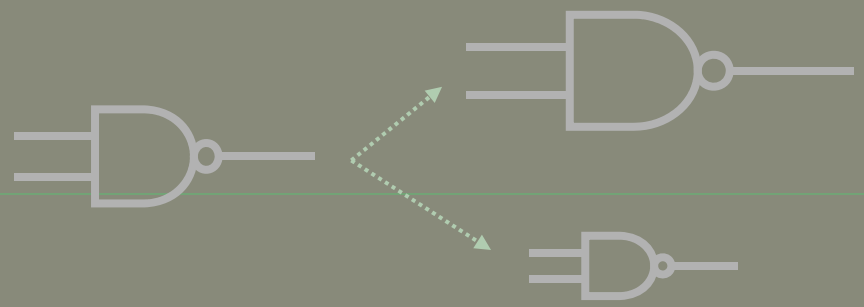
Tsay, DAC 90

- Can solve by applying necessary and sufficient Kuhn-Tucker conditions => Lagrange Multiplier = "added net weighting"
  - Approximated Solution

$$\lambda_{ij} = \left(\frac{\frac{(x_{ij} - u_{ij})}{u_{ij}}}{\frac{1}{a_{ii}} + \frac{1}{a_{jj}} - \frac{2c_{ij}}{a_{ii}a_{jj}}} \right)$$

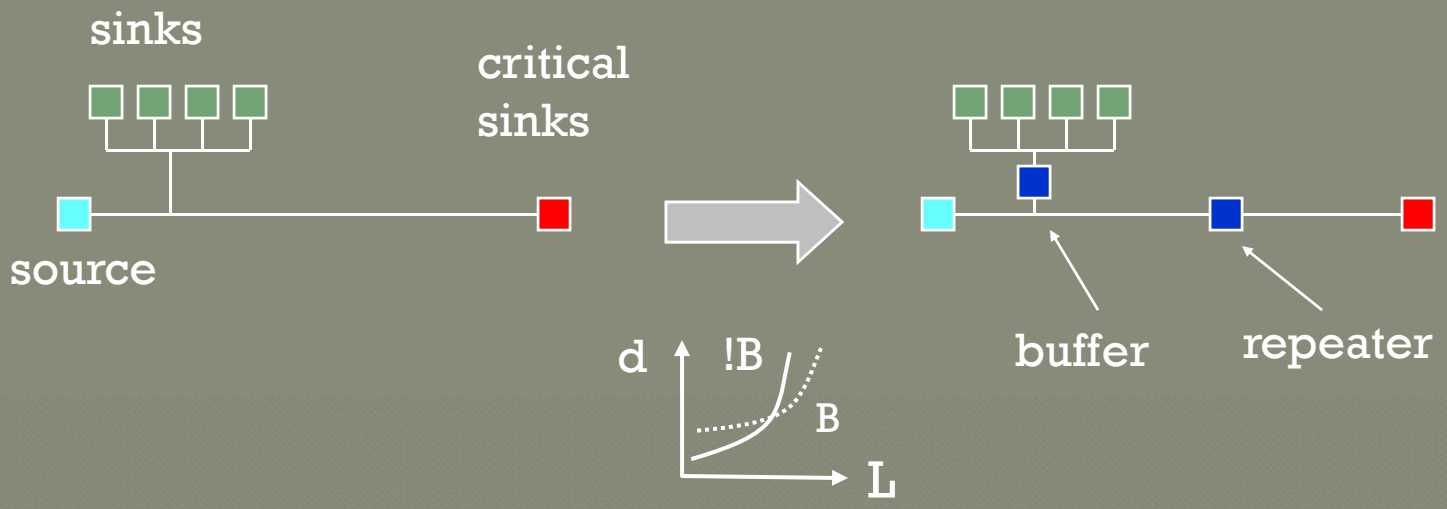


Cell Sizing



- Minimize total cell size while meeting timing constraints
  - optimize timing on critical paths
  - size down in non-critical paths
  - Experiments show 30~40% performance gain, with reduced total cell area

Buffer/Repeater Insertion



- ✓ Buffer blocks off unnecessary capacitance load to critical sink.
- ✓ Repeater reduces "quadratic" interconnect delay.

Timing-Driven Example

7K cells

TDP	TDR	Relative cycle time
–	–	1.00
√	–	0.58
–	√	0.74
√	√	0.40

Progressive Optimization