Physical Design Challenges Beyond the 22nm Node

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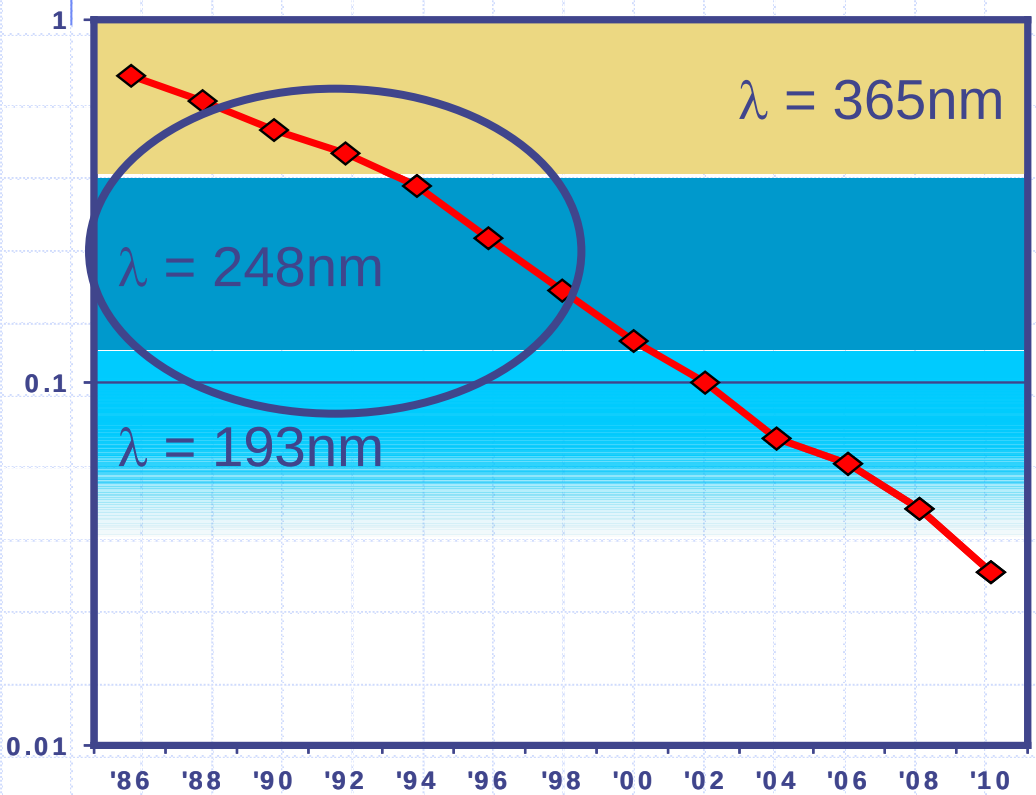
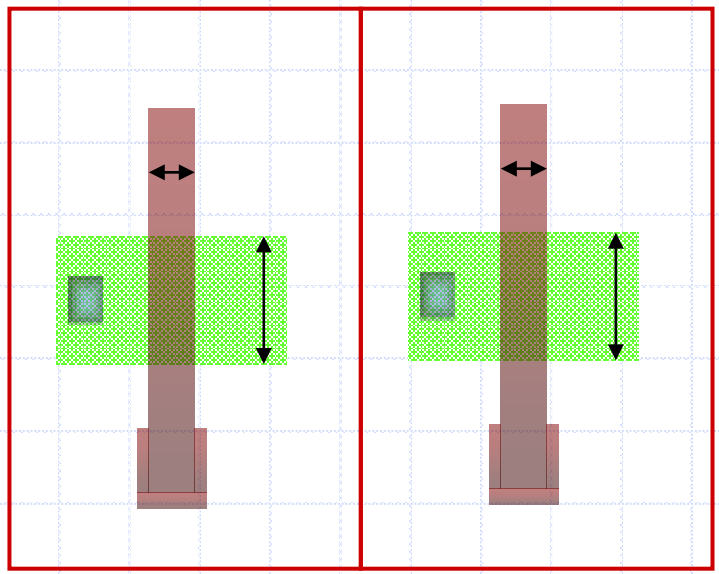
Outline

- Background
  - How have we gotten to where we are?
  - What lies at 22nm and beyond
- Challenges in achieving something better than the path we are on
  - Image fidelity
  - Defectivity
  - Accounting for multi-scale pheneomena
  - Variability and “resilience” failures
- Summary

Technology Resiliency -- Past

Defects were the major yield detractors for technology in the early days, yield and area were the major tradeoffs.



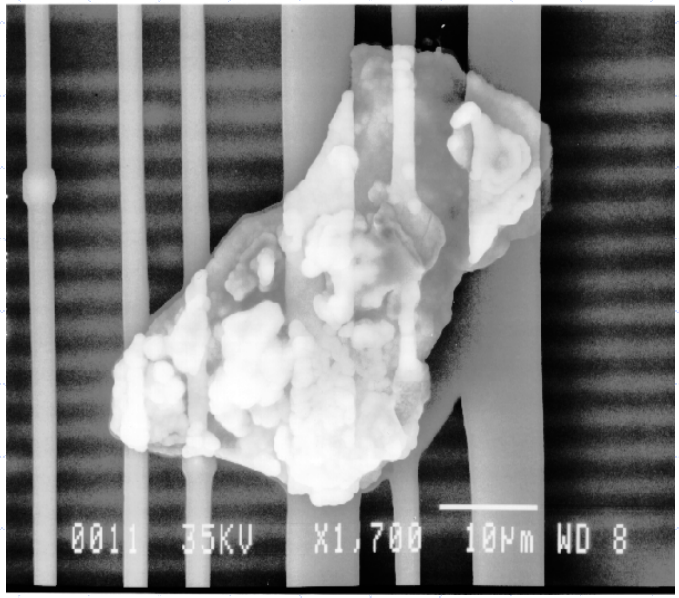


Defect driven groundrules

Relative cell independence => Composable design

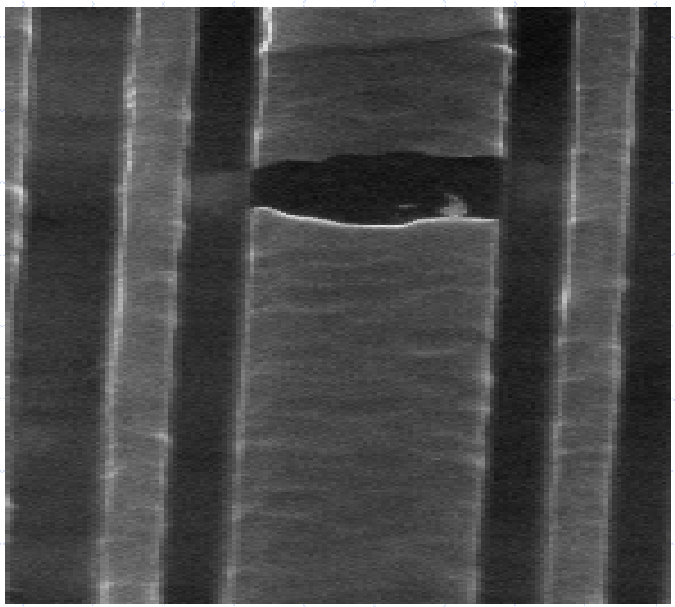
Past: Rules for shorts and opens

- Extra conducting material
  - Photolithographic printing error
  - Conductive particle contamination
  - Incomplete etch
  - Incomplete metal polish
- Missing conducting material



Bridging short

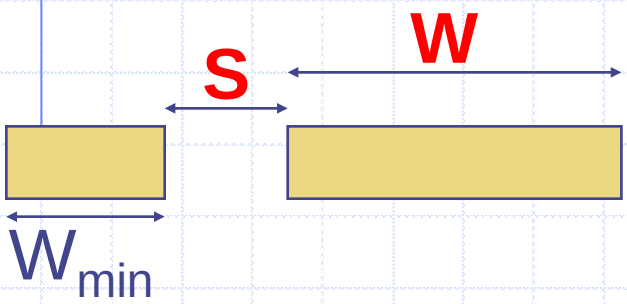
- **Electromigration**
  - Fast electrons transfer momentum to metal atoms at grain boundaries, causing diffusive movement, thinning, open failure

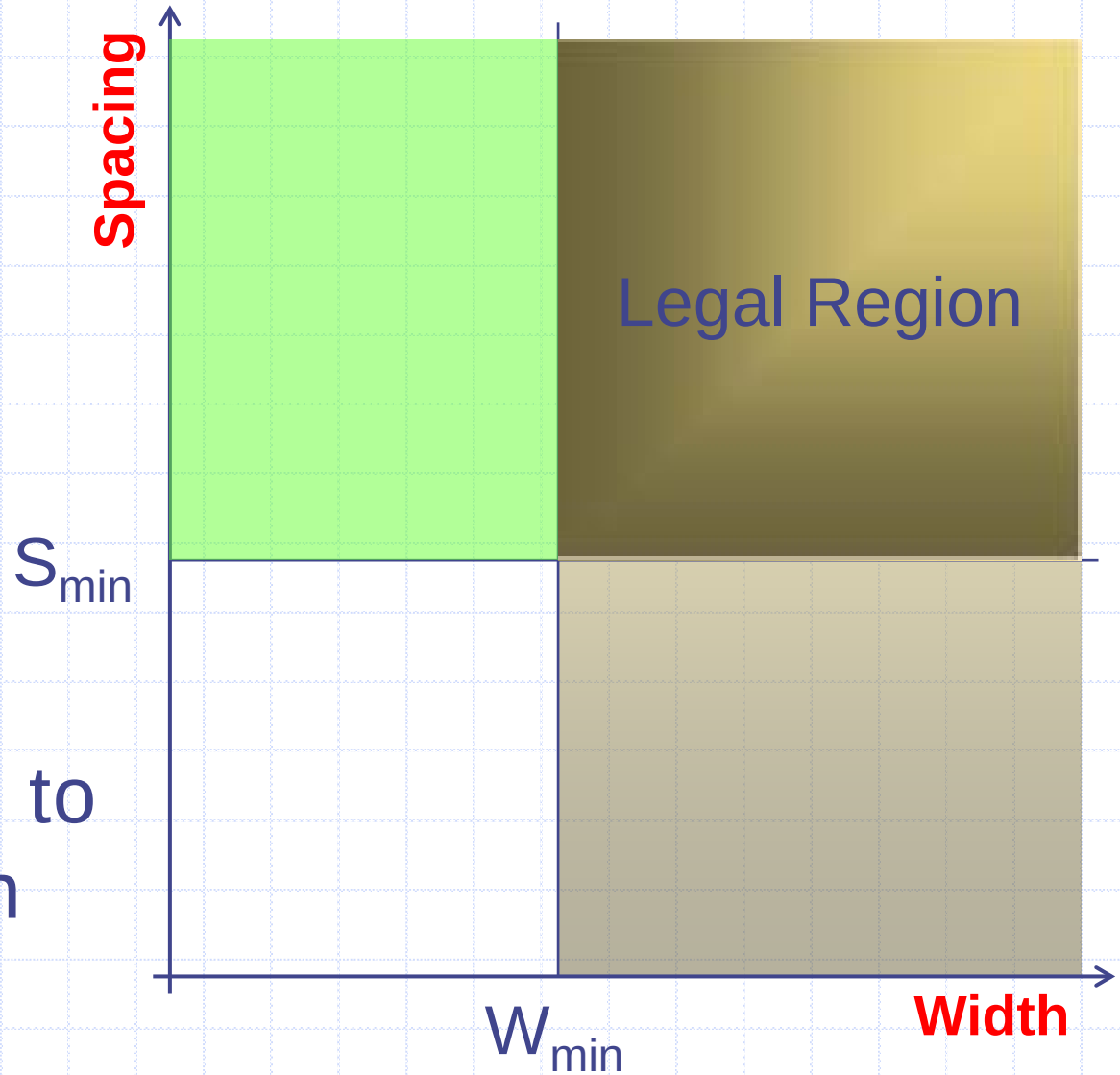


EM fail

Technology Rules (History)

- Resulting wire rules

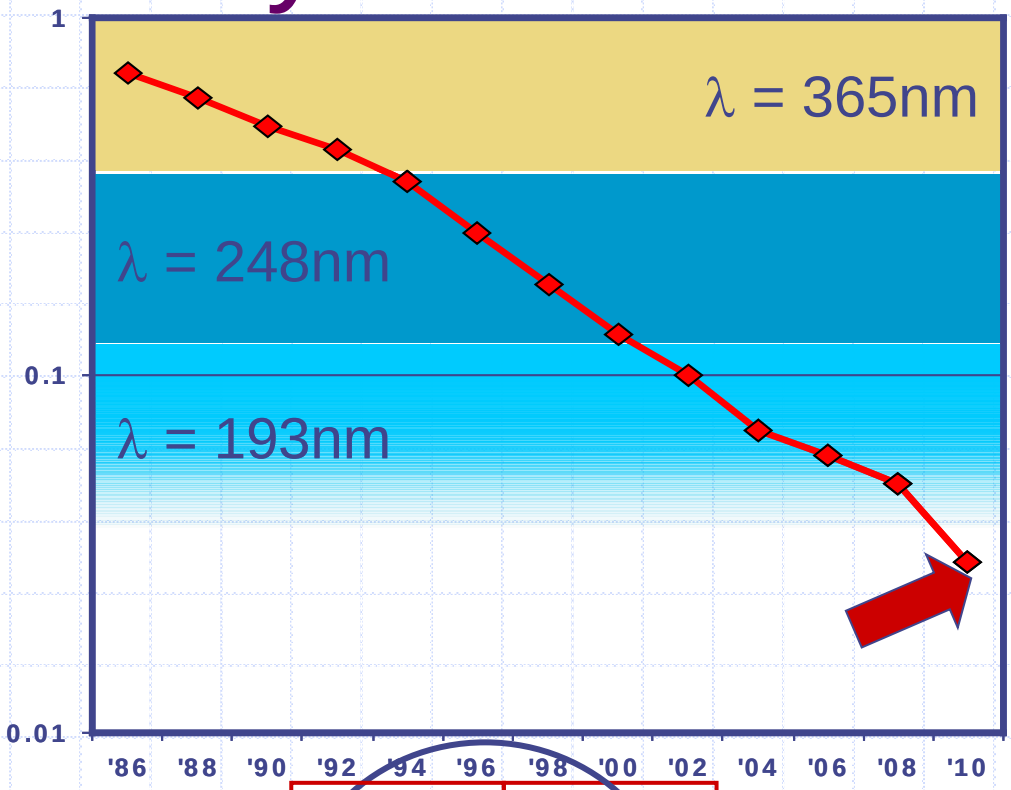


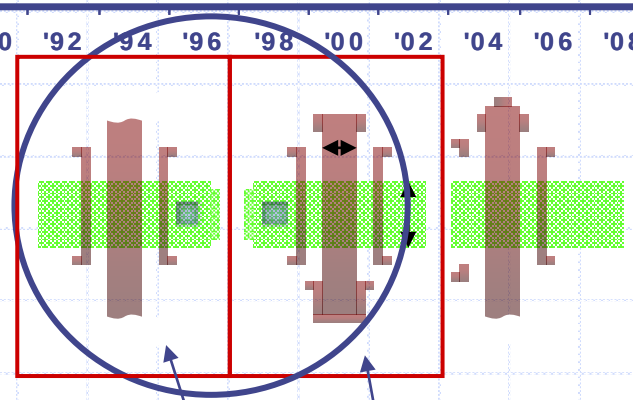


- Two rules suffice to define the design space!

Technology Resiliency – 22nm

- Serious lithography challenges
- Now in a régime where atomistic effects are significant – gate oxide variation, random dopant variation, line edge roughness...
- No silver bullets - difficult engineering problems

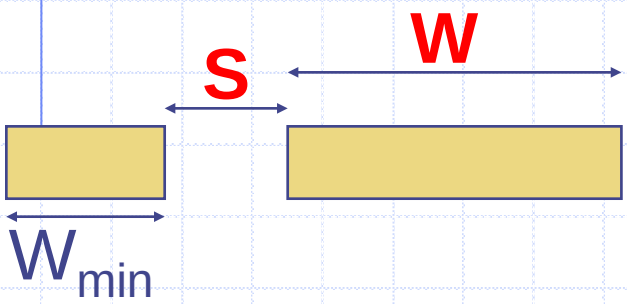


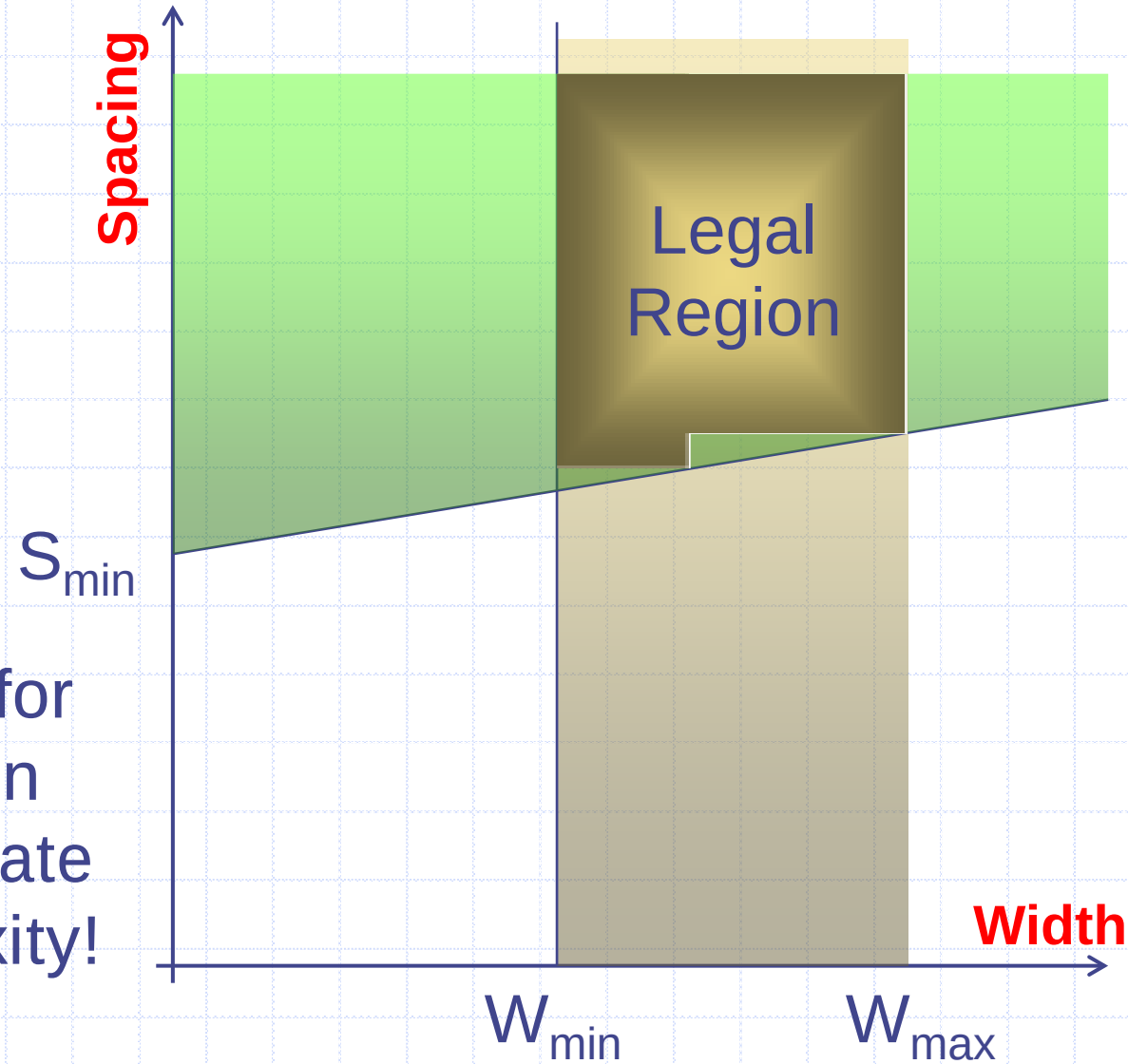


Cell you place here determines behavior of this cell

Technology Rule Explosion

- Impact of CMP, Dishing, Erosion as well as lithography...





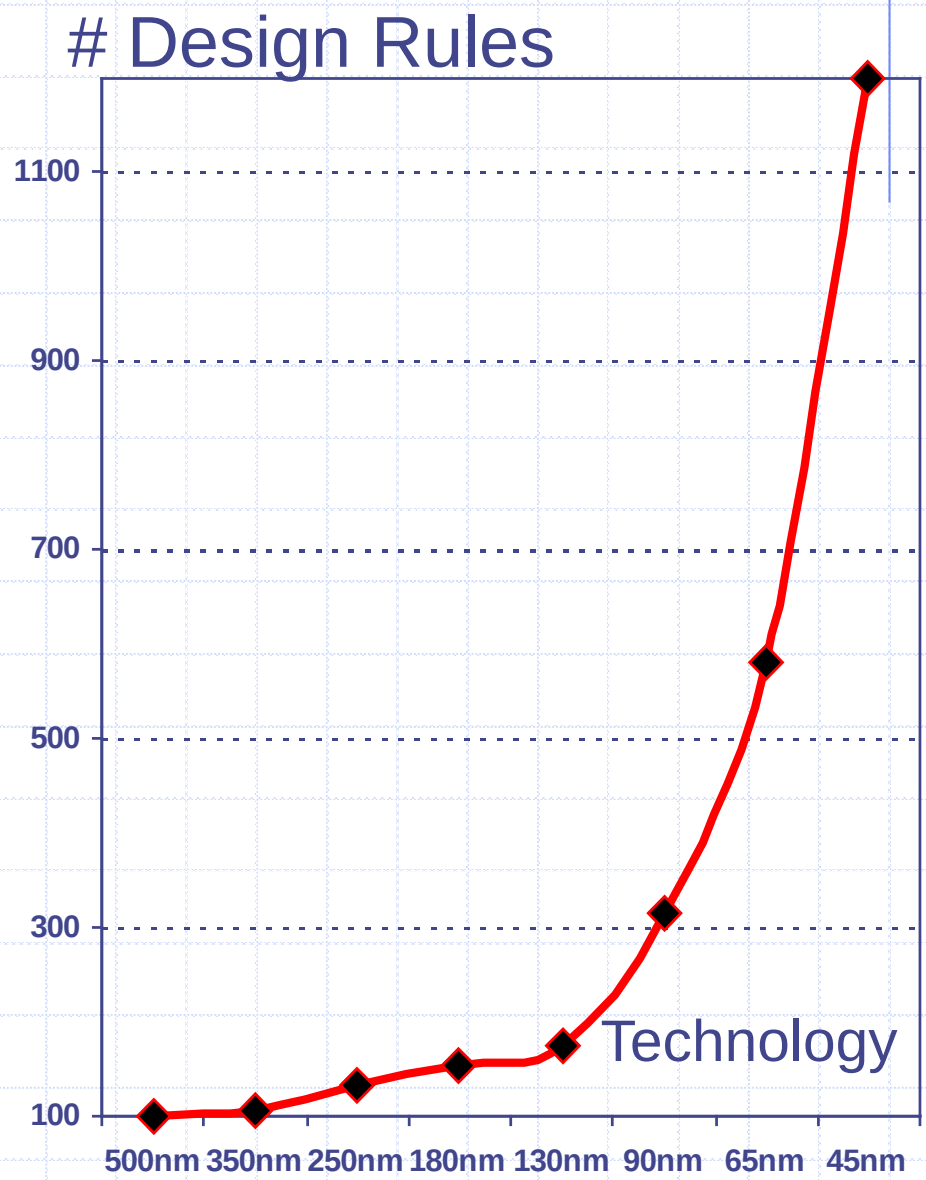
- Four or more rules for the same situation in order to accommodate technology complexity!

Technology Complexity

Technology has become so complex that it is not well represented by “rules”.

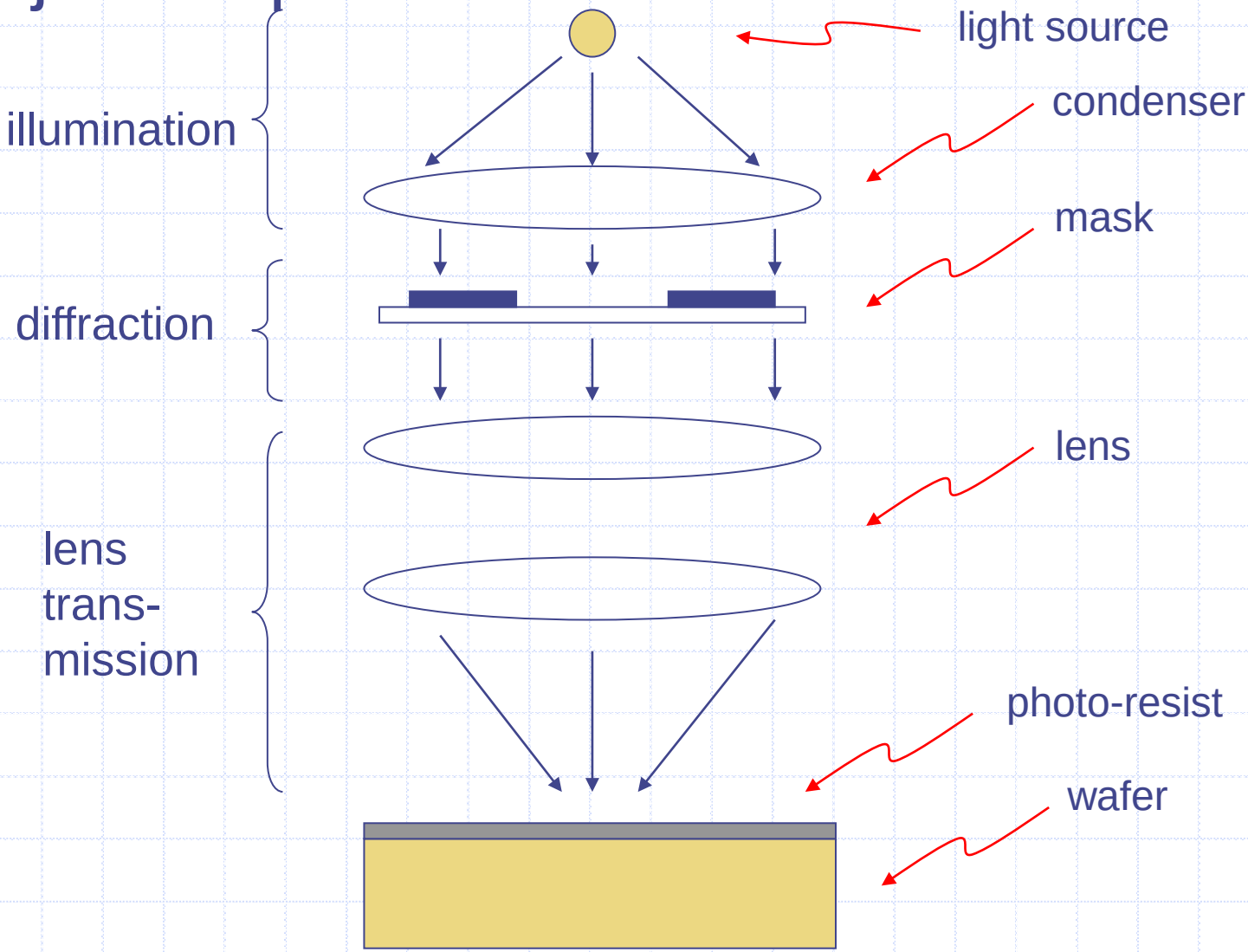
Design / Technology interface information bandwidth needs are skyrocketing!

Expressing complex non-linear realities via rules is becoming difficult.



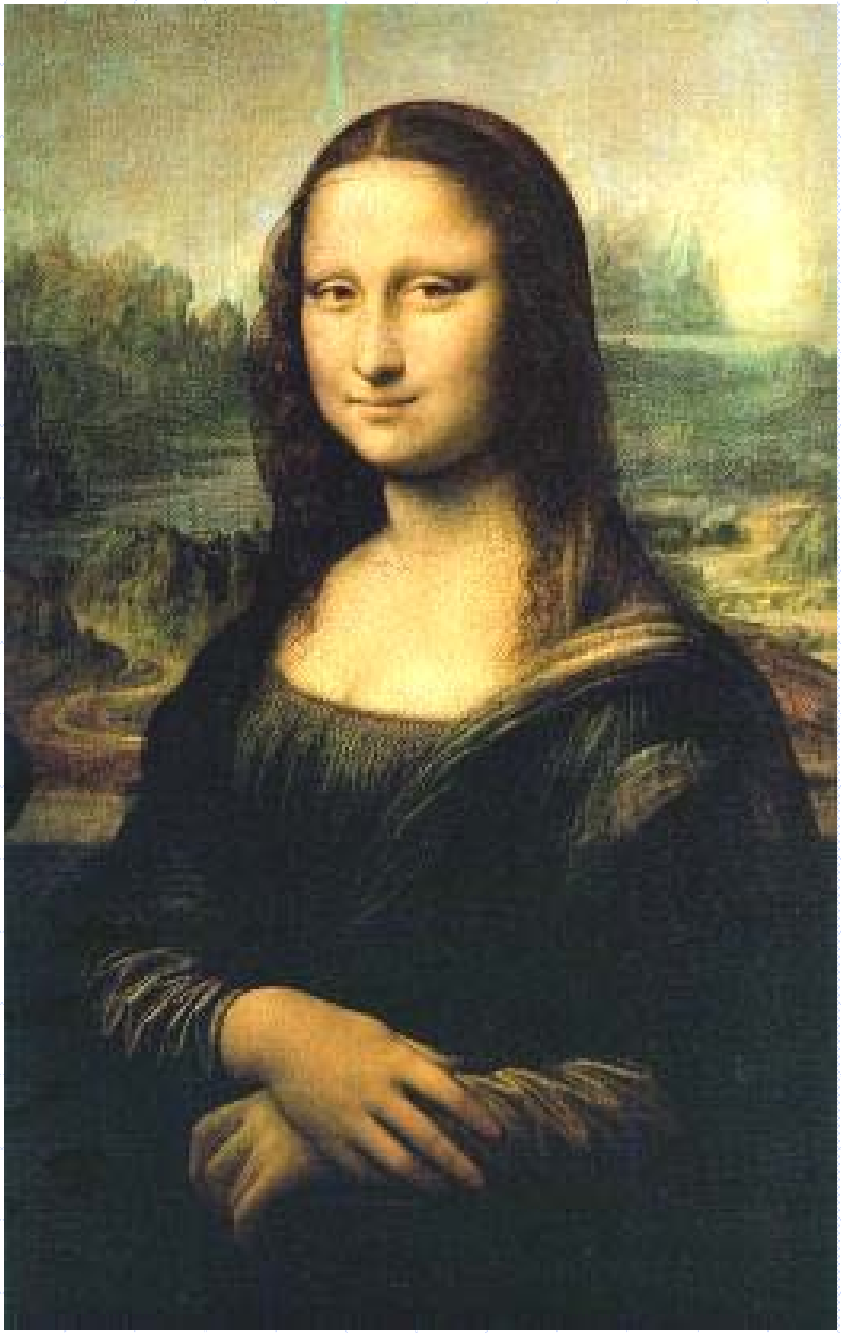
Basics of Optical Lithography

- Three major components



source: Liu, CASS 2010

Optical Lithography at 22nm
Get painting!

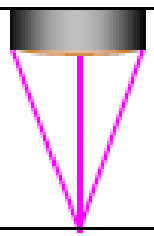
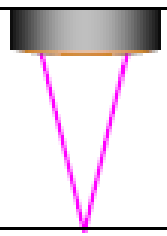
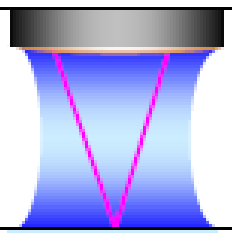
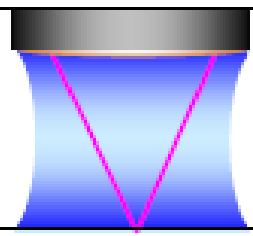
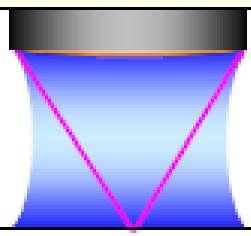
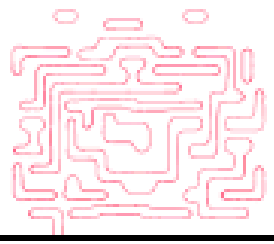
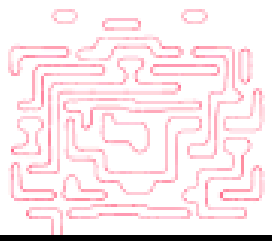
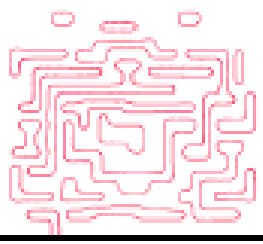
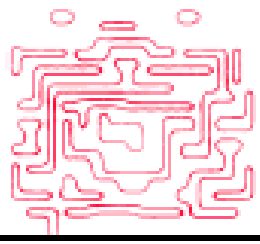
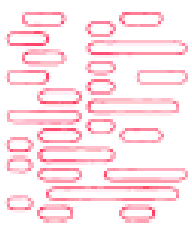


Using 193nm wavelength to image sub-20nm features ~=

Using a 1 inch brush to create 2mm strokes

Litho Progression

$$\text{Resolution} = k_1 \frac{\lambda}{NA}$$

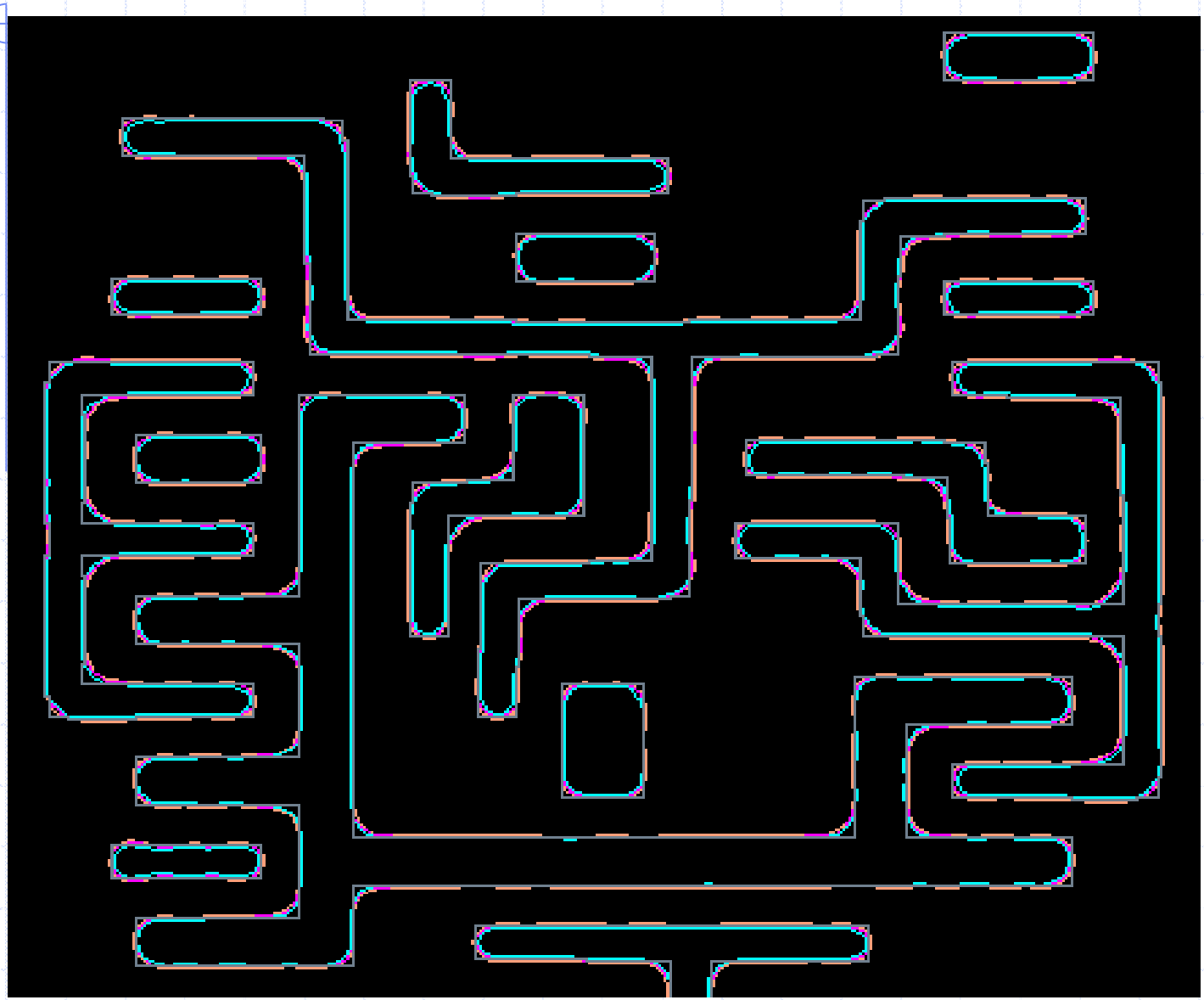
Node	90nm	65nm	45nm	32nm	22nm
Year	2003	2005	2007	2009	2011
Pitch	250nm	200nm	140nm	100nm	70nm
λ	193nm				
NA	.75	.85	1.2	1.35	
k_1	.5	.44	.44	.35	.25
Enabling Innovation		Off Axis Illumination & Assist Features			
			Water Immersion		
				Variability-aware Design	
					Gridded Des.
Litho					
Layout (M1)					

source: Liebmann, Semicon West '08

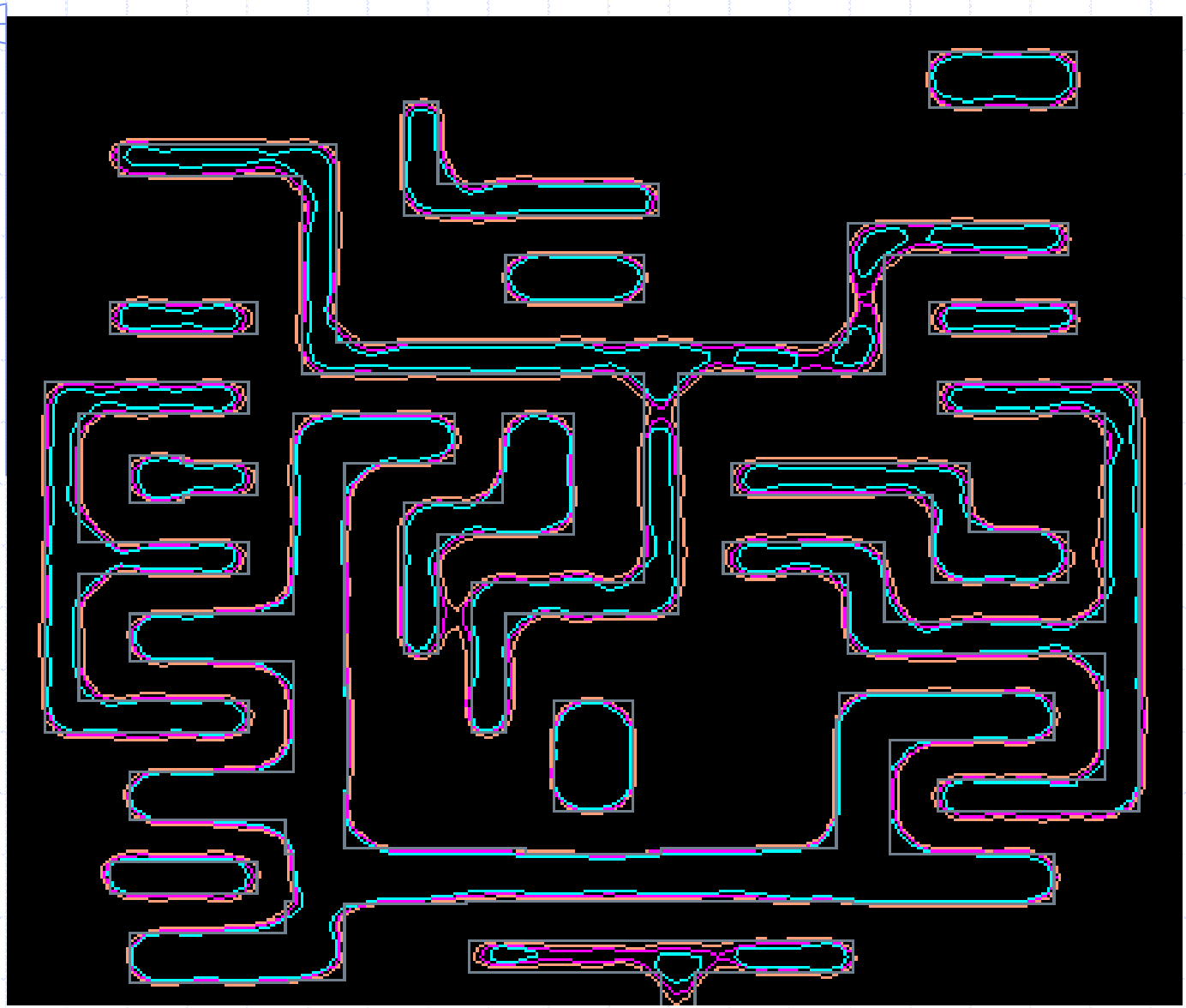
Zeiss Starlith® 1700i lens

source: zeiss.com

65nm M1 litho simulation

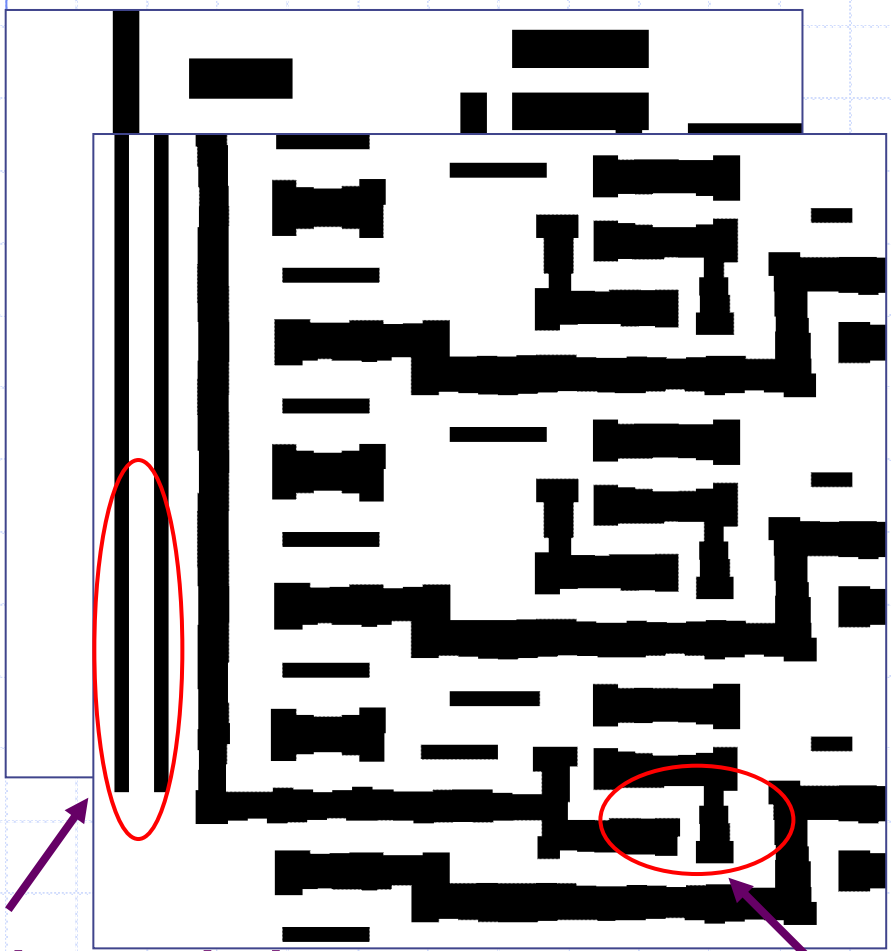


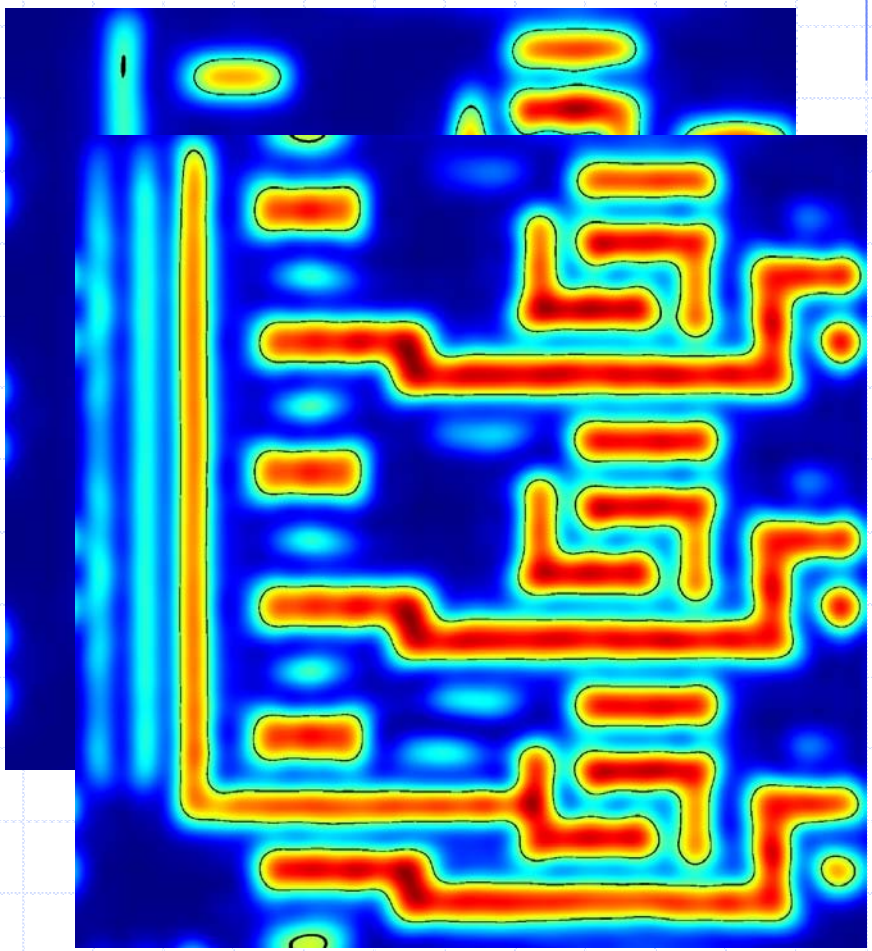
32nm M1 litho simulation – no assist



Improving Litho Variation with RETs

- Simple shapes aren't so simple!





Sub-Resolution Assist Feature

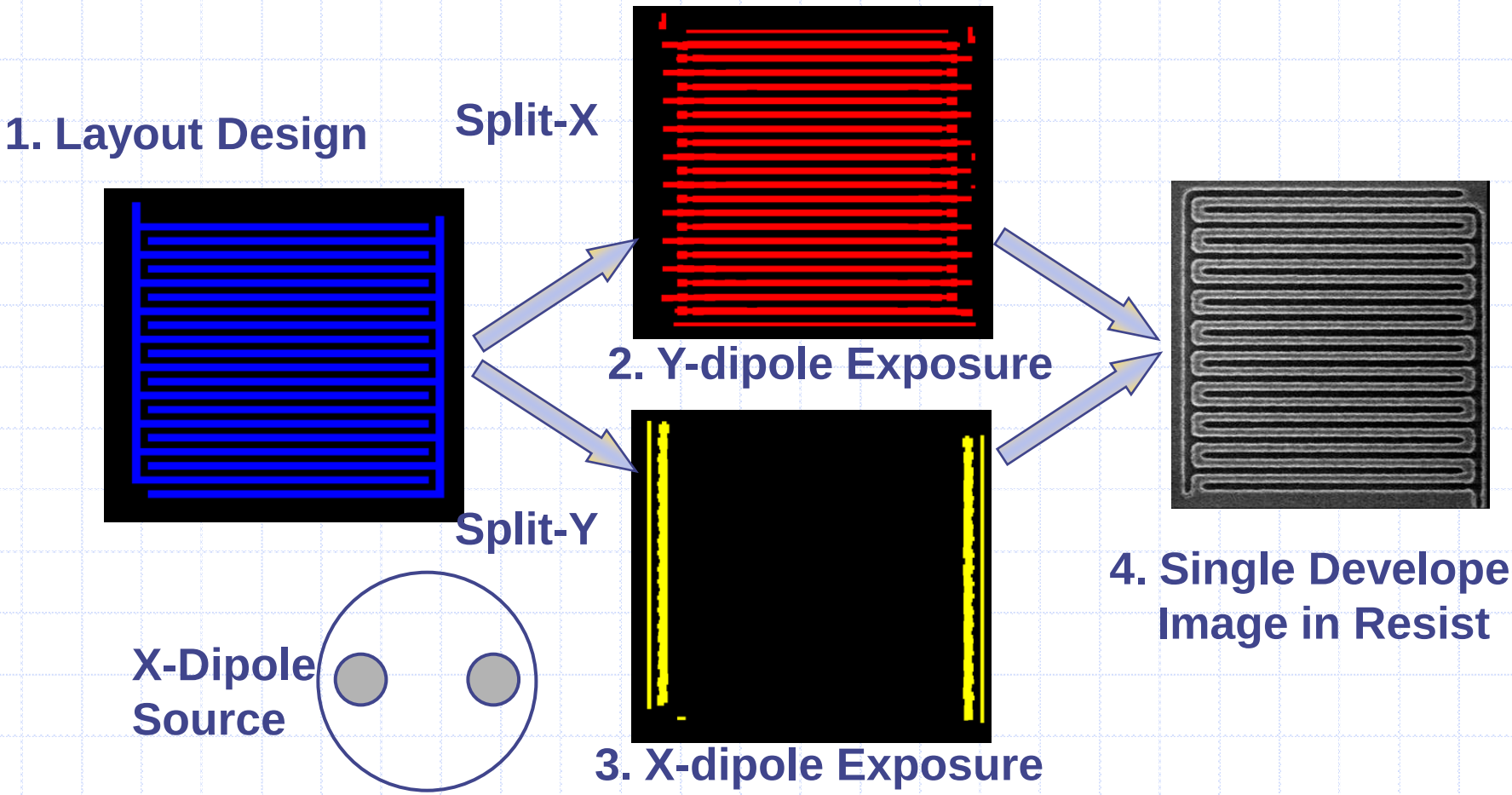
Optical Proximity Correction

source: Liu, CASS 2010

Improving Litho with Double Exposure

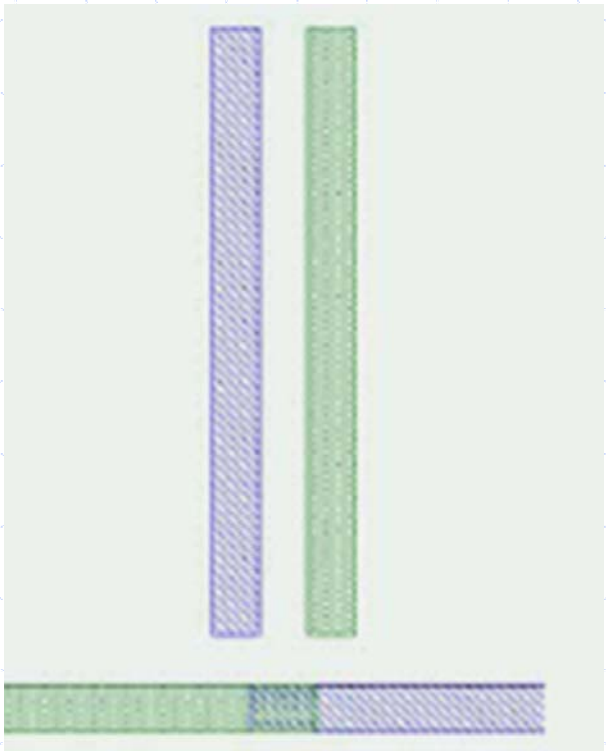
Double Exposure (DE) extends the use of current exposure technology to tighter pitch structures

- A pattern (interconnect metal level) is broken into two segments
  - Optimized exposure conditions are used for each segment, overcoming “corner effects” with single exposure



Improving Litho with Double Patterning

- Frequency doubling through assignment of shapes into two phases

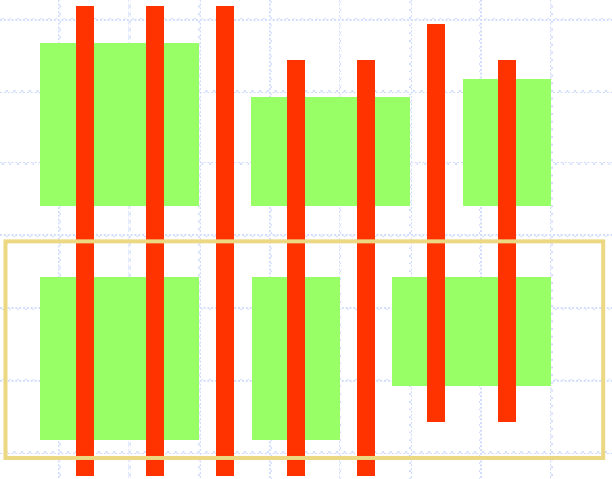


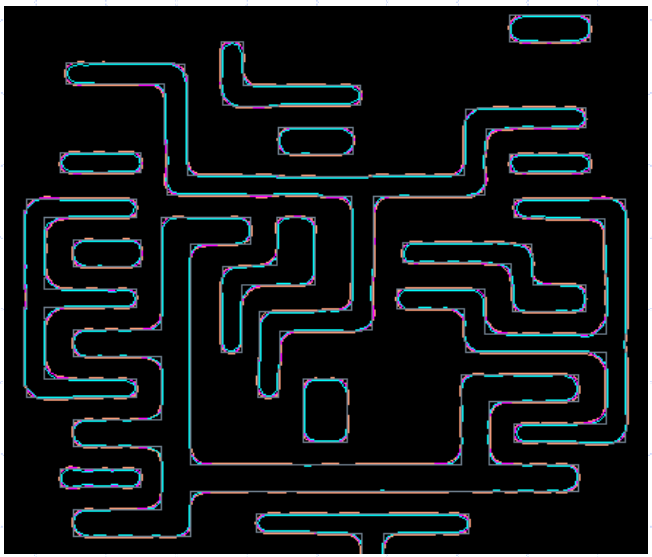
Phase assignment problem can be exceptionally difficult

source: Wiaux, et al., “Split and Design Guidelines for Double Patterning”, SPIE 2008
Liebmann, Semicon West ‘08

What designers can do: Restrict Design

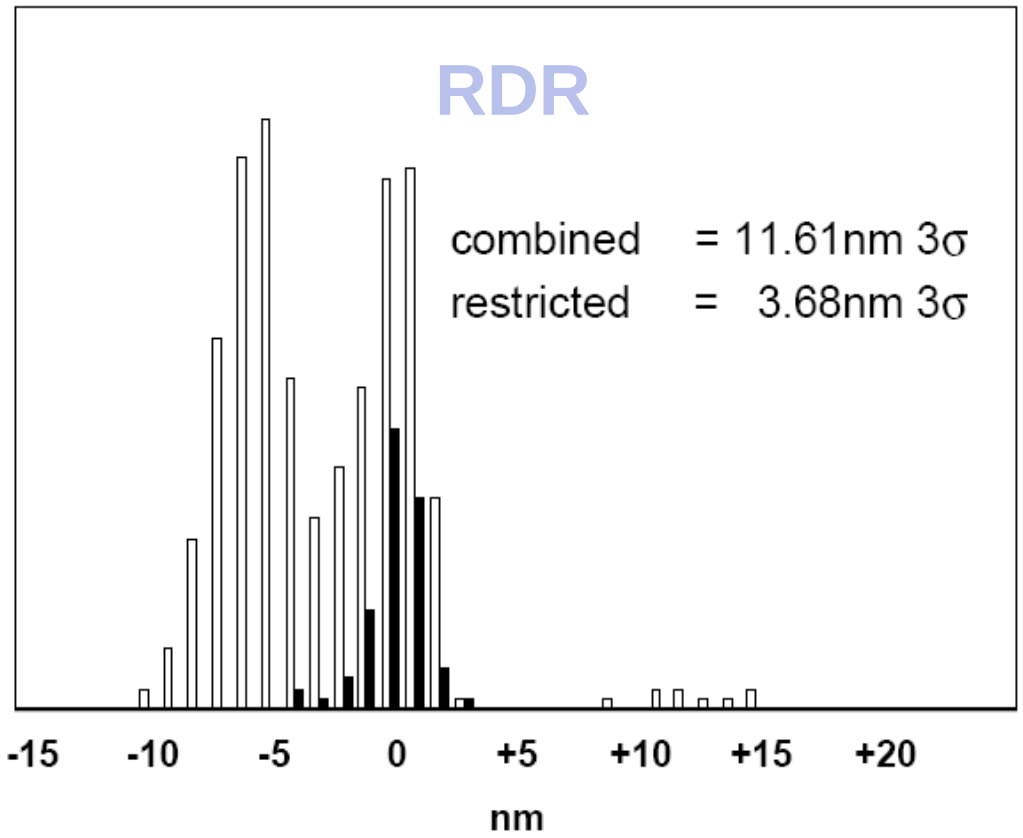
- The technology cannot guarantee the outcome of a free form layout. Thus more restrictions are imposed on the layout.
- Usually driven by the technology limitations
- Started from FEOL, gradually migrate to BEOL
- Typical examples:
  - Only allow uni-directional shapes (at least for critical portion which defines the gate)
  - Only allow discrete width and spacing
  - Use Dummy shapes
  - Avoid jogs
- Can't come for free => AREA





What designers can do: Regularity

- Restricted Design Rules shows ~3x improvement in variability.

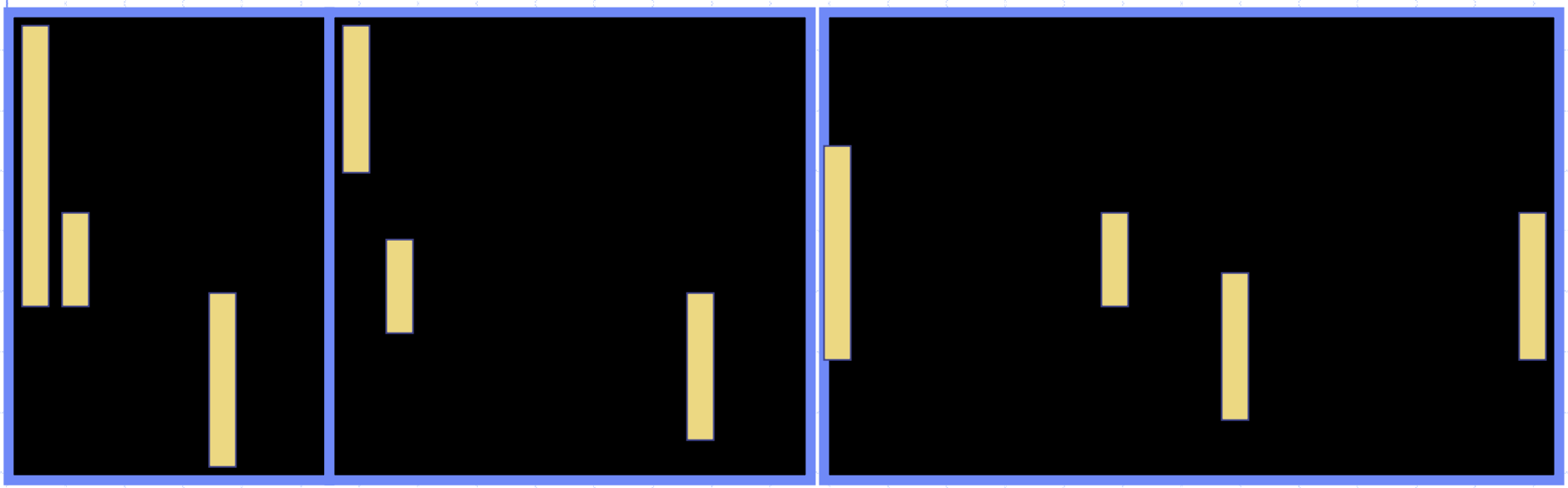


Source: L. Liebman, SPIE 04

PD Challenges for 22nm and beyond

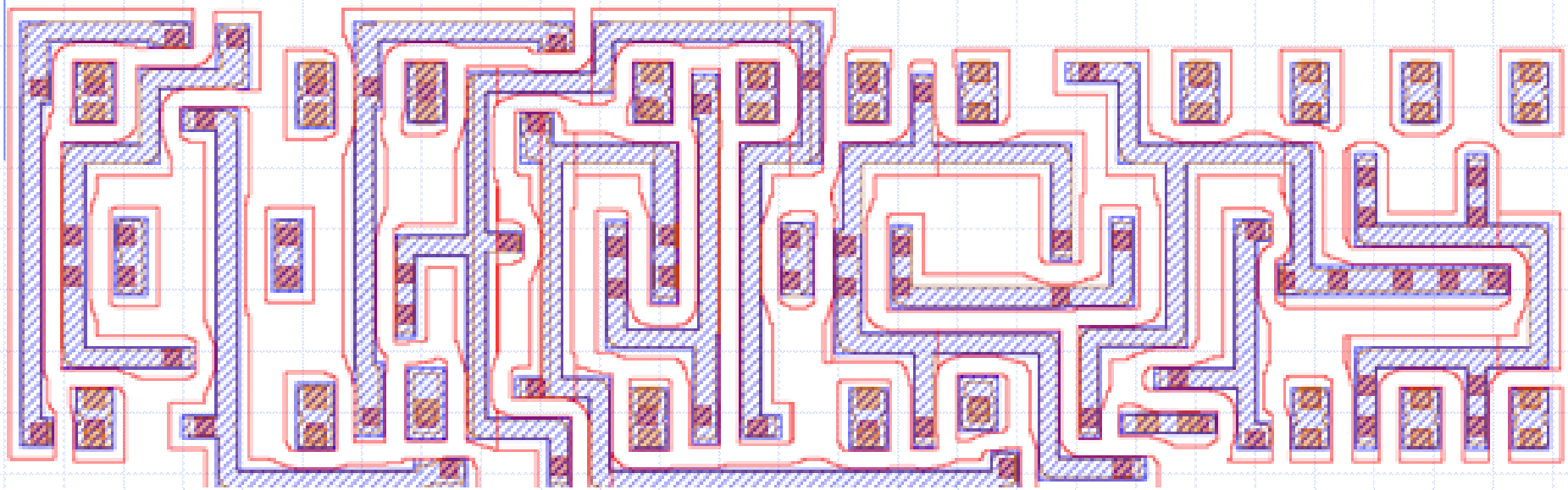
One: What can PD do to help balance the desire for density and the need for image fidelity?

Is this the right abstraction for PD tools?



- At/beyond 22nm …. Only at significant cost
  - Means to maintaining arbitrary composability are costly … probably too costly

Is this the right abstraction?

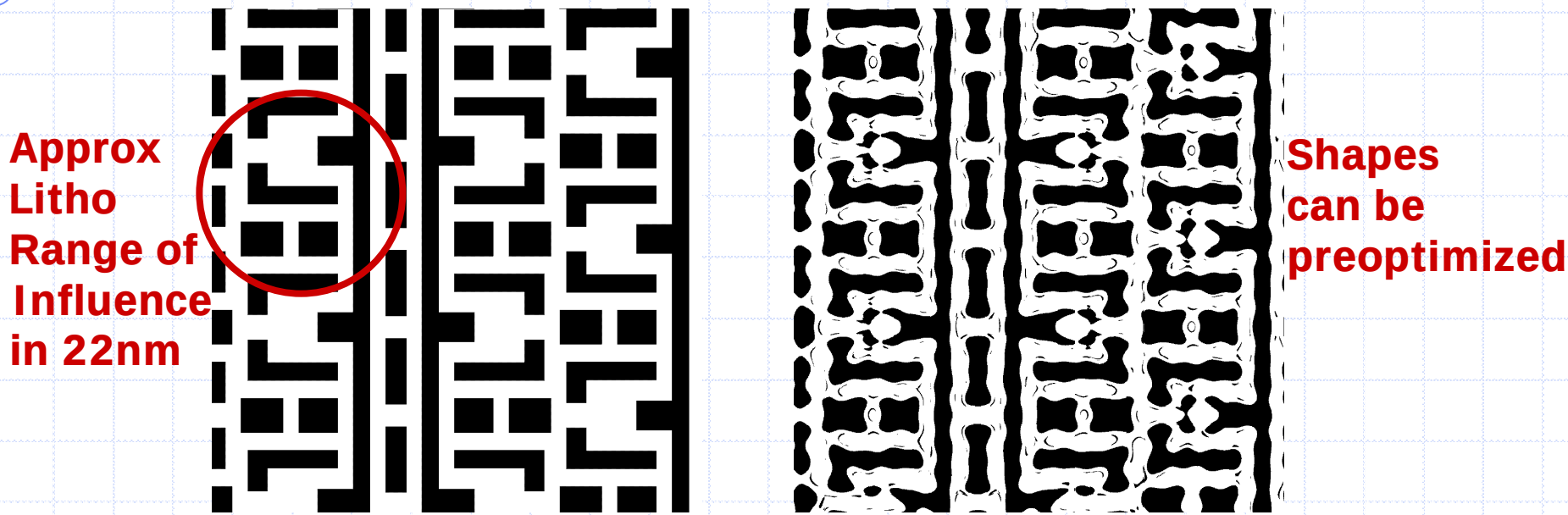


- No – PD shouldn't need to go to PV band level

Why does abstraction matter?

- Visibility into / effect on the library
  - Poly/contact/M1 within cell influence performance, power, routability
  - PD needs to be a partner in the tradeoffs made within cell
    - Placement clearly has effects within 22nm “range of litho influence” for performance critical Poly and yield critical M1
    - Low level routing can have same effect for yield-critical M1

Learning from SRAMs

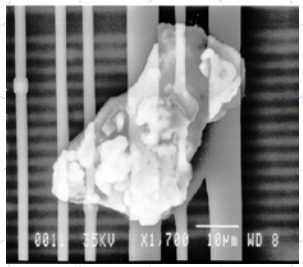


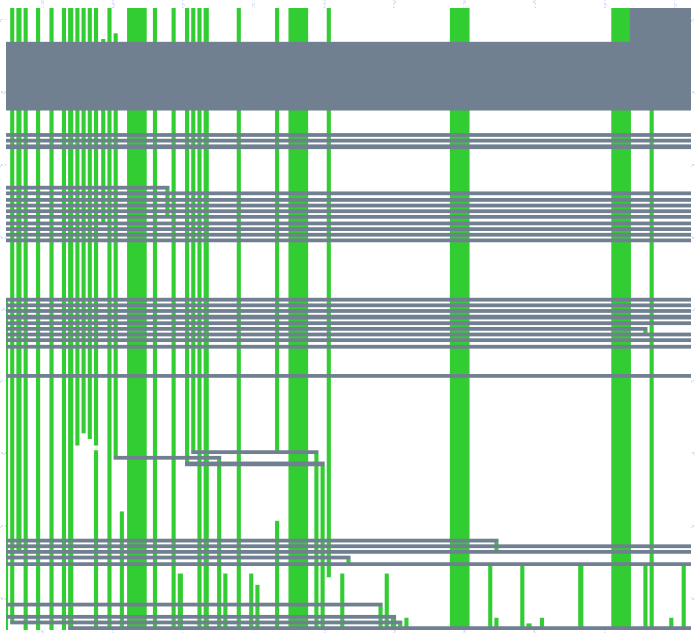
- Poly regularity is a done deal
- M1 is the 22nm design/manufacturing battleground:
  - If litho range of influence is avoided in placement/routing, we can envision preanalysis and library optimization for improved density, robustness...
- Library avoidance of M1 – cost?
- Future: Just reapply at each level up the stack?

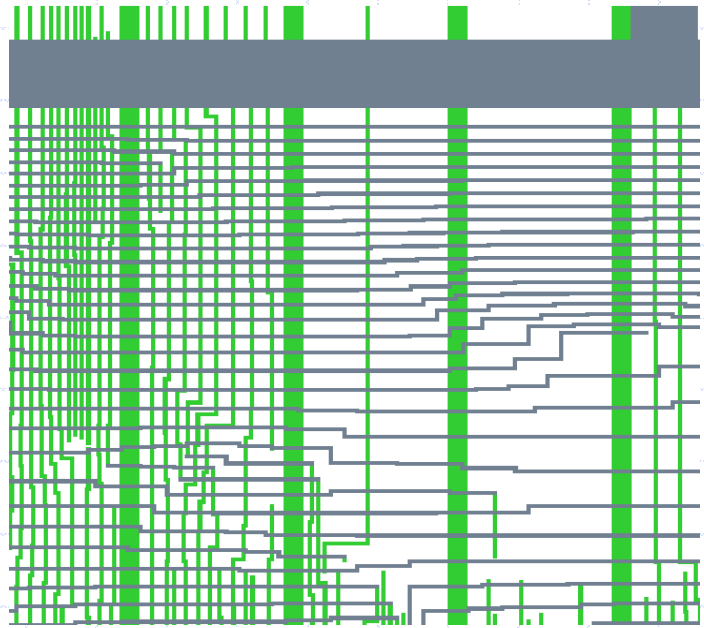
PD Challenges for 22nm and beyond

Two: What can PD do to help balance the requirements of density and defectivity?

Critical Area Improvement



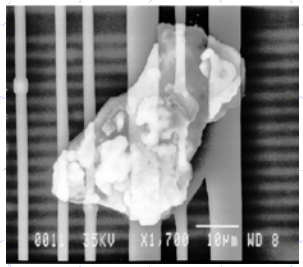


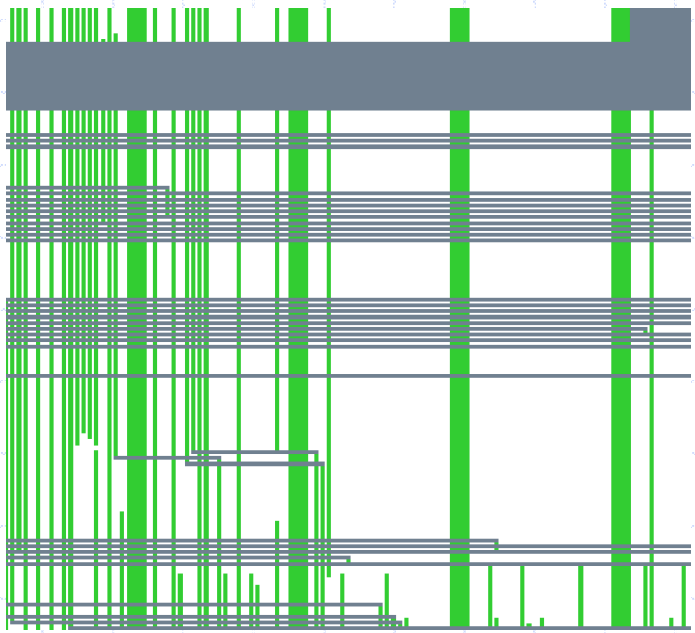


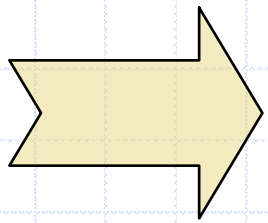
ISQED '03, Dan Maynard, "Productivity Optimization Techniques for the Proactive Semiconductor Manufacturer"

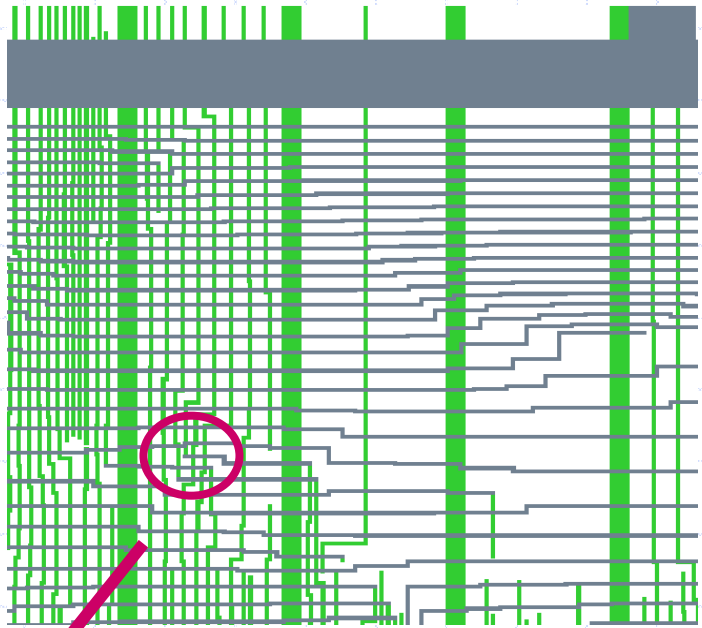
Improved robustness to particle contamination!

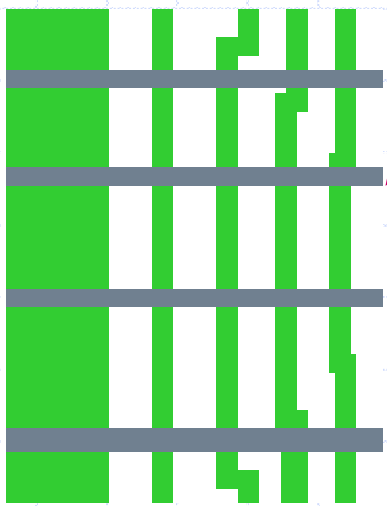
Critical Area Improvement









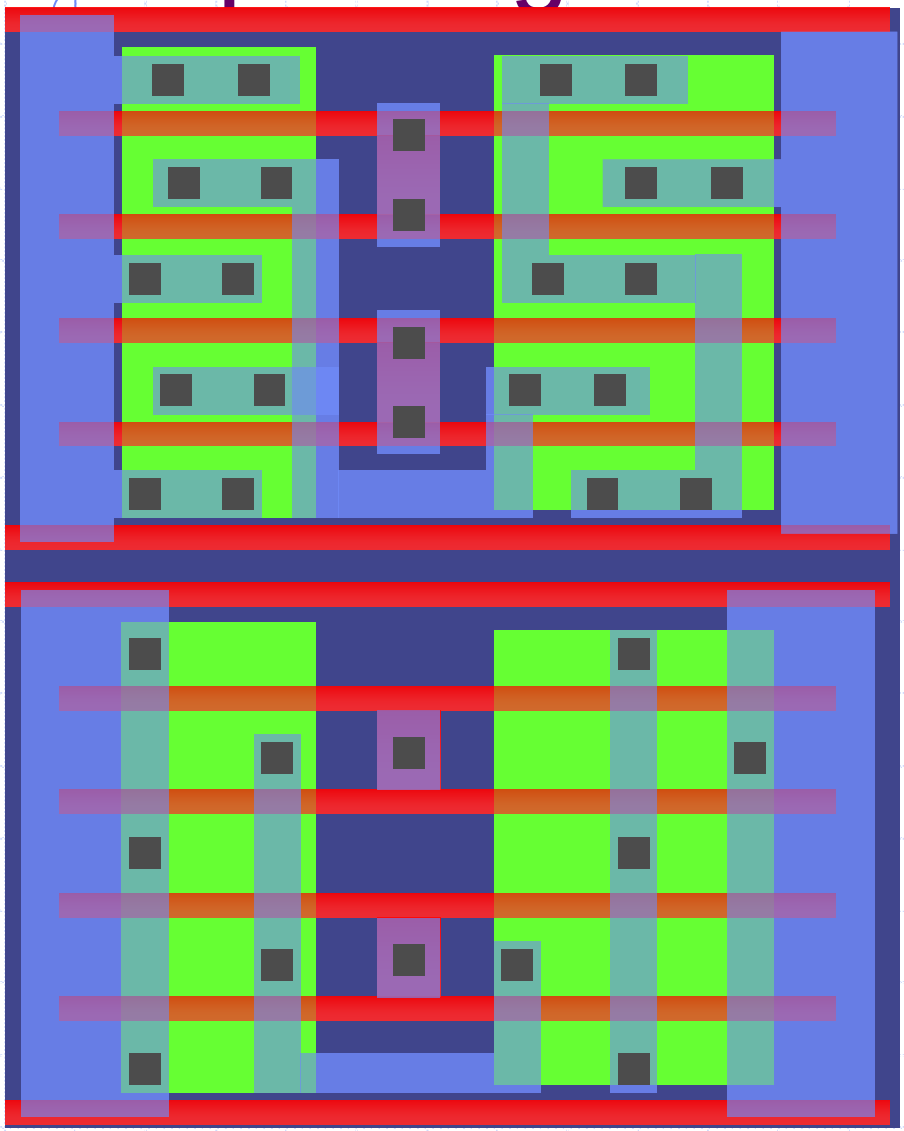


ISQED '03, Dan Maynard, "Productivity Optimization Techniques for the Proactive Semiconductor Manufacturer"

Litho $&!*

Net: Better or worse?

Improving Yield with Via Redundancy



Less yield loss due to via redundancy

M1 litho more difficult

M1 litho much easier

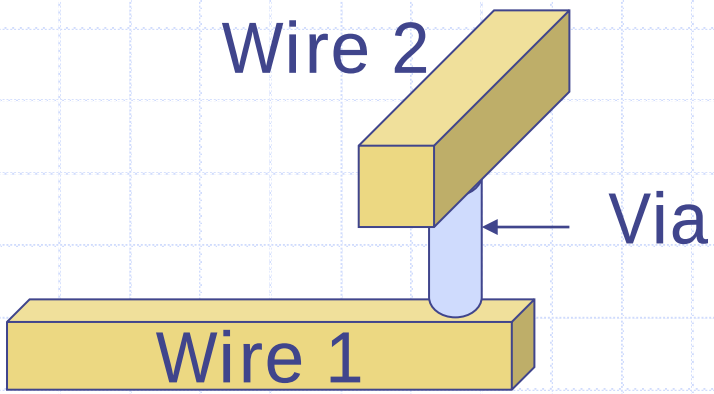
More yield loss due to via coverage

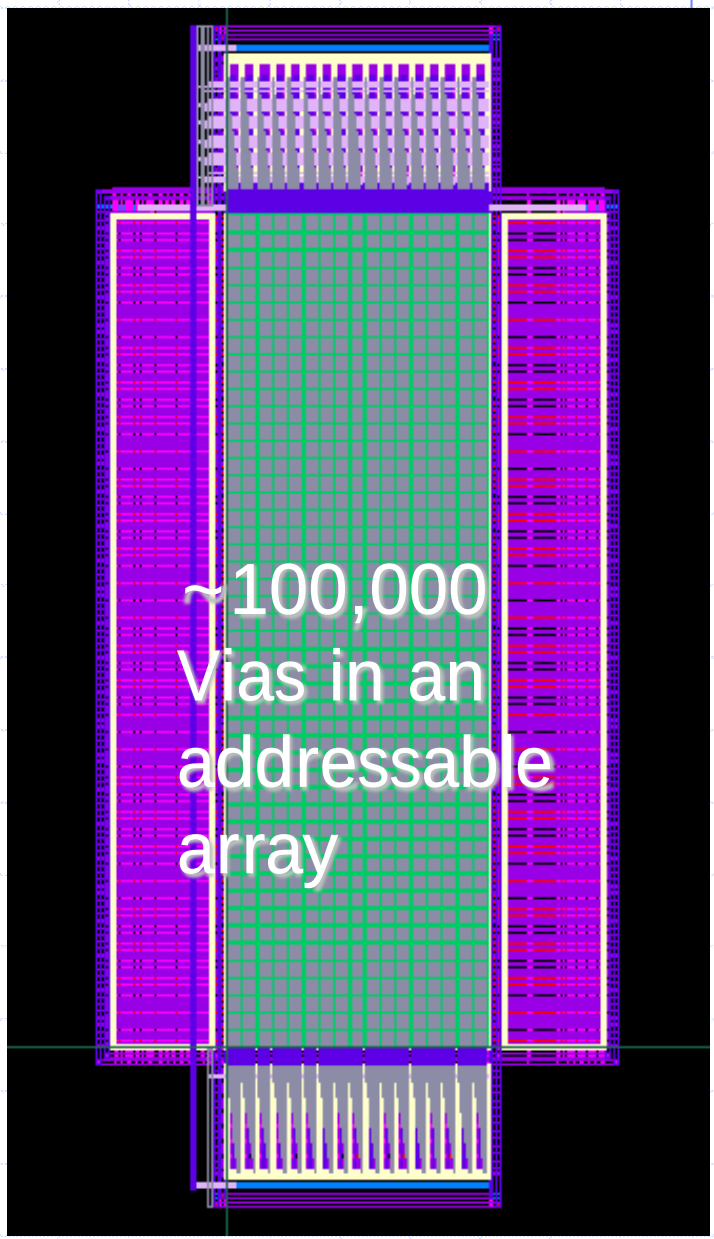
How do we manage this tradeoff?

What about performance?

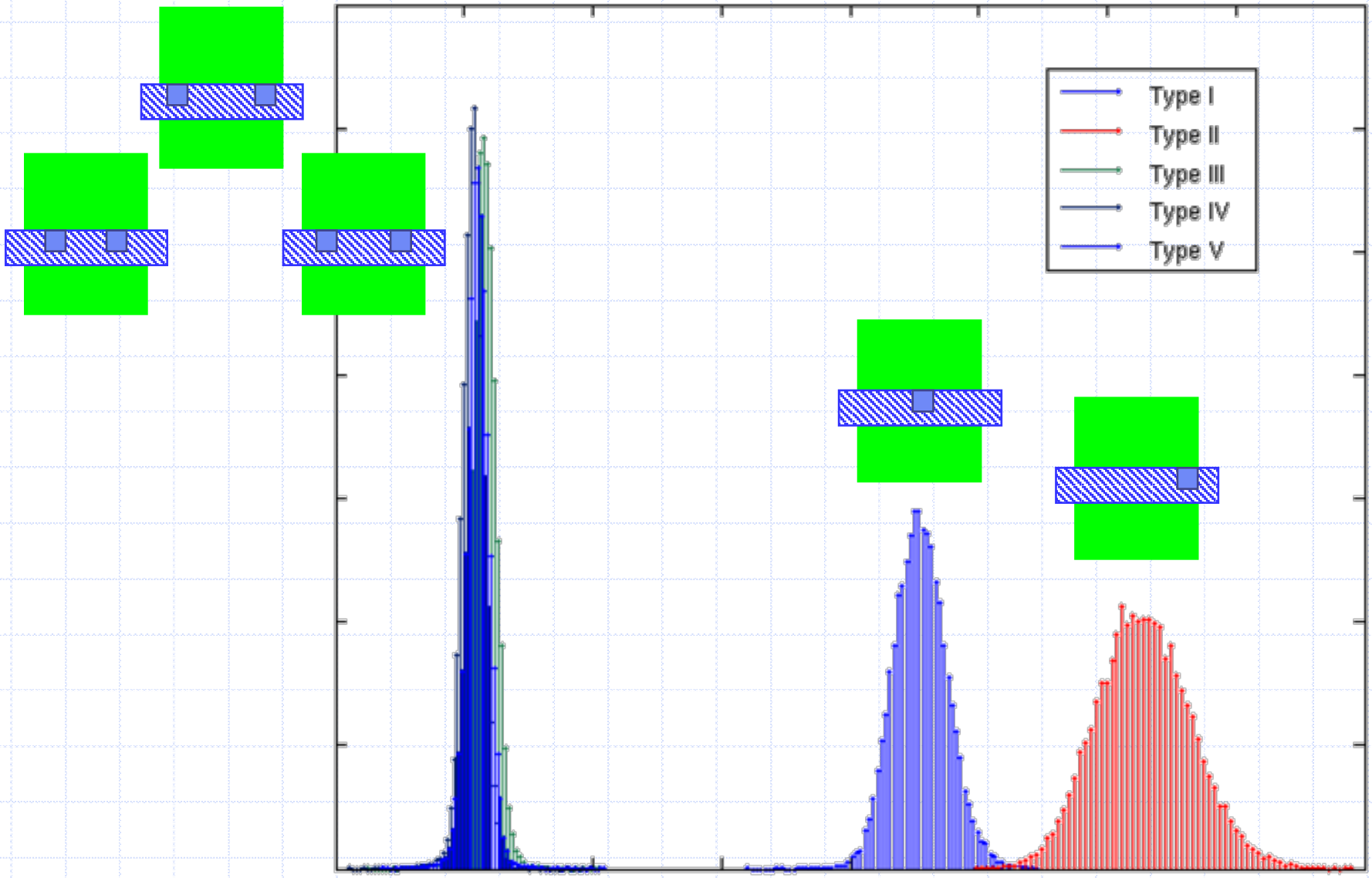
Steps toward DfM for redundant vias

- Measuring via resistance distributions key.
  - Placement and redundancy systematically effect resistance
- We created a special structure to measure resistance of individual vias for various configurations.





Quantifying via resistance distributions



- Use in area vs yield tradeoff analysis

Balancing density with defectivity

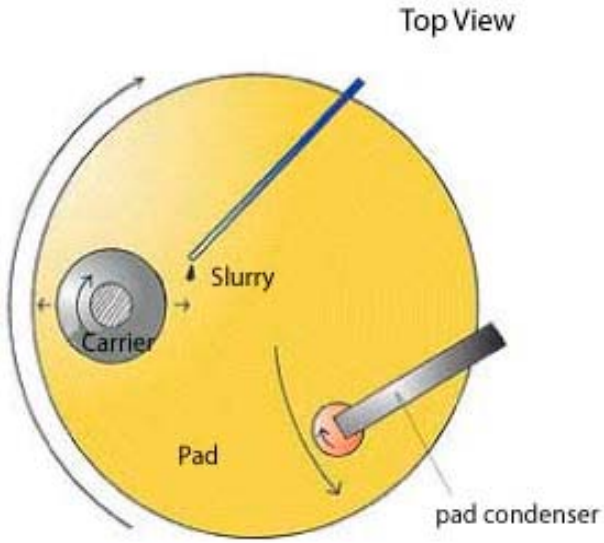
- Need better models of yield vs area/power/performance for library designer, placement, routing, buffer insertion, ...
- Manufacturing / Design / Automation all affected

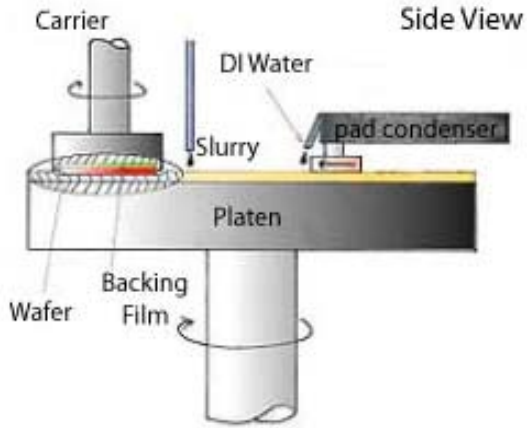
PD Challenges for 22nm and beyond

Three: How can PD affect multiscale phenomena?

Long Range (mm-scale) Effects - CMP

- Chemical-mechanical polishing (CMP) is used to planarize the wafer surface
- Routinely used in dual damascene copper interconnect definition steps

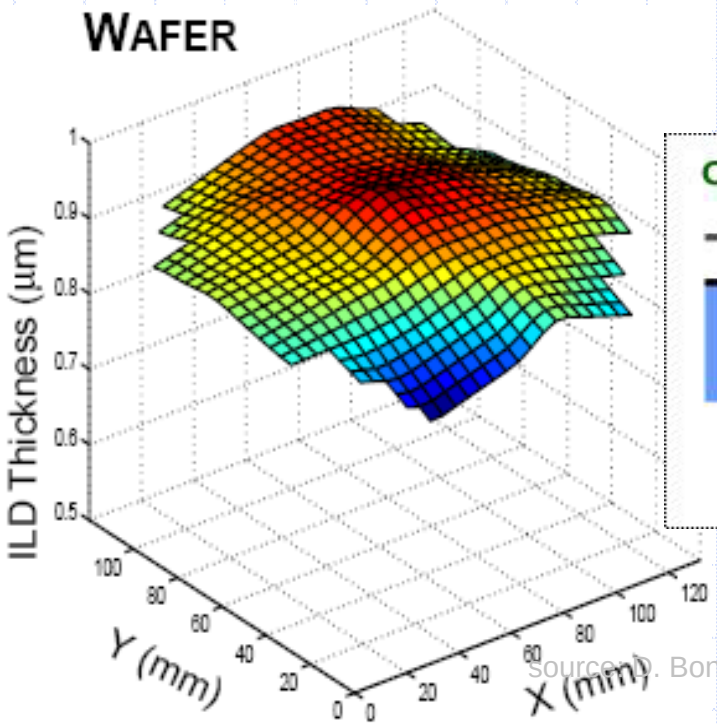


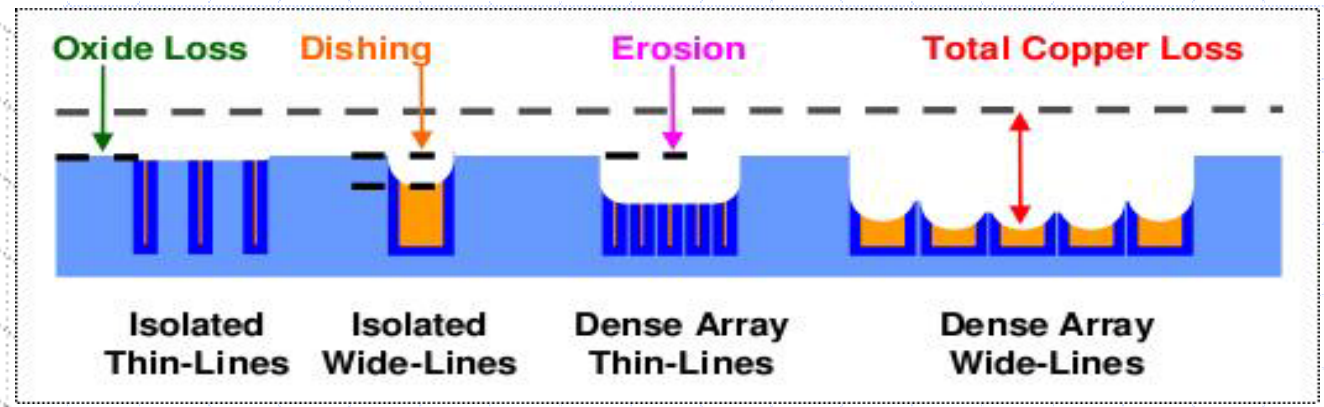


source: horibalab.com

CMP Dishing

- Different metal wire density can cause changes in the height of ILD and metal layers
  - Change of wire resistance and capacitance
- Can further affect the up metal layer shape due to the tight photolithography latitude
- CMP awareness showing up in tools flow

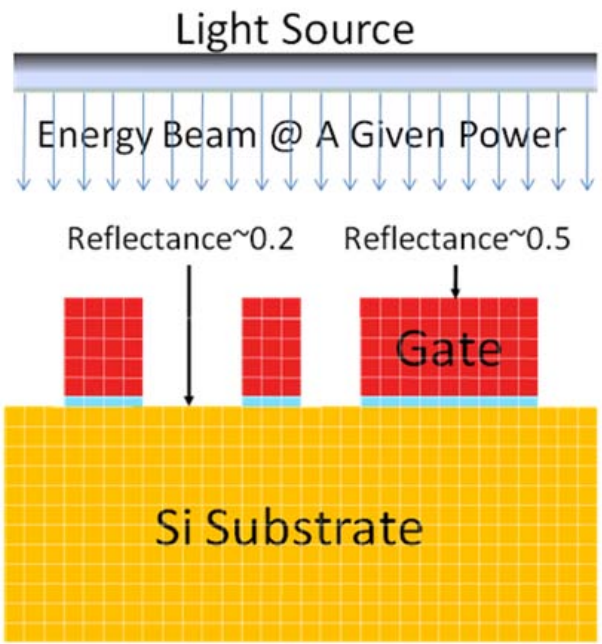


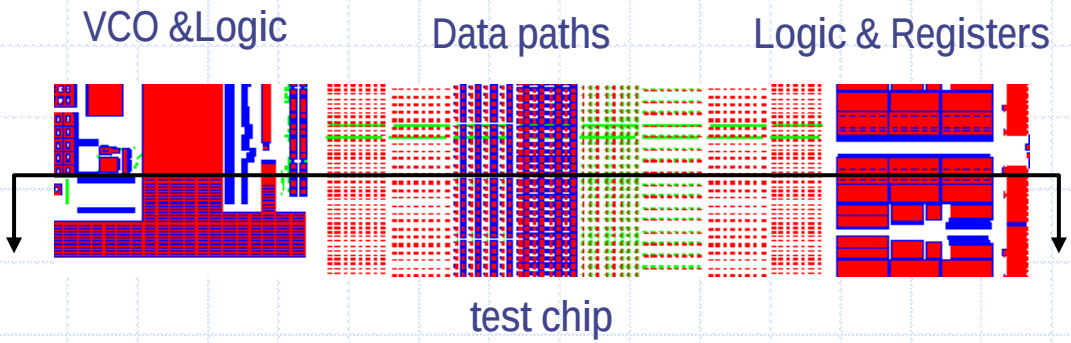


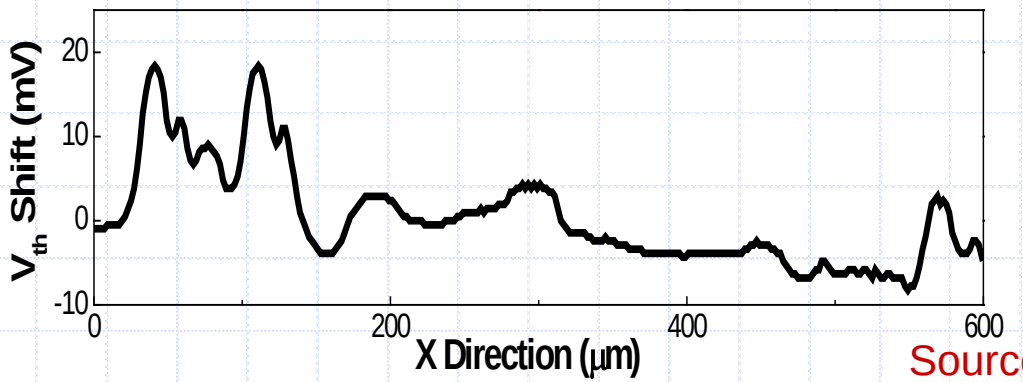
Source: D. Boning

Long Range (mm-scale) Effects - RTA

- Rapid thermal anneal (RTA)
- Length scale: ~mm; layout pattern density dependent
- Approach: Joint TCAD-compact modeling efforts
- Can we do something better than fill?







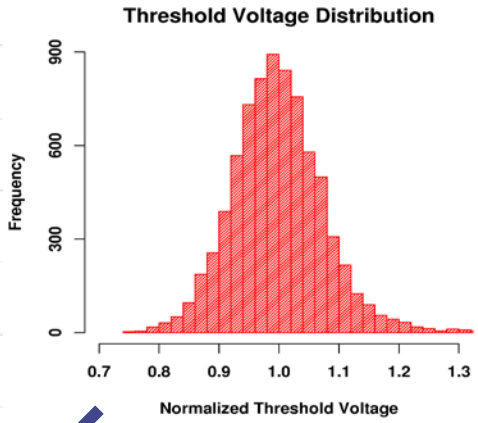
Source: Y. Ye

PD Challenges for 22nm and beyond

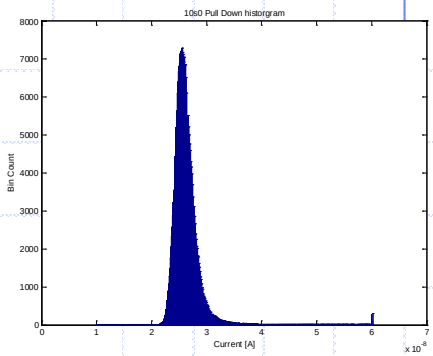
Final: Variability and “resilience” failures

Confluence of variability effects -> SRAM "resilience" fail exposure

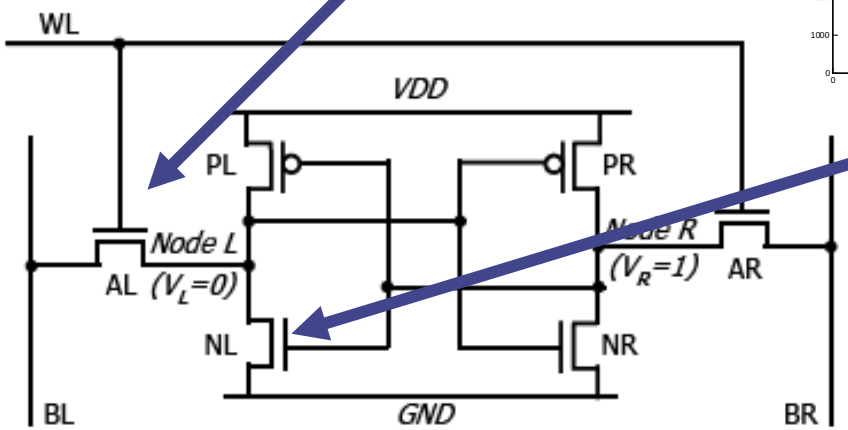
- On-die arrays
  - Need ~5 σ effective cell yield for Mb arrays
  - Vmin issues
- Symmetry/regularity allow
  - Precharacterization / litho optimization
  - Higher array supplies/assist
  - Row/column redundancy
  - ECC



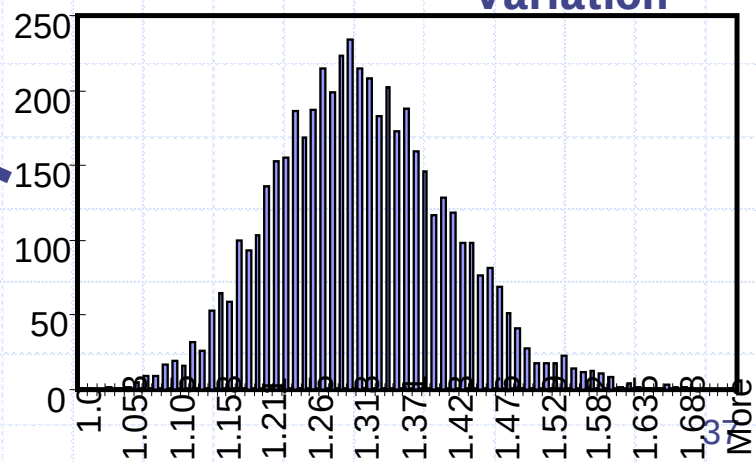
Access device threshold

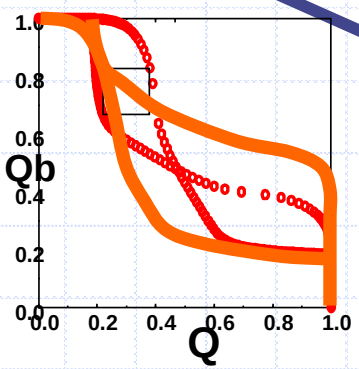


NFET Tunneling



Bitline Cap Variation





Confluence of variability effects: future of "resilience" fail exposure

- Latch, adder, mux, AOI, buffer, wire … resilience?
- Lack of symmetry/regularity
  - What topological, functional analogs do we have to:
    - Precharacterization/litho optimization
    - Higher array supplies/assist
    - Row/column redundancy
    - ECC
  - …. and how would they be supported in our design flows?

Summary

- Skills and expertise that surround silicon implementation at the technology, circuit, system and CAD levels all will play significant role in continued scaling at 22nm and beyond.
- Isolation of skills, however, will be increasingly less possible.
  - eg. Effective routing algorithms will need to leverage knowledge of how wires are created, and how router decisions will impact the resulting electrical parameters of the wire.
- Simple technology abstractions that have worked for many generations like rectangular shapes, Boolean design rules, and constant parameters will not suffice to enable us to push designs to the ultimate levels of performance.
- Physical design must become more technology aware to fully contribute to solving challenging scaling problems.