The Challenges of Correlating Silicon and Models in High Variability CMOS Processes

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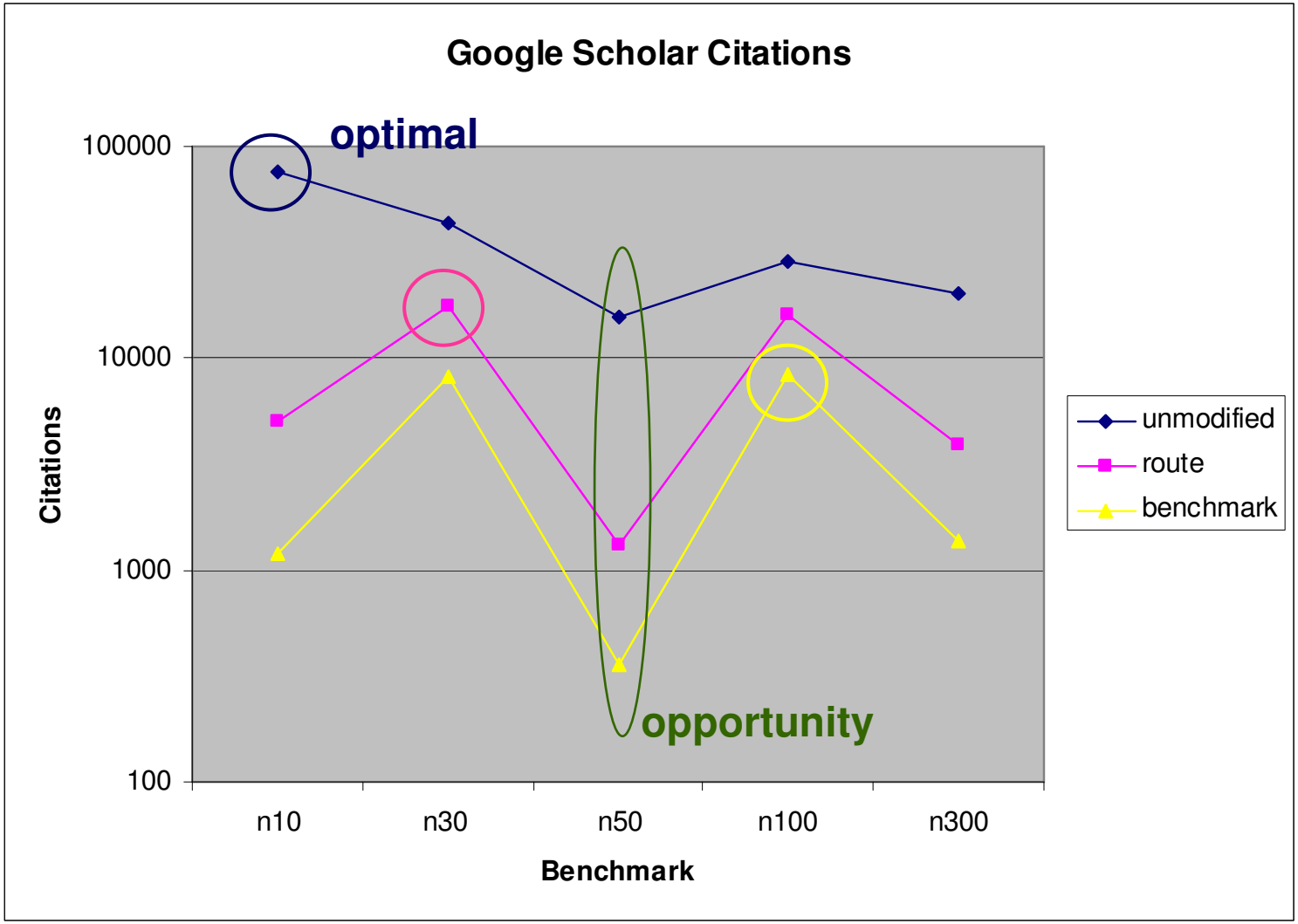
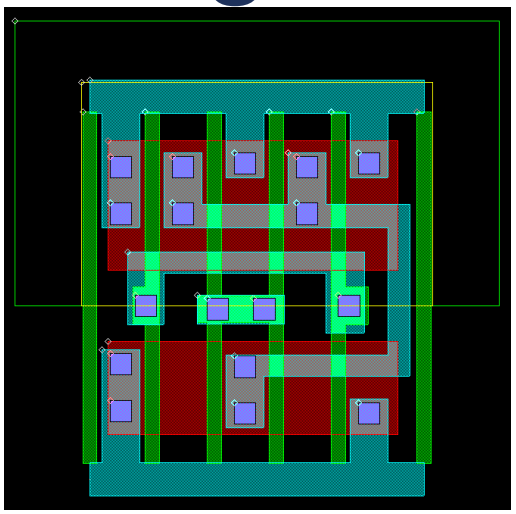
Outline

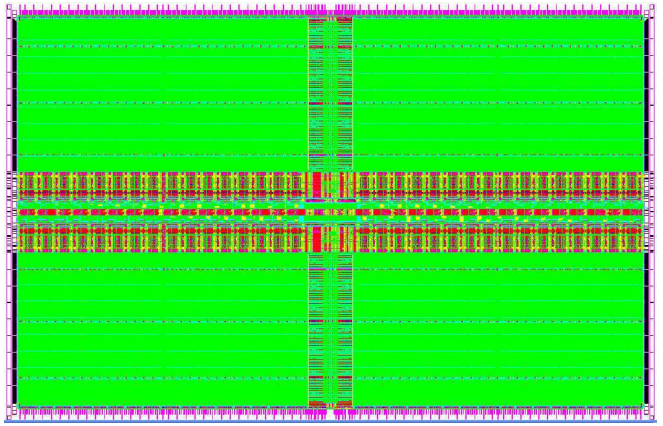
- Background
  - Variability
  - Characterization
- Library validation
- Debug examples
- Conclusions

Benchmark Results



Physical IP is more than NAND gates



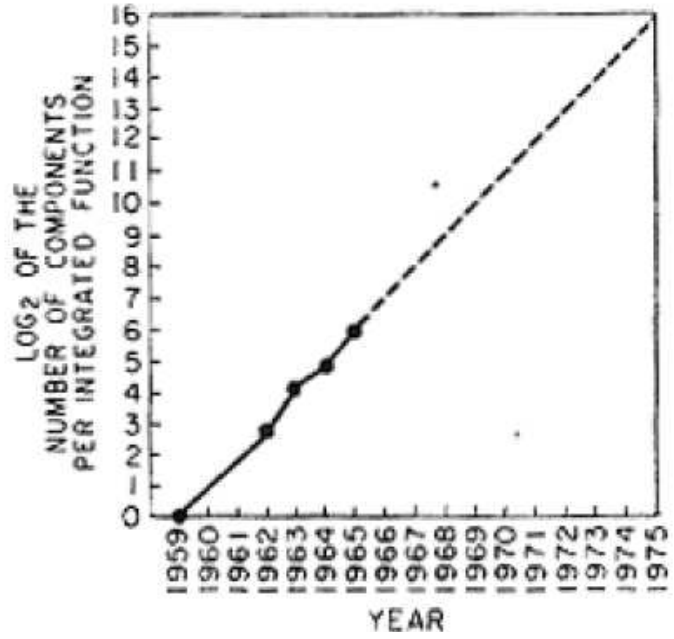


- 15+ foundries
- Up to 8 process generations per foundry
- Up to 11 variants in each generation
- 6+ memory generators
- 900+ standard cells per library
- 200+ I/Os
- 10+ views per cell
- Plus PHY, analog IP, etc.

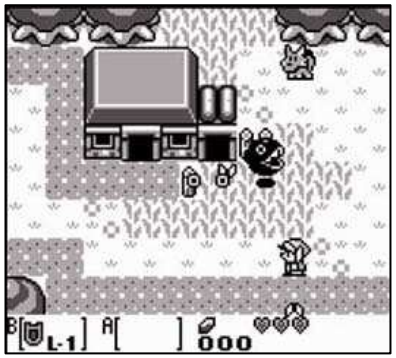
- 300+ libraries per year, each with thousands of individual data elements

Moore's Law

- Original Paper:
  - "Cramming more components onto integrated circuits"
  - *Electronics*, 38-8, 4/19/65
- Tracks changes from 1959 to 1965 and predicts trend going forward
- It's still going…



Feedback: Moore's Law and Consumer Expectations



Nintendo GameBoy (1989)

CPU: 8-bit Z-80 processor, 1.05 MHz
Screen: 2.6" 160 x 144 LCD 4 b/w
Connectivity: 4 players by serial cable

Introductory price - $169

>1000x performance for the same price

© Nintendo

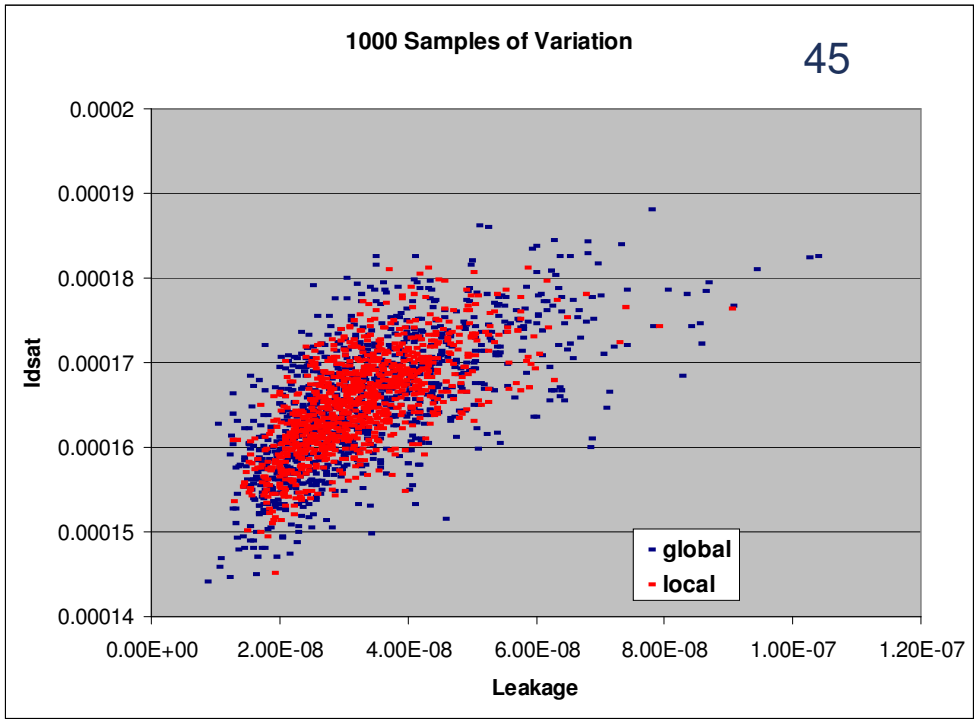
Nintendo DSi (2008/2009)

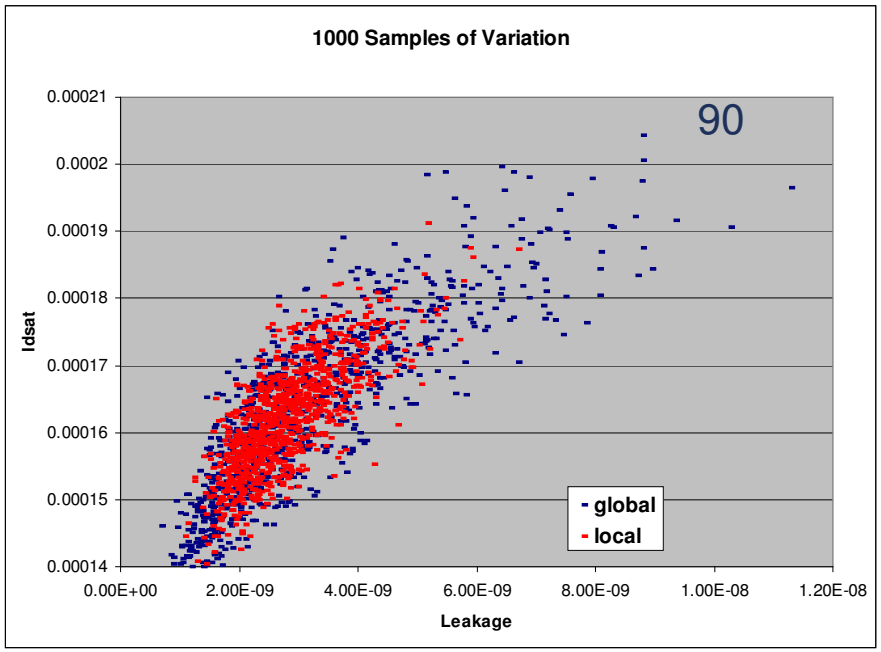
CPU: ARM9™ (133 MHz), ARM7™ (33MHz)
Screen: Two 3" 256 X 192 color LCDs
256MB Flash, AAC audio, 2 VGA cameras
Connectivity: Wifi, web browser, shopping

Introductory price - $169

Variability trends

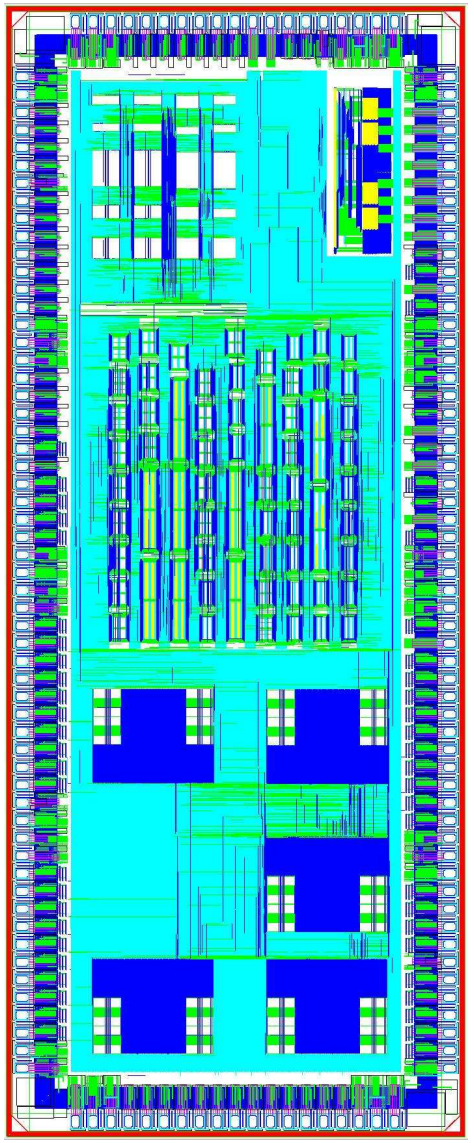
- Non Gaussian behavior
- Local spread close to global
- Reduced correlation





Background

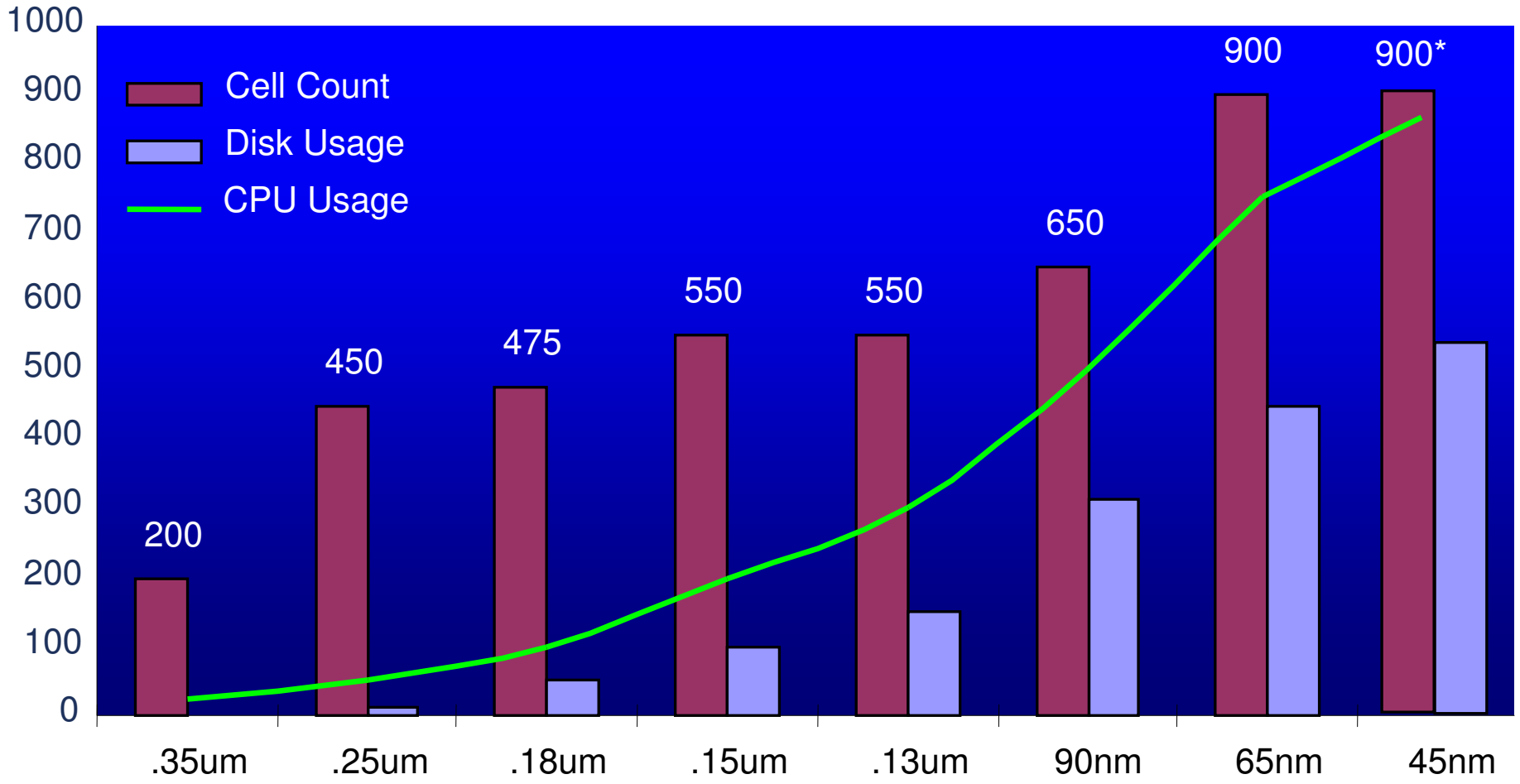
- Classes of test chip:
  - ARM has multiple classes of test chip
    - Library qualification chips
    - Processor qualification chips
    - Experimental test chips
- Chips:
  - 2 32nm tapeouts since 9/08
  - ~40 Tapeouts in 2008, mainly first group
  - Part of shuttle or multi-project wafer
  - Usually 40-100 packaged chips
- Challenge:
  - Silicon validation of library elements (standard cells, memory, IO)



Background cont.

- The library qualification test chip program objectives
  - Verify basic functionality
  - Validate new architectures in silicon
  - Provide silicon correlation for timing and power measurements
- Objectives for other programs (not these chips)
  - Serve as yield predictors or measure defect density
  - Evaluate transistor properties or develop SPICE models
  - Study lithography issues
  - Determine the statistical properties of a process (FEOL or BEOL)
  - Measure reliability

Library characterization history



Characterization History

- Three delay numbers: slow, typ, fast
  - Just too inaccurate
- Linear delay: f(cap)
  - What about slew rates?
- NLDM: table f(cap, slew), interpolate between points
  - Which table? How many points?
  - Multiple voltage support complicated
  - Complex interconnects not modeled well
- Current source models (CCS, ECSM)
  - More complex modeling of device behavior
  - Allows for more accuracy, especially at intermediate points
  - Giant files
- Statistical models…

How much accuracy do you need?

- Depends on tools, stage of design flow
- Need for accuracy varies
  - Preliminary floorplanner needs different accuracy than final extraction flow
- Interconnect modeling needs good, but not perfect accuracy
  - 3D field solver not required, but need more than interpolation between table data points, especially for complex shapes, long distances
- Accuracy is important, but needs to be defined correctly

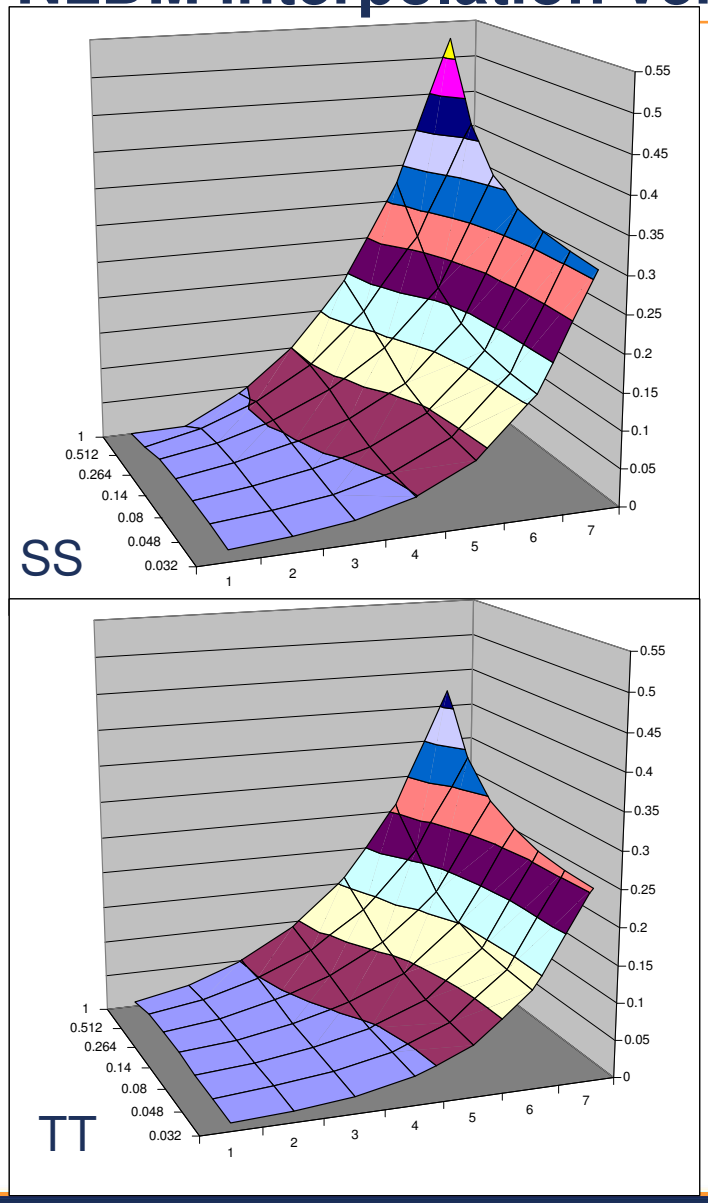
```
"0.015667, 0.020832, 0.030359, 0.048810, 0.086296, 0.161212, 0.311795", \
"0.017252, 0.023636, 0.033981, 0.052357, 0.089780, 0.164684, 0.315177", \
```

These are not “within X% of SPICE”, they are SPICE!

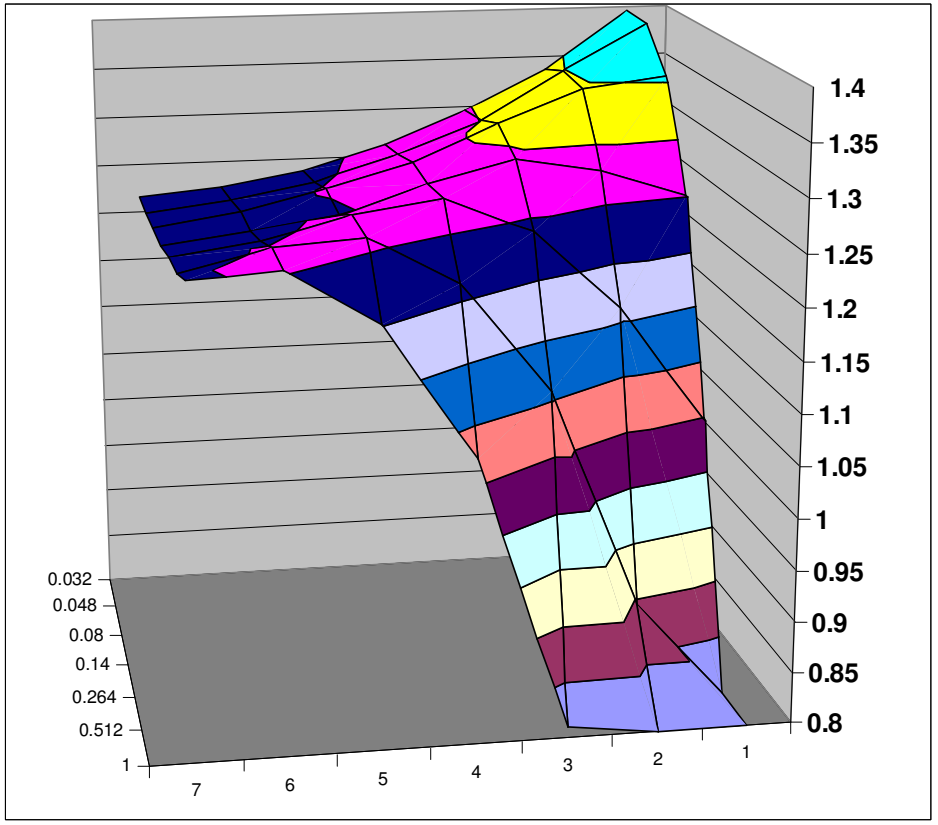
So are these.

```
values("7.117695e-03, 1.329720e-02, 3.667810e-02, 4.492980e-02, 5.068780e-02, 5.180790e-02,
    5.086270e-02, 4.749920e-02, 5.026640e-02, 4.425650e-02, 2.832520e-02, 2.129720e-02,
        1.605390e-02, 9.854060e-03, 5.124280e-03, 2.224300e-03, 1.424661e-03");
```

Accuracy and precision:
NLDM interpolation versus transistor variability

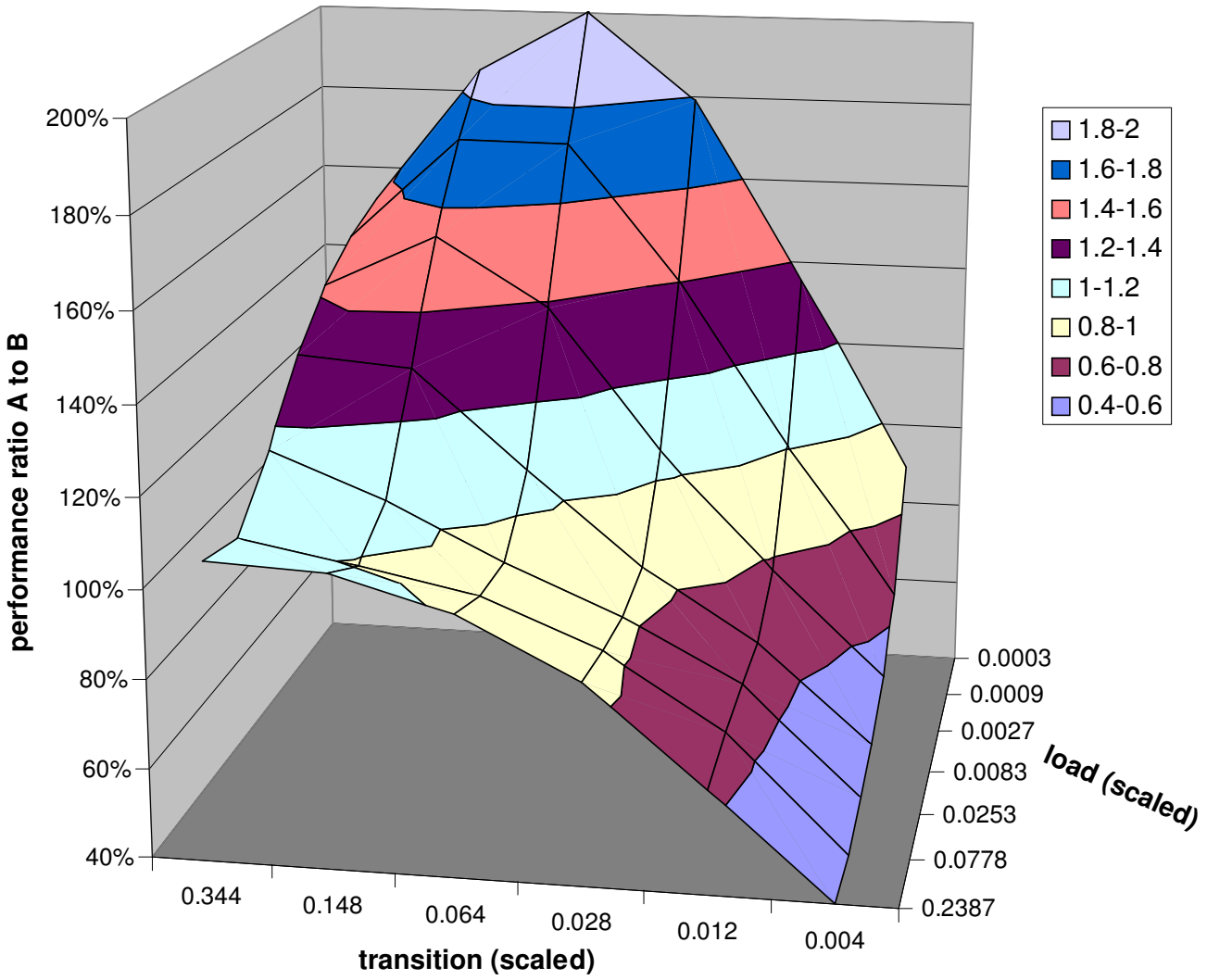


- Interpolation accuracy: 2-3%
- Temperature, voltage variation handled with current source models
- Variability: SS versus TT: -20% to 40%



“Scaling” of standard cell delay

- Relative delay for equivalent cells in two different technologies A and B
- Is A slower than B or faster?



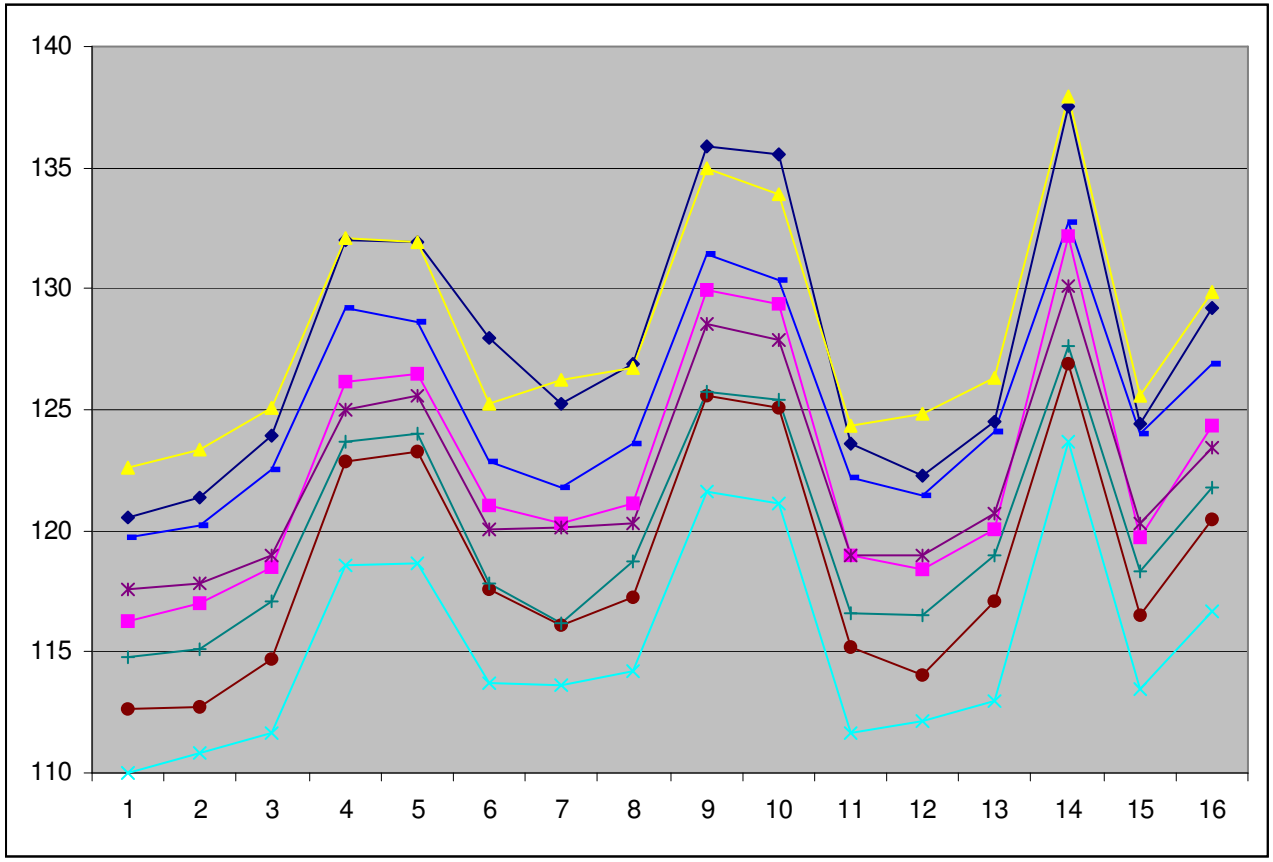
Silicon Validation of Libraries

- Basic idea
  - Measure silicon, compare with model prediction
- Things to measure
  - Delay
  - Power
    - Leakage
    - Dynamic
- Challenges
  - Where does silicon fit in “corners”
  - Measurement accuracy
  - Single point versus table
  - Model versus SPICE
  - SPICE versus silicon
  - Parametric variation
  - Presence of “soft” defects

Overcoming challenges

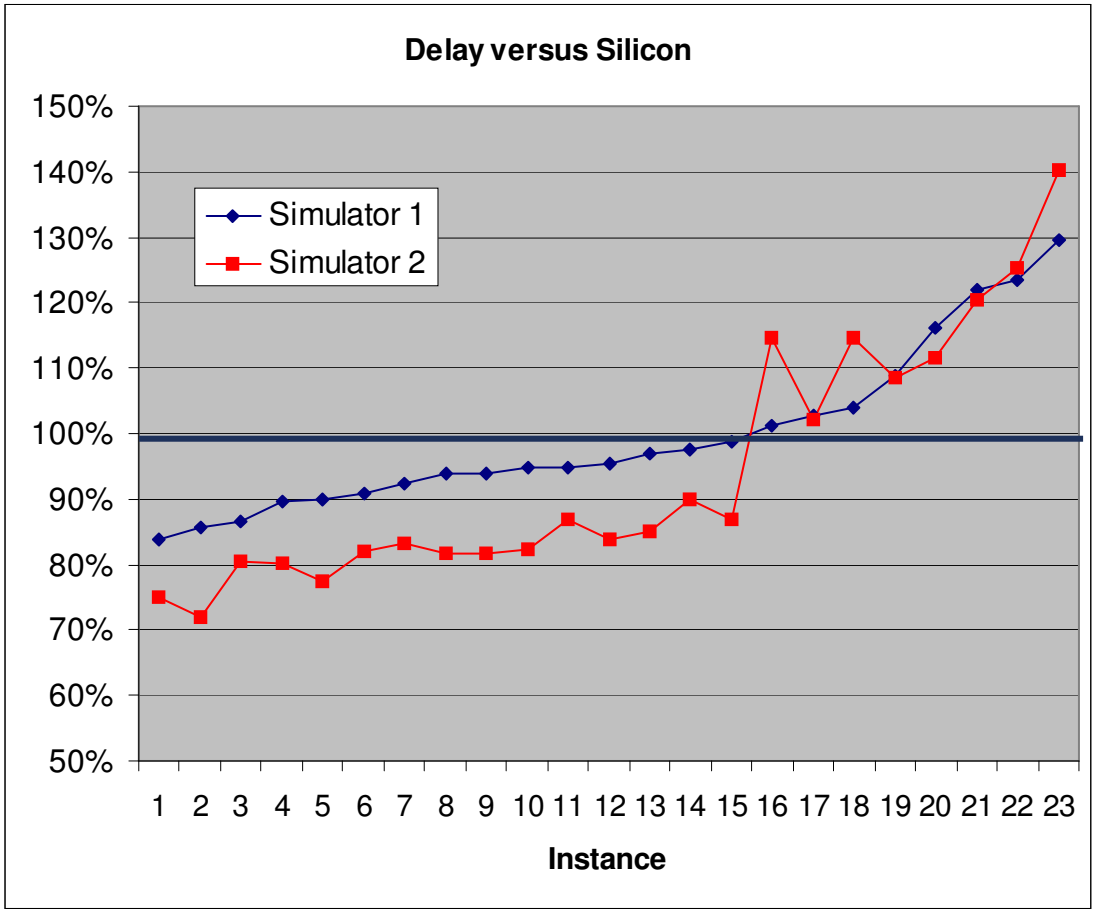
- Challenges
  - Where does silicon fit in “corners”
    - Oscillator data, test structure data
  - Measurement accuracy
    - Understand equipment, measure deltas
    - Big challenge for power
  - Single point versus table
    - Carefully select design point
    - Shmoo across voltage, temperature
  - Model versus SPICE
    - Understand characterization issues
  - SPICE versus silicon
    - Work with foundries to understand
  - Parametric variation
    - Design around local variation
  - Presence of “soft” defects
    - Look for trends across chips

Validation in practice



- Variability observed for similar objects across chips
- "Correct" value somewhere in the middle
- Does this validate it?

How Close is it to SPICE?

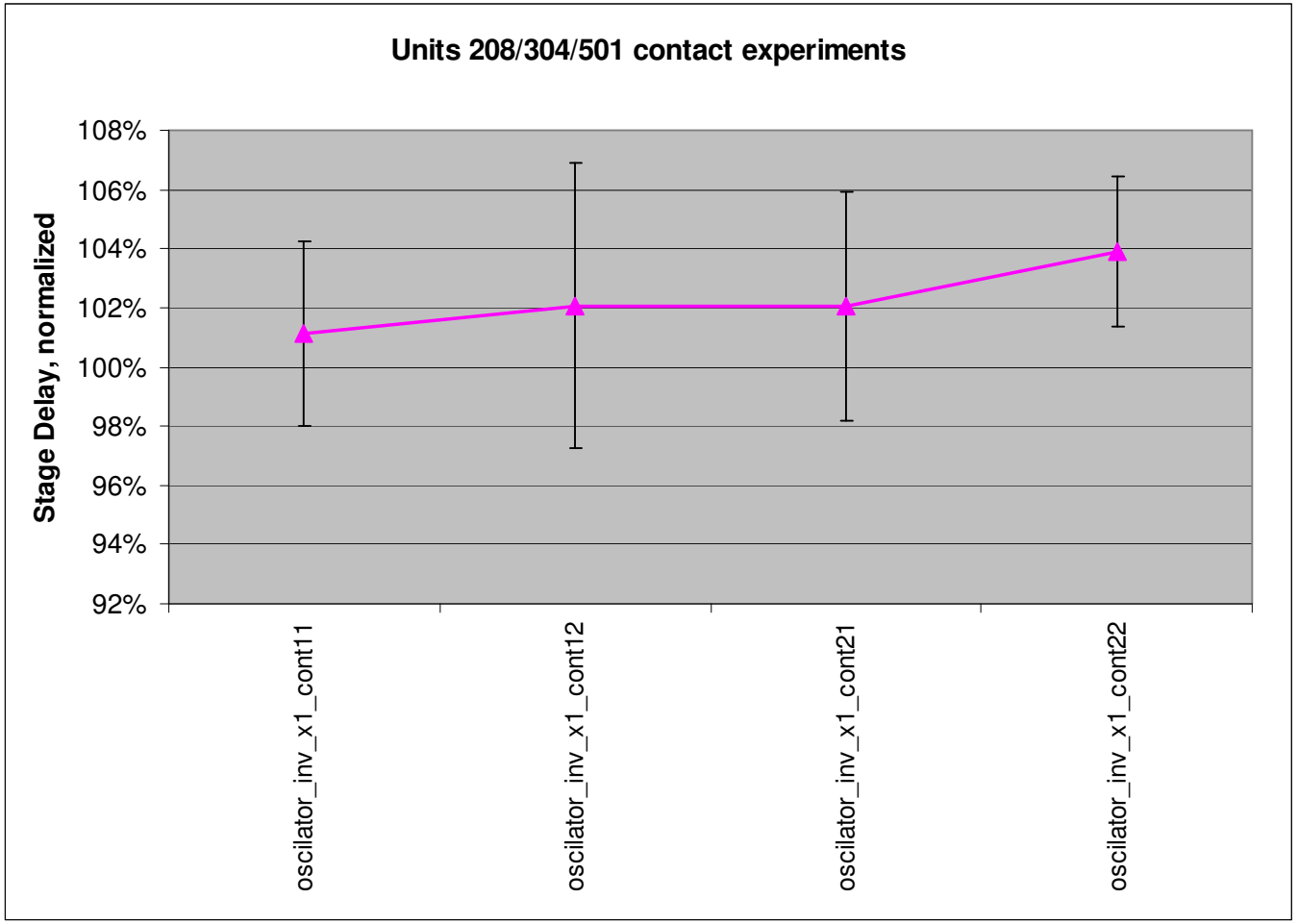


- Significant difference between simulators observed
- Variety of issues represented
  - Model file interpretation
  - Performance options
  - Extraction issues
  - Silicon variability

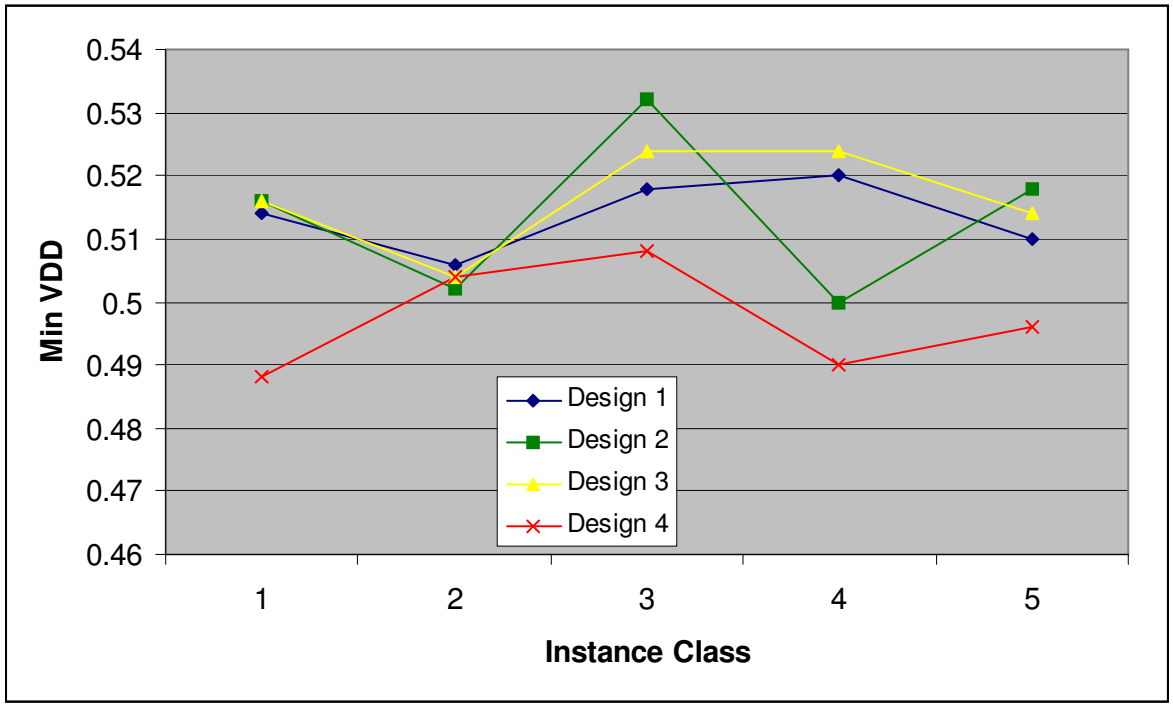
Remember this the next time some tool claims to be within X% of SPICE

Number of Contacts (Yield vs Speed)

- Typical questions after early data collection (small number of units)
- 3% shift in mean but what is mean – 3σ?

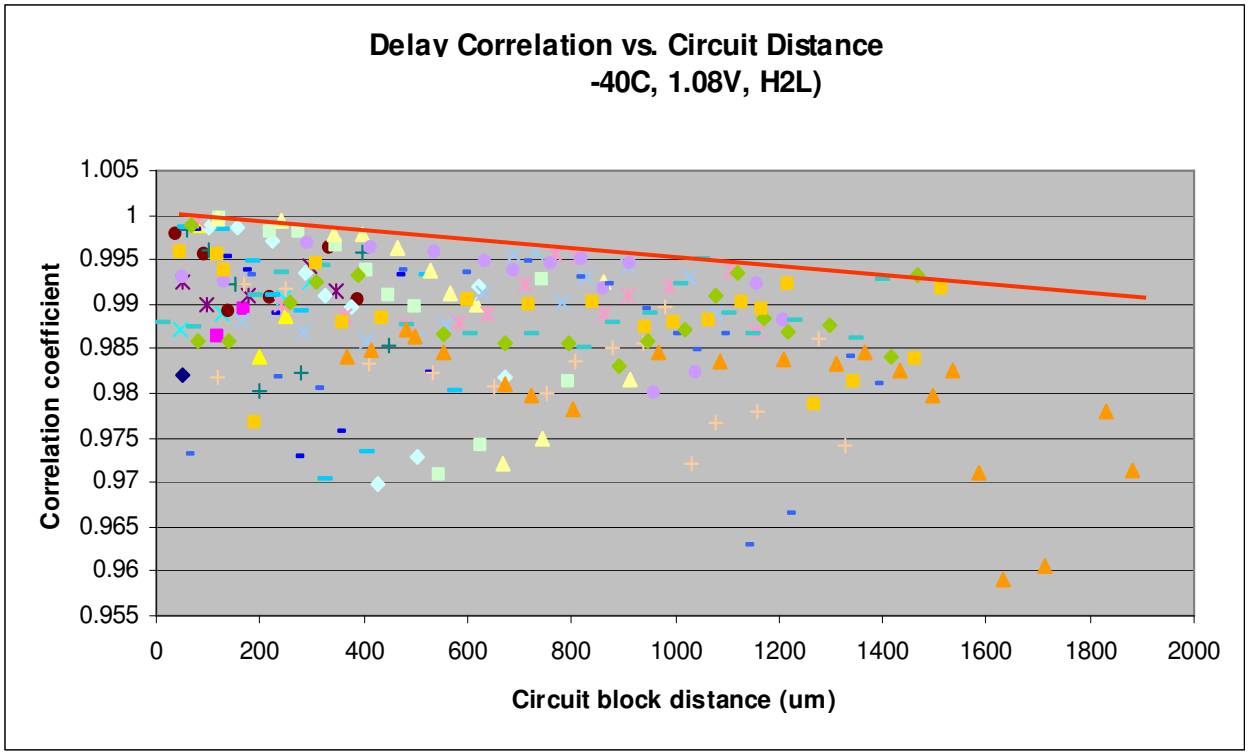


Min VDD for Different Design Styles



- Question: Are any of these designs better?
- Statistically: No
- But: More data might give the edge to design 4

Variability and Validation



- Look for correlation
- 65nm data
- Result: small, but measurable, distance-based effect observed

Sources of Variability

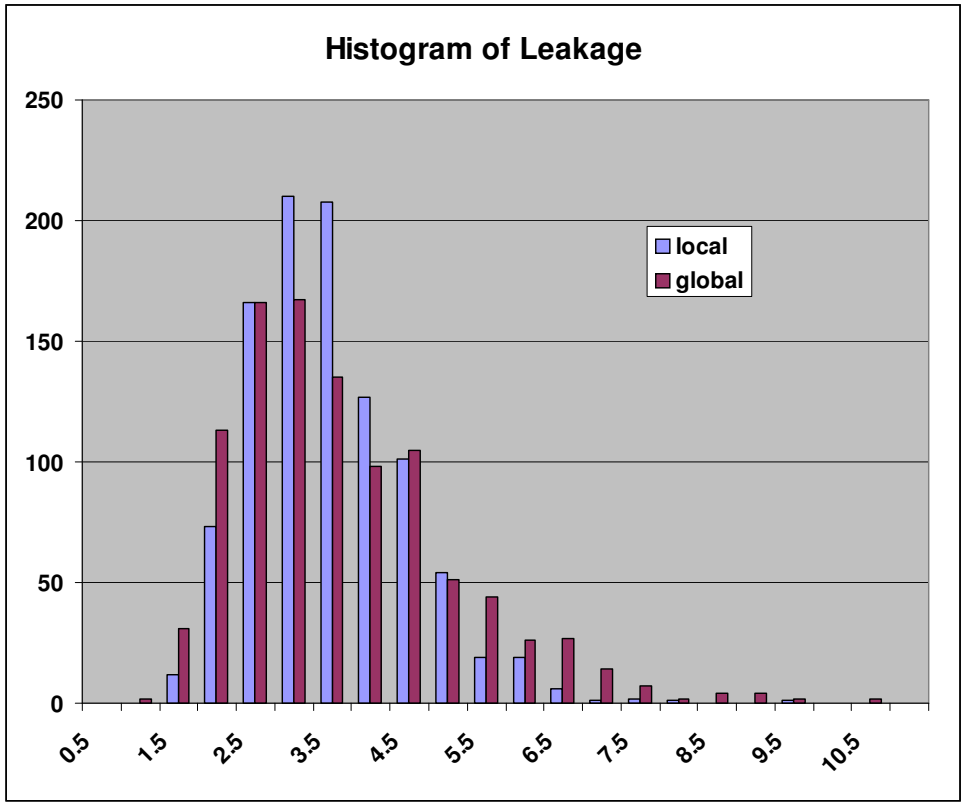
- Lithography
  - Line edge roughness
  - CD variation
  - Influence of neighbors
- Device
  - Well boundary effects
  - Variation between N and P
  - Stress/strain effects
- Interconnect
  - Dielectric variation
  - Via/contact quality
  - Metal width/height variation
- Deterministic versus Random

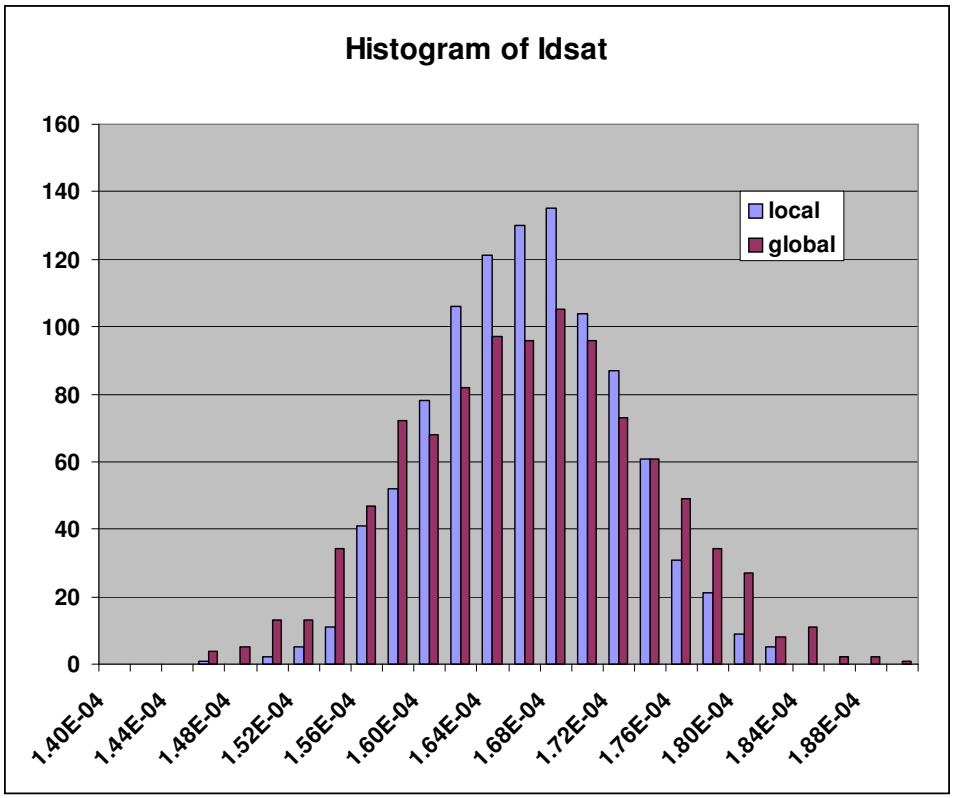
Effects of Variability

$$I_d \approx \mu \cdot C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_t)^{\alpha}$$

- Leakage
  - Variation in L, Vt, μ, t_{ox}
- Performance
  - Changes in L, W, R, C, Vt, μ,
- Min VDD
  - Changes in Vt, L, W
  - SRAM bit cell main limiter
- Dynamic power
  - Changes in C
  - Side effect of changes in performance, leakage
- Yield
  - Indirect result of others
  - Parameter goes beyond spec + tolerance

Local Variation Dominates in VDSM

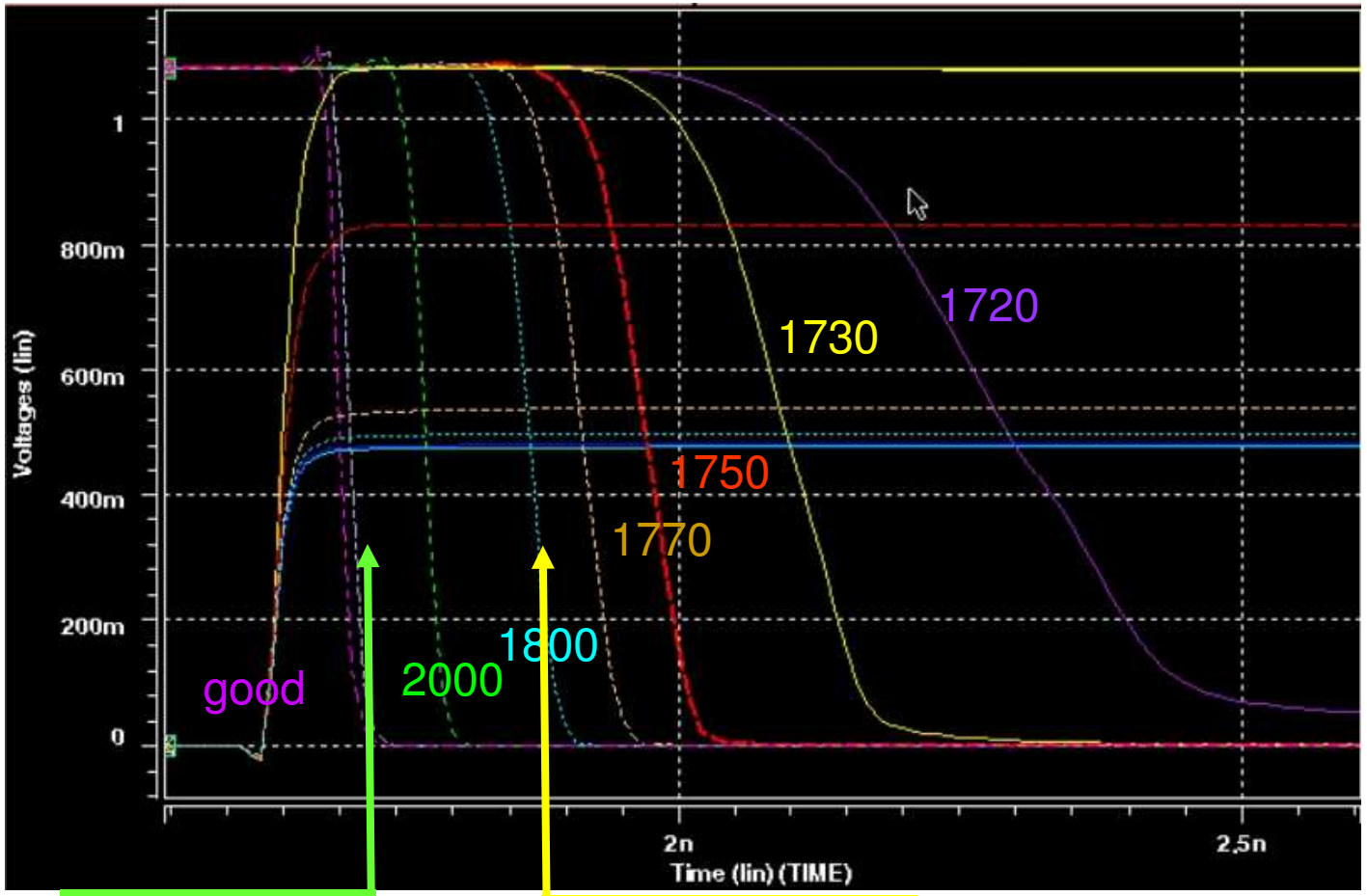




1000 Monte Carlo samples, 45nm technology

- Local variation (within chip) is nearly as much as global variation (between chips) at 45nm

Critical Defect Behavior



Resistance (Ω)	1700	1720	1730	1750	1800	2000	3000
Delay	SA1	600ps	400ps	250ps	150ps	70ps	<10ps

Critical Variability

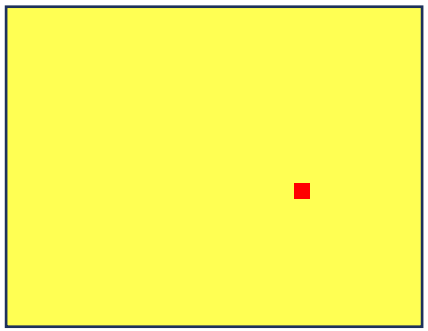
- Designed for a predetermined operating point, plus margin
- Example: SS Corner, 0.9V, 125C, 0 slack
  - Case 1: TT silicon, 0.9V, 85C
    - >2X nominal delay will still function correctly
  - Case 2: SS silicon, 0.9V, 85C
    - ~20% extra delay will cause failure
  - Influential factors:
    - Process, voltage, temperature, slack, noise
  - Expected silicon distribution: SS < 1%, TT(+/-) > 50%
    - Might expect a 1-2% yield hit if SS corner just misses timing
  - Guaranteed silicon distribution: None (usually)
    - Could wind up with no yield 1-2% of the time (1 week per year)
    - Or worse…

Outline

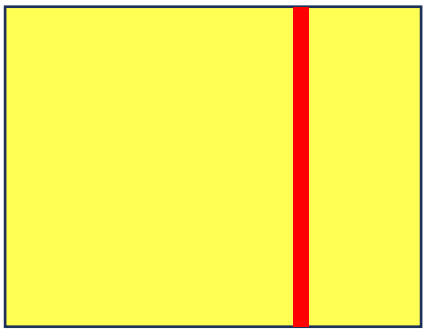
- Background
  - Variability
  - Characterization
- Library validation
- Debug examples
- Conclusions

Key to Memory Debug: Bit Mapping

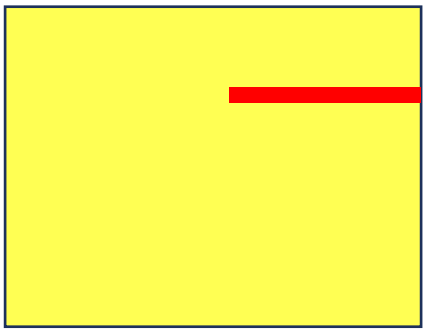
- Pass/Fail information is adequate for production testing
- For yield improvement, debug, system bring-up, etc., it is also useful to be able to identify each failing address and data pattern
- Need logical to physical mapping for this also
- Some common patterns are shown below:



Single Cell

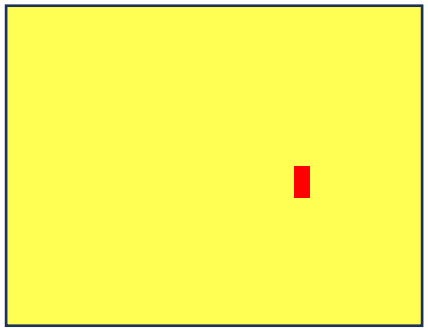


Entire Column

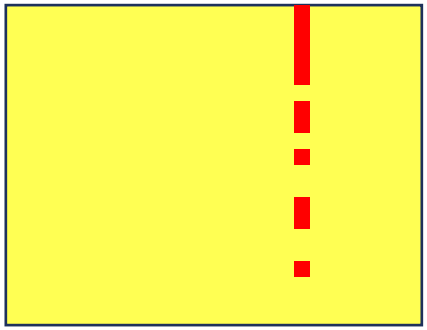


Half Row

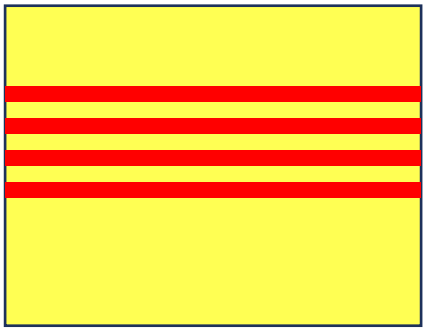
Learning From Bit Maps



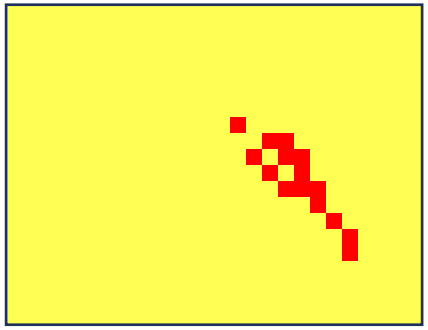
Vertical Pair:
Bit Line Contact



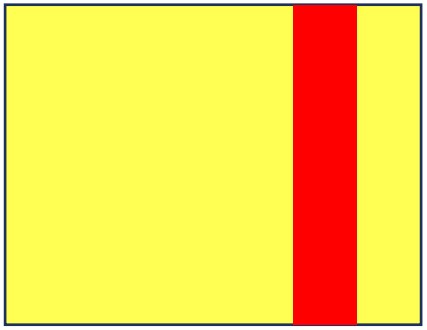
Partial Column:
Resistive Bit Line Short



Multi-Row:
Address Decoder



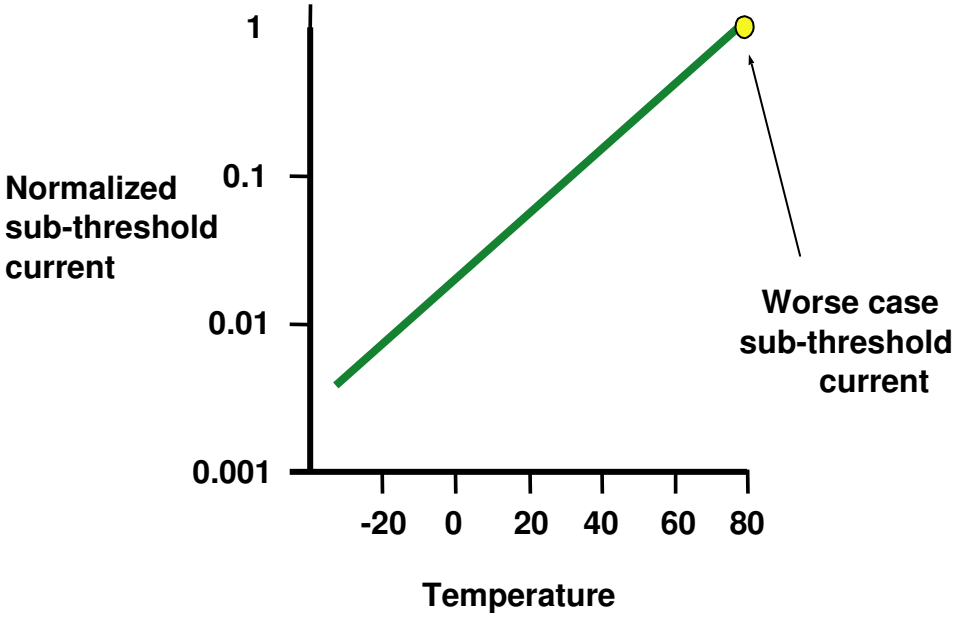
Swath:
CMP Scratch



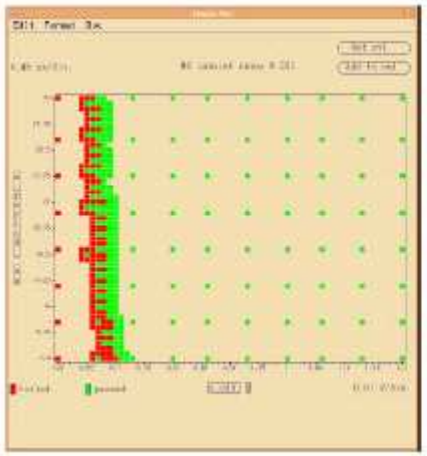
Entire Bit:
Sense amp, I/O

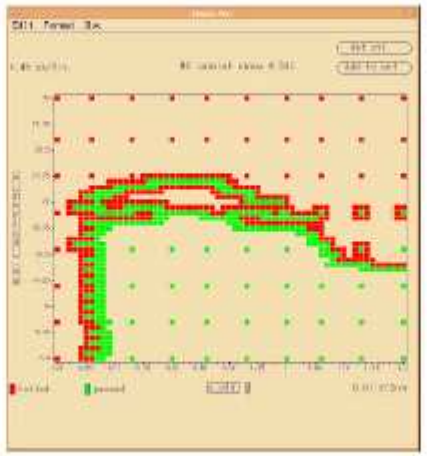
Catastrophic:
Timing circuit

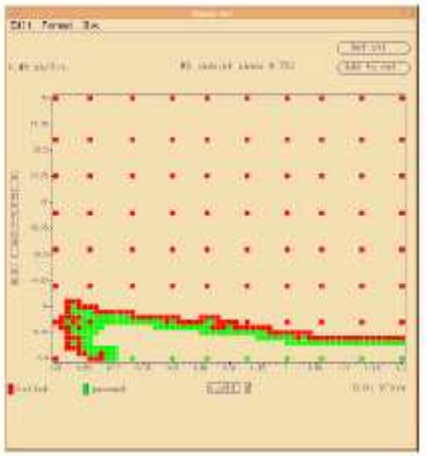
What can happen?



- Temperature related leakage problem
- Root causes
  - 5-10X worst case leakage
  - Circuit marginality

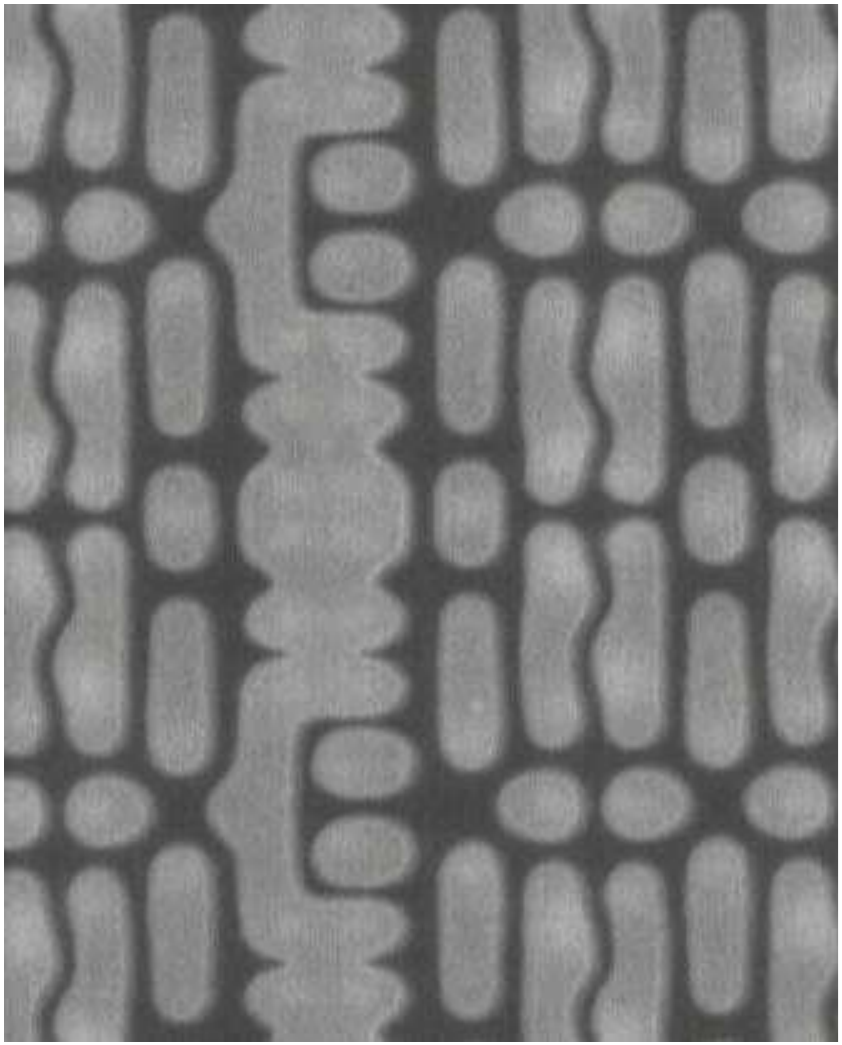




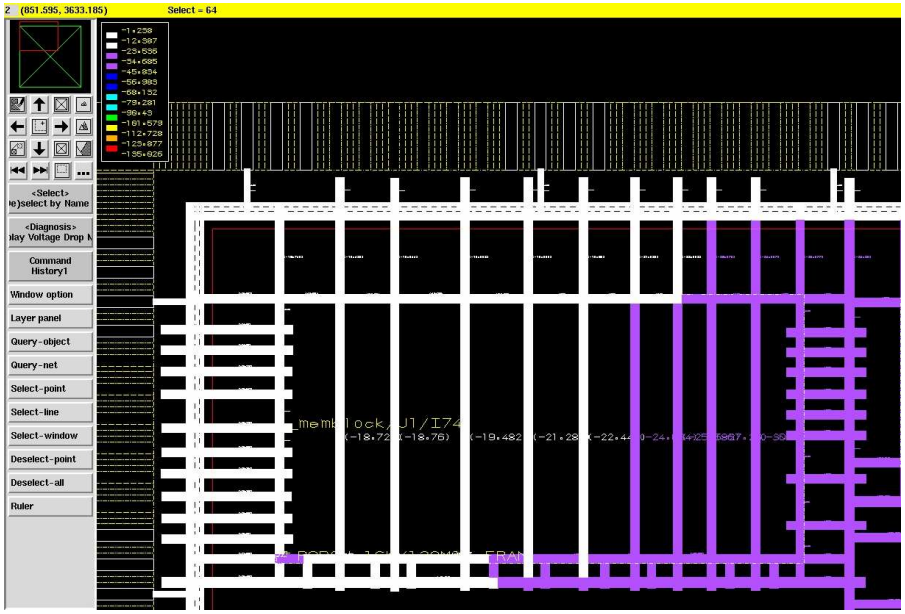


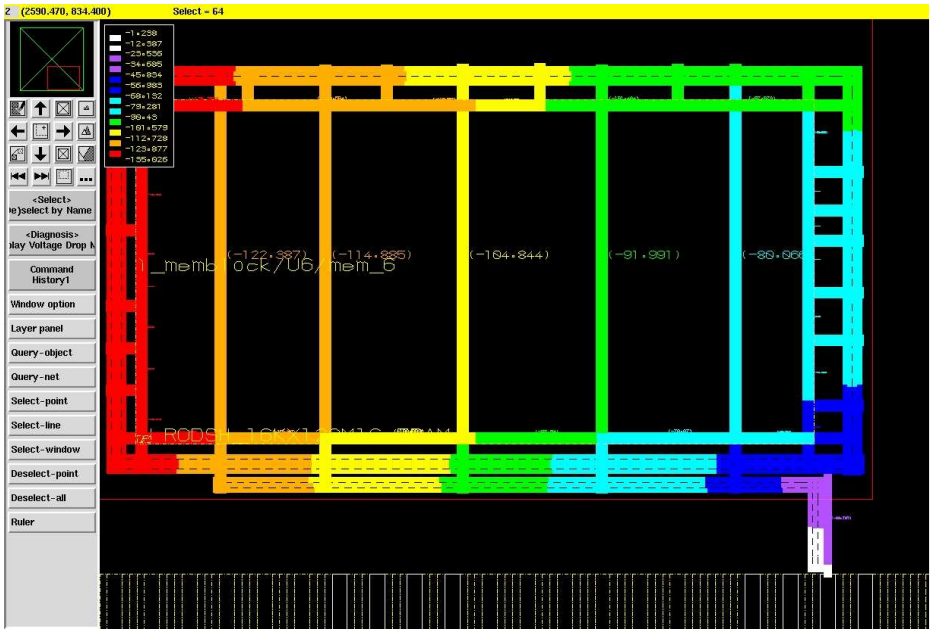
Lithography troubles

- Early silicon may be affected by incomplete or improper processing
- This is less common later in process cycle (memory optimized first)
- May still be an issue for logic



Power Design





- The good and the bad of power connection
- Memory provider can only account for so much!
- More margin = less performance

Analog problem: Read disturb fault

- Data node voltage increases with successive reads
- Given time, settles back to zero
- Root cause: defective ground contact

Conclusions

- Validation is more complicated than you'd think
- Variation increasingly important
- Understanding sources of variation helps
- An effective debug methodology helps when new troubles arise
  - Tools
  - Infrastructure (silicon, equipment, software)
  - Experience

- Feel free to send questions to rob.aitken@arm.com