New Strategies for Gridded Physical Design in 32nm Technologies and Beyond

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Outline

Manufacturing Challenges

Litho dominates a long list of threats to design intent

Solution Roadmap

Equipment enhancements are no longer the knight in shining armor

Design/Manufacturing Co-optimization

What can we actually manufacture?

1D GDR Results

Physical design can be simultaneously manufacturable and efficient

Future Directions

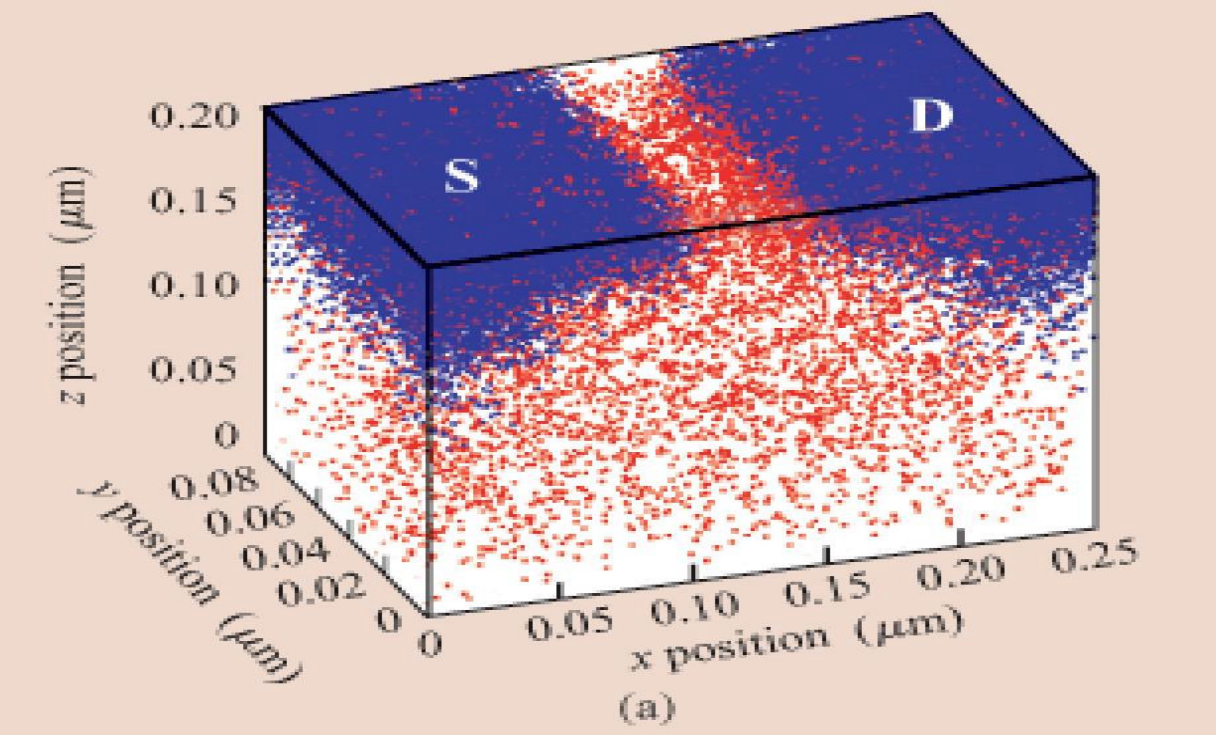
DP plays well with 1D GDR

Conclusions

Manufacturing Challenges

Random Dopant Fluctuation (RDF) -> dVt

- Causes significant Vt variation
- Under 100 dopant atoms per channel
- Dopant atom location matters

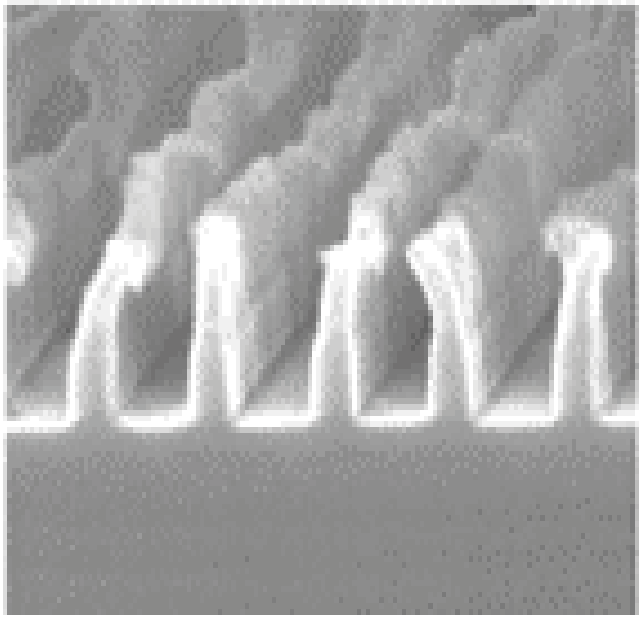


Picture: IBM Journal of Research and Development

Manufacturing Challenges

Line Edge Roughness (LER)

- Due to a variety of factors, including high aspect ratio and problems controlling soft photoresist
- Wider poly lines can short to Con
- Narrowing of poly lines increases I_{off}
- Can also affect vias, increasing resistance



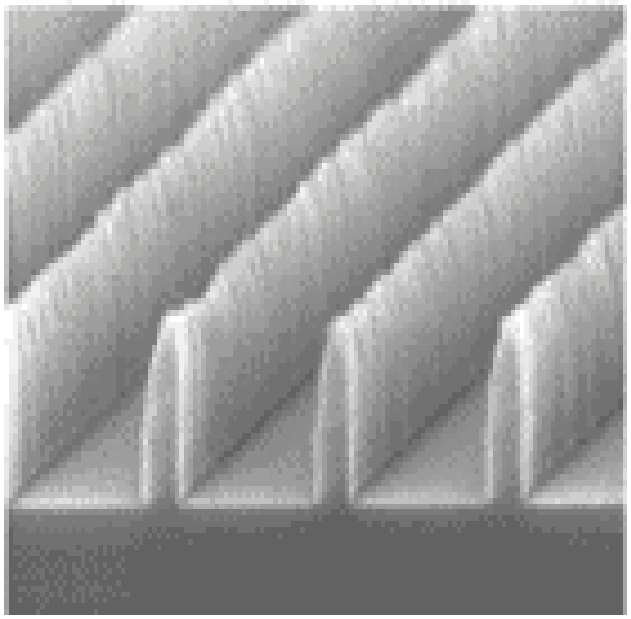


Figure from Bill Bosch, Solid State Techology, July 2004

Manufacturing Challenges

Critical Area / Random Particle Defects

- Sensitive to Pitch

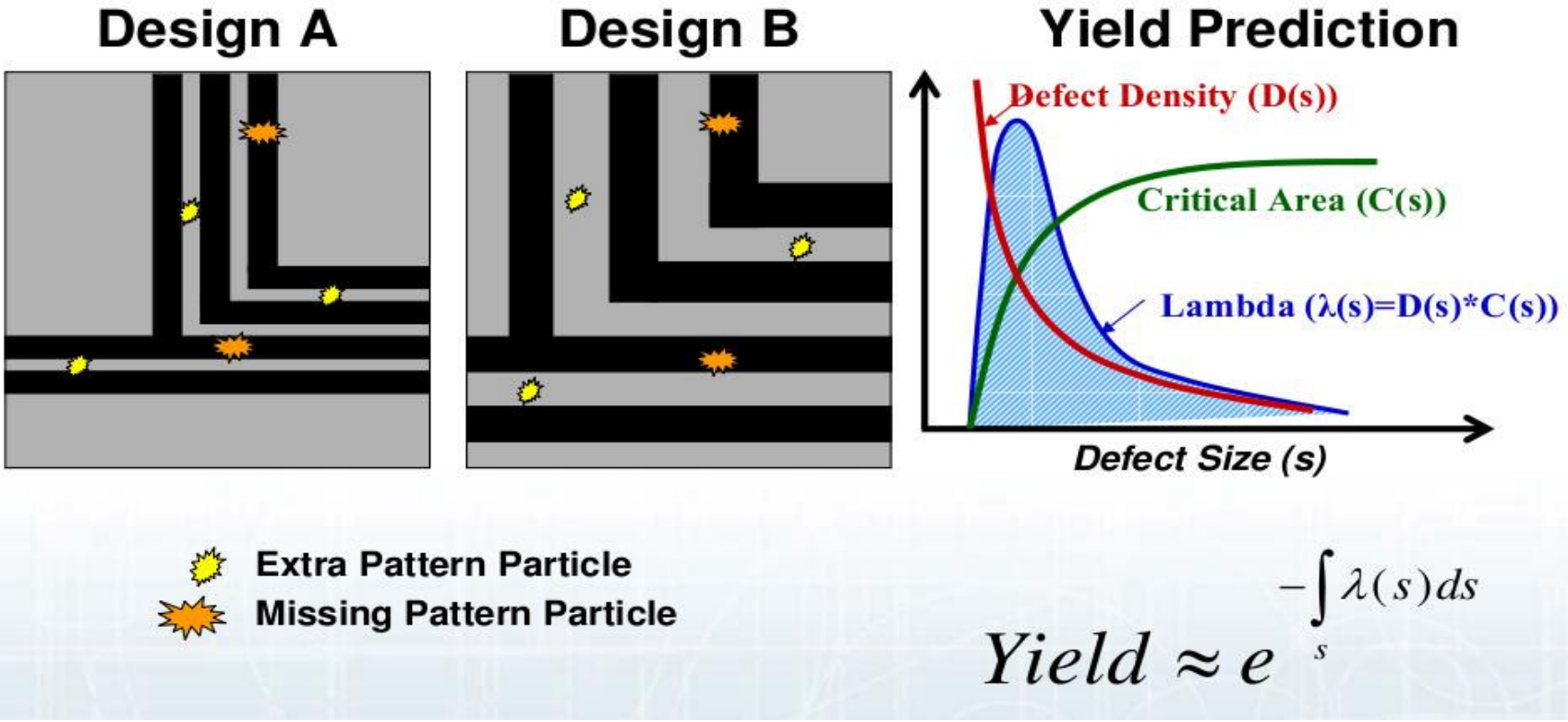


Figure from David Abercrombie, Mentor Graphics, EDA Tech Forum, 2007

Manufacturing Challenges

Chemical Mechanical Polishing (CMP) dishing and erosion caused by

- Variable pattern density
- Soft metal
- Porous low-K dielectrics.

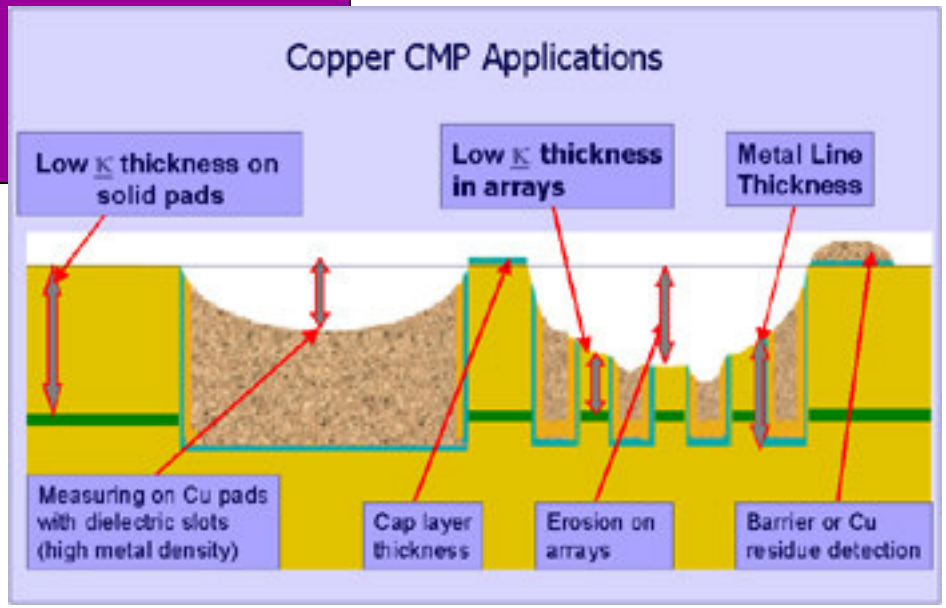


Figure: http://www.nova.co.il/134-en/Nova.aspx

Etch Skew and Microloading

- Pattern density variability also leads to different rates of etchant consumption and variable etch depth.

Manufacturing Challenges

Stress Variation

- Potential for > 40% Idsat shift
- Sensitive to poly-STI distance
- Contacts disrupt strain layer
- BSIM4 device model does not include context impact on stress

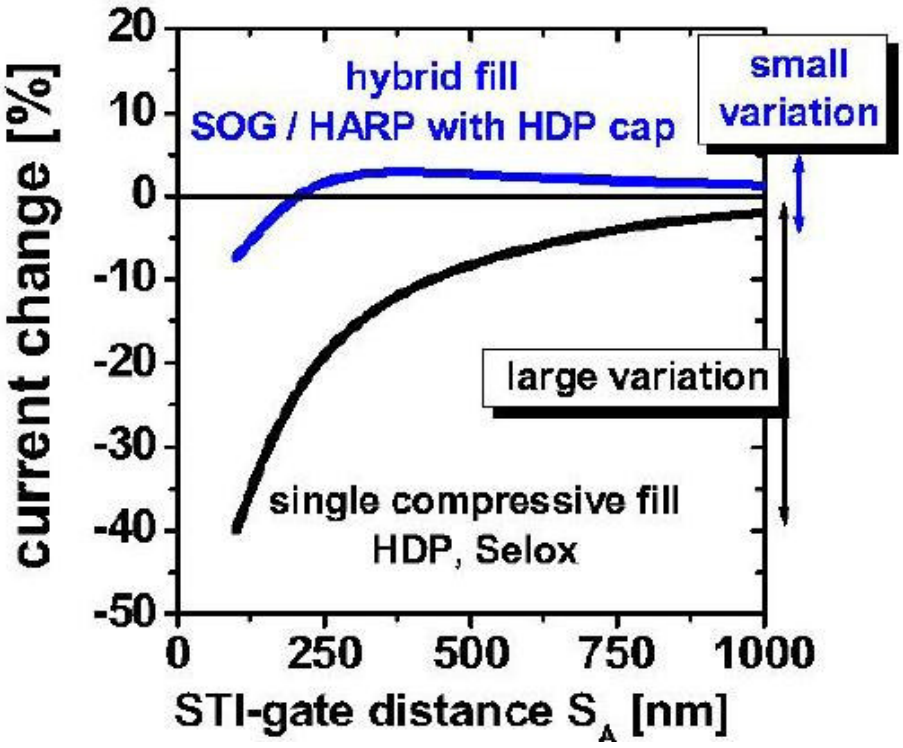
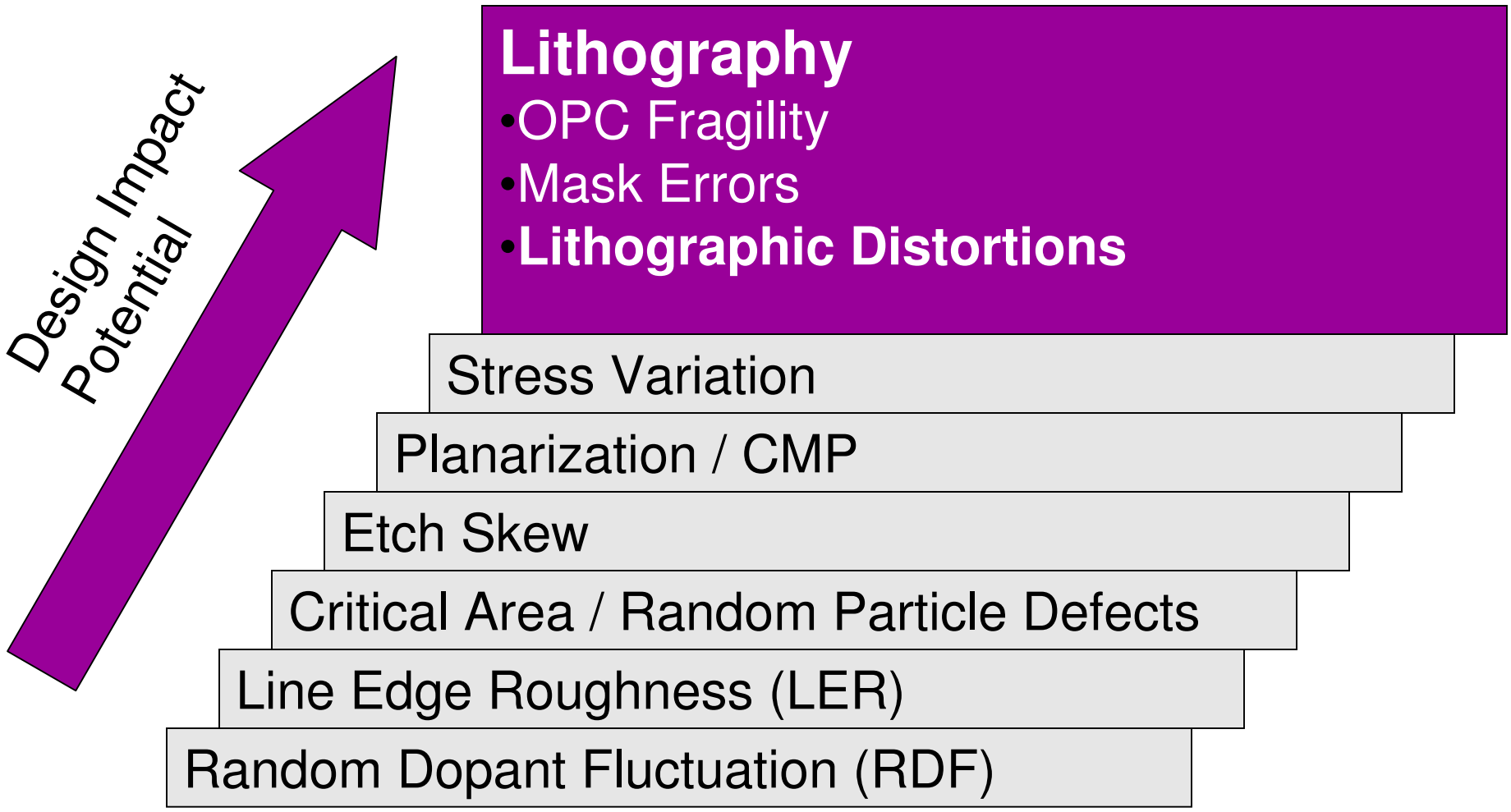


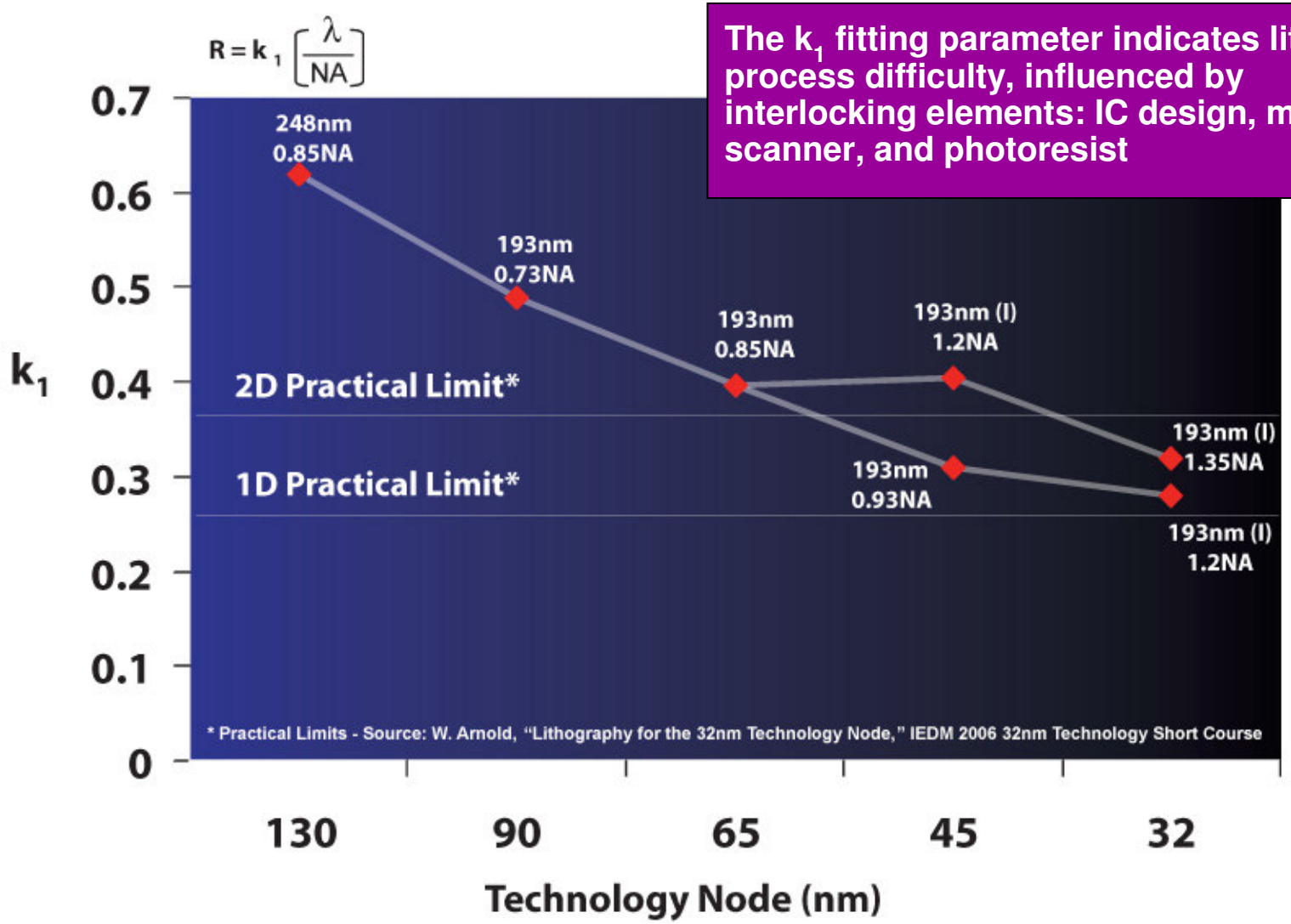
Figure: M. Stadele, et. al, Qimonda AG, VLSI-TSA 2008

Manufacturing Challenges



Optical Equipment Trends

The k_1 fitting parameter indicates litho process difficulty, influenced by interlocking elements: IC design, mask, scanner, and photoresist



Litho Impacts: Sub-threshold Leakage

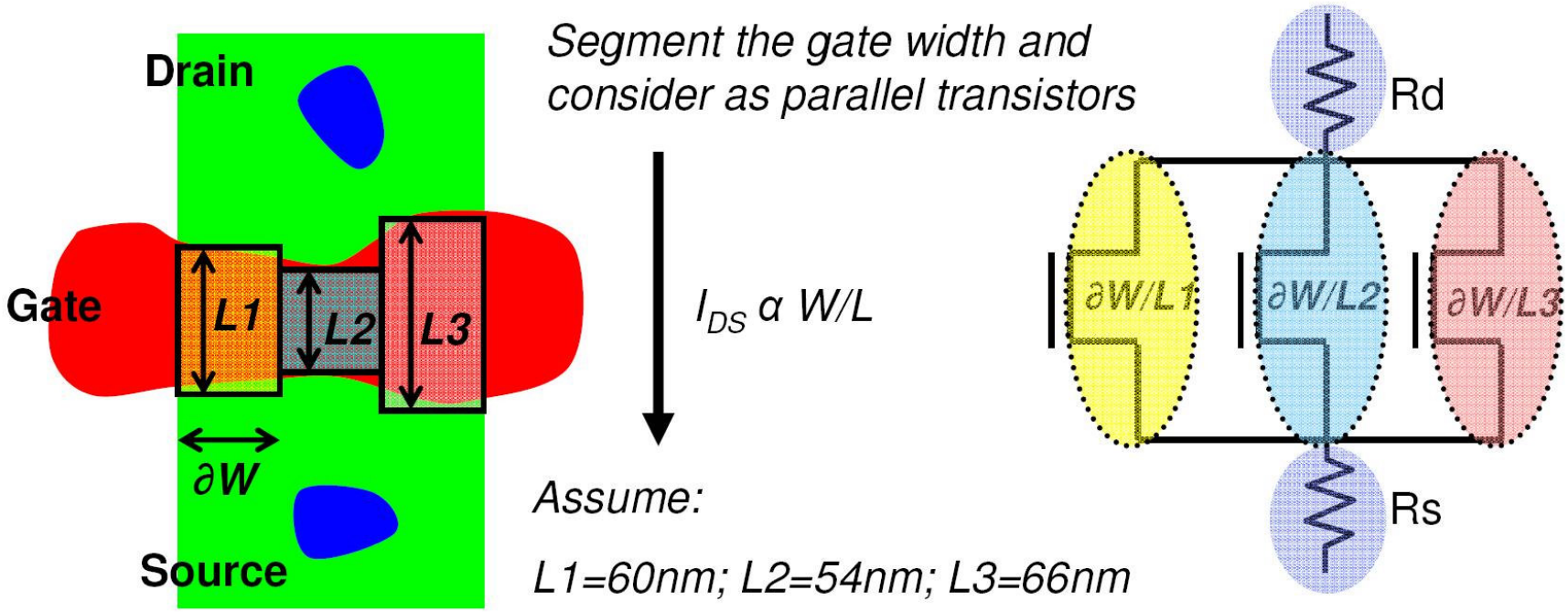
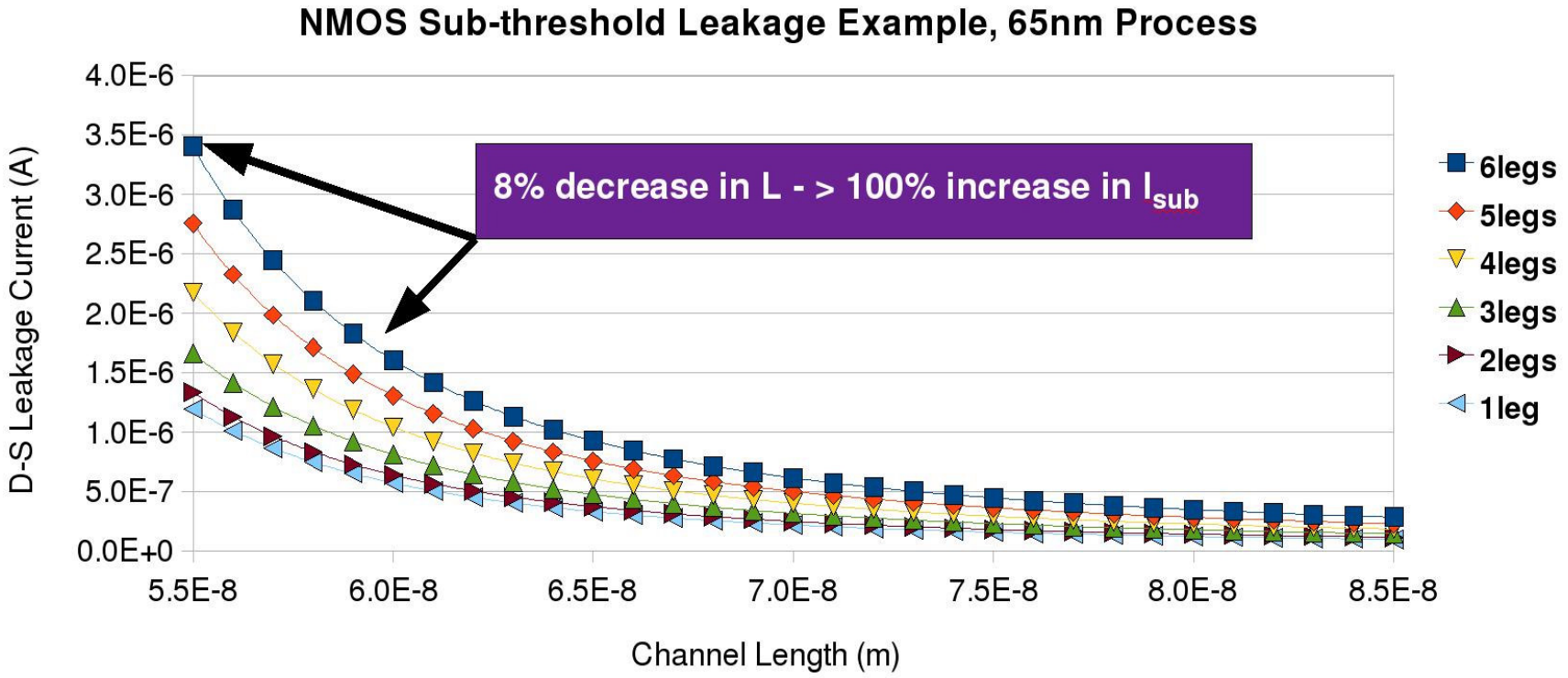


Figure from IBM presentation, SPIE Advanced Lithography Course, 2008

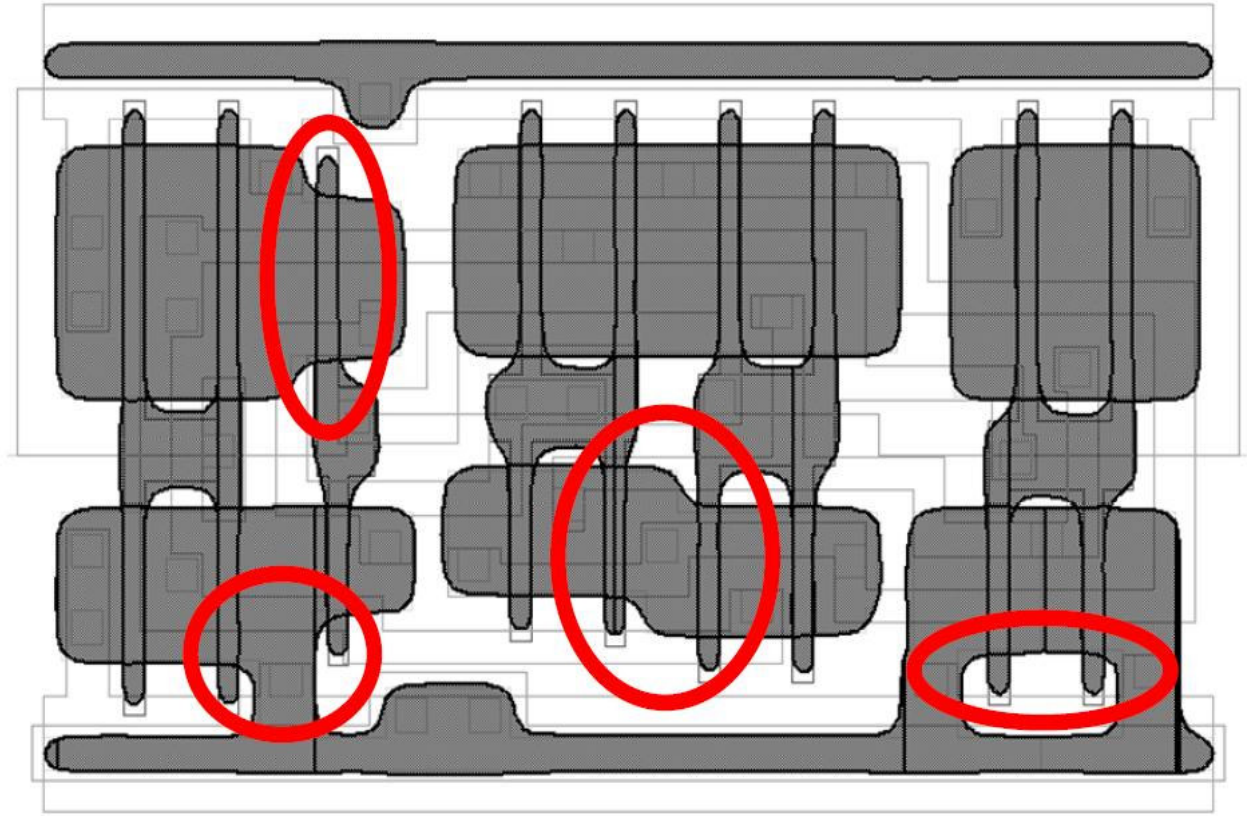
- **Lithographic pattern distortion such as channel necking (pinching) and line-end shortening change effective gate lengths**
- **Contact resistance and effective channel width can also affect I_{on} & I_{off}**

Litho Impacts: Sub-threshold Leakage



- **Increase in sub-threshold leakage is non-linear with L decrease**
- **Short width effects amplify the effect**

Litho Impacts: Drive Variability



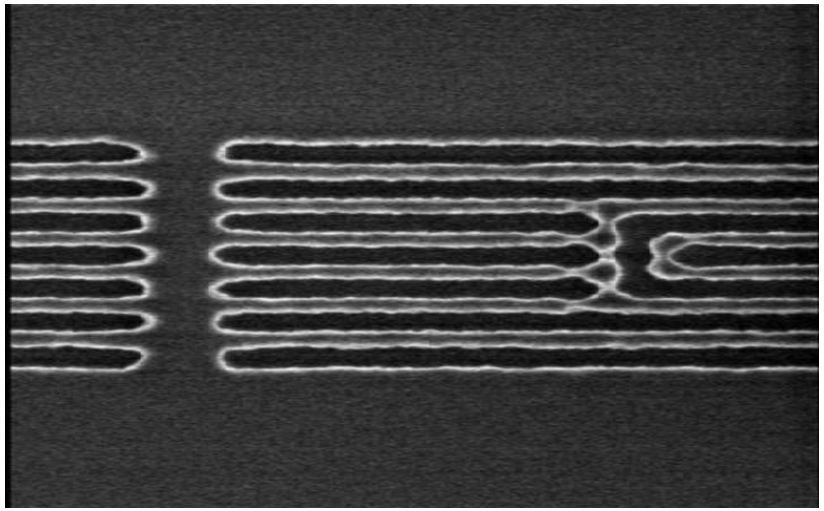
Lithographic simulation results, 90nm process

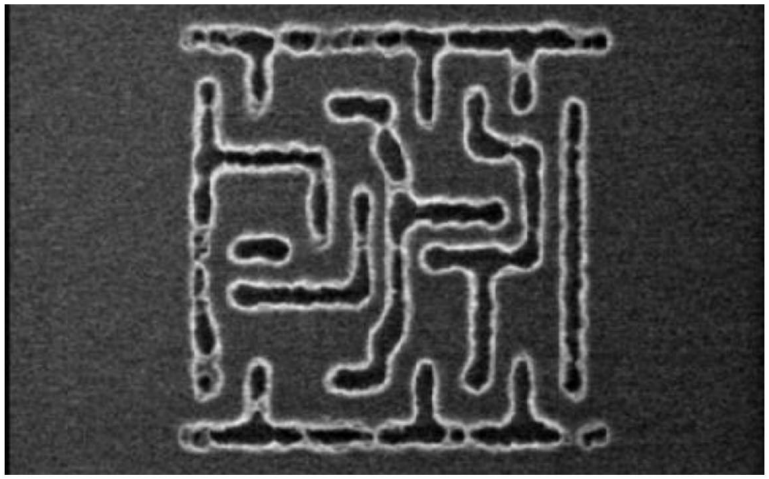
Image: Puneet Gupta, DAC 2008

- **Diffusion rounding another source of drive variability**

Litho Impacts: Defectivity

Even 45nm structures with OPC/RET that are DRC clean can fail.





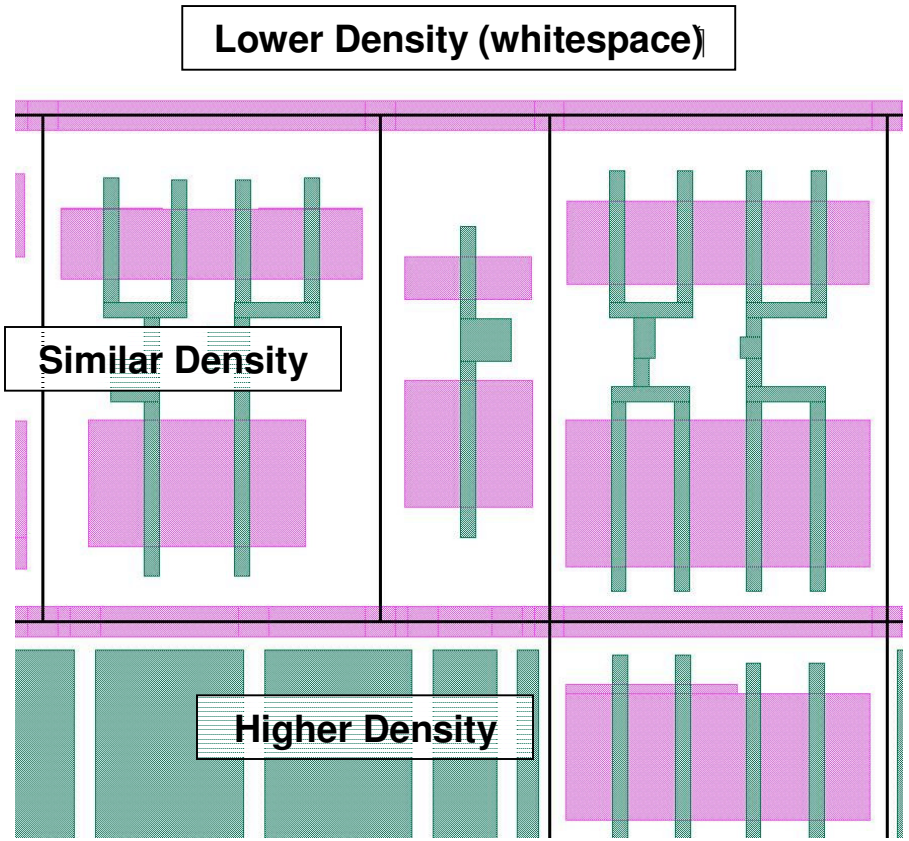
SEMs for 0.93NA ArF litho; SPIE 2007

Bridging: Shorts

Necking: Opens

Litho Impacts: Composability

- Random cell placements guarantee unpredictable shape relationships and density around the cell, increasing litho distortions
- In-situ litho simulation not practical
- Cell characterization flows that ignore litho distortions increase risk of fatal hold time errors or performance degradation



- Litho-aware standard cell verification flows increase safety, but must evaluate context extremes and over-margin cell timing models

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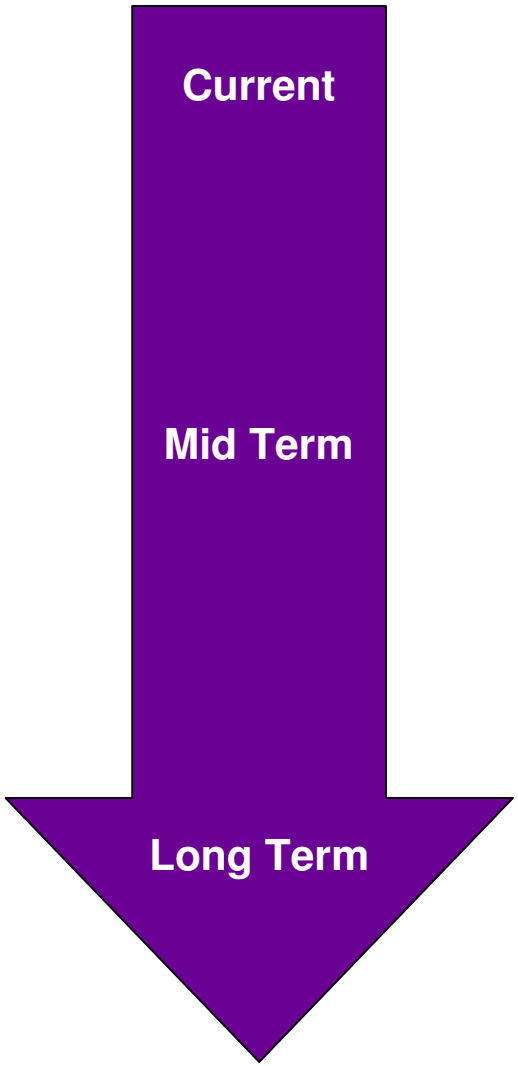
Solutions



Optical Wavelength Equipment Advances

Recommended Design Rules

DFM (Design Repair)

Computational Lithography Advances

Design and Process Co-optimization, Gridded Design Rules

Double-Patterning

Maskless Lithography

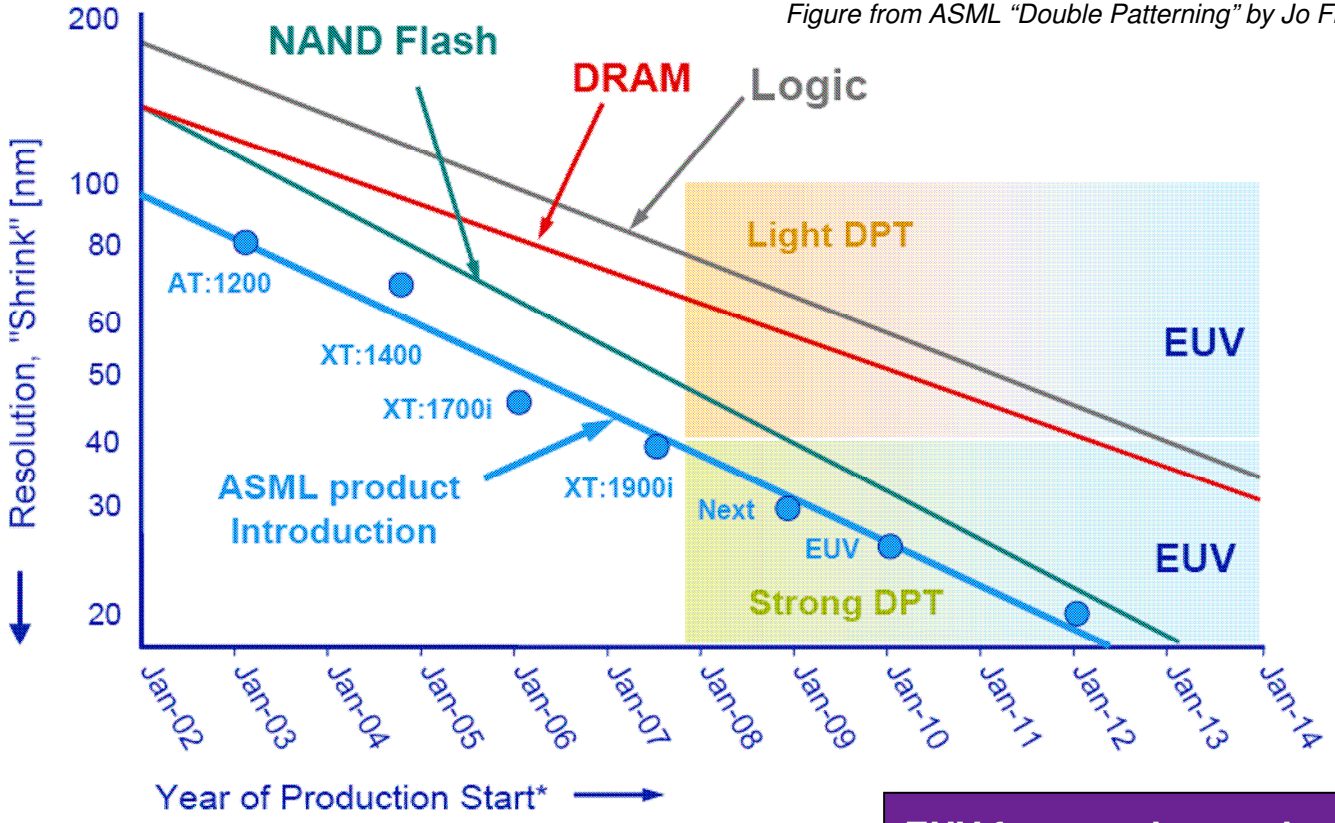
(examples: e-beam, interference litho, nano-imprint)

Advanced Structures (example: VeSFET)

Extreme Ultraviolet (EUV) Lithography

Strategies: Scanner Evolution

Figure from ASML "Double Patterning" by Jo Finders, October 2008



Rayleigh: $R = k_1 * \lambda/NA$

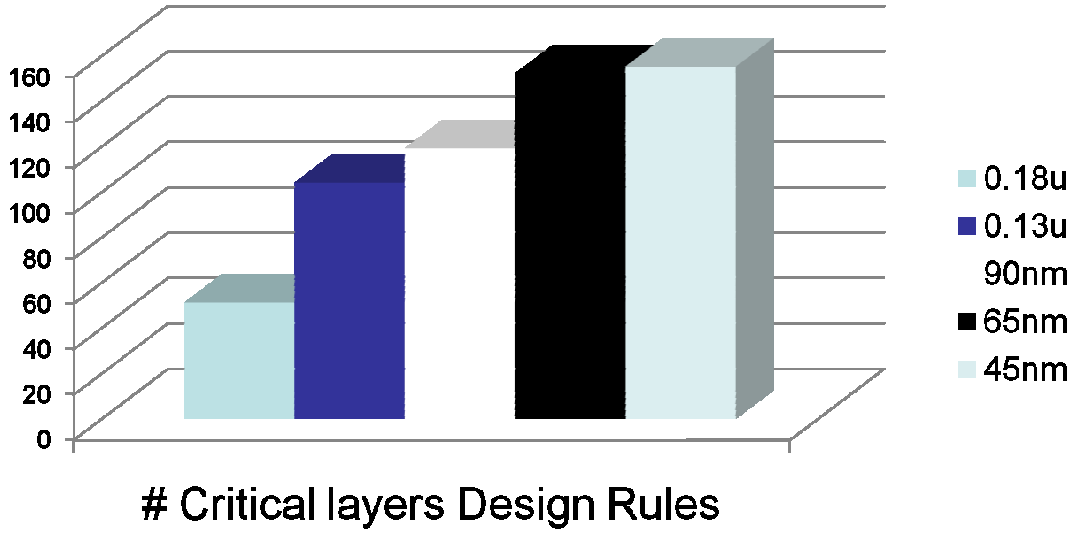
Conventional scanner technology has hit 3 walls:

λ= 193nm, NA = 1.35, k_1 = 0.26

EUV faces major production hurdles, current throughput ~4 wph.
This is due in part for the need for high vacuum and a 14x increase in photon energy compared to 193nm.

Recommended Design Rules

- ***Required*** **design rules are proscriptive, disallowing certain shape relationships but otherwise enabling random layout.**
- ***Recommended*** **design rules are associated with a subjective prediction of increased yield. These guidelines are frequently disregarded as their cost can be directly evaluated but their benefit cannot.**
- **Application of required and recommended rules does not necessarily result in highly regular layout.**

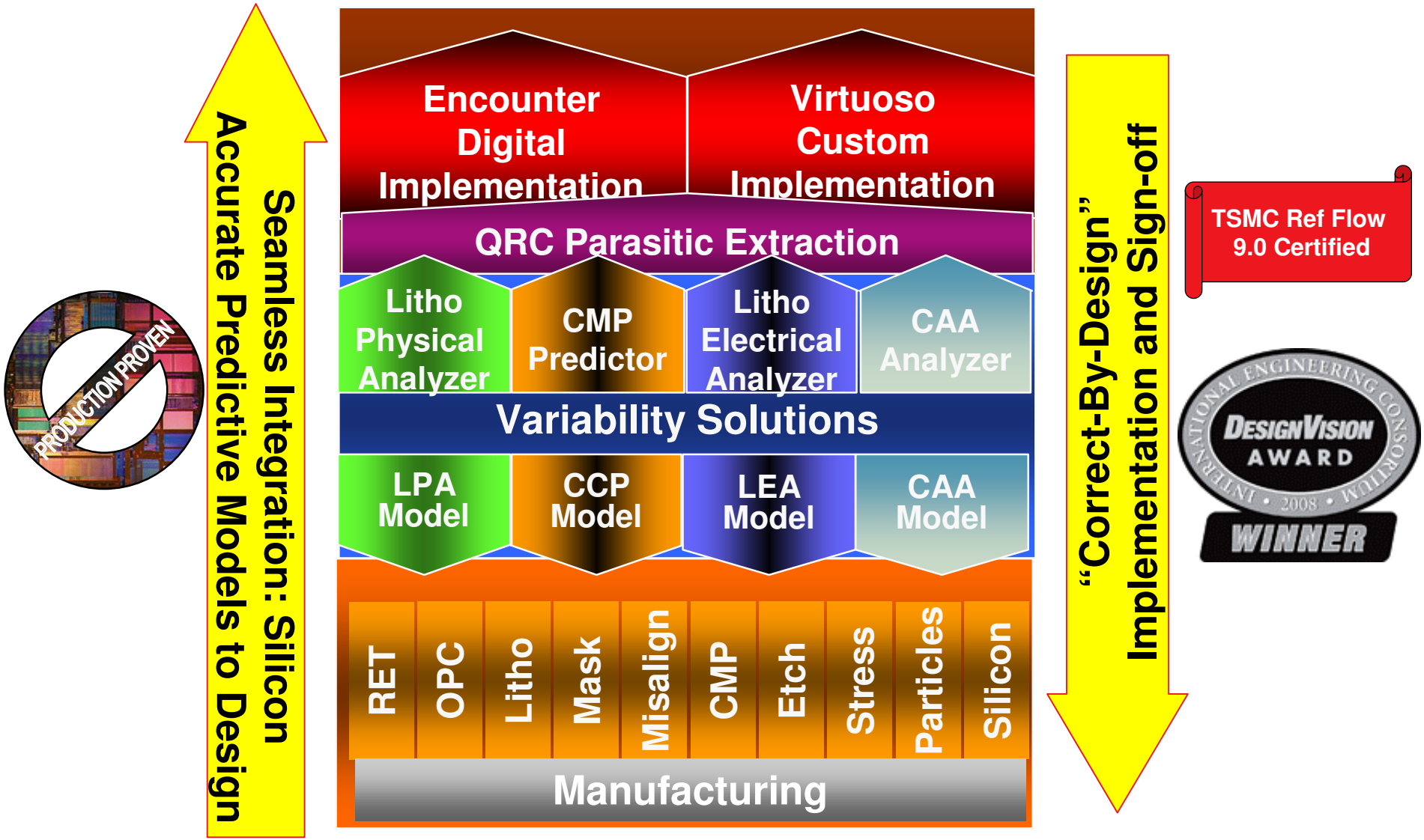


Critical layers include: diffusion, poly, contact, M1, M2, VIA12

To cover all layers, advanced node DRMs may include thousands of rules and recommendations

Enabling "Correct-By-Design" Flow

Prevention, Analysis, Optimization and Sign-Off



Mentor DFM Tool Suite

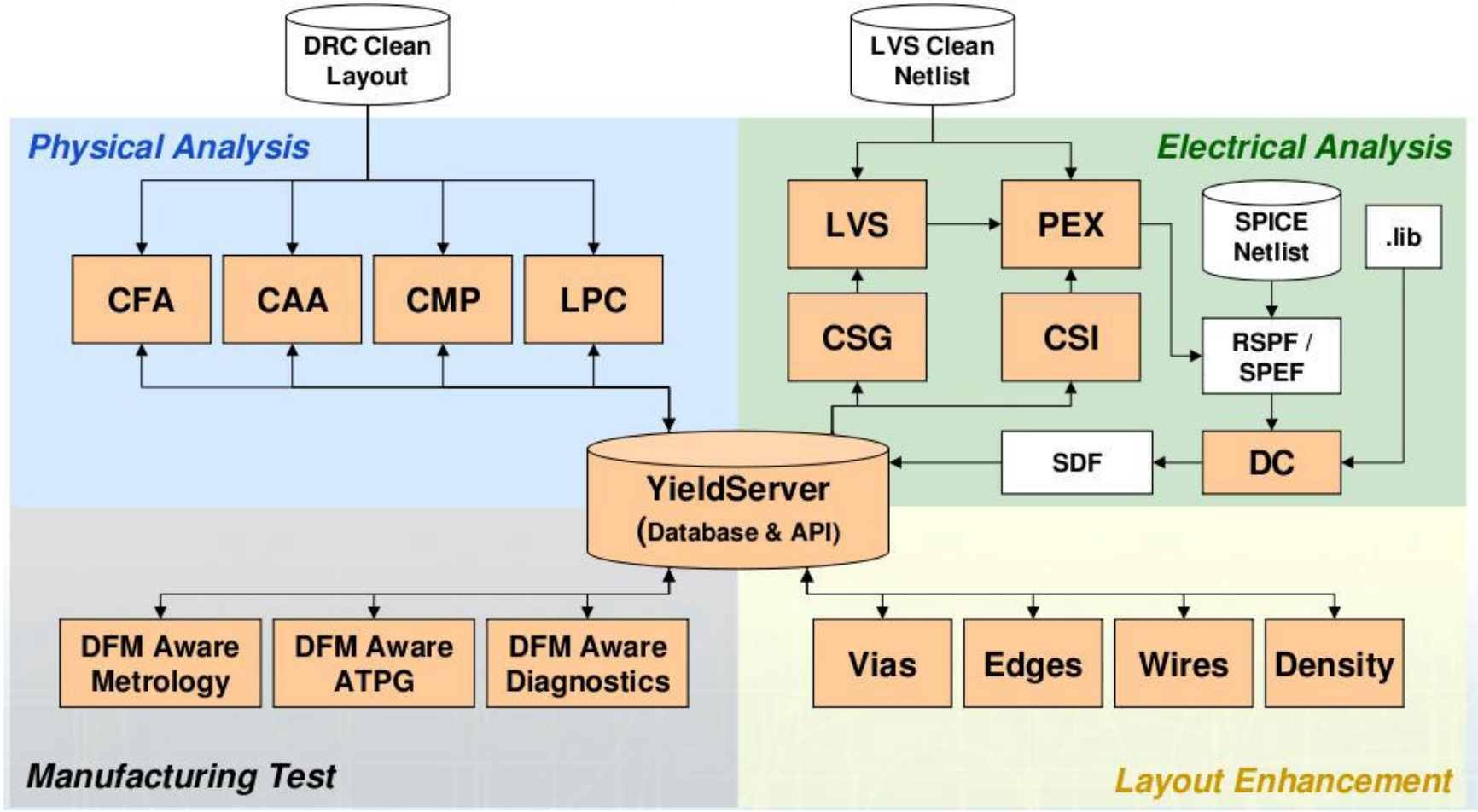
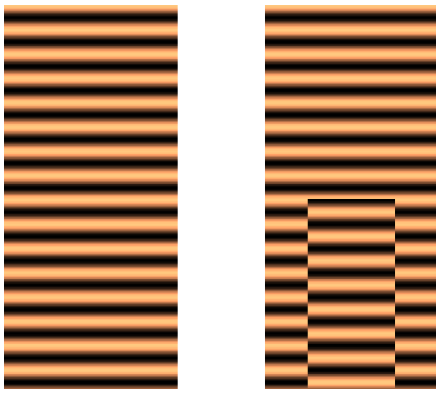


Figure from David Abercrombie, Mentor Graphics, EDA Tech Forum, 2007

Computational Lithography

- **Computational Lithography (Computational Scaling) is foundational to Resolution Enhancement Techniques (RET) that control wave amplitude, direction, and phase to improve resolution:**
  - **Optical Proximity Correction (OPC)**
    - Alter mask shapes to correct exposure problems

    "Treating focus and exposure as variables would increase the computing requirements ... to approximately one CPU-century" *(Jim Wiley, Brion Technologies Inc.)*
  - **Phase Shift Masks (PSM)**
    - Alter masks to induce useful interference patterns
  - **Off-Axis Illumination (OAI)**
    - Tilt illumination using advanced sources to optimize Depth of Focus (DOF)
  - **Source Mask Optimization (SMO)**
    - Optimize light source and mask in tandem



Example: 180deg Phase Shift

Image: Wikipedia.org

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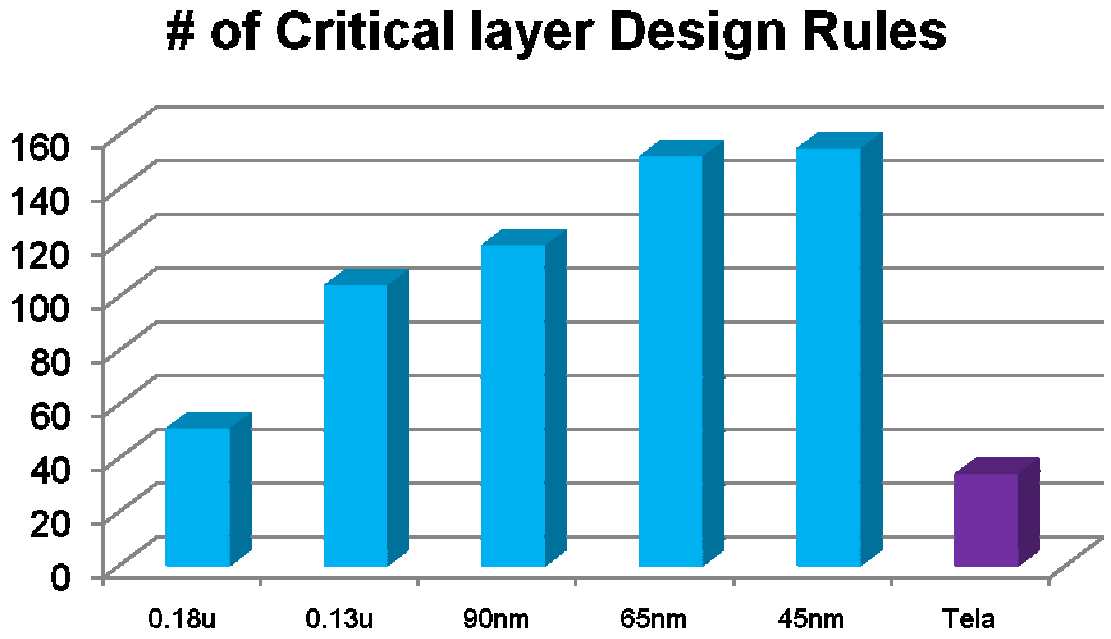
Design-Process Co-optimization

Share the burden of advancing Moore's Law with chip and cell layout designers; starting with a simple question:

What structures are optimal for manufacturing?

- Eliminate random patterns
- Use "=" sign vs. "<", ">".
- Use fewer design rules
- Implement highly regular layout (greatly reducing lithographic distortions)



By limiting rules, we limit the number of allowed structures and shape relationships.

This simplifies DFM, OPC, fab ramp up, and enables structure-process optimization through simulation and silicon (similar to memory cell development).

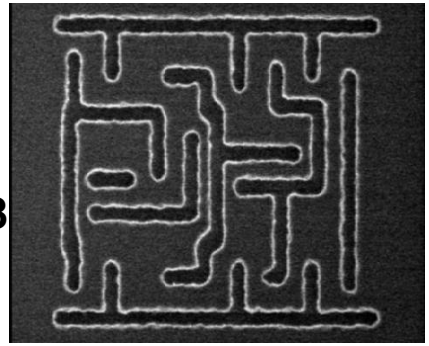
1D Gridded Design Rule Layout Style

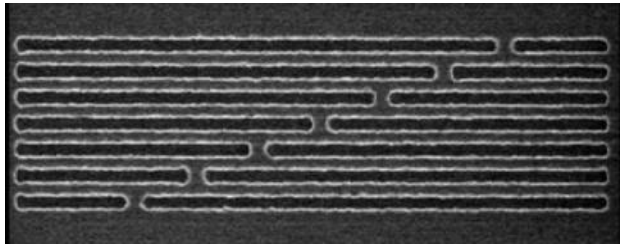
Design-process co-optimization supports a layout style with 1-dimensional shapes and Gridded Design Rules (1D GDR):

- Rectangular shapes with fixed width and spacing
- Fixed pitch on a pre-determined grid, single orientation
- Predictable poly to diffusion interactions

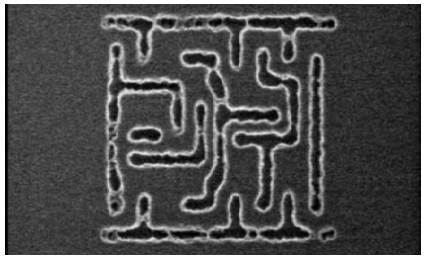
Despite identical equipment and k1 values, the quality of manufactured results changes dramatically - entirely based on layout style.

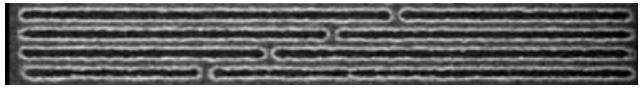
65nm
k_1=.43





45nm
k_1=.31





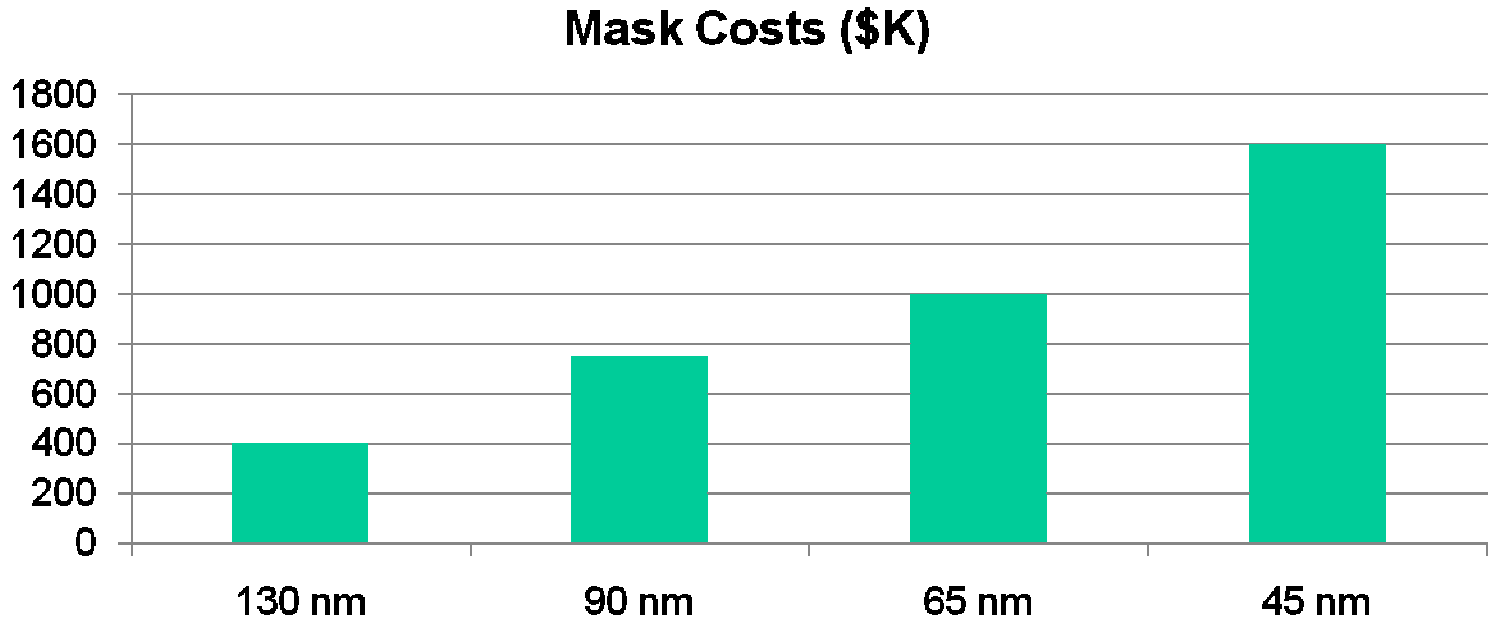
SEMs for 0.93NA ArF litho; from SPIE 2007 poster

1D GDR Benefits: Product Competitiveness

Physical Improvements translate directly to a better product:

- **Tighter pitches**
  - Cell area savings
  - These translate to the block level by maintaining routability
- **More rectangular channels (less necking, line end shortening)**
  - Reduced sub-threshold leakage
  - Reduced device variability
- **More rectangular interconnect**
  - Reduced parasitic variability
  - Reduced litho-related bridging and pinching defects
- **Improved cell timing independence from placement context**
  - Timing models no longer need to be over-margined
- **Reduced pattern density variability**
  - Improved CMP/planarization
  - Reduced etch skew

1D GDR Benefits: TTM and Costs



- **Mask costs are reduced as OPC is simplified**
- **DFM tool reliance is reduced, improving Time To Market**
- **Design is scalability is improved**
  - 1D GDR layout is an excellent fit for future manufacturing strategies
- **Existing equipment can be used for more advanced processes**
  - Intel's use of dry litho for 45nm was enabled by layout style, contributing to cost savings of 27%. *(ASMC 2007, H. Banisaukas)*

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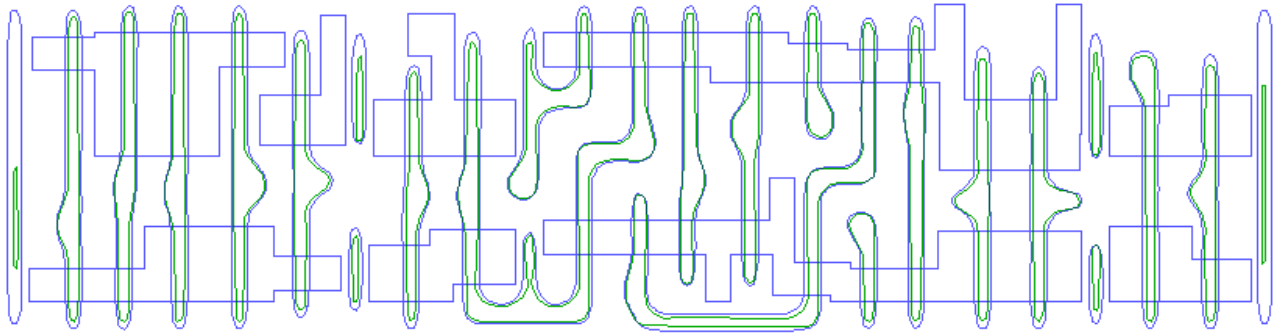
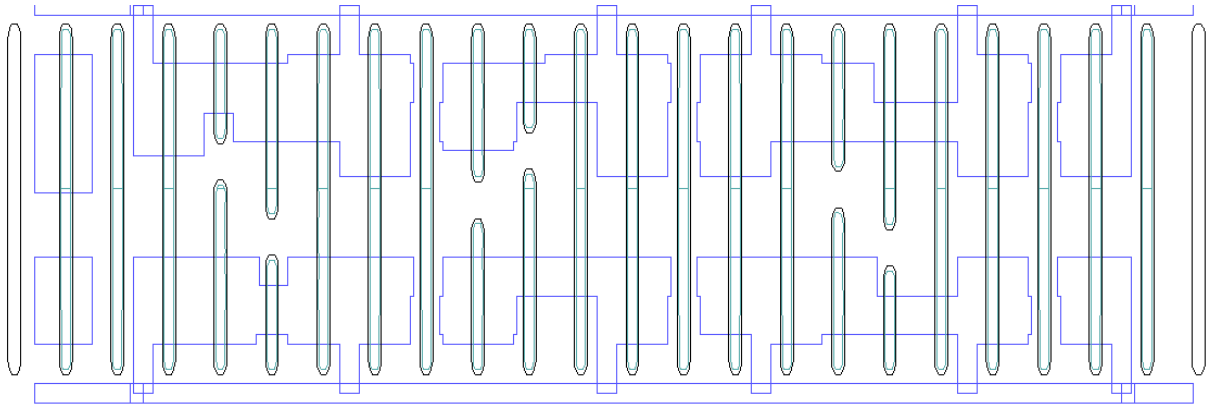
1D GDR Results: Lithography Simulations

Lithographic distortions are significantly reduced with 1D GDR



2D Conventional Layout



1D GDR Layout

Scan D Flip Flop, 45nm Process

1D GDR Results: Cell Area

- **Weighted average cell area reduction: 15%**

Image Not Available

2D Conventional Layout

Image Not Available

1D GDR Layout

Scan D Flip Flop, 45nm Process

1D GDR Results: Block Area

Image Not Available

- 90nm Example – Si validated
- 20% Area Reduction on Floating-Point Unit Block
  - 15.7% reduction in aggregate cell area
  - 5% improvement in cell utilization

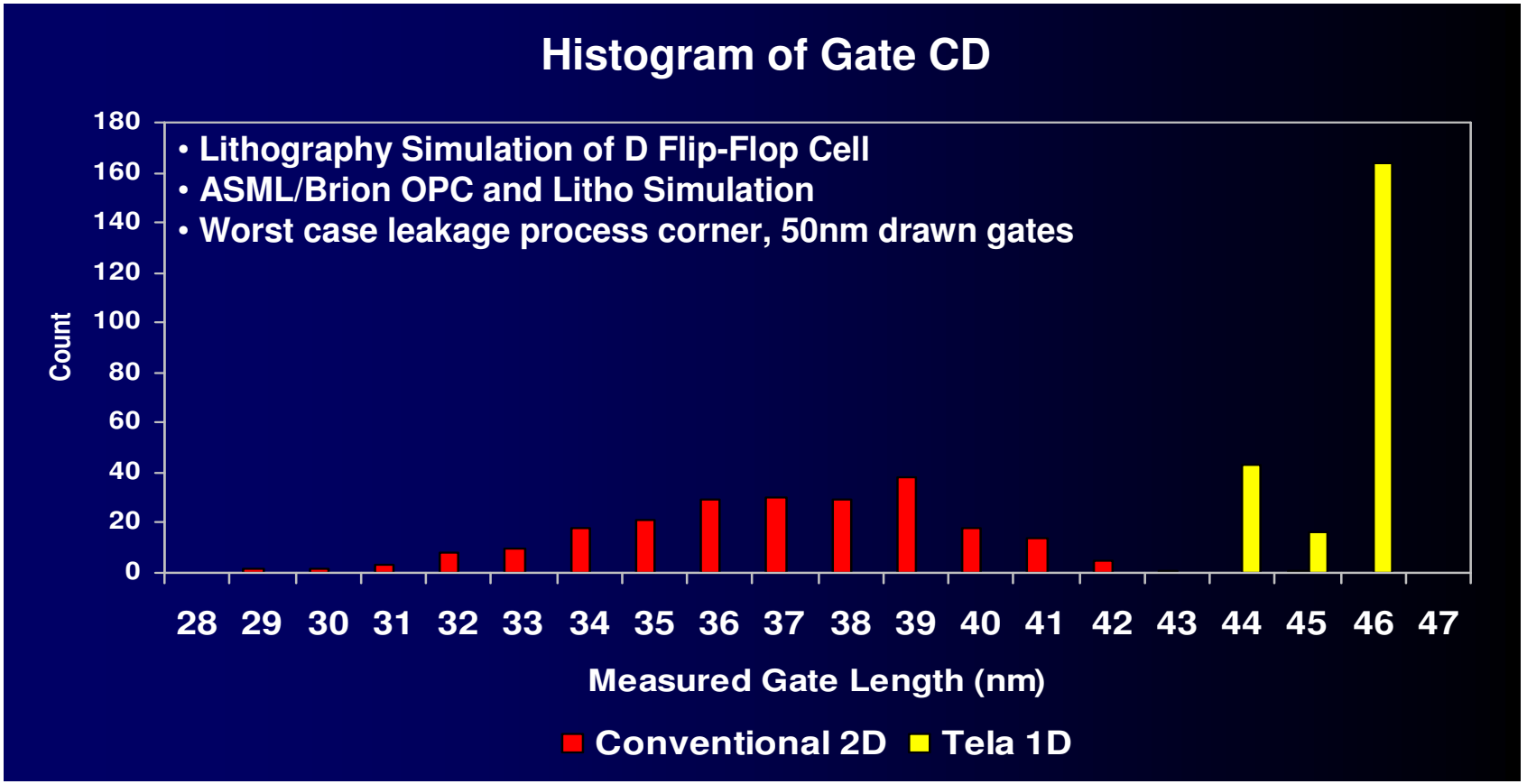
Image Not Available

- 65nm Example – Si validated
- 20% Area Reduction on Multiplier
- Comparing 1D GDR vs. existing foundry library

Image Not Available

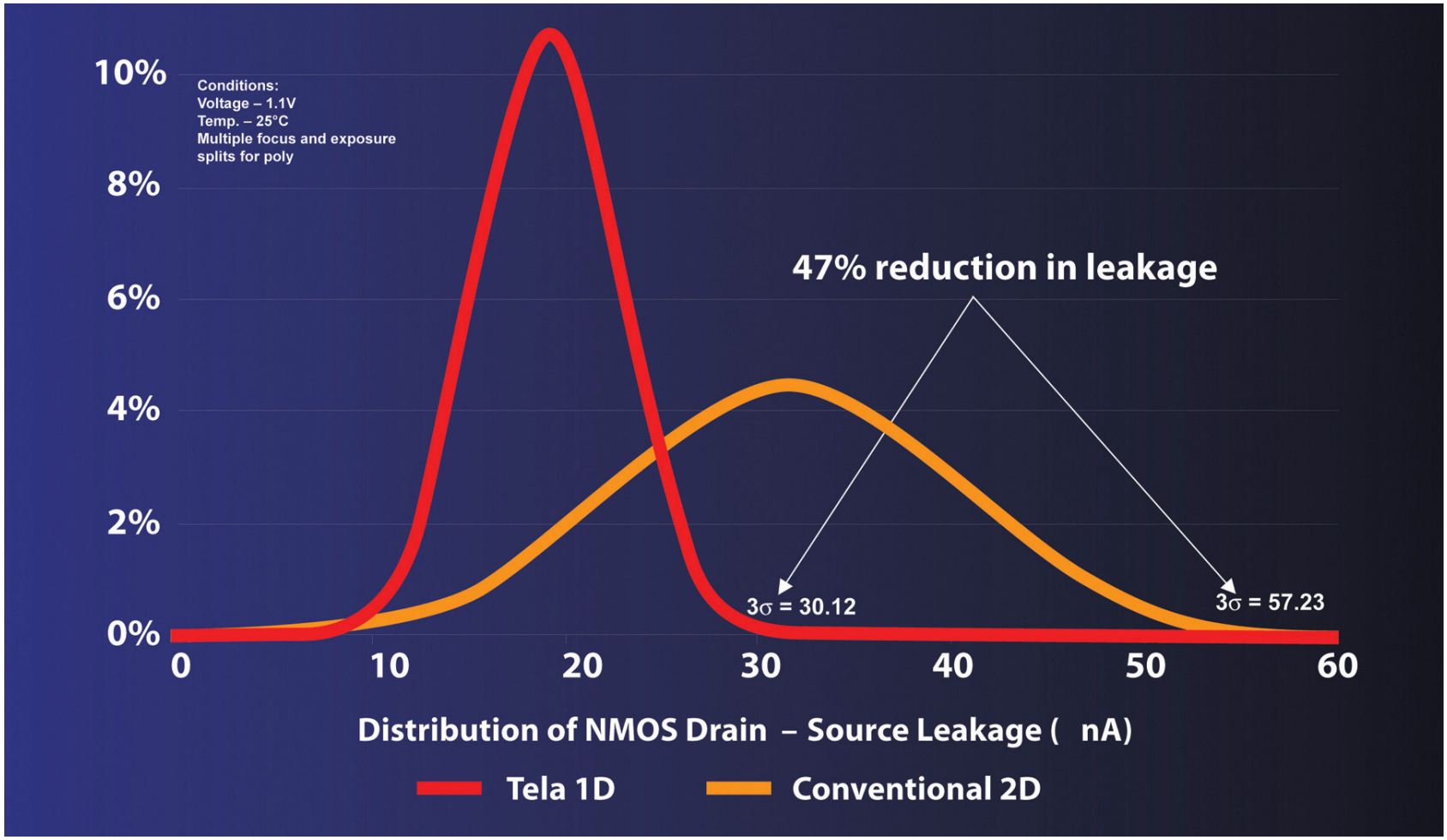
- 45nm Example – Si validated
- 20% Area Reduction on 45nm test-chip
- Comparing 1D GDR vs. existing fabless library

1D GDR Results: Gate CD



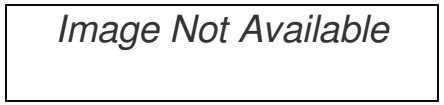
Gate CD distribution for 1-D and 2-D layout styles under worst-case simulated exposure process

1D GDR Results: Sub-threshold Leakage



Leakage Results: 45nm Test Chip using 1D GDR layout

1D GDR Results: Defectivity Results



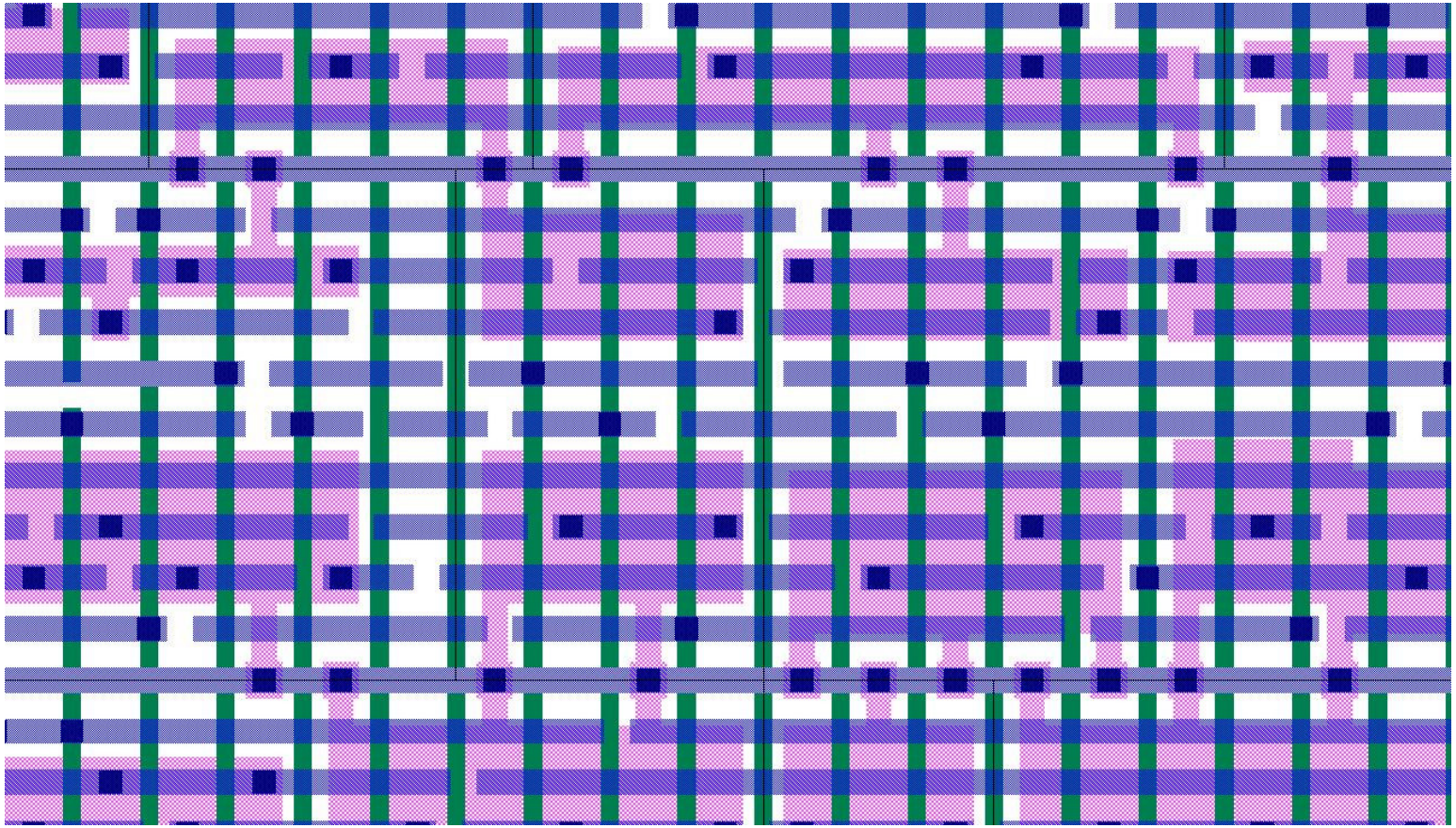
Test Si Results

- Test silicon results in for several chips in 65nm and 45nm processes
- Test structures include: FPUs, Multipliers, Ring Oscillators, misc. logic, device-level test structures
- To date no failures reported for structures using proposed 1D GDR layout

1D GDR Results: Composability

Cell boundaries are hard to distinguish - demonstrates context independence.

Cell characterization is more deterministic - narrower timing model window.



Partial view of FPU block, 90nm process

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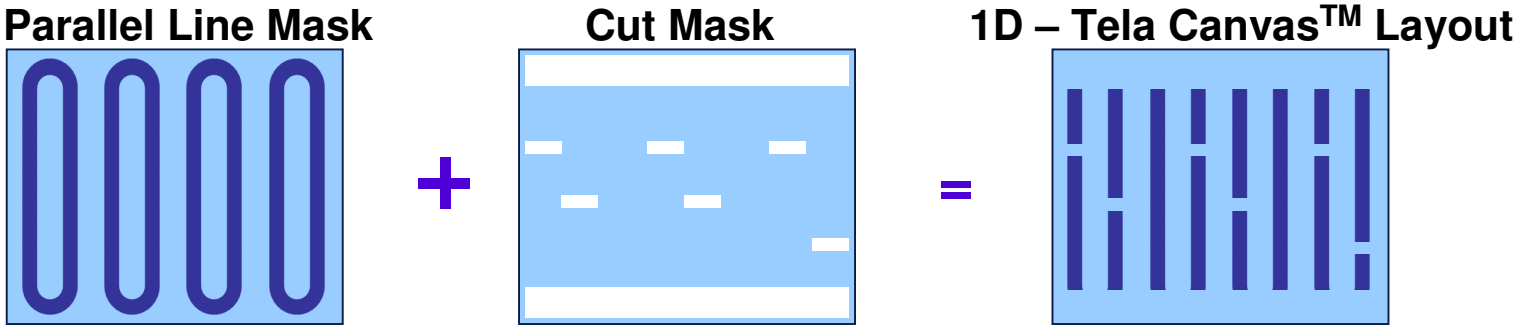
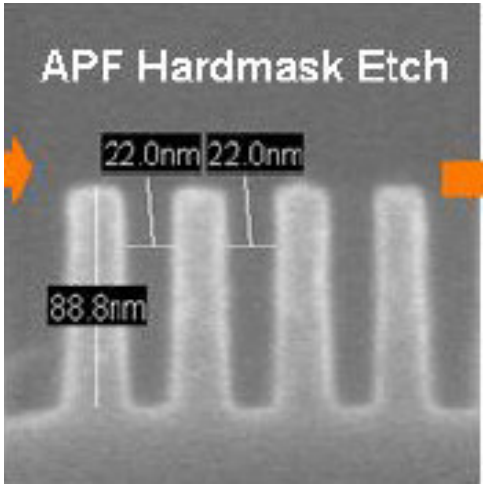
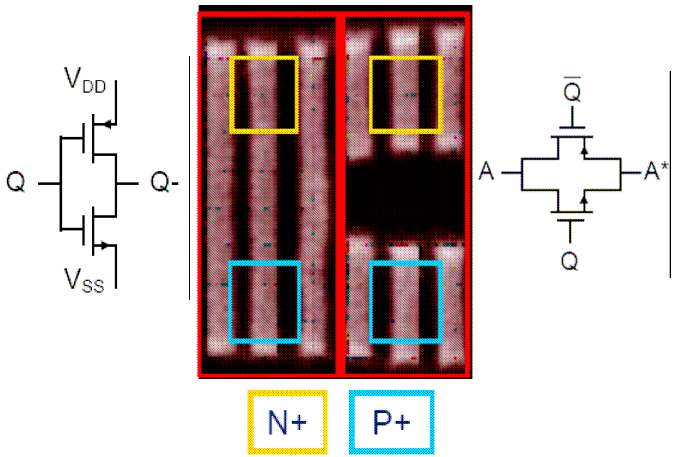
Future Directions: Self Aligned Double Patterning

- SADP – Self aligned Double Patterning
- APF™ - Advanced Patterning Films

APPLIED MATERIALS
think it. apply it.™







22nm CMOS Inverter and Transmission Gate

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  - *What can we actually manufacture?*
- 1D GDR Results
  - *Physical design can be simultaneously manufacturable and efficient*
- Future Directions
  - *DP plays well with 1D GDR*
- **Conclusions**

Conclusions

- Optical lithography equipment has hit physics-based limits
- Design/Process Co-optimization is transitioning from a “nice to have” to a “must”
- 1D GDR triggers a number of simplifications:

  Co-optimization -> 1D GDR -> Design rule simplification

  -> Regular layout -> Finite layout sub-structure count

  -> cell timing context independence -> Reduced DFM complexity

  -> Reduced OPC complexity -> Optimal processing
- Product benefits: reductions in area, leakage, timing variability, defectivity
- Strategic benefits: lower risk chip design, lower mask costs, expanded process equipment capability, compatibility with future technologies