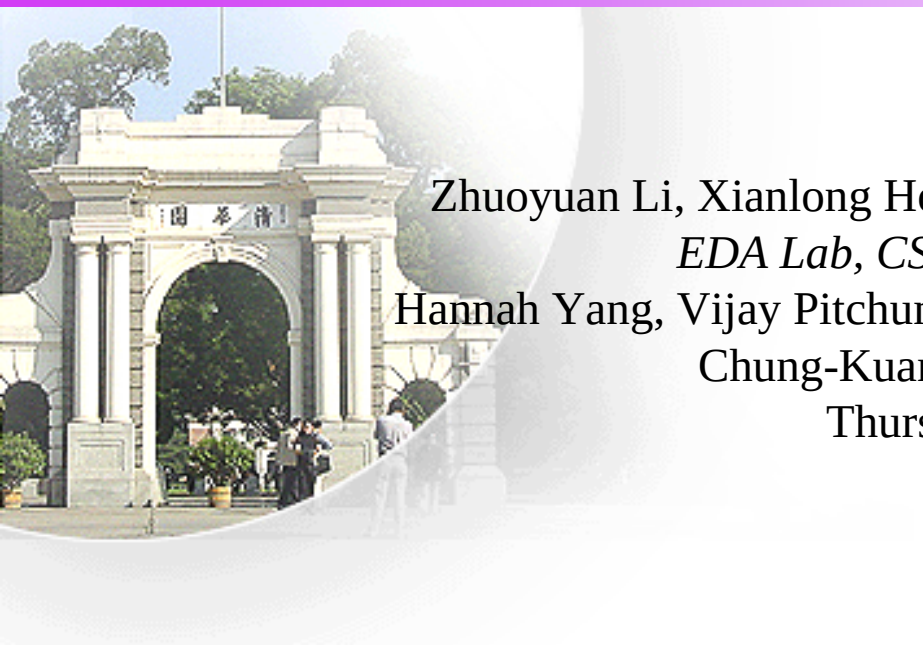
Integrating Dynamic Thermal Via Planning With 3D Floorplanning



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Outline

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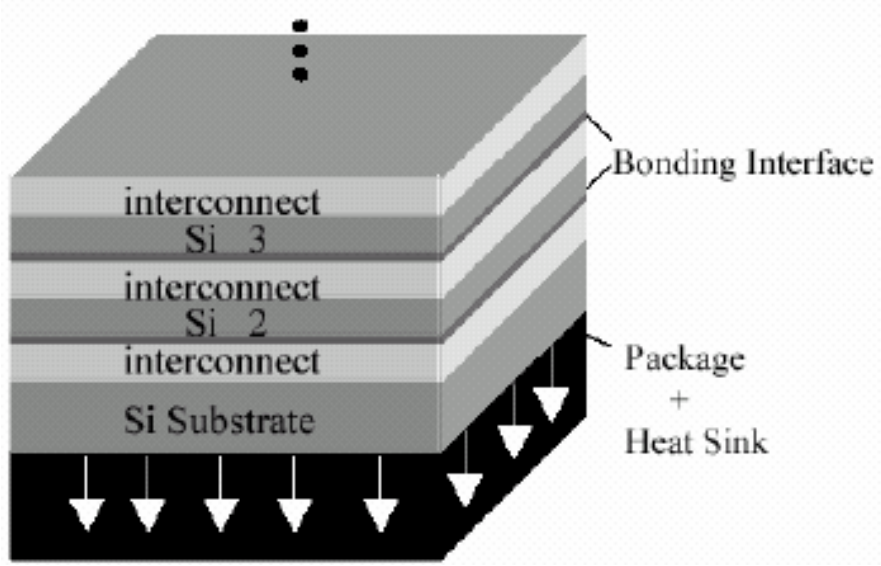
  - Our Contribution
- Our Solution
  - Analytical solution for detailed thermal via distribution
  - Integrating thermal via planning into 3D floorplanning
- Experimental Results
- Conclusion

Background

- 3D Integration: Driving Forces
  - Improved global Interconnect performance
  - Reduce footprint / Improve packing density
  - "Mixed Signal" Integration
- Challenges for 3D Integration
  - Heat Dissipation
  - Reliability
  - Design Complexity



Previous Work

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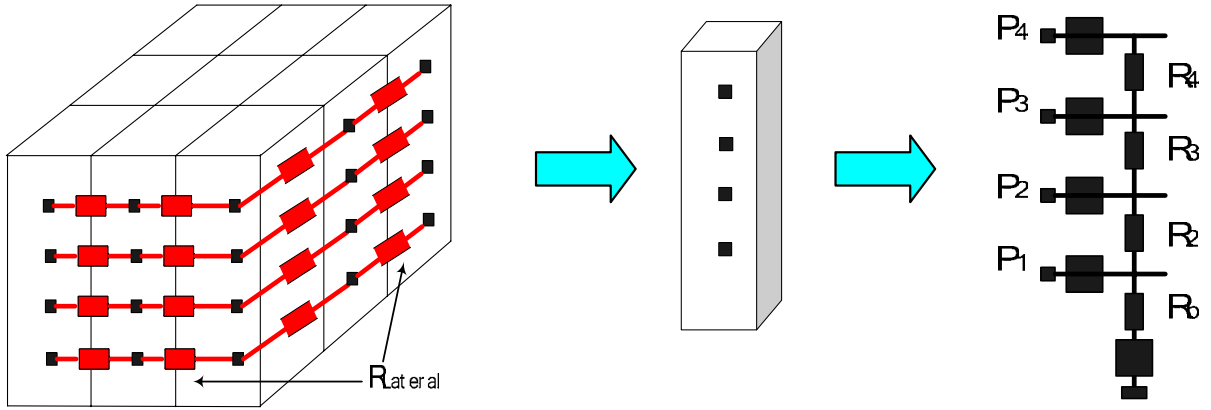
- UCLA, Prof. Jason Cong's Group
  - Thermal-driven 3D floorplanning, ICCAD'04
  - 3D global routing with thermal via planning, ASP-DAC'05
  - Post-floorplanning thermal via planning, ICCAD'05
  - MEVA-3D: Performance evaluation in 2D/3D designs, ASP-DAC'06
- UMN, Prof. Sachin Sapatnekar's Group
  - Thermal-driven 3D placement, ICCAD'03
  - Post-placement thermal via planning, ISPD'05
  - Thermal-driven 3D global routing, ASP-DAC'06
- Gatech, thermal/power noise/congestion optimization in 3D ICs (ISCAS'04, ASP-DAC'04 & ASP-DAC'05)
- MIT, 3D placement & routing tool for wirelength/performance and thermal optimization (ASP-DAC'03 & ISPD'04)
- U Wisconsin, Chip-level 3D Thermal Analysis Tool (ISPD'03)

Thermal Model

- Resistive Thermal Model (CFD Research Corporation)



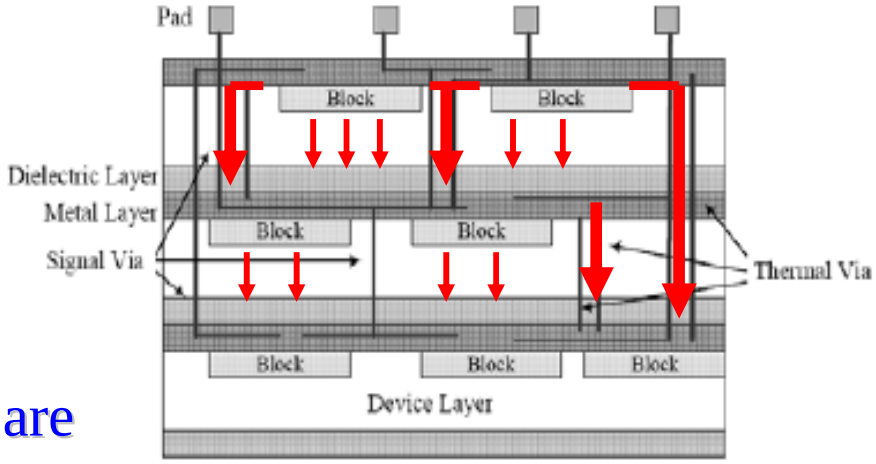
- The 3D circuit stack is divided by a two-dimensional array of tile stacks. Each tile stack is composed of several vertically-stacked tiles, one from each device layer.

- These tile stacks are connected by lateral thermal resistances. Within each tile stack, a thermal resistor is modeled for each device layer.

- Through solving the linear system $RT = P$, the temperature on each node could be determined.

Thermal Via Planning

- Thermal Vias
  - Lowering the thermal resistance between different layers
  - Thermal resistance: $\frac{1}{R_e} = \frac{1}{R_{layer}} + \frac{1}{R_{via}}$

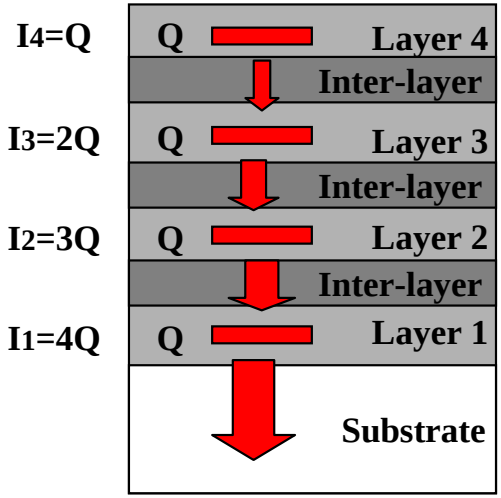


- T-Via number should be minimized and they are placed to hot areas to make the greatest impact.
- Heuristic Method for T-Via Planning
  - Thermal via number is in proportional to the heat flow inside that tile

$$n_j : n_k = I_j : I_k$$

  - Thermal via number in the figure is

$$n_4 : n_3 : n_2 = 1 : 2 : 3$$



Thermal Via Planning

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- Heuristic Method (ASP-DAC'05 & ISPD'05)
  1. Initialize tile grids on floorplanning/placement results;
  2. Temperature analysis by solving linear equations;
  3. If temperature constraint is satisfied, exit;
  4. Update heat flow in each tile;
  5. Assign thermal vias to each tile;
  6. Update thermal resistance of each tile, Goto 2.
- Divide-and-conquer Method (ICCAD'05)
  - Given initial floorplanning results, determine vertical and horizontal thermal via distribution sequentially;
  - Vertical thermal via distribution: analytical solution;
  - Horizontal thermal via distribution with heuristic method.
  - Implemented in a multi-level global routing framework.
- Drawbacks: (i) The heuristic method cannot generate optimal T-Via planning; (ii) It is too time consuming to be integrated into floorplanning

Our Contributions

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- Analytical solution for thermal via planning
  - Heuristic method: $n_i : n_j = I_i : I_j$
  - Divide-and-conquer method:
    $Vertical: \ n_i : n_j = \sqrt{I_i} : \sqrt{I_j}$
    $Horizontal: n_i : n_j = I_i : I_j$
  - Our solution $n_i : n_j = \sqrt{I_i} : \sqrt{I_j}$

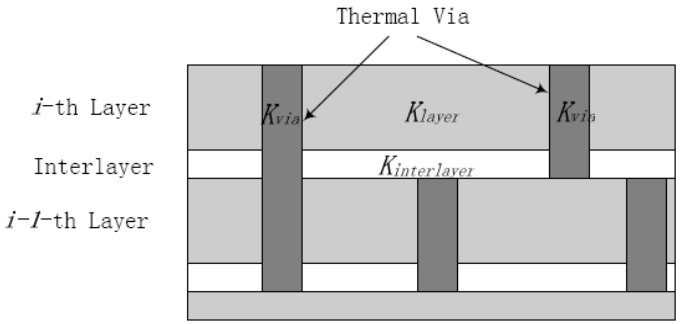
  1. Optimal solution for detailed thermal via distribution;
  2. Analytical solution with low computational complexity.

- Integrate thermal via planning into hierarchical 3D floorplanning
  - Inter-layer partition problem to minimize total number of thermal vias are formulated and solved.
  - Fast white space redistribution to generate floorplans feasible for thermal via insertion.

Our Solution: V-TV Distribution

- Thermal conductivity calculation

$$K = m_i K_{via} + (1 - m_i) K_{layer}$$



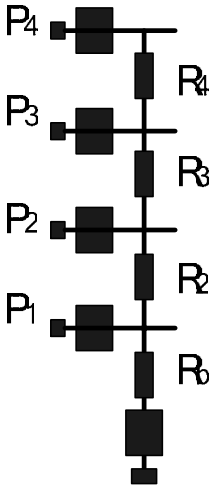
- The relationship between R and K

$$R = \frac{\alpha}{K} \times \frac{l}{s}$$

- Temperature rise on the i-th layer

$$T_i = R_b \sum_{j=1}^{k} P_j + \sum_{l=2}^{i} (R_l \sum_{j=l}^{k} P_j) + T_{amb}$$

$$T_i = F(R) = F(m_i)$$



V-TV Distribution: Analytical Solution

- Temperature-constrained vertical thermal via planning problem:

$$\min \sum_{i=2}^{k} m_i$$

$$s.t. \quad \sum_{i=2}^{k}\left(\frac{R_{layer}}{1+\lambda m_i}\sum_{j=i}^{k} P_j\right) + R_b \sum_{j=1}^{k} P_j + T_{amb} \le T_0$$

$$\lambda = \frac{K_{via} - K_{layer}}{K_{layer}}$$

- The convex programming problem could be solved directly by *KKT* optimal condition.

$$f = \sum_{i=2}^{k} m_i + \mu\left(\Delta T - \sum_{i=2}^{k}\left(\frac{R_{layer}}{1+\lambda m_i}\sum_{j=i}^{k} P_j\right)\right)$$

$$where \quad \Delta T = T_0 - T_{amb} - R_b \sum_{j=1}^{k} P_j$$

$$\partial f / \partial m_i = 0, \quad 2 \le i \le k$$

$$m_2 = \left(\frac{R_{layer}\sqrt{I_2}\sum_{i=2}^{k}\sqrt{I_i}}{T_0 - T_{amb} - R_b I_1} - 1\right)/\lambda,$$

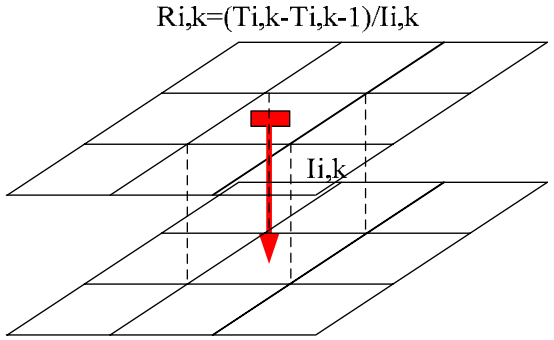
$$1+\lambda m_i : 1+\lambda m_{i-1} = \sqrt{I_i} : \sqrt{I_{i-1}}, \quad 2 \le i \le k$$

$$where \quad I_i = \sum_{l=i}^{k} P_l$$

Our Solution: H-TV Distribution

- Optimal V-TV Distribution: Desired temperature rise on each layer

$$T_i = R_b \sum_{j=1}^{k} P_j + \sum_{l=2}^{i} (R_l^{'} \sum_{j=l}^{k} P_j) + T_{amb}$$



- Desired thermal gradient for each tile

$$T_i - T_{i-1} = \Delta T_i = I_{ik} R_{ik} = g(m_{ik})$$

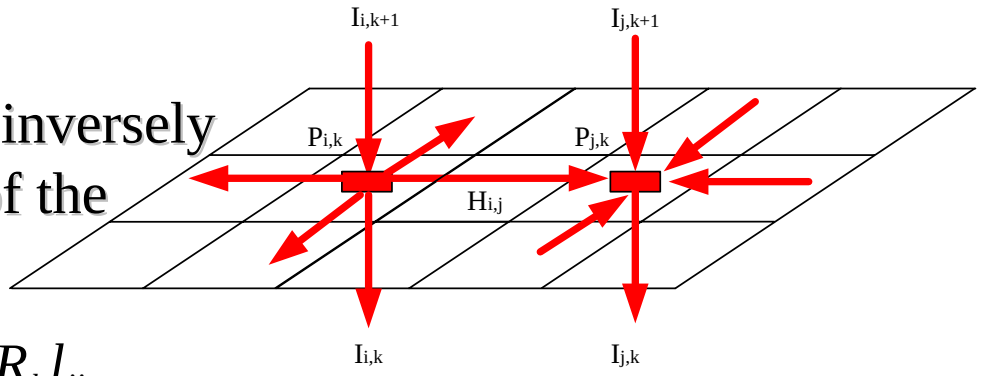
- I is related to R so it should be updated frequently.

- Heat Flow Analysis

- Vertical heat flow in a grid is the sum of heat flow from all other grids

$$I_{jk} = \sum_i H_{ijk} = f(R_{ik}) = f(m_{ik})$$

- Heat flow from a grid to other gird is inversely proportional to the thermal resistance of the flow path.



$$H_{ijk} = (P_{ki} + I_{k+1,i}) \frac{1}{R_{ij}} / \sum_l \frac{1}{R_{il}} \qquad R_{ij} = R_i + R_h l_{ij}$$

H-TV Distribution: Analytical Solution

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- Temperature-constrained horizontal thermal via planning problem:

$$min \quad \sum_{k=1}^{N} m_{ik}$$

$$s.t. \quad R_{ik} \times I_{ik} = R_{ik} \times \sum_{j=1}^{N} (P_{ij} + I_{i+1,j}) \frac{1/R_{ijk}}{\sum_{l=1}^{N} 1/R_{ijl}} \le \Delta T_i$$

$$k = 1, \ldots, N$$

- Simplified convex programming problem formulation:

$$min \quad \sum_{k=1}^{N} m_{ik}$$

$$s.t. \quad \frac{1}{R_i} \sum_{k=1}^{N} \sum_{j=1}^{N} \frac{P_{ij} + I_{i+1,j}}{1 + R_h l_{jk} / R_{ik}} \le N \Delta T_i$$

- Nearly optimal solution for CP:

$$m_{ik} : m_{is} = \sqrt{\sum_{j=1}^{N} \frac{P_{ij} + I_{i+1,j}}{l_{jk}}} : \sqrt{\sum_{j=1}^{N} \frac{P_{ij} + I_{i+1,j}}{l_{js}}}, 1 \le k, s \le N \qquad m_{ik} : m_{is} = \sqrt{I_{ik}} : \sqrt{I_{is}}$$

Design Flow of 3D FP-TVP

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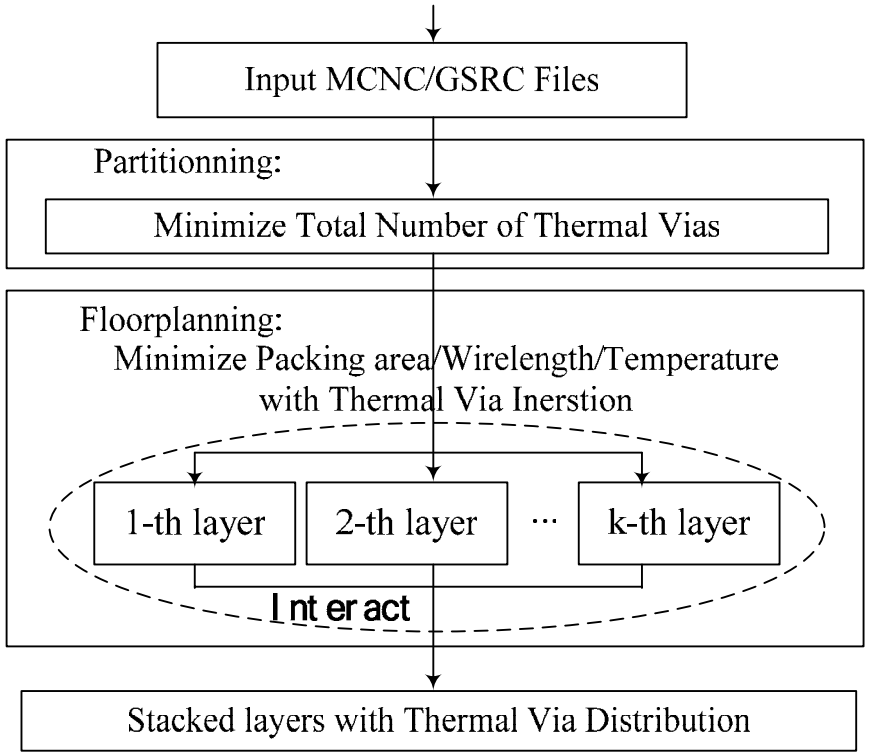
- Hierarchical 3D Floorplanning
  - Partition blocks into different layers
  - Generate floorplans for all these layers



- This 3D floorplanning flow has been implemented for wirelength optimization (ISCAS'05) and thermal optimization (TODAES'06).
  - Smaller solution space
  - More stable for thermal optimization

- Key Problem:
  - Formulate and solve the inter-layer partitioning problem for thermal via planning.

Inter-layer Partitioning

- Problem Formulation:

$$\min \sum_{i=2}^{k} m_i$$

$$s.t. \quad \sum_{i=1}^{k} P_i = const$$

$$\frac{1}{\beta} \le \left| \frac{A_i}{A/k} \right| \le \beta, 1 \le i \le k$$

$$\sum_{i=2}^{k} m_i = \frac{R_{layer} (\sum_{i=2}^{k} \sqrt{\sum_{l=i}^{k} P_l})^2}{\lambda (T_0 - T_{amb} - R_b \times const)} - k$$

$$\min \sum_{l=2}^{k} \sqrt{\sum_{i=l}^{k} P_i}$$

$$s.t. \quad \sum_{i=1}^{k} P_i = const$$

$$\frac{1}{\beta} \le \left| \frac{A_i}{A/k} \right| \le \beta, 1 \le i \le k$$

- Solution Method:

$$\max \quad P_1$$

$$s.t. \quad \frac{1}{\beta} \le \left| \frac{A_1}{A/k} \right| \le \beta$$

$$\max \quad P_2$$

$$s.t. \quad \frac{1}{\beta} \le \left| \frac{A_2}{A/k} \right| \le \beta$$

Solving knapsack problem: determine P1

$$\min \sum_{l=3}^{k} \sqrt{\sum_{i=l}^{k} P_i} + \sqrt{\sum_{i=2}^{k} P_i} = \sum_{l=3}^{k} \sqrt{\sum_{i=l}^{k} P_i} + \sqrt{const'}$$

$$s.t. \quad \sum_{i=2}^{k} P_i = const - P_1^* = const'$$

$$\frac{1}{\beta} \le \left| \frac{A_i}{A/k} \right| \le \beta, 2 \le i \le k$$

- The inter-layer partitioning problem could be solved through solving a sequence of knapsack sub-problems.

3D FP with T-Via Planning

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- Inter-layer partitioning: determine desired temperature on each layer.
- Floorplanning using SA engine based on CBL representation

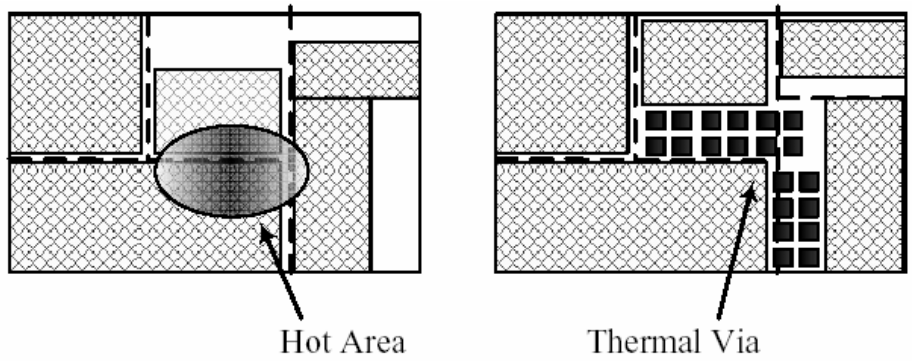
  - Cost function:

$$\Psi = A + w_1 W + w_2 (T_{\max} - T_0)$$

  - Thermal resistances are updated after horizontal thermal via planning and the maximal temperature is calculated by solving linear equations.

- Thermal vias should be arranged in the white space between blocks.

  - White space resources may be not enough for thermal via insertion in hot area.



- A fast and simple white space redistribution method is proposed to deal with it during floorplanning process.

Experimental Results

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- Compare our algorithm with UCLA's algorithm in ICCAD'05

	3D Floorplanning + m-ADVP					*3DFP-TVP*				
	T_{max}	T-via#	L_{total}	Area	Cpu(s)	T_{max}	T-via#	L_{total}	Area	Cpu(s)
ami33	78.2	920	29705	4.58E+05	359	78.5	689	28028	4.11E+05	434
ami49	79.2	21847	477858	1.58E+07	654	78.9	16490	487496	1.55E+07	835
n100	77.1	17122	85718	6.52E+04	3012	78.1	12820	82458	6.41E+04	3868
n200	76.8	15430	178999	6.56E+04	5728	77.6	11578	178943	6.63E+04	7283
n300	77.4	23015	299576	10.8E+04	8851	77.3	16025	281992	11.2E+04	11467
Avg.	1.00	1.35	1.03	1.02	0.79	1	1	1	1	1

Conclusion

- Mathematical modeling and analytical solution for minimizing thermal via number with maximal temperature constraint.
  - Optimal vertical thermal via distribution.
  - Nearly optimal horizontal thermal via distribution.
- Thermal via planning is integrated into 3D floorplanning process with our two-stage approach.
  - Inter-layer partitioning problem is formulated and solved for thermal via number minimization.
  - Fast white space redistribution method is proposed for thermal via insertion during floorplanning.

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Thank you!