Tutorial on Design For Manufacturability for Physical Design

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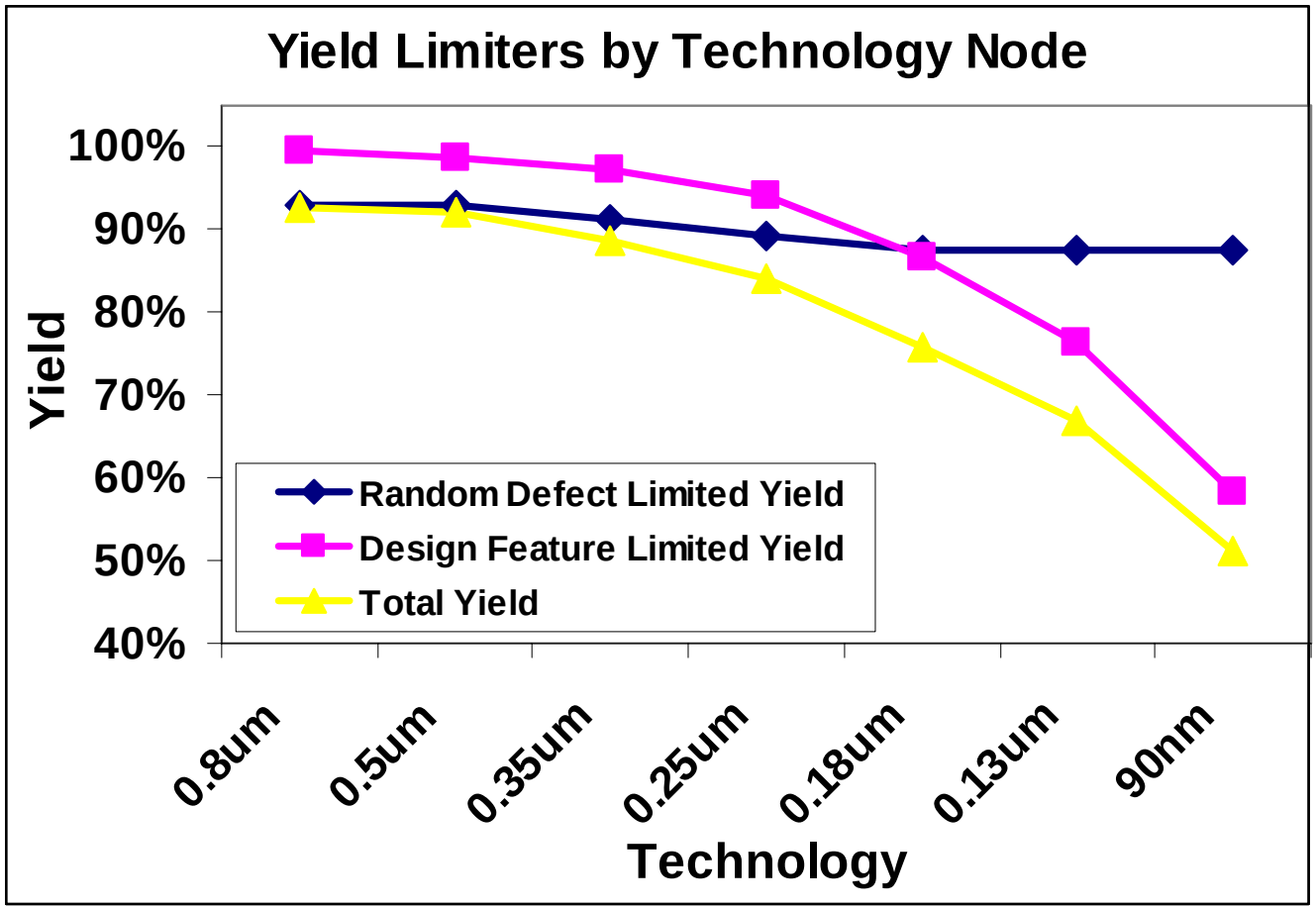
Overview of Presentation

- Yield Loss Mechanism Evolution
- Classification of DFM Approaches
- True DFM: Defining Proactive DFM
- Necessary Conditions for Proactive DFM
- Process Characterization
- Design Flows that Provide Proactive DFM
- DFM Results
- Looking into the Future: Extreme Layout Regularity

The Evolution of Product Yields



- Random defects are no longer the dominant yield loss mechanism
  - Yields are limited by design features, systematic and parametric effects

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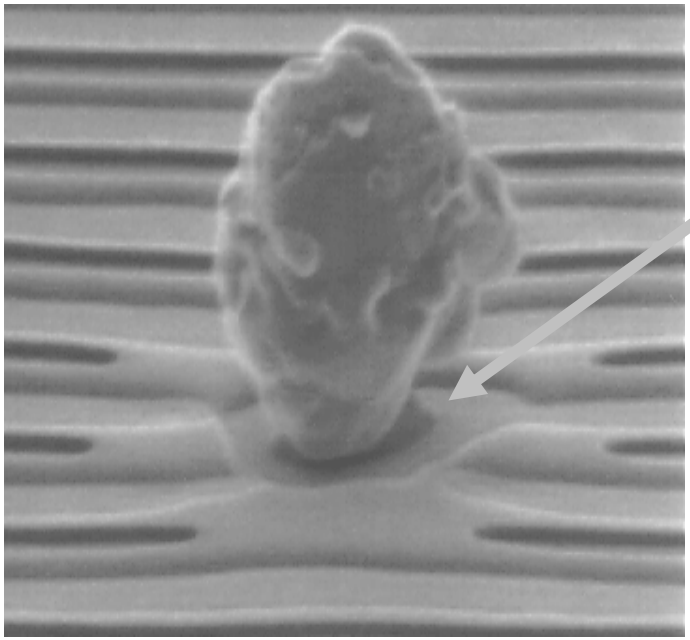
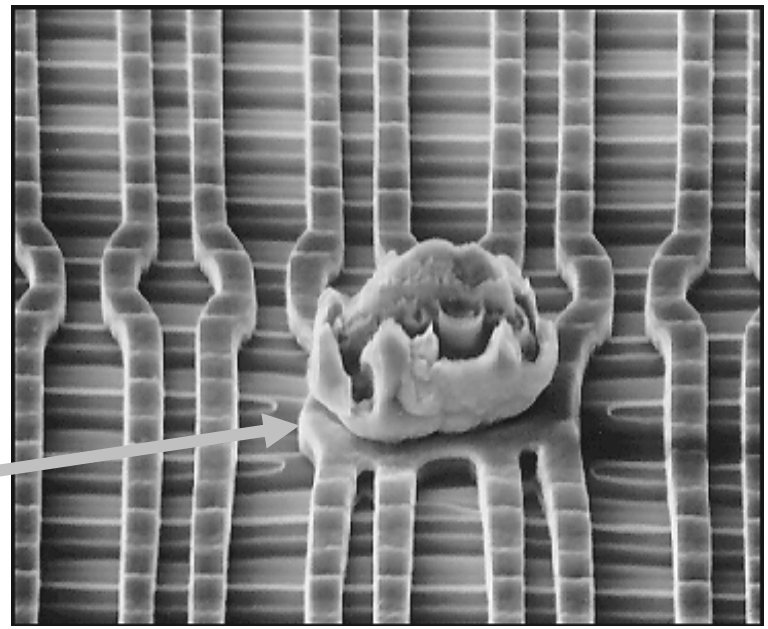
Random Yield Loss Mechanisms – Al Interconnect



Material opens

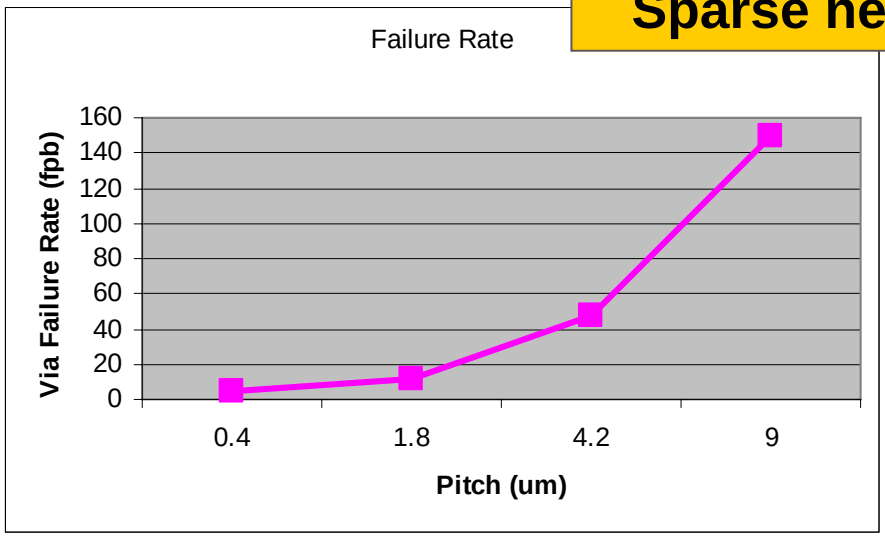
Material shorts

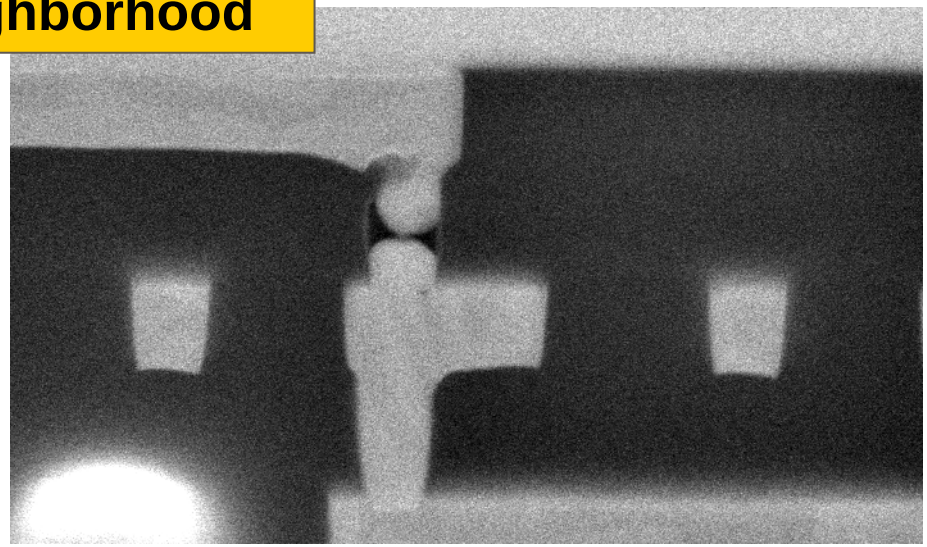


Type	Yield Loss Mechanisms
Random	Active, poly and metal shorts and opens due to particle defects
	Contact and via opens due to formation defectivity

Systematic Yield Loss Mechanisms - Cu Interconnect

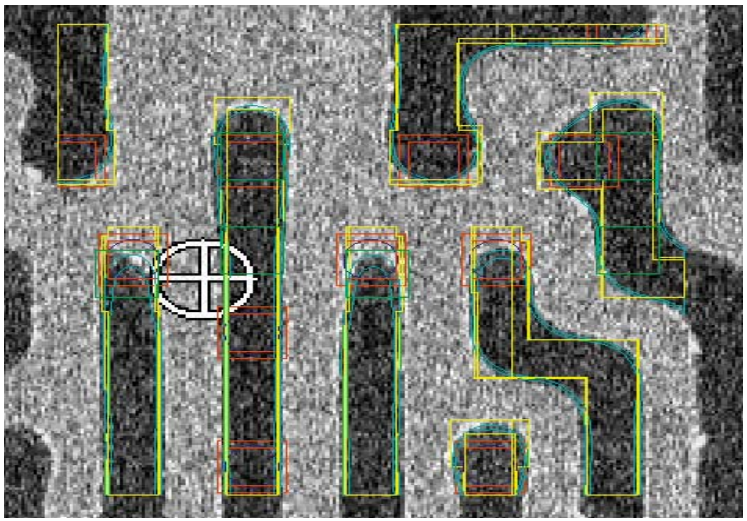
Sparse neighborhood

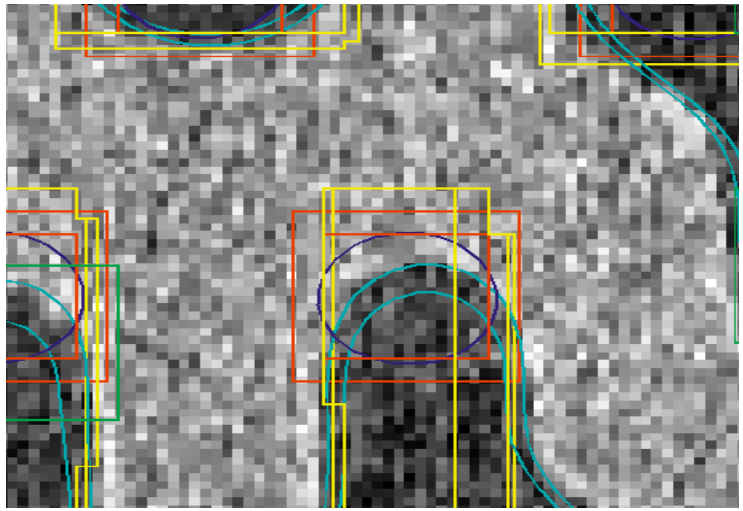




Type	Yield Loss Mechanisms
Systematic	Impact of micro/macro loading design rule marginalities
	Leakage from STI related stress
	Contact/via opens due to local neighborhood effects (e.g. pitch/hole size)
	Misalignment, line-ends/borders

Systematic Yield Loss: Printability – Nanometer Era

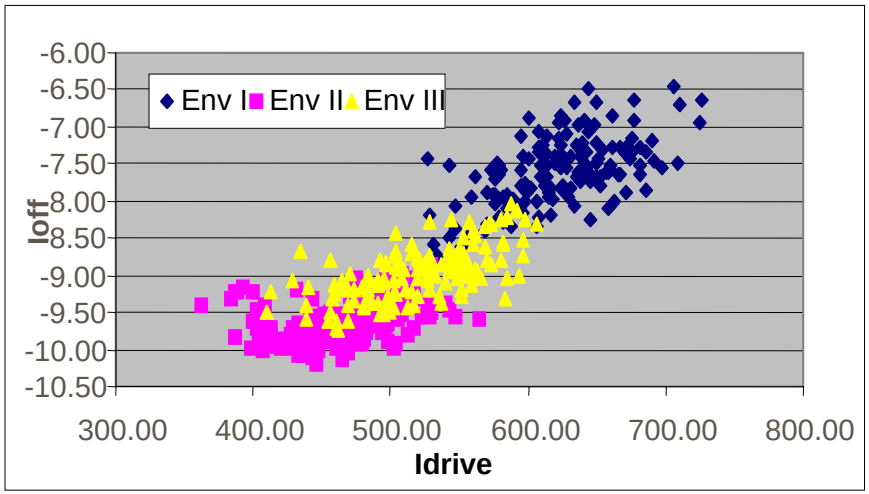




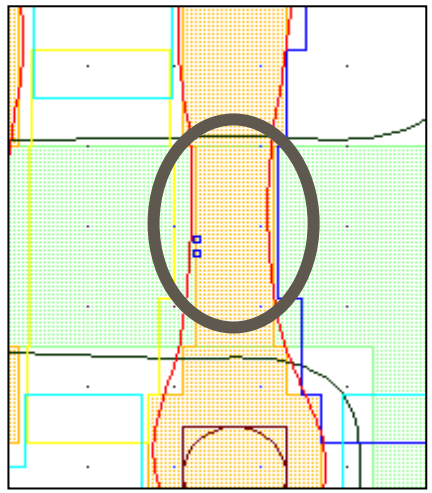
Type	Yield Loss Mechanisms
Systematic	Poor contact coverage due to misalignment and defocus/pull back
	Poly/Metal shorts
	Material opens

Parametric Yield Loss Mechanisms – Nanometer Era

Environment dependent poly CD variation

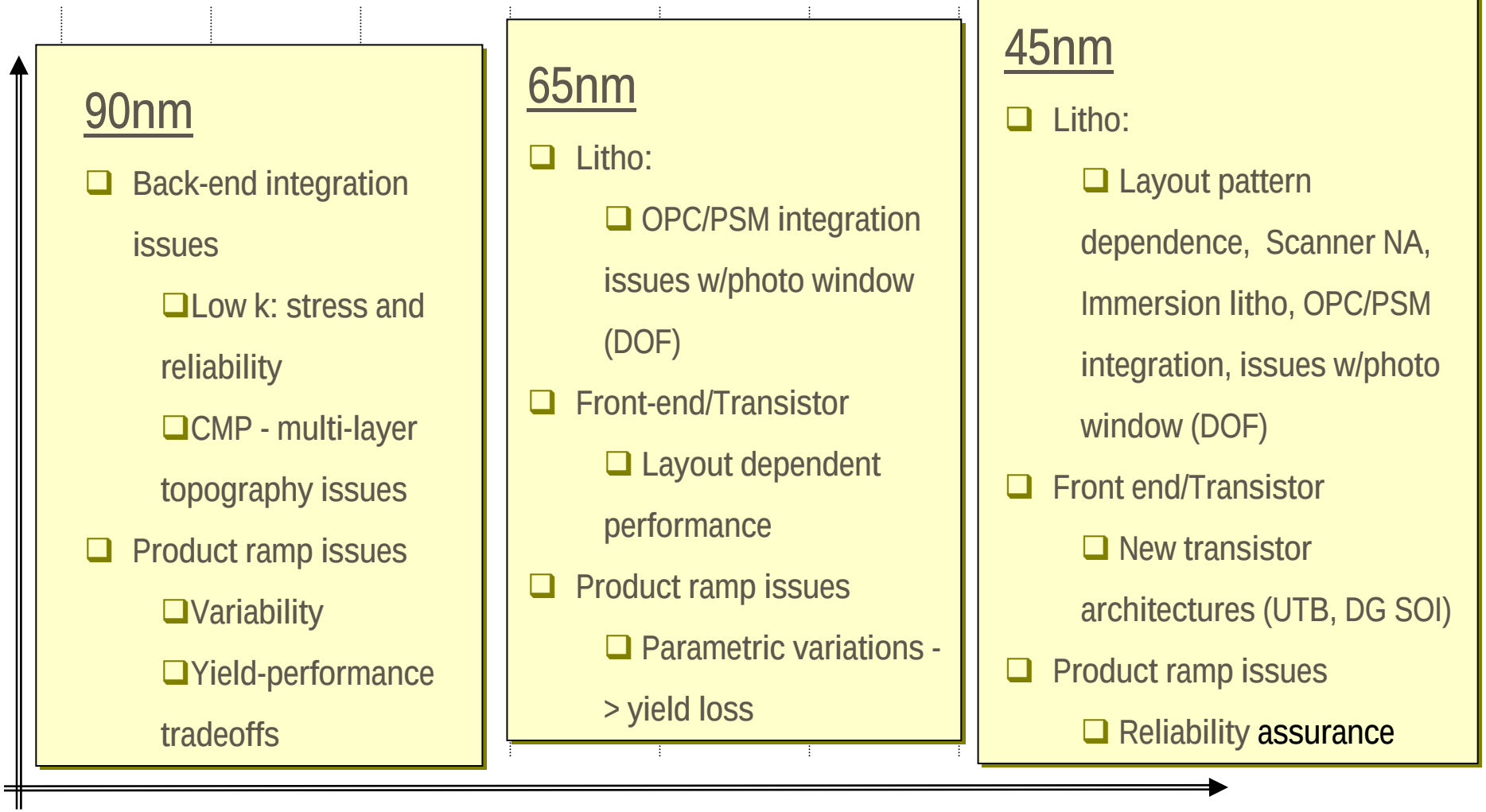


ACLV / CD Variation



Type	Yield Loss Mechanisms
Parametric	Performance variation from lithography effects e.g., contact/via coverage, active/poly flaring, CD variation
	Dummy fill parasitic effects
	Device mismatch
	Non-physical corner modeling

Technology Challenges: Implications for Manufacturability



DFM is a Business Opportunity
"Seamless" DFM Can Contribute 5% More Good Die

What's 5% more good die worth?

- $50M over the life of a cell phone
- $80M over the life of a game chip
- $100M per year per fab at 90nm

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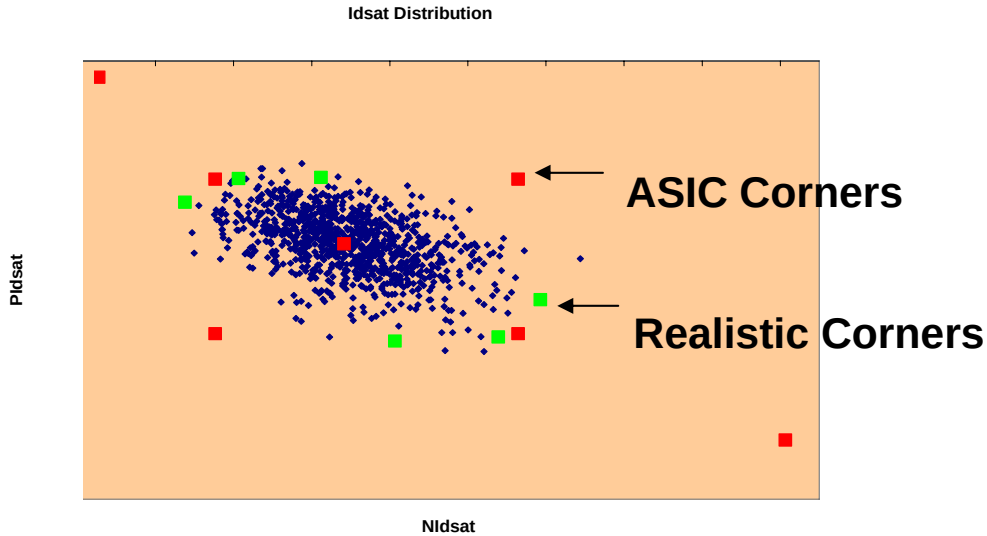
A Brief History of DFM

Functional Yield means Rules

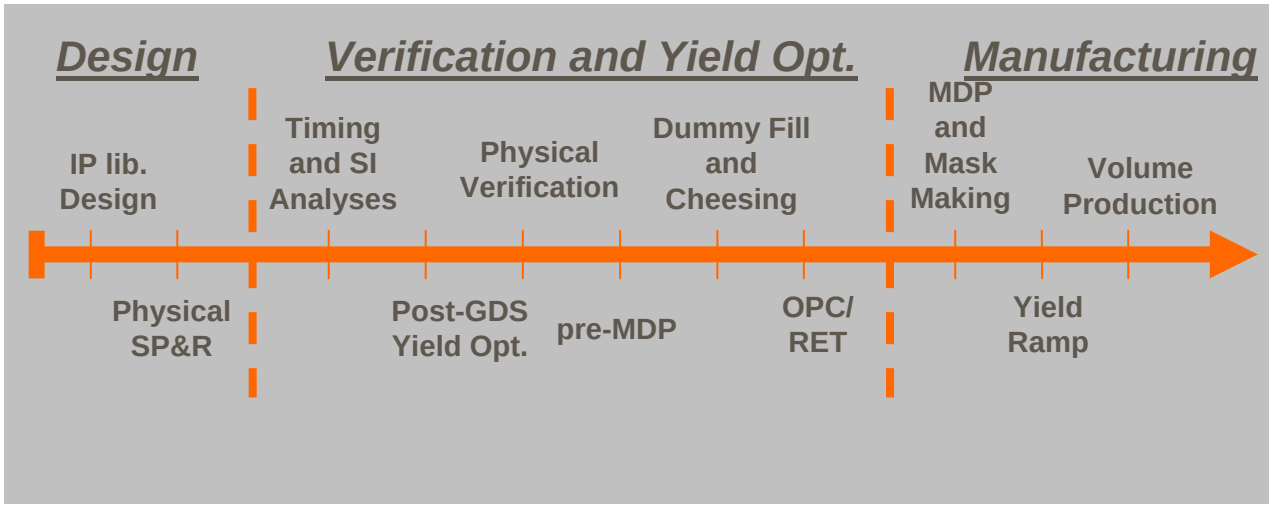
- Design rules guarantee yield!…well, not really…
- …then recommended rules
- …and opportunistic design data base post-processing to enforce them

Performance Yield is Covered by Corners



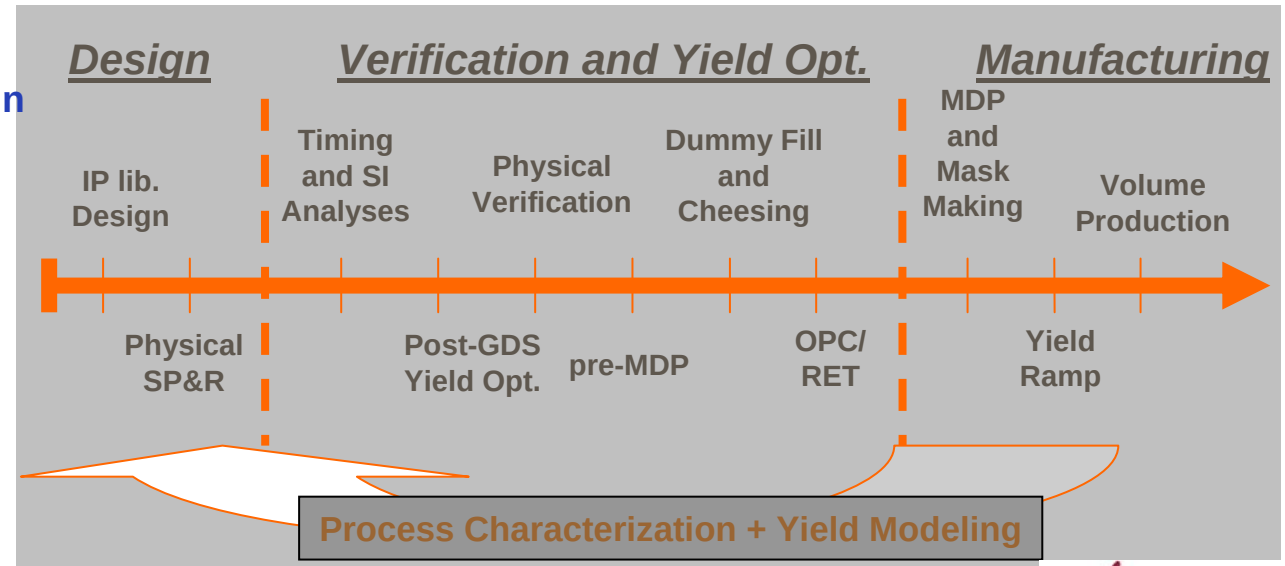
- The corners represent the process
- …The corners don't represent the process but they are conservative
- …Within chip variations are important so..
  - Restrict transistor layouts?
  - Statistical timing simulation?

Proactive DFM



- Designer access to the process is limited
- Most DFM today is Reactive
  - Increase in design cycle time
  - Misaligned mask GDSII and design database
  - Risky design feature changes

- DFM needs to be Proactive
- Occurring early in the design flow
- Up-front accurate process characterization
- Yield modeling to characterize IP and drive EDA tools



Necessary Conditions for Pro-Active DFM

- Accurate characterization of design-interactions at target fab(s)
- Effects modeled across the whole process window
- Quantification of alternatives that allow EDA tools to make millions of DFM trade-offs
- Integration early in the design flow where there are more degrees of freedom
  - Floor planning
  - SP&R
- Modifications made prior to verification

Yield Simulation is Core to Proactive DFM

Yield Simulation allows for better understanding of the DFM universe

- **A yield model for DFM:**
  - **Model of failure rate of a design element (e.g., transistor, contact, via) as a function of the layout design**
  - **Example:**
    - **What is the failure rate of a single via vs. double?**
    - **What is the probability of a short in two metal lines if there are lots of vias underneath them**
- **To do this, we need process characterization**

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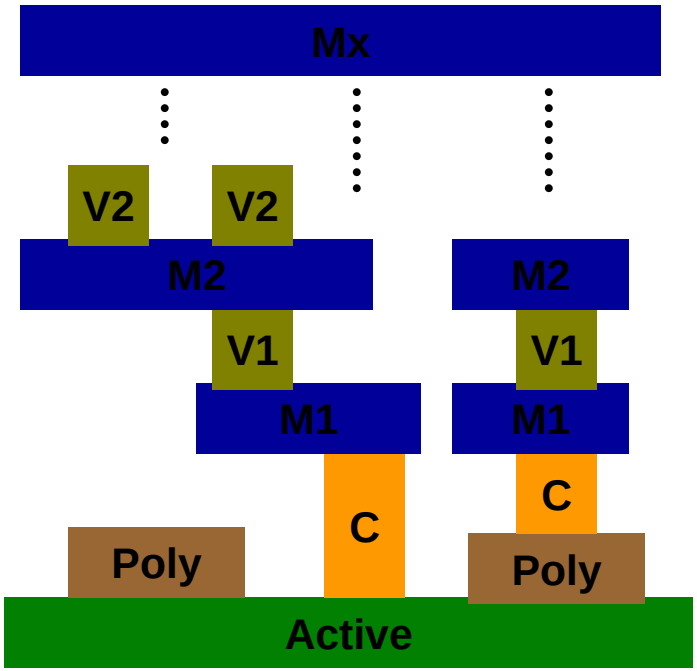
Process Yield Loss Mechanisms

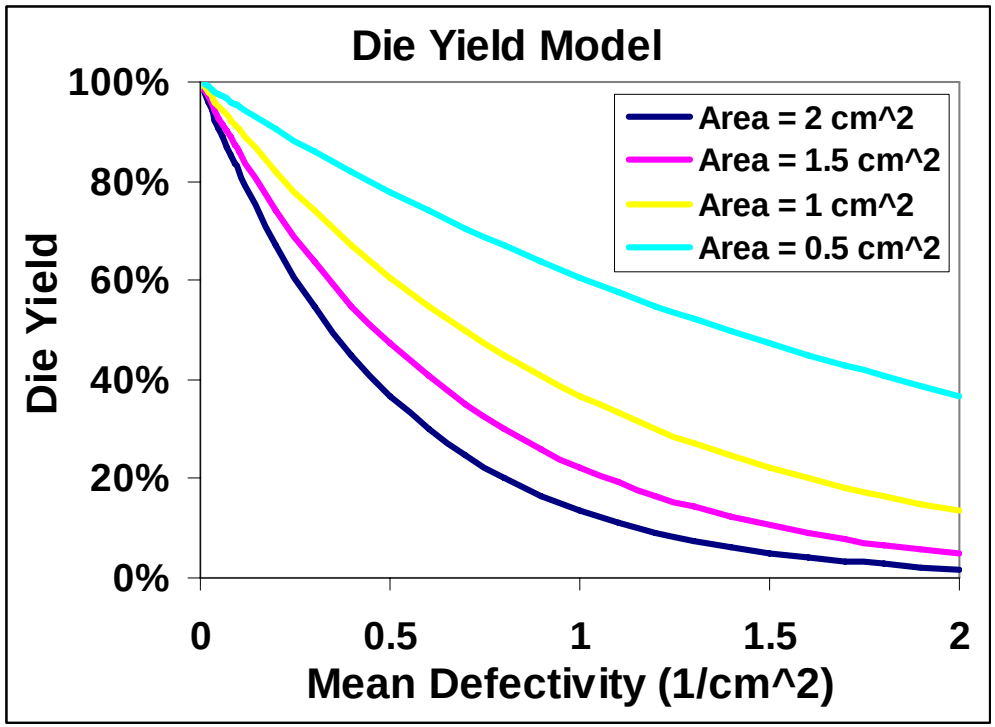


Yield Loss Mechanisms

- Layer defect densities
- Attribute dependent failure rates
- Lithography / CMP driven interactions
- …

- *Yield Loss Mechanisms (YLM's)*
  - Root causes of process related yield loss
  - Each YLM must be characterized in the process with a specific test structure – Characterization Vehicle (CV)

Typical Die Yield Estimation



$$Y = e^{-D_0 A}$$

where,

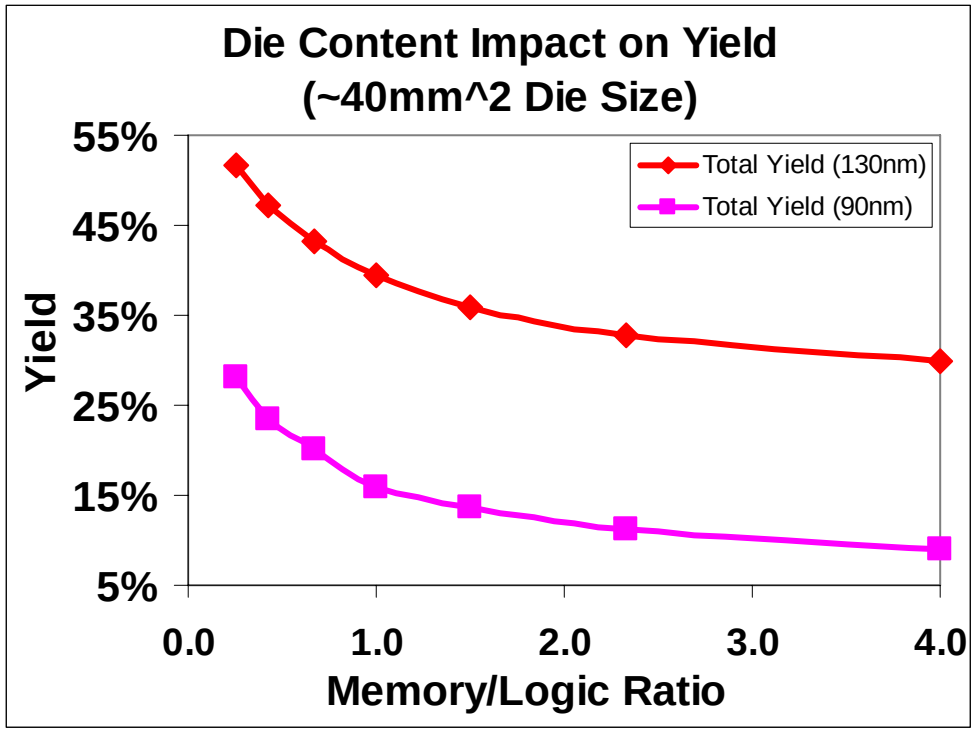
$Y = die\ yield$

$D_0 = mean\ defects\ (1/cm^2)$

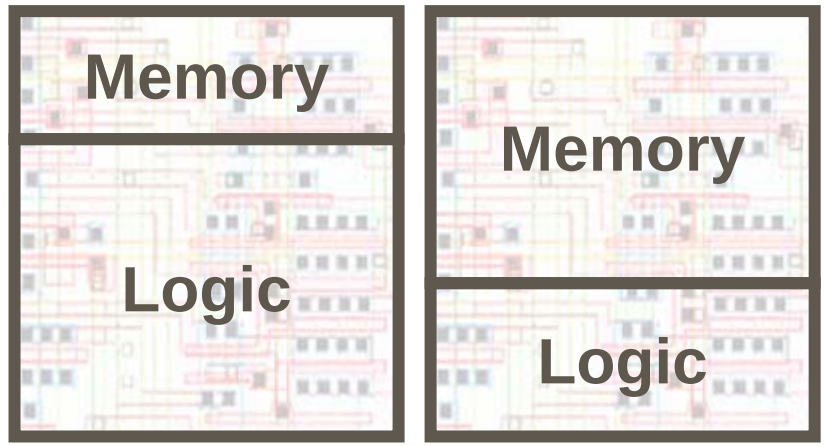
$A = die\ area\ (cm^2)$

- Model implies that for a given die size, yield is based only upon process maturity – this is not correct
  - Yield is different for different IP content
  - Process defectivity is different for each module

Process-Design Interaction



Ratio << 1.0 ***Ratio >> 1.0***



$$Y = Y_{MEMORY} Y_{LOGIC}$$

- Chip Yield is a strong function of design content
  - Physical design features interact with specific module weakness

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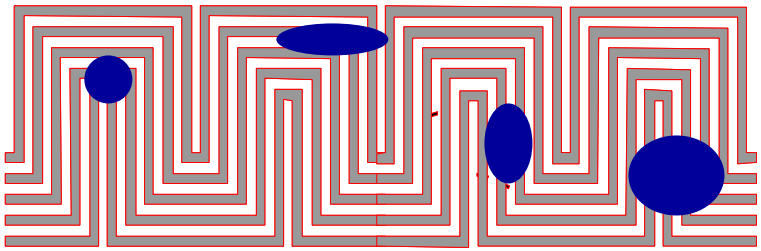
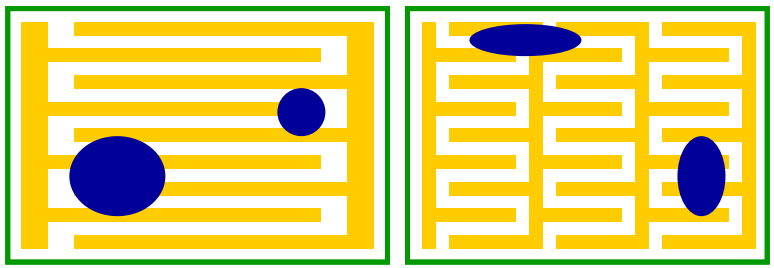
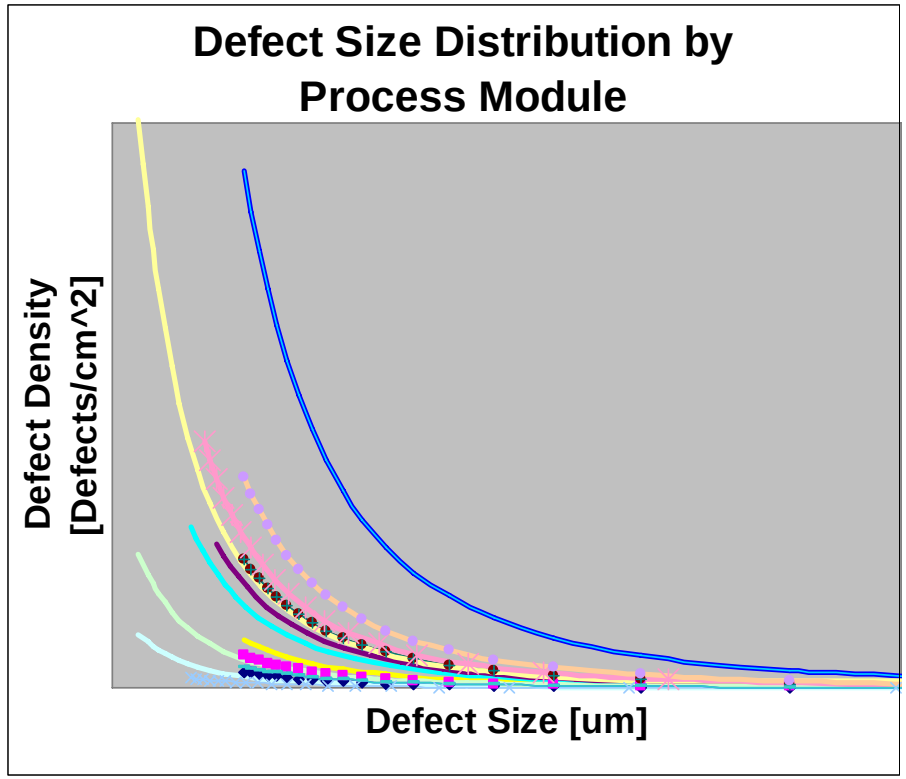
Accurate Process Characterization

Metal Opens/Shorts Characterization Vehicle



Poly and Active Opens/Shorts Characterization Vehicle





$$DSD(x) = \text{defect size/count distribution}$$

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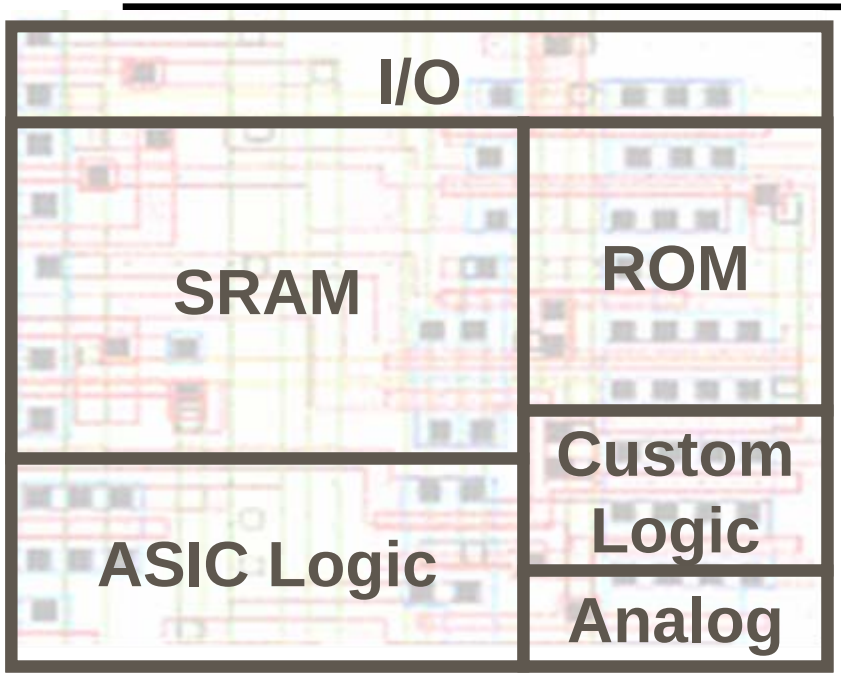
Product Design Attributes



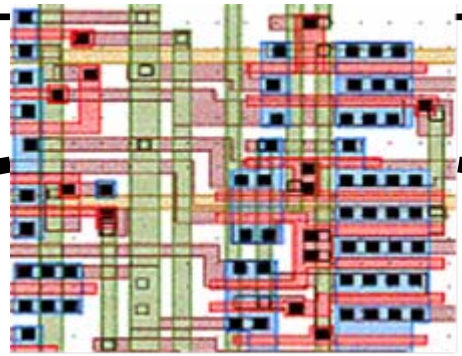
Design Attributes

- **Widths, lengths and spacing**
- **Counts**
- **Densities**
- **Overlaps/enclosures**
- **…**

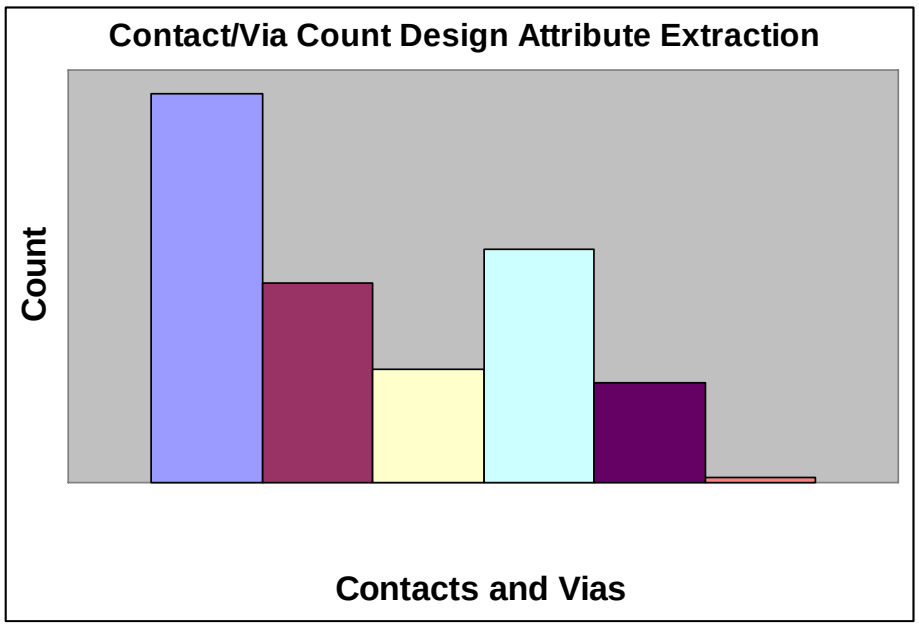
- *Design Attributes:*
  - Physical design properties that interact with specific module marginalities
  - Each attribute can be extracted from physical layout
  - Design attribute extraction (DAE) enables quantification of design content specific YLM models

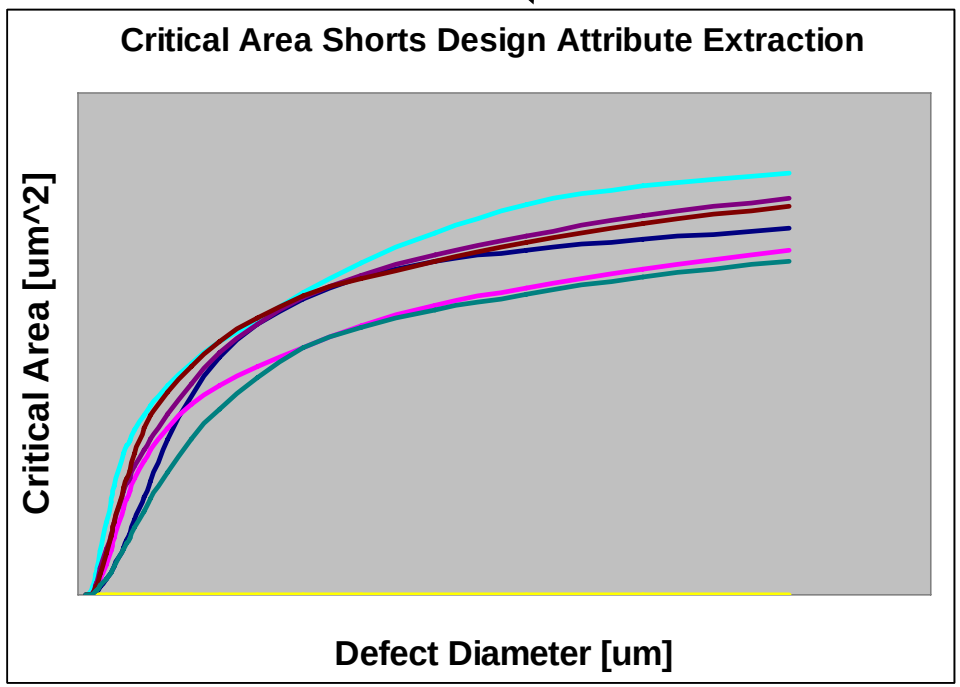
Design Attribute Extraction

Contacts/Via Counts
- N/P Active
- Poly
- V1-Vx



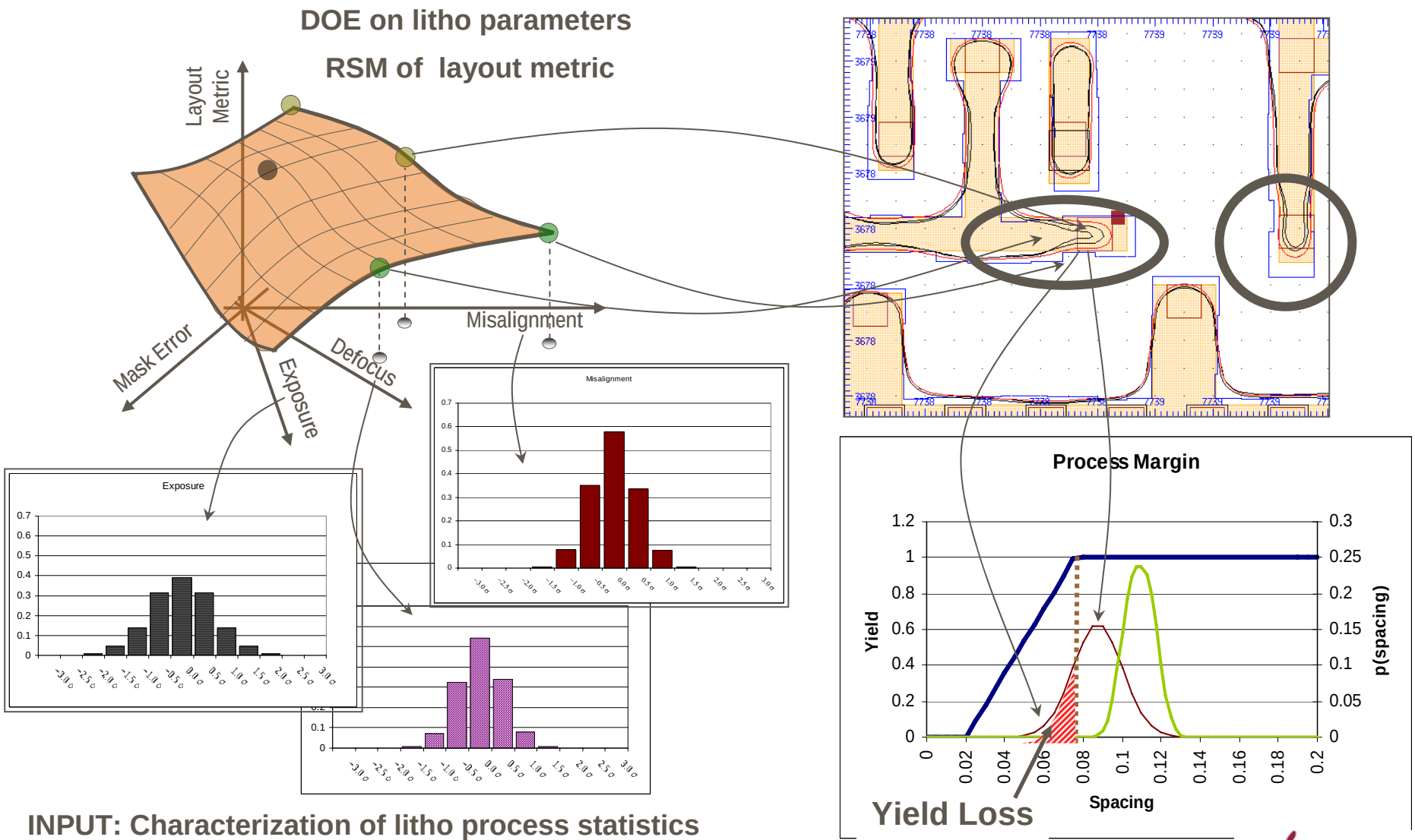
Critical Area Shorts Sensitivities
- AA
- Poly
- M1-Mx





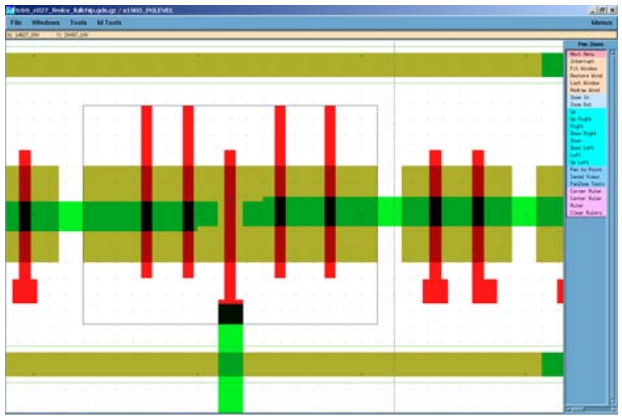
$$A_C(x) = \text{design attribute sensitivity to } x$$

Accurate Process Characterization

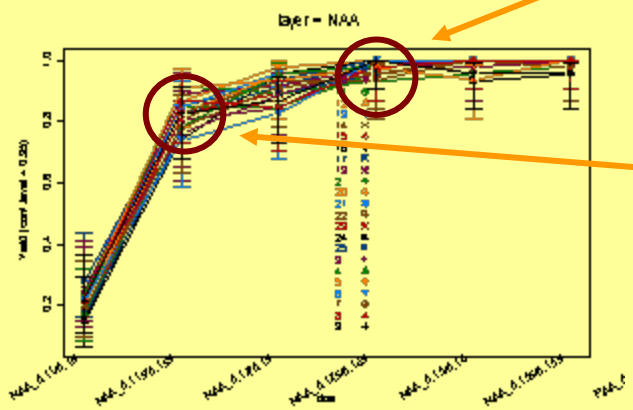


INPUT: Characterization of litho process statistics

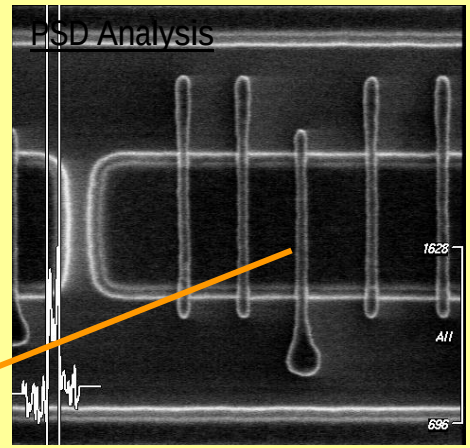
Implicit YLM model: process window effects



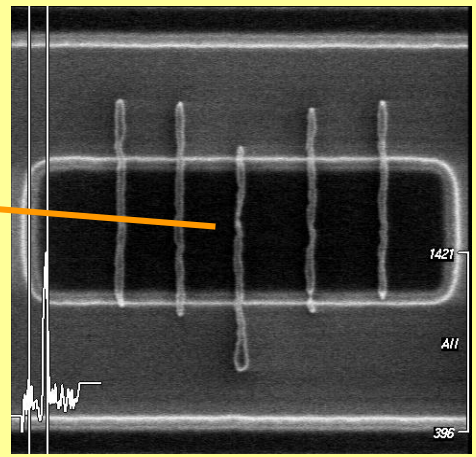
Process Margin data from CV



PSD Analysis

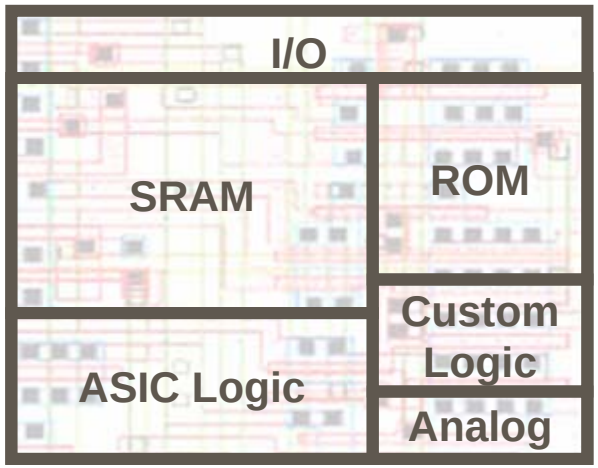


PSD: condition 1



PSD: condition2

Yield Simulation Results: Yield Impact Matrix



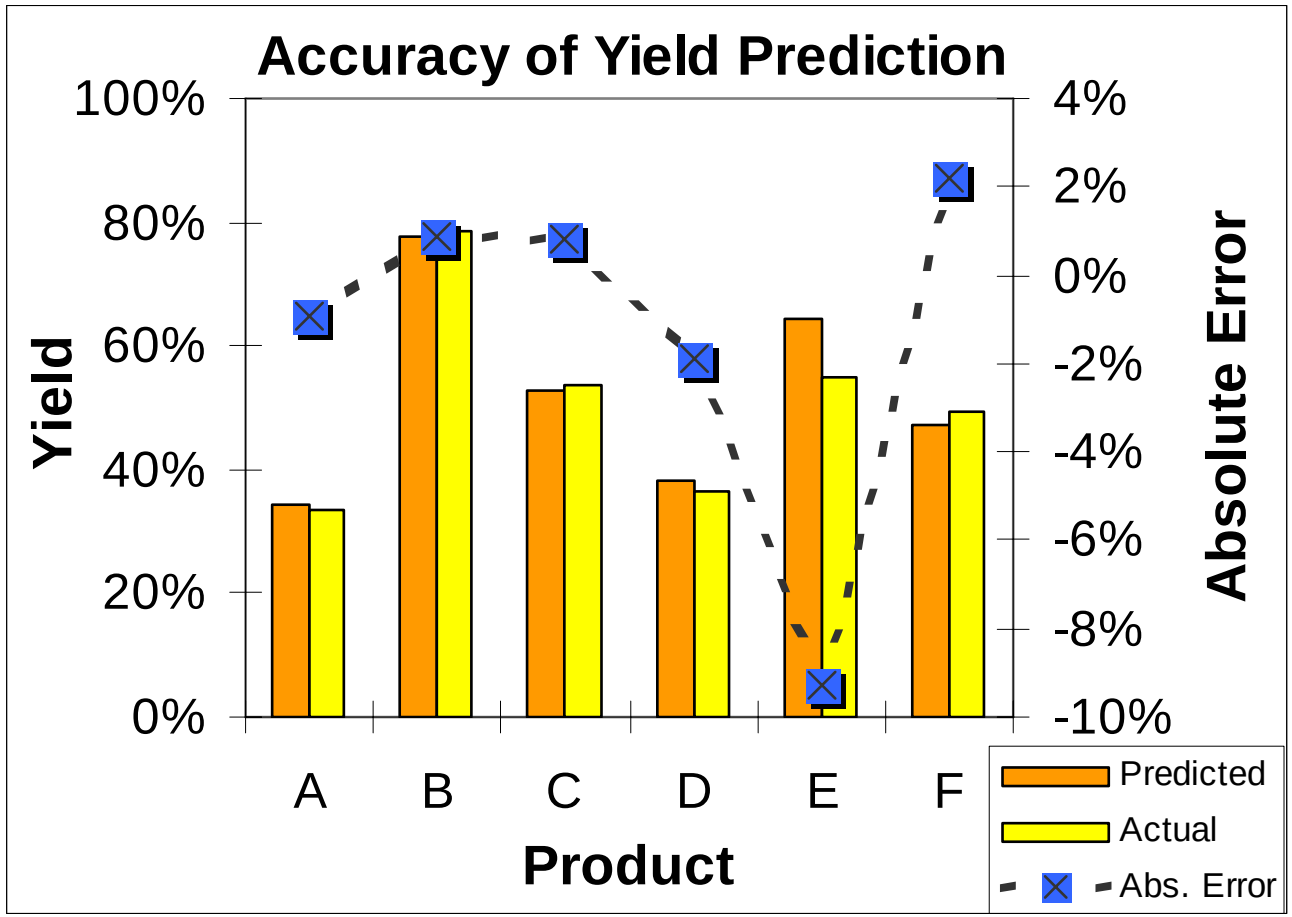
Design Attributes

- Widths, lengths and spacing
- Counts
- Densities
- Overlaps/enclosures
- …

YIMP Matrix				Limited Yield		
Failure Mode				Full Chip	SRAM	LOGIC
Random Defects		Active	Random	98%	99%	99%
			Pattern Dependent	99%	99%	100%
			Total	97%	98%	99%
		Poly	Random	97%	98%	99%
			Pattern dependent	94%	95%	99%
			Total	91%	95%	96%
		Metal	Random	97%	98%	99%
			Pattern dependent	97%	98%	99%
			Total	94%	95%	99%
		Holes		97%	98%	99%
	Total			81%	82%	99%
Systematic		Metal Islands		87%	89%	90%
		Pattern Density		91%	93%	94%
		Narrow Space Wide Neighbor		97%	99%	100%
		Via induced Metal Shorts		77%	78%	79%
	Total			62%	64%	64%

- **Physical design properties that interact with specific module defectivities**
- **Each attribute can be extracted from GDSII**
- **Design attribute extraction (DAE) enables quantification of die content specific yield models**

Yield Simulation Accuracy

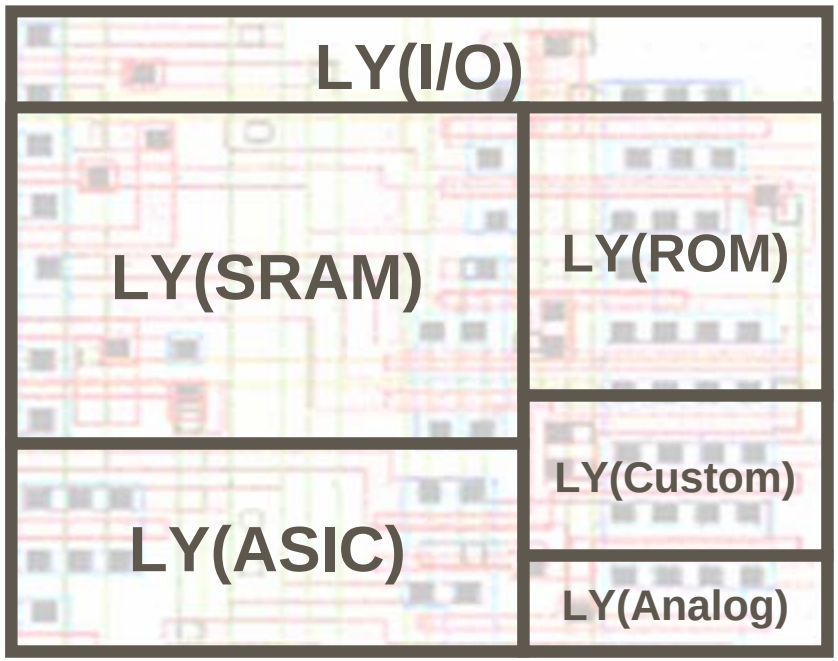


- **Yield modeling accuracy is excellent when you characterize right**
  - **Error represents unidentified yield loss mechanisms or lack of yield model**

Overview of Layout Design for Manufacturability

- **Critical Area Based Wire Spreading**
  - Most useful in Al interconnect era (random metal shorts – dominant yield loss mechanism)
- **Contact/via Doubling**
  - Effective in reduction yield losses due to random hole opens (Al & Cu)
- **Systematic Yield Model Based Local and Global P&R Layout Modifications**
  - Essential for 3-D topography effects due to Cu CMP and low-k interconnect
- **Printability and Performance Variability Driven Layout Generation**
  - Absolute must in the Nanometer Era
  - Pro-active (not afterthought in RET)

Limited Yield Optimization



$$LY_{GAIN} = \prod_{j} \frac{(Y_j)_{v_1}}{(Y_j)_{v_2}}$$

where,

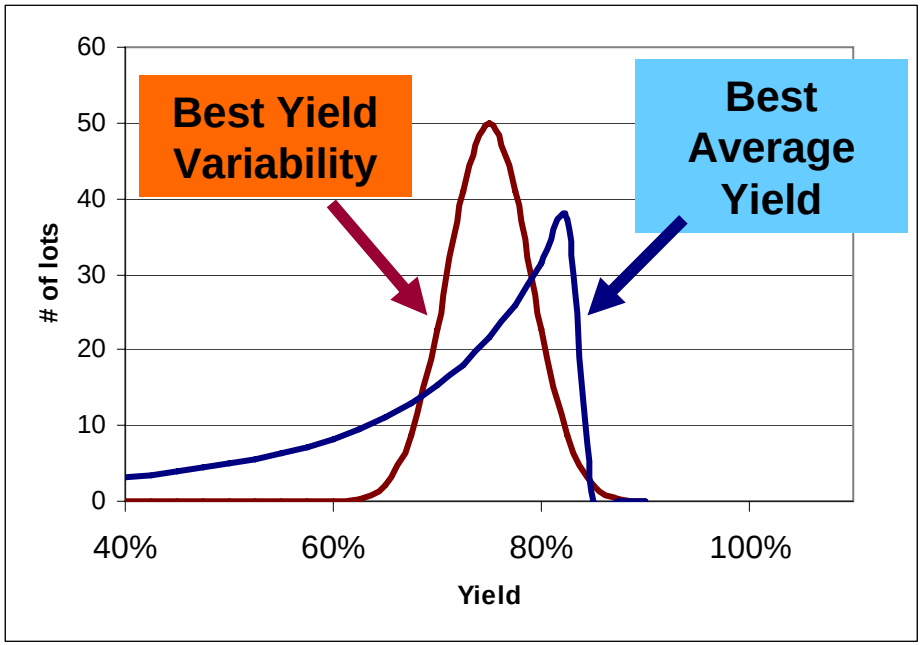
$j = Random, Systematic, Parametric$

$v_1 = optimized\ variant$

$v_2 = original\ variant$

- **Product yields must be optimized by improving LY's**
  - **LY_{GAIN} → ratio of improvement for any specific optimization**
- **Prioritizing which LY's to improve requires an understanding of the specific *Design Manufacturability Objectives***

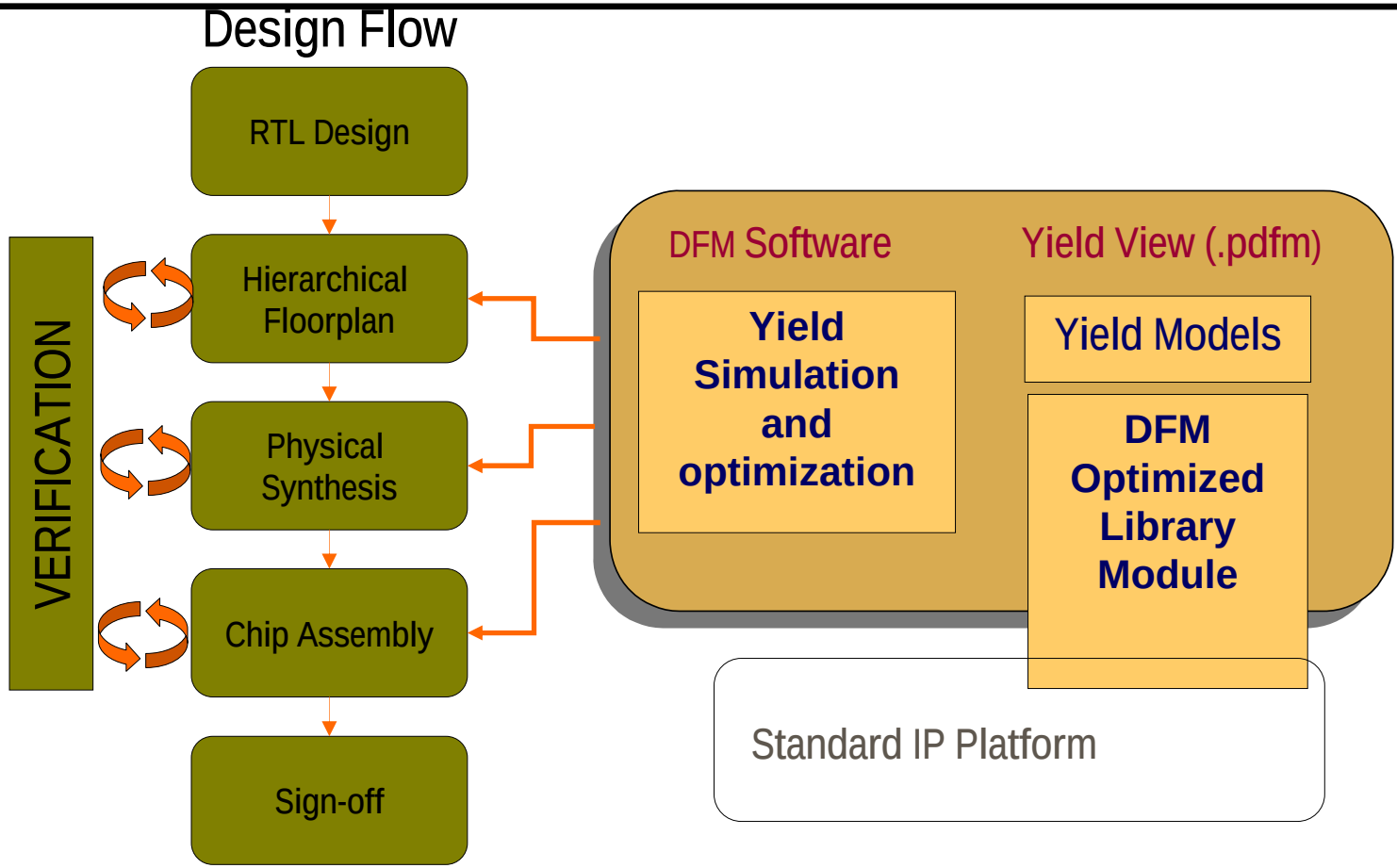
Design Manufacturability Objectives



Objectives	Products
Average Yield	DVD, STB, Cell Phone, Digital Cameras
Yield Variability	Networking, Graphics, DSP
Performance Variability	Microprocessors
Custom	Tailored specifically for a process and product

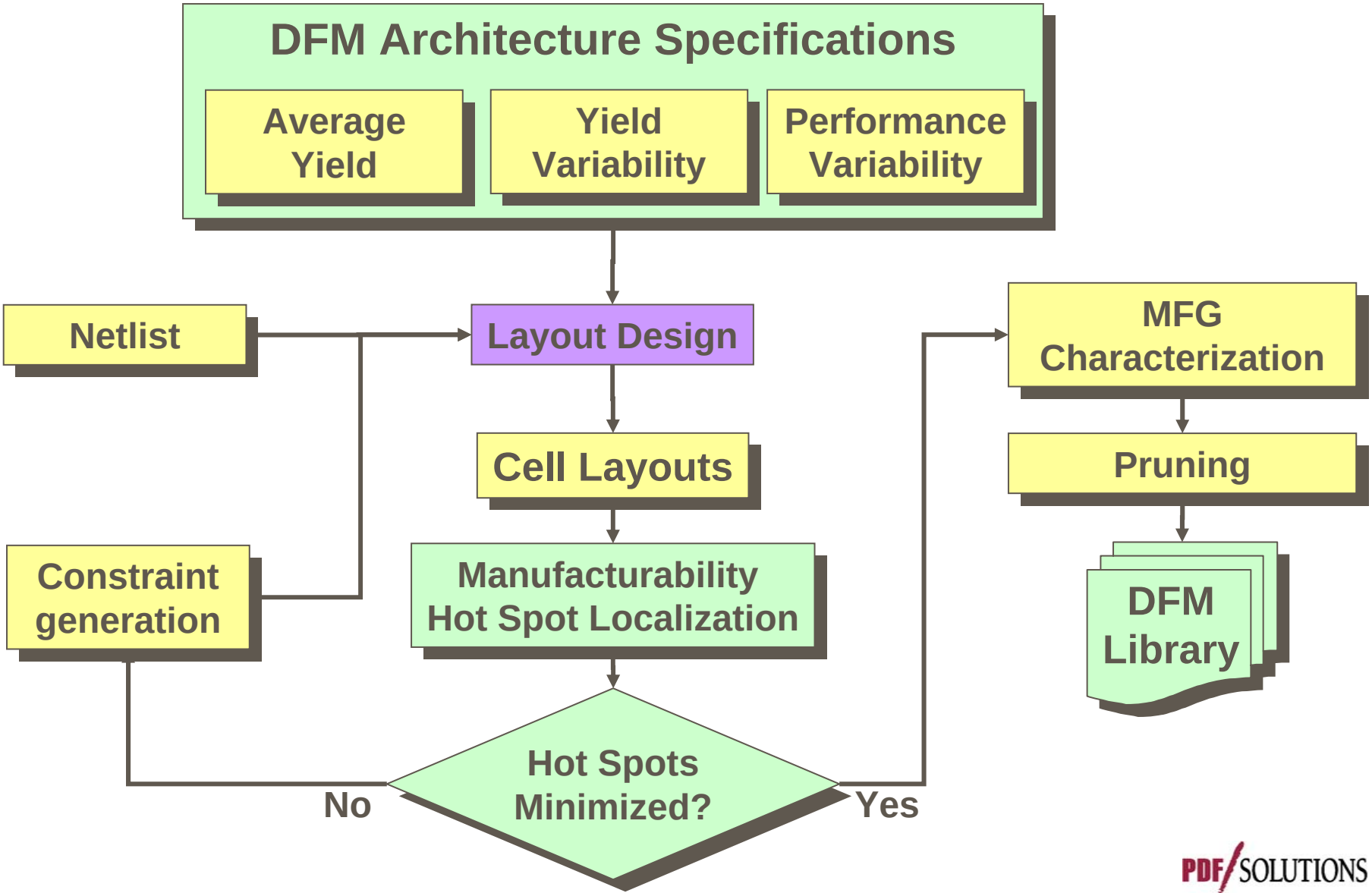
- **Customization of DFM objectives**
  - **High volume parts in mature process**
  - **Lower volume parts during ramp**

Enabling Proactive DFM For Designers



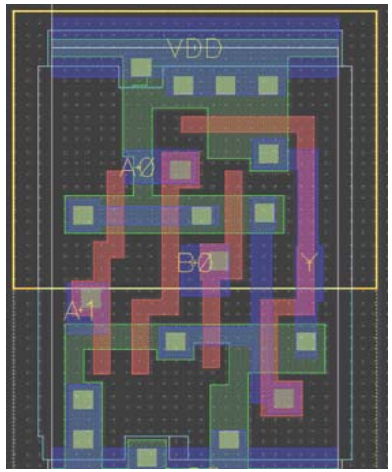
- Three components to enable Proactive DFM
  - DFM library module
  - Layout attribute dependent yield models (DFM library view)
  - Yield simulation and optimization software

DFM Variant Generation Flow

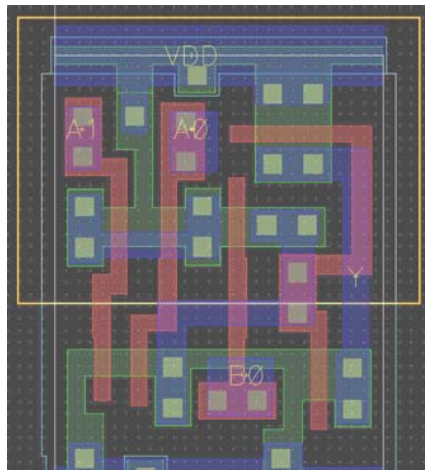


Yield Variants Example

High Density



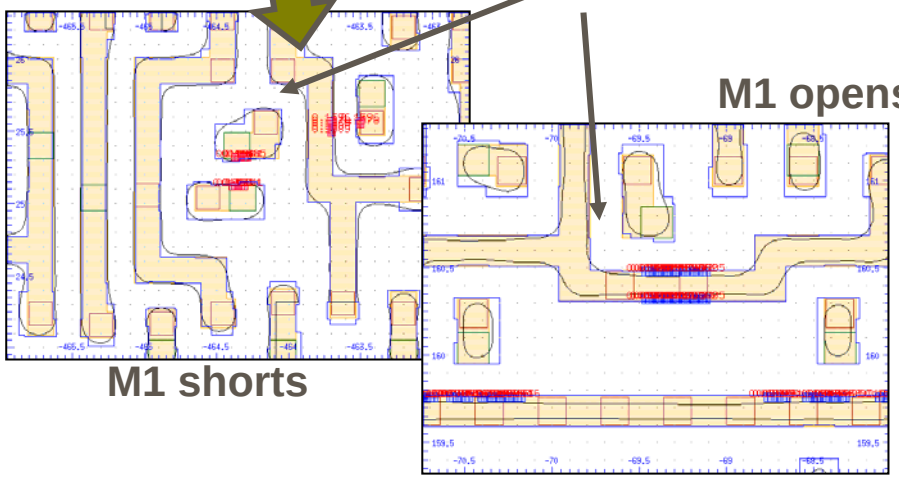
Random/Systematic Yield Variant



+20% area

-50% FR (ppb)

Litho hot spots



M1 opens

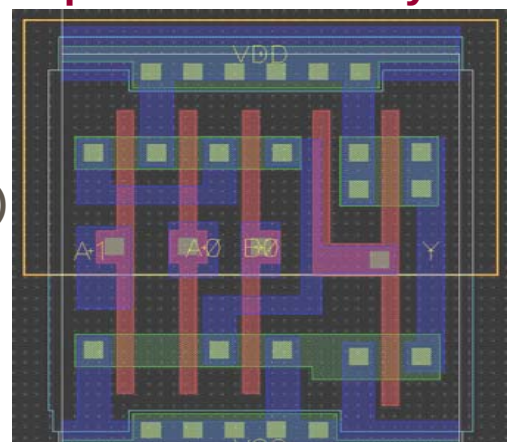
M1 shorts

Yield/Speed Consistency Variant

+40% area

-50% FR (ppb)

-85% YV (std.dev)



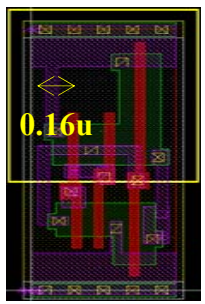
Standard Cell Optimization Flow

Original Netlist

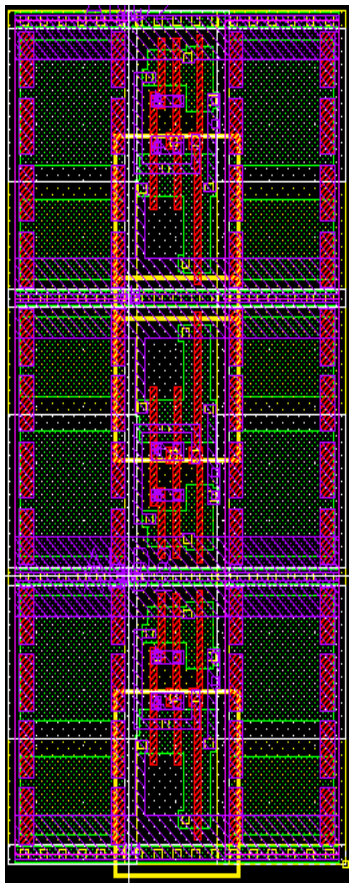
```
MOS1 d g s b nmos L=0.13u W=1u
MOS2 d g s b pmos L=0.13u W=0.8u
MOS3 d g s b nmos L=0.13u W=0.7u
MOS4 d g s b pmos L=0.13u W=1.2u
MOS5 d g s b nmos L=0.13u W=1.3u
MOS6 d g s b pmos L=0.13u W=1u
```

Cell Architecture

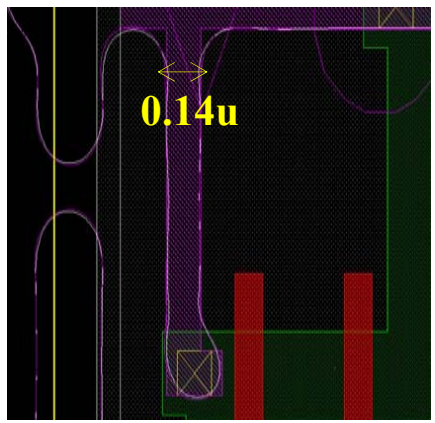
Contact redundancy definition
Spacing rules definition
Transitions rules definition
Metal islands definition
Taps
...



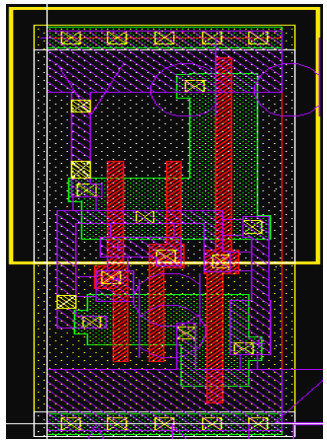
Synthesized Layout



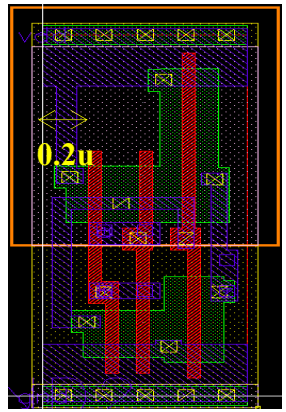
Litho Environment



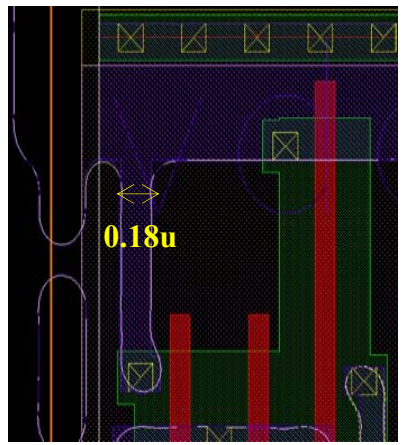
Litho Simulated Layout



Hot Spot Analysis

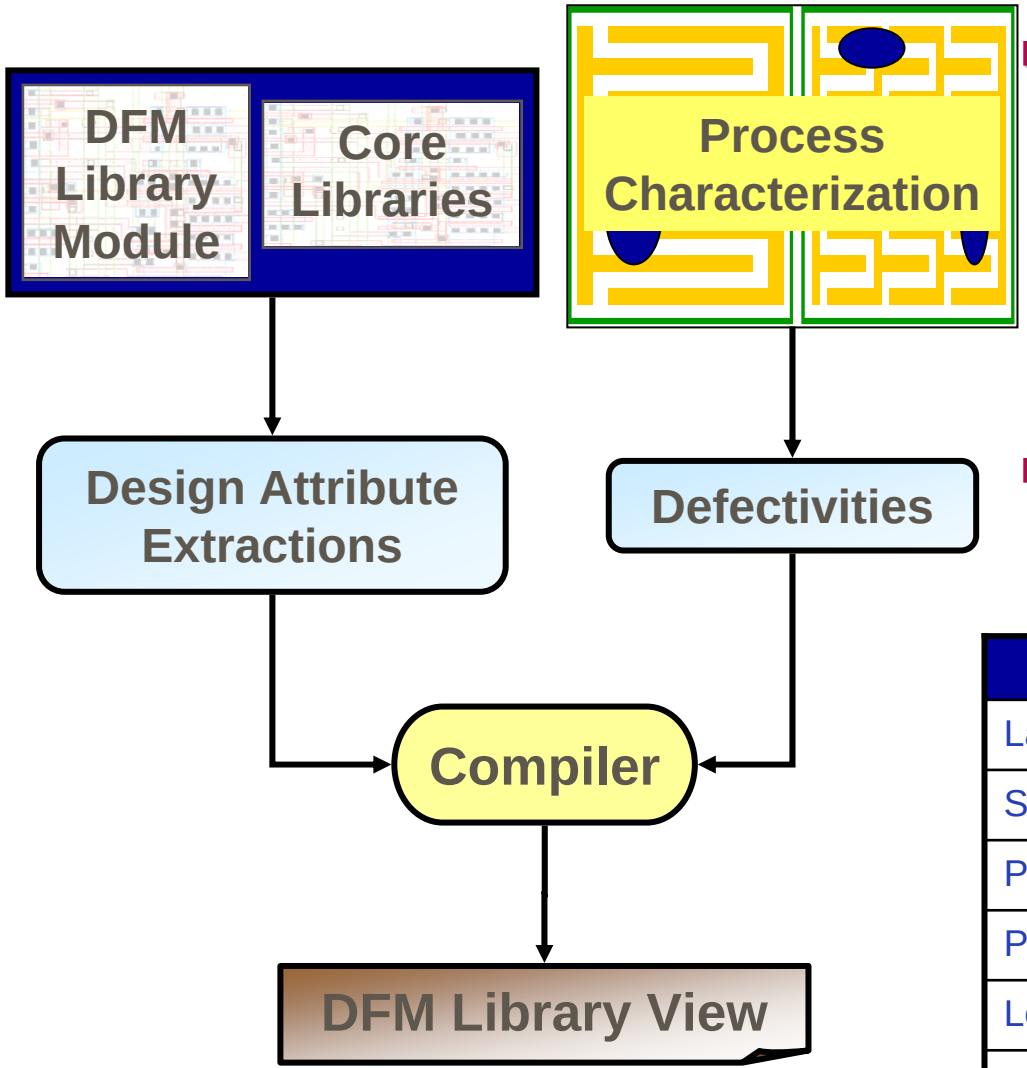


Optimized Layout



Optimized Layout

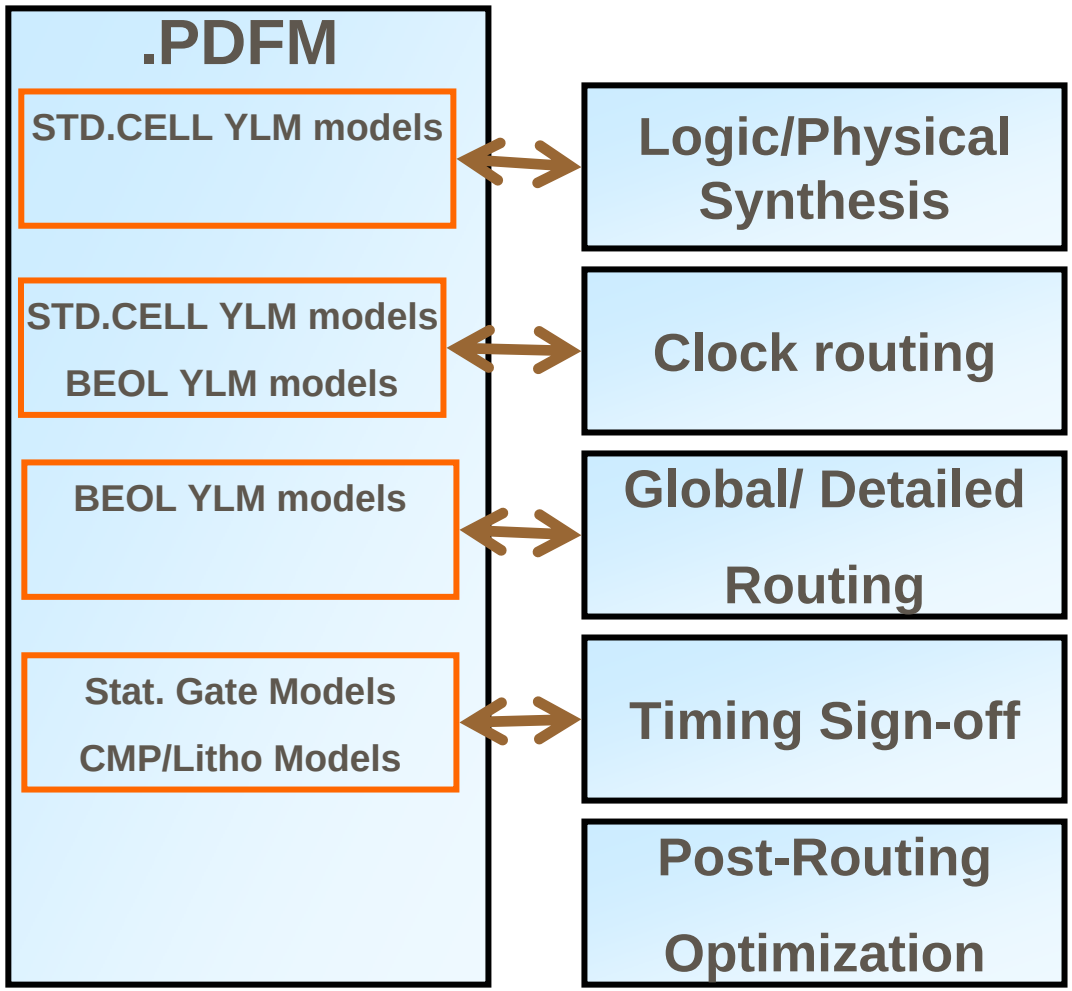
DFM Library View for EDA



- ***.pdfm view*** **includes relevant data to enable EDA tools to make yield tradeoffs**
  - **Process Defectivities**
  - **Design Attributes**
  - **Yield and Manufacturability Models**
- **.pdfm data also enables BEOL routing optimzation**

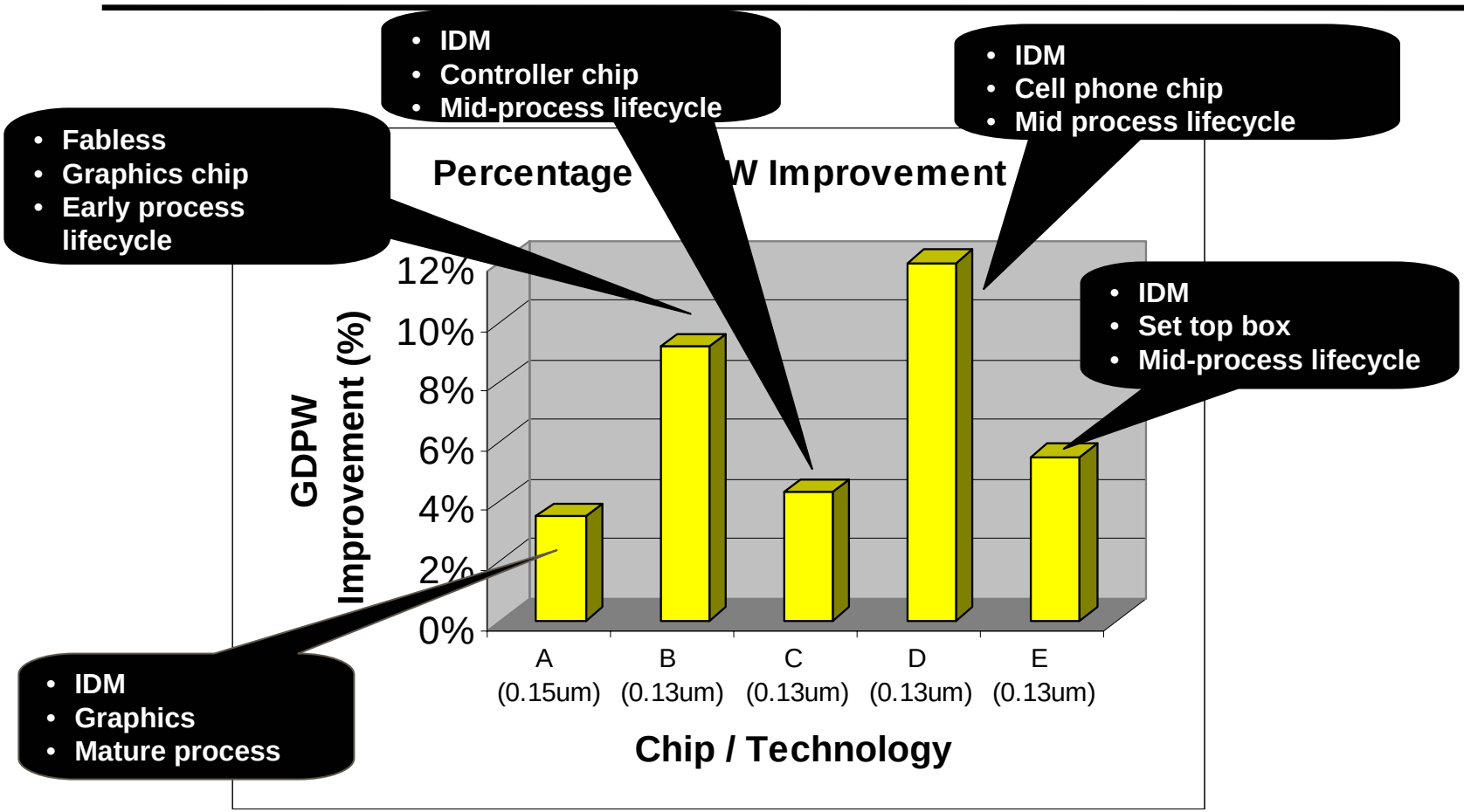
Characteristic	Library View
Layout	GDSII
Schematic	SPICE Netlist
P&R Footprint	LEF
Performance	.lib
Logic Function	Verilog
Manufacturability	.pdfm

“pDfx enabled” P&R



- Include yield in the cost function
- Take advantage of design slacks
- Timing convergence properties unchanged

And the Silicon Says…

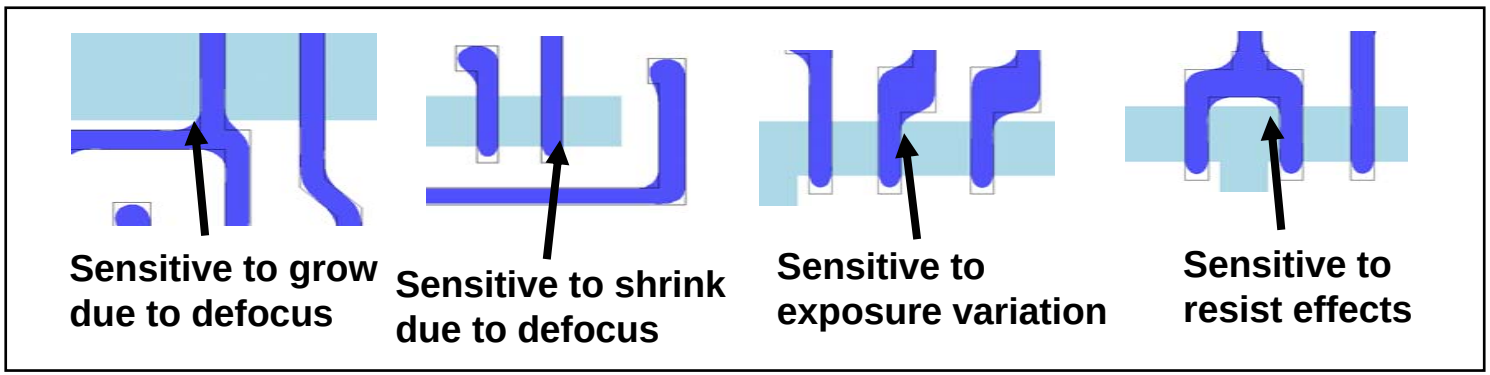


- *Silicon shows up to 12% GDPW improvement by applying our Proactive DFM methodology*

PDF SOLUTIONS
Yield, Performance, Profitability

Looking Into the Future: Extreme Layout Regularity

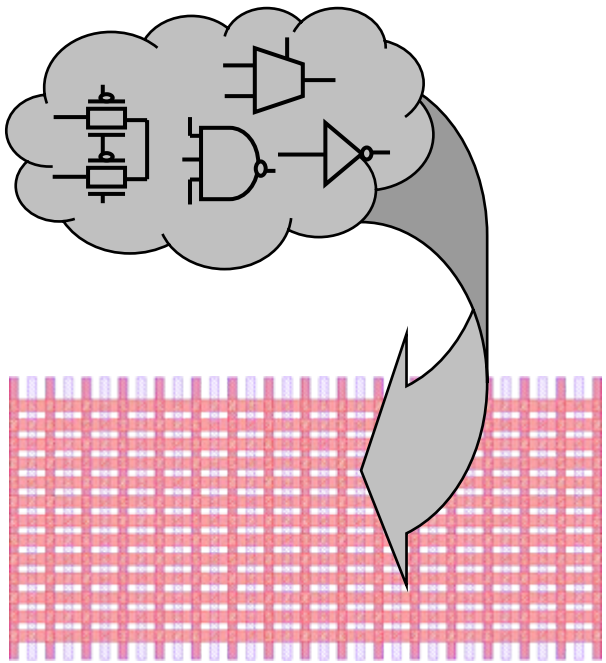
- **RETs are time-consuming and difficult to optimize for large process windows**
  - **Defocus, Illumination conditions, Pattern neighborhood**



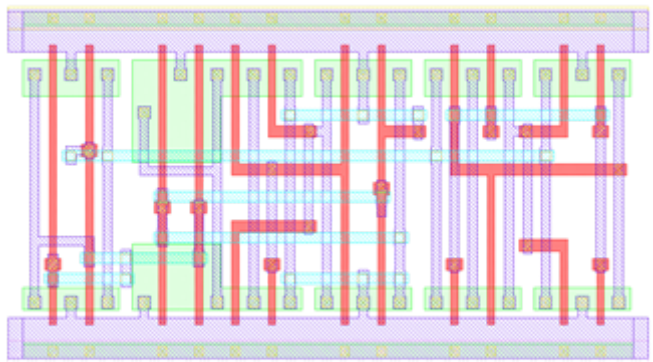
- **Conventional design rules are becoming insufficient to guarantee design's adherence to RETs**
  - **Increasing need for more *geometry regularity by design***

Regular Logic Bricks

- Arrays offer advantages for silicon characterization and even inventory, but at a high area penalty
- Regular Logic Bricks can offer more efficient use of area, and still provide the required regularity



Map a simple set of logic primitives onto regular fabric patterns to form logic bricks



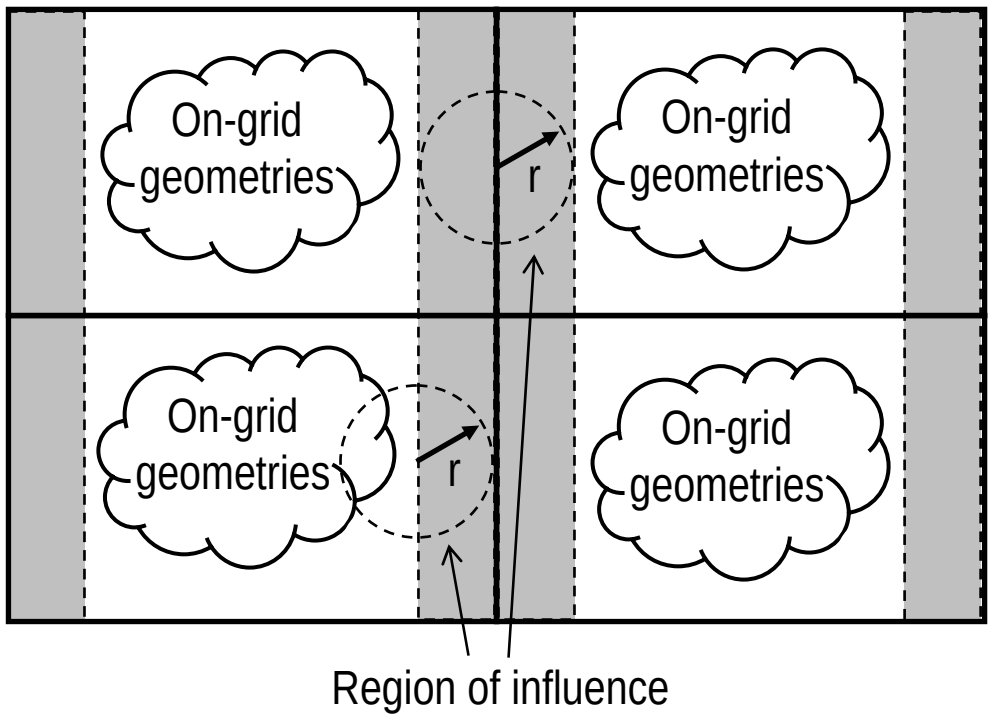
Macro Regularity

- Regular fabric ensures that logic bricks share geometry regularity with all other bricks and registers
- Fabric “rules” co-optimized for memories, IPs, and bricks
- Compatible RETs and geometries at brick boundaries

Optical proximity:

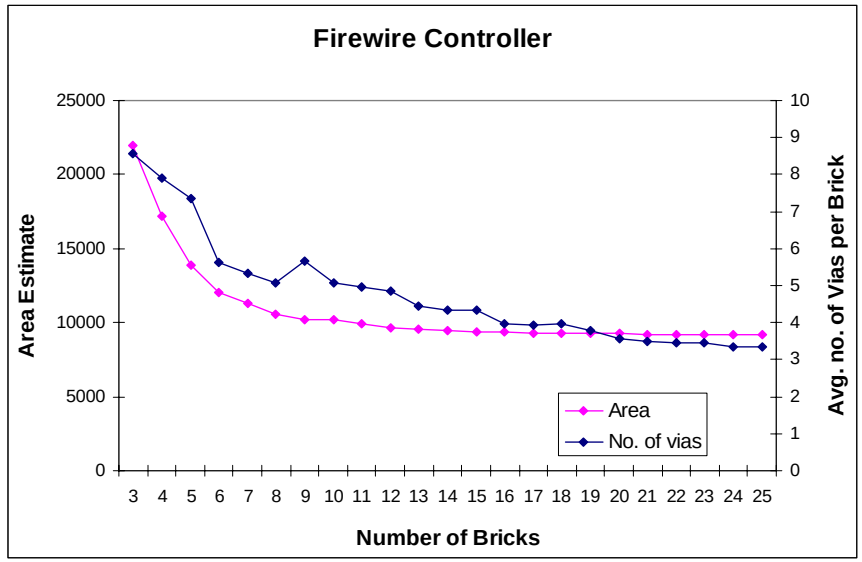
r ≈ 1um

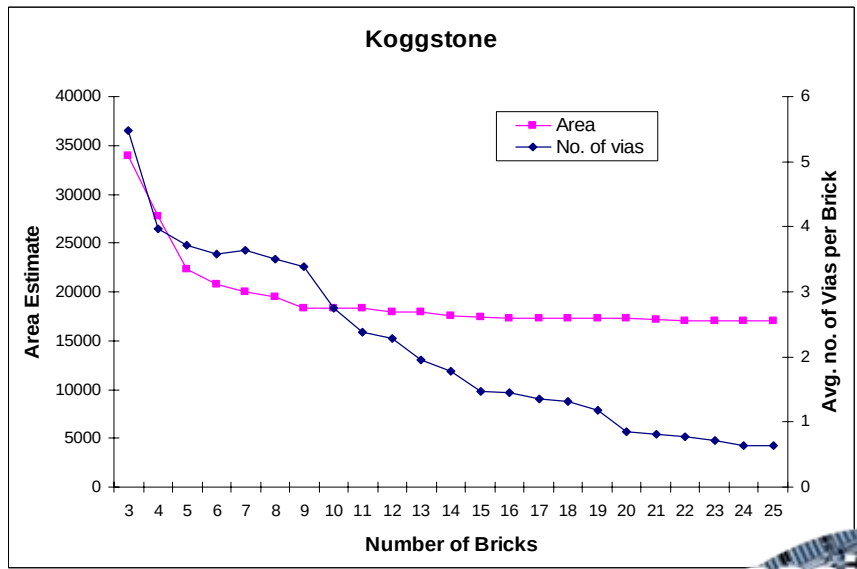
2-3 INVs on boundaries of logic bricks



Some Experimental Results

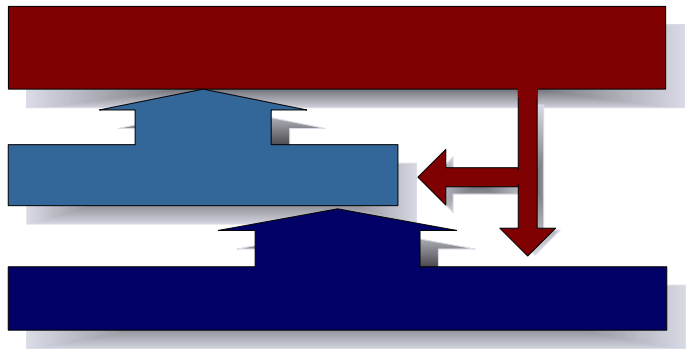
- **Little area benefit for using more than 10 unique bricks**
  - **Few unique bricks allows for macro regularity and silicon validation analogous to CLBs and bit cells**
- **Trade-off between number of geometry patterns and area/performance**
- ***Ideally, regular fabric synthesis tool would determine this for each design in an application-specific manner***

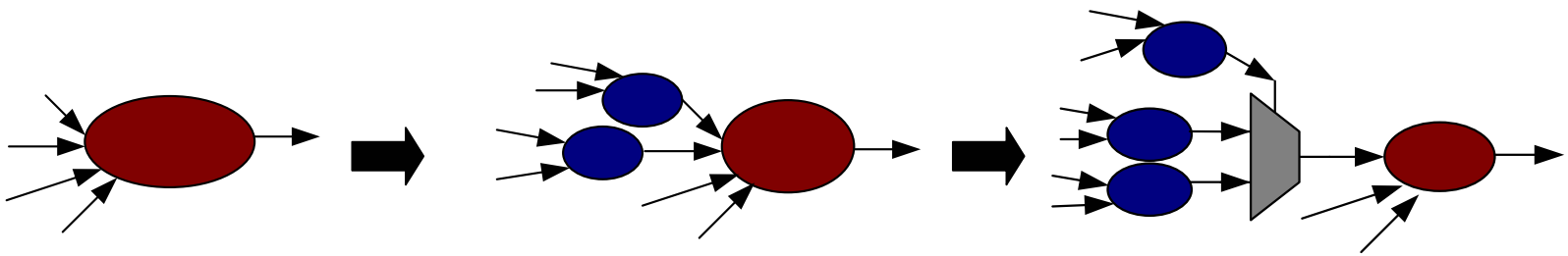




Exploiting Regularity

- **Logic regularity provides *opportunities* for new predictable methodologies**
  1. **Small library of primitives**
  2. **Mapping into a set of configurable pre-defined bricks**



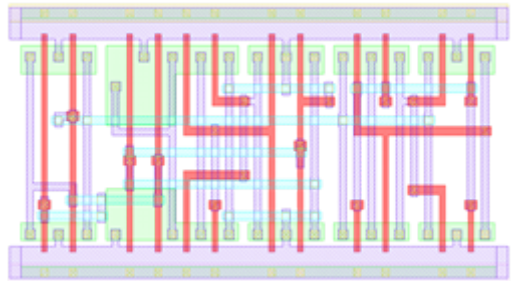


Factors f & f' from F

G_1 & G_2 are positive & negative cofactors with respect to function f

Ultimate Goal

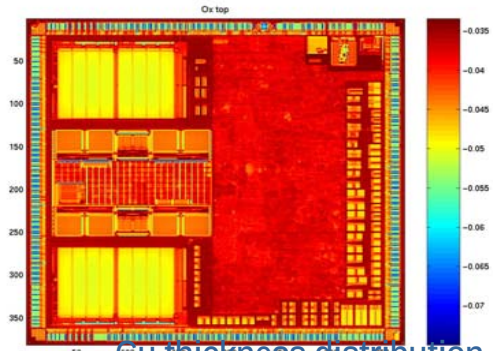
- From synthesis we define the set of regular logic bricks that *cover* the extracted logic modules
- From the fabrics level, perform shapes-level physical-synthesis to construct configurable bricks
  - Nano-scale constraints allow us to simplify this shapes-level physical synthesis problem
  - Can be optimized with simulation-based printability modeling



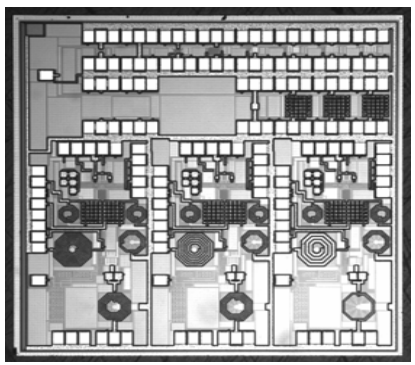
Automated layout

Further Considerations

- **Global effects and system-level issues**
  - **Memory and logic compatibility**
  - **Regular BEOL – structured routing**
  - **Analog components**



Cu thickness distribution



WLAN WCDMA GPS