Layout Impact of Resolution Enhancement Techniques: Impediment or Opportunity?

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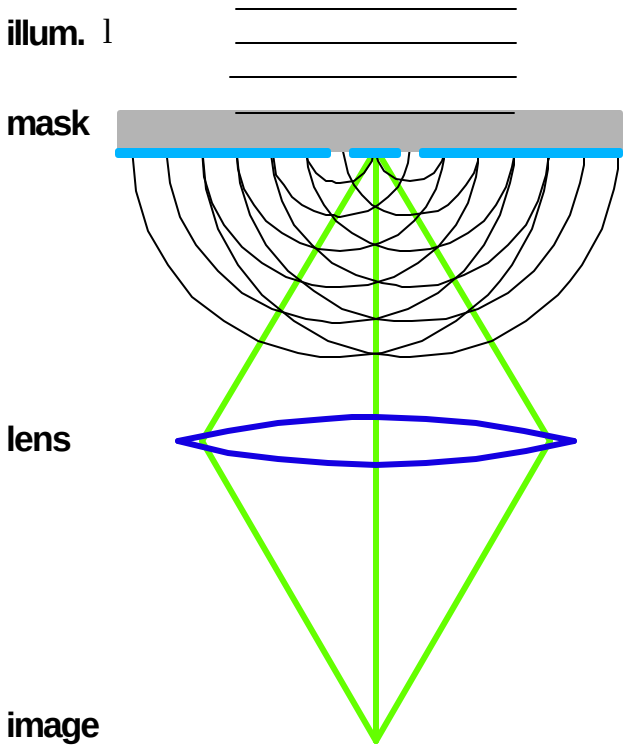
Outline

- Brief Lithography Primer
- Current Lithography Tool Options
- Intro to Resolution Enhancement Techniques
- Future Lithography Tool Options
- Strong RET, Benefits, Challenges, Opportunities
  - strong RET require layout restrictions
  - break the established 'DRC-driven' layout flow
  - RET-embedded layout
  - Layout based on Radical Design Restrictions

Conventional Lithography



$$\sin\theta_m = m\,\frac{\lambda}{P}$$

$$P_{min} = 1\,\frac{\lambda}{\sin\theta}$$

$$P_{min} = 1\,\frac{\lambda}{NA}$$

$$R_{min} = 0.5\,\frac{\lambda}{NA}$$

$$R_{min} = k_1\,\frac{\lambda}{NA}$$

$$k_1 = 0.5$$

$$DOF = \frac{\lambda}{2\,NA^2}$$

1) resolution is controlled by λ and NA
2) improving resolution by increasing NA hurts DOF (NA = sinθ ...1 is the limit -- in air)
3) k_1 = 0.5 resolution limit is real physical barrier

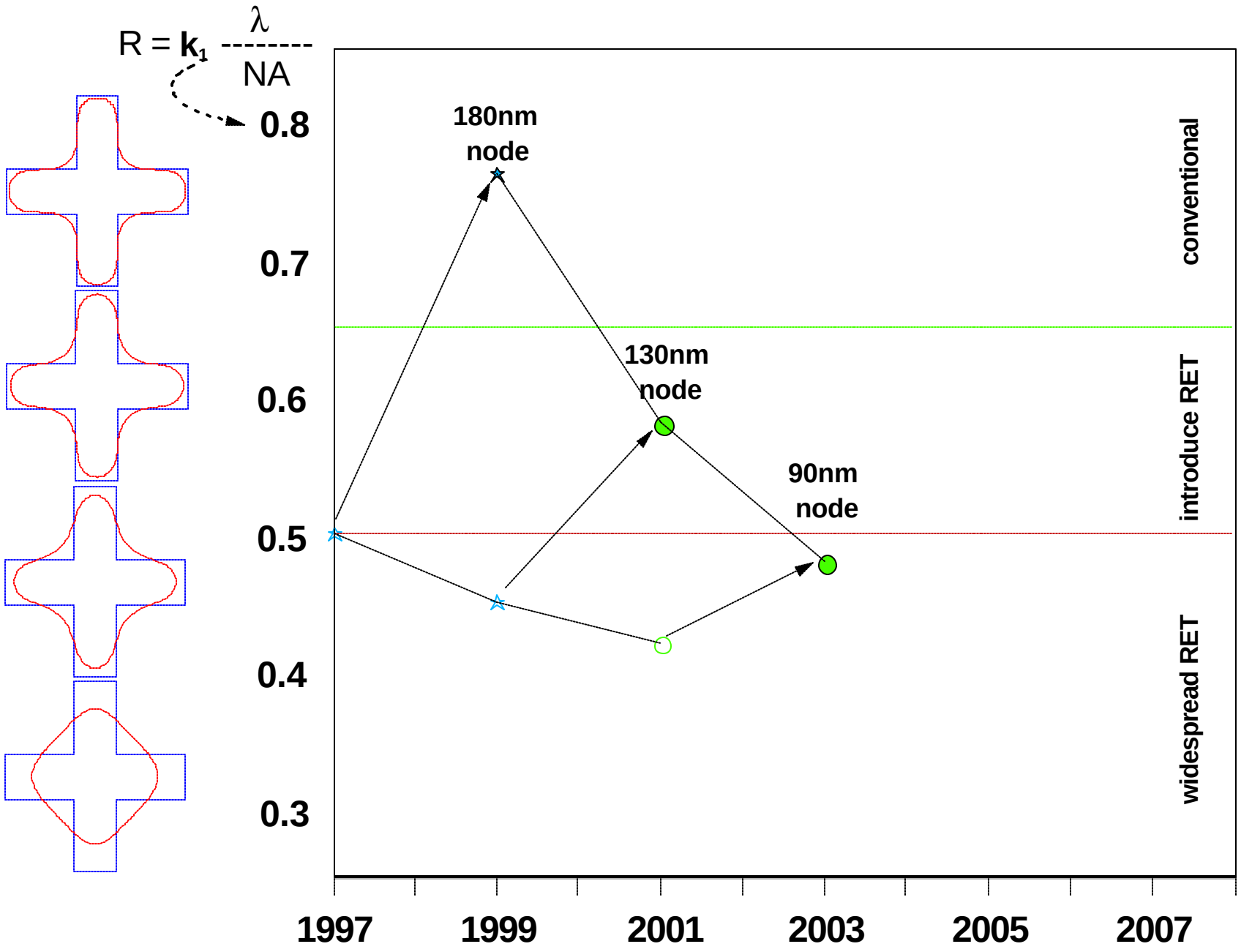
Resolution, Past - Present

ITRS Node	Year of Man.	min. Pitch	development λ/NA	manufacture λ/NA	development k_1	manufacture k_1
180	1999	500	248 / .50	248 / .75	.50	.76
130	2001	300	248 / .75	193 / .75	.45	.58
90	2003	214	193 / .75	193 / .85	.42	.48
65						
45						

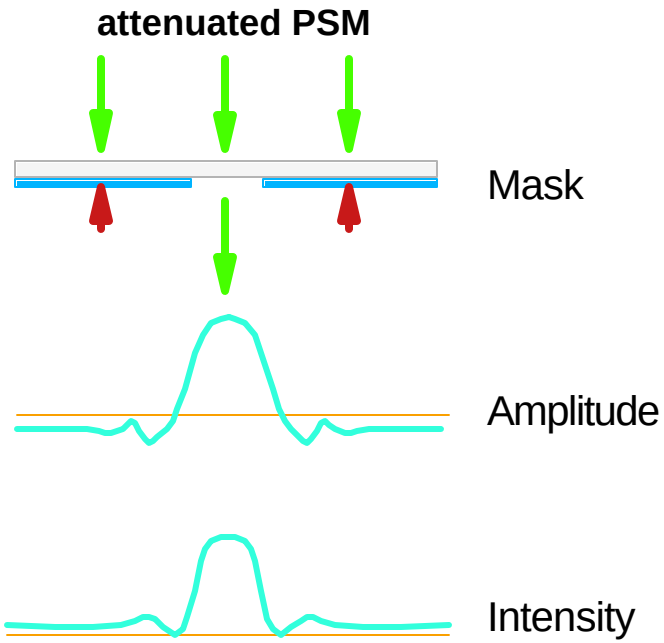
1) Spite continuous reduction in wavelength and increase in NA
.....k_1 has been eroding (i.e. litho has gotten harder)

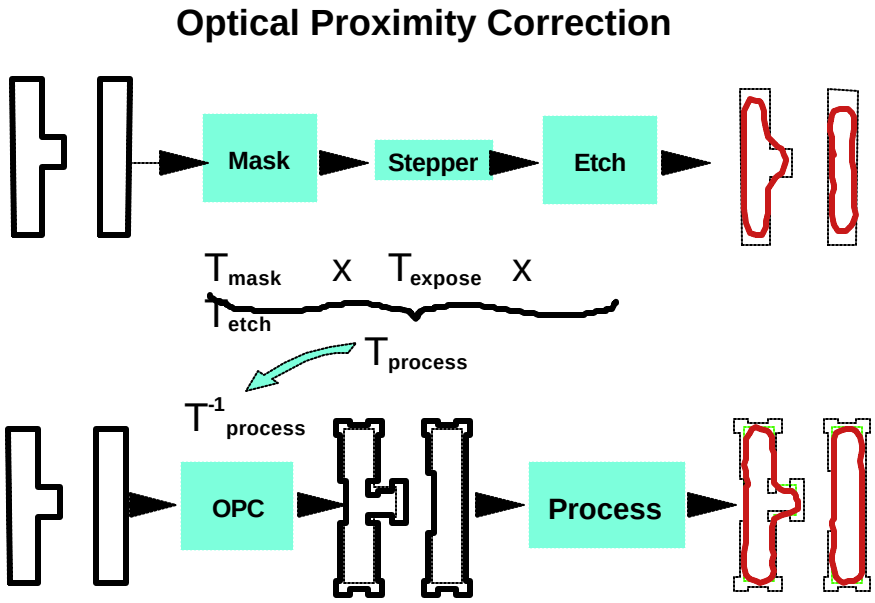
2) For k_1 near 0.5 'mild RET' have been introduced

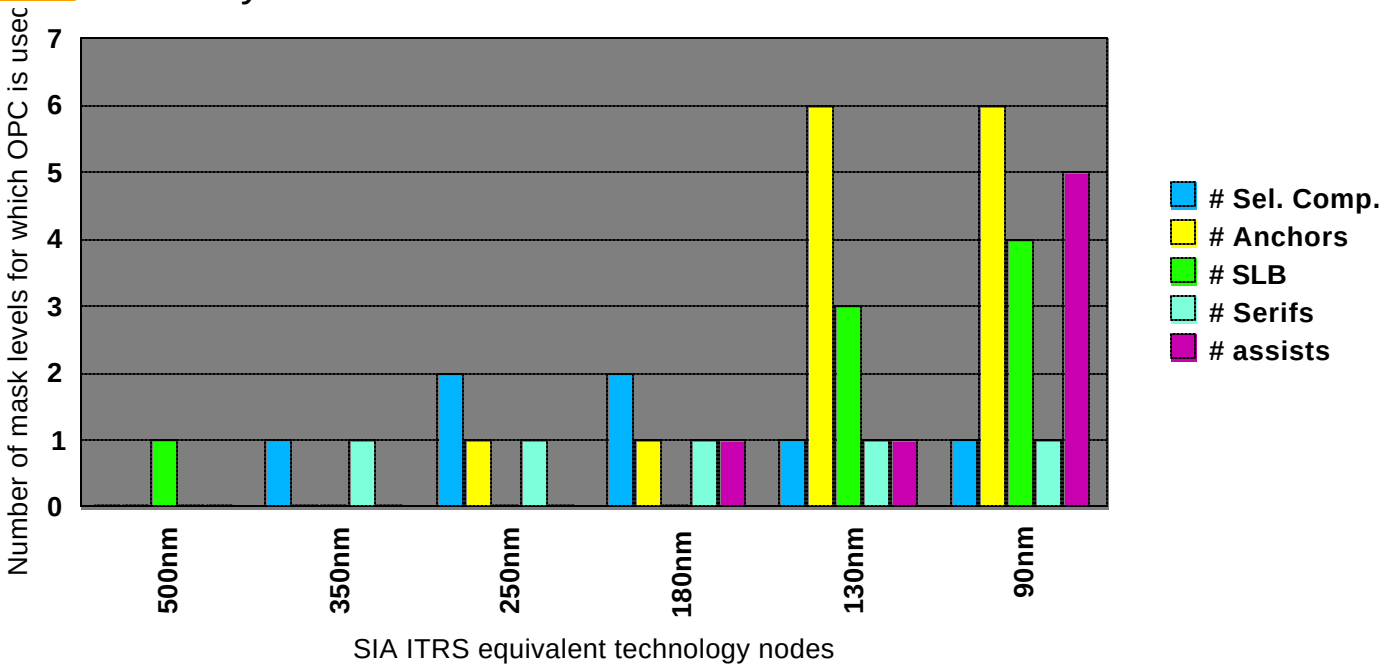
Rayleigh constant for various technologies ... the 'past'



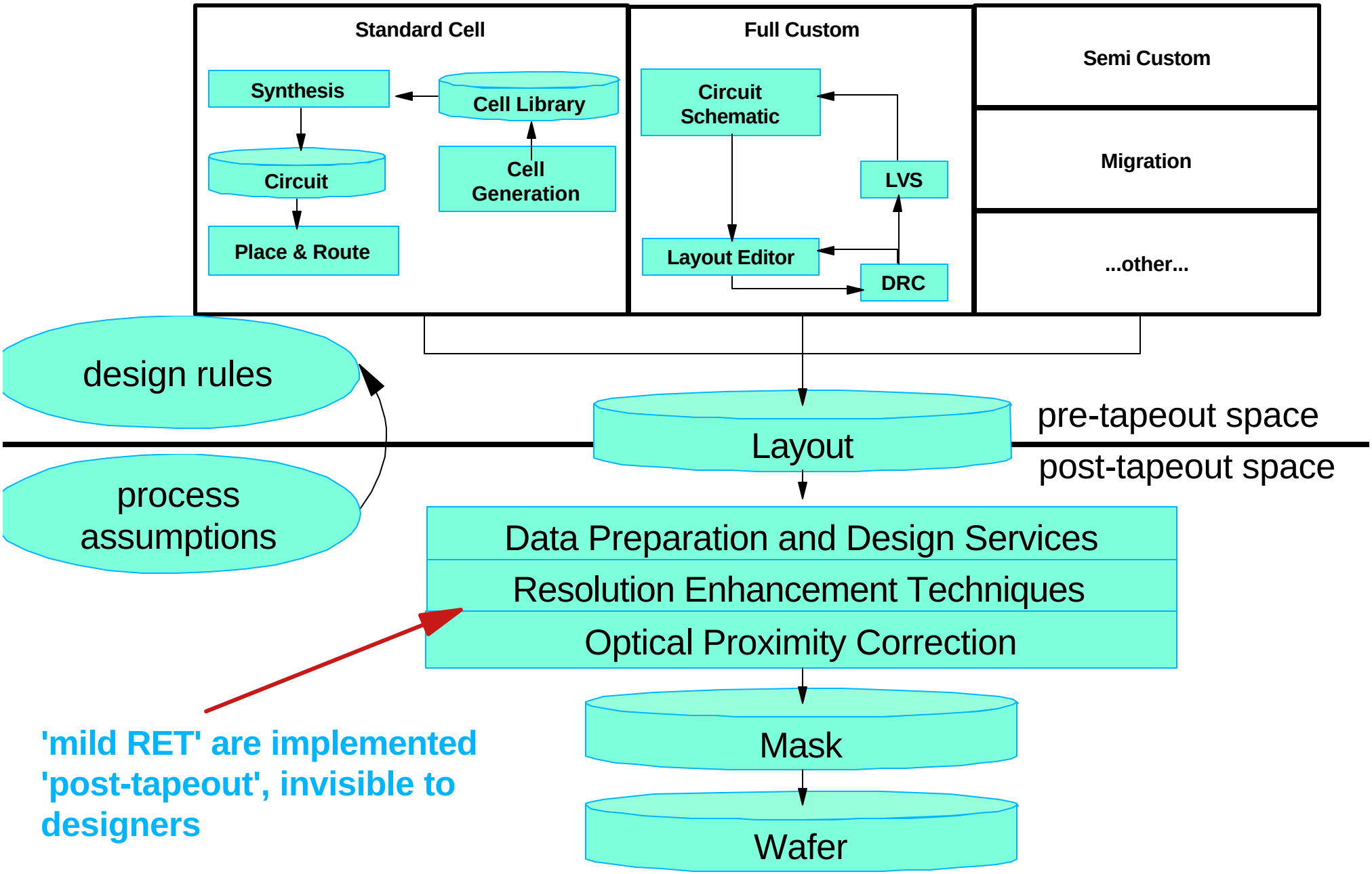
Two examples of mild RET







Current approach: design flow with mild-RET



'mild RET' are implemented 'post-tapeout', invisible to designers

key 65nm node parameters ... litho

The International Technology Roadmap For Semiconductors: 2002 Update

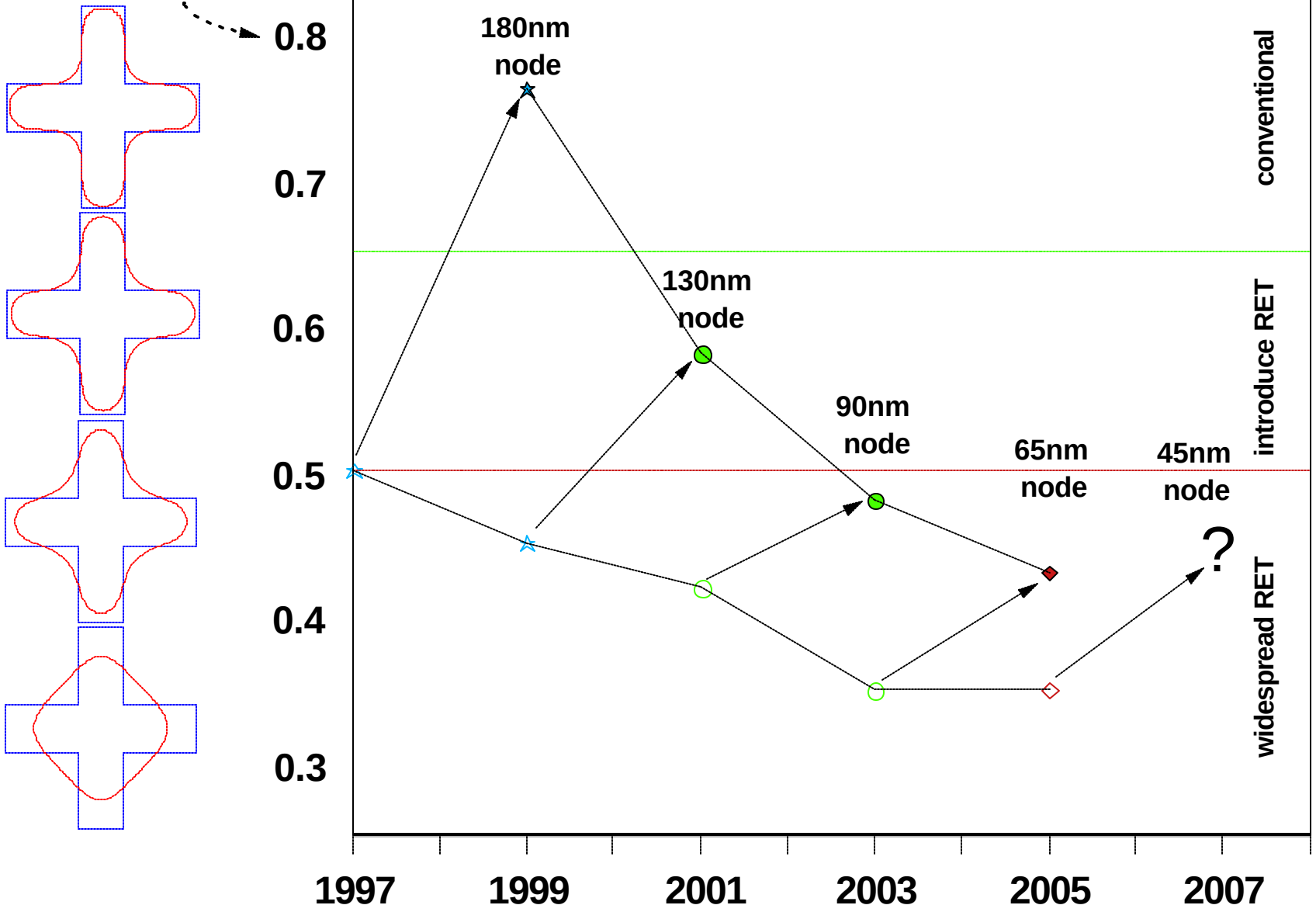
Year of Production	2001	2002	2003	2004	2005	2006	2007
MPU 1/2Pitch (nm)	150	130	107	90	80	70	65
MPU gate in resist (nm)	90	70	65	53	45	40	35
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
Gate CD control (3 sigma) (nm)	5.3	4.3	3.7	3	2.6	2.4	2
ASIC/LP 1/2 Pitch (nm)	150	130	107	90	80	70	65
ASIC gate in resist (nm)	130	107	90	75	65	53	45
ASIC/LP gate length after etch (nm)	90	80	65	53	45	37	32
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
CD control (3 sigma) (nm)	7.3	6.5	5.3	4.3	3.7	3	2.6

Common Terminology: **130nm node** **90nm node** **65nm node** **45nm node**

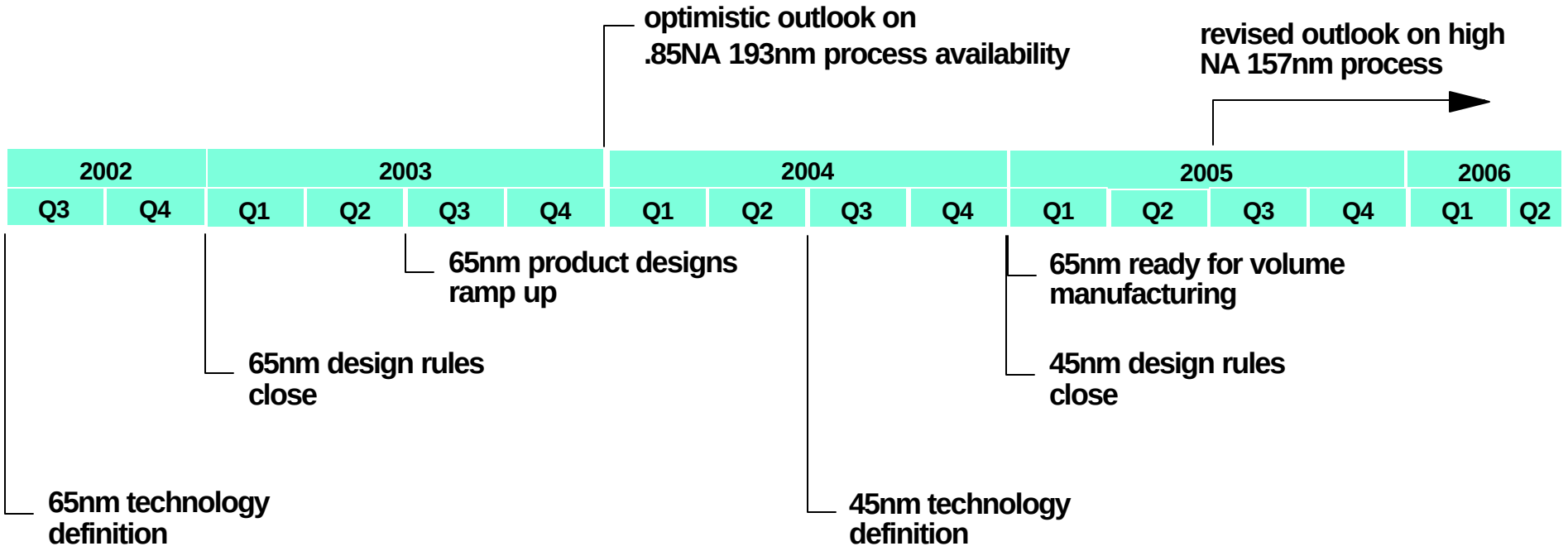
Resolution, Future

ITRS Node	Year of Man.	min. Pitch	development λ/NA	manufacture λ/NA	development k_1	manufacture k_1
180	1999	500	248 / .50	248 / .75	.50	.76
130	2001	300	248 / .75	193 / .75	.45	.58
90	2003	214	193 / .75	193 / .85	.42	.48
65	2005	160	193 / .85	(157 / .85)	.35	(.43)
45	2007	130	(157 / .85)	?	(.35)	?

Rayleigh constant for various technologies ... the future

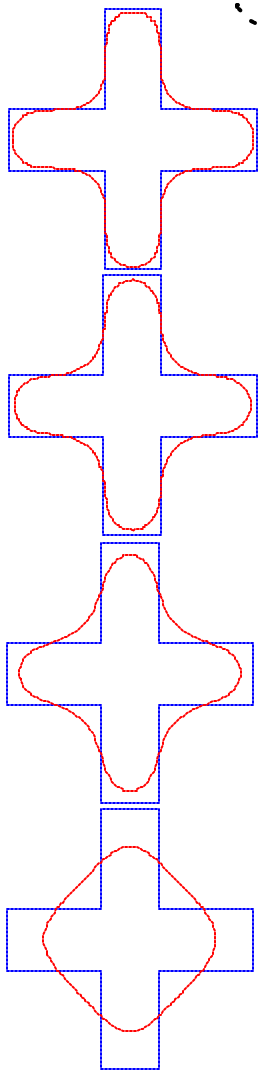


Resolution, Future

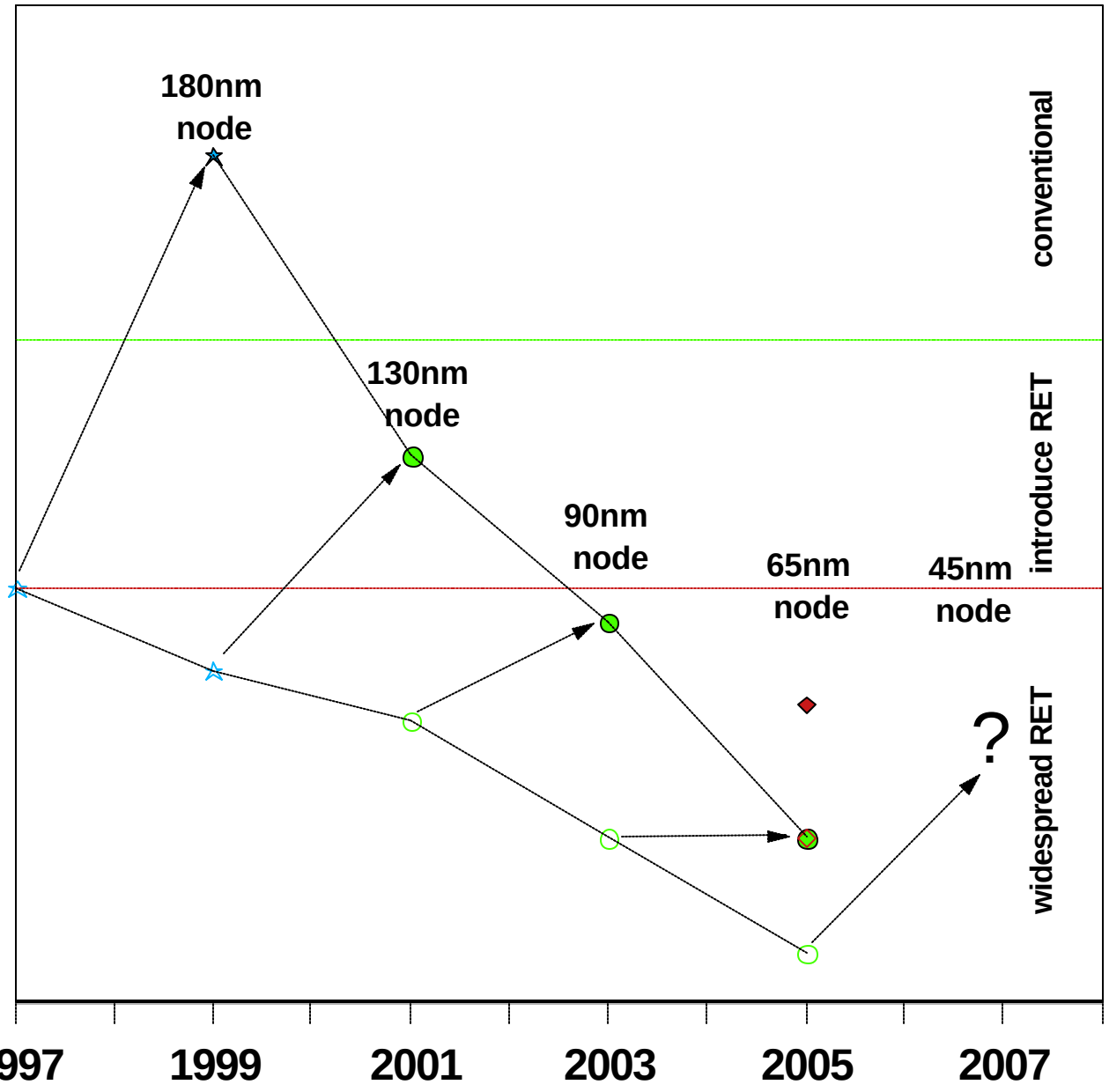


Lithography options beyond high-NA 193nm are 'limited':
157nm is late,
alternatives: 193nm immersion, extreme ultra violet ... tbd

Rayleigh constant for various technologies ... sans 157

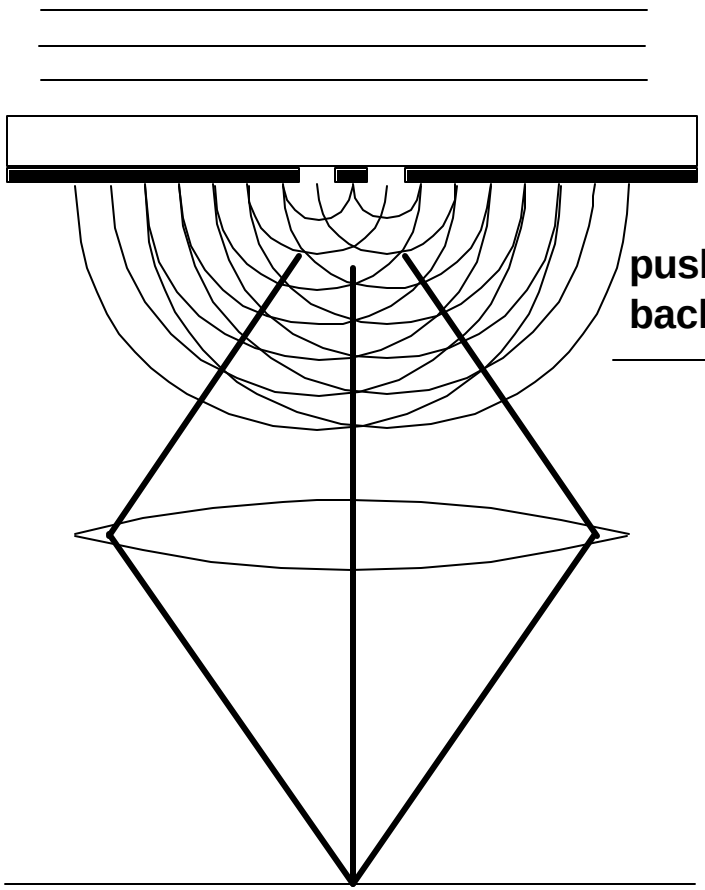


$$R = k_1 \frac{\lambda}{NA}$$

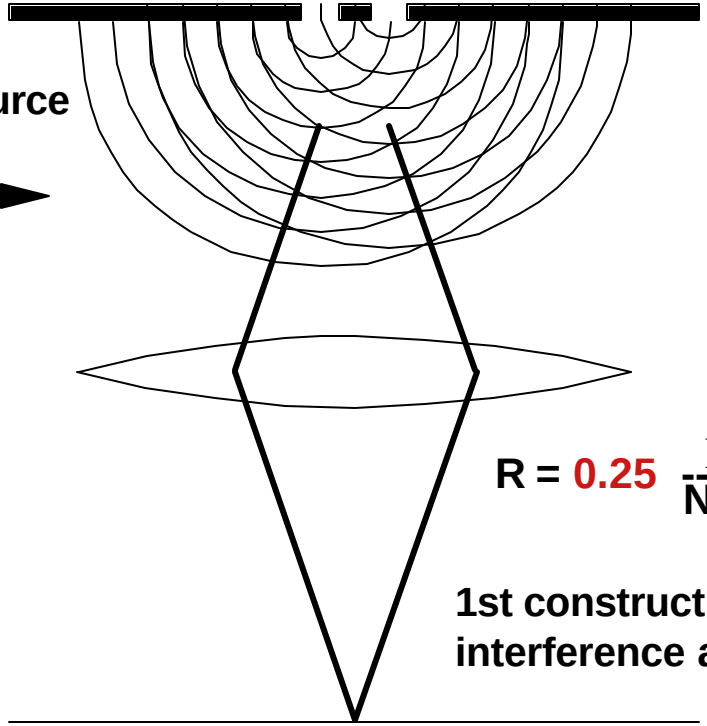


Wavelength

- 248 Dev.
- 248 Man.
- 193 Dev.
- 193 Man.
- 157 Man.
- 157 Dev.



push one point source back by .5λ



R = 0.25 $\frac{\lambda}{NA}$

1st constructive interference at 0.5λ

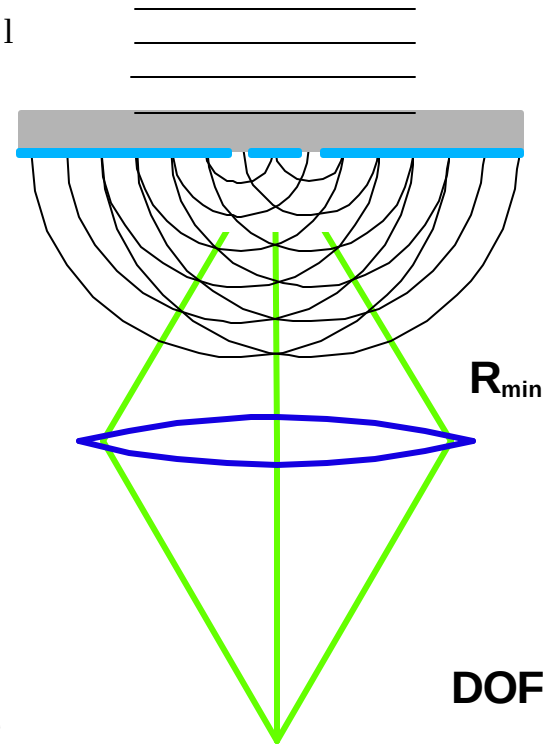
R = 0.5 $\frac{\lambda}{NA}$

DOF = $\frac{\lambda}{2\,NA^2}$

DOF = 'infinite'
... two beam imaging, no pathlength difference

Strong-RET Lithography

conventional lithography

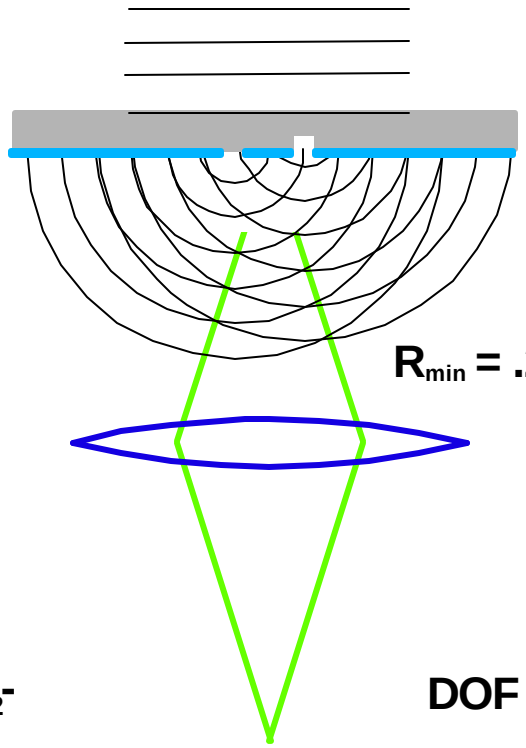


$$R_{min} = 0.5 \frac{\lambda}{NA}$$

$$DOF = \frac{\lambda}{2\,NA^2}$$

strong RET lithography

altPSM



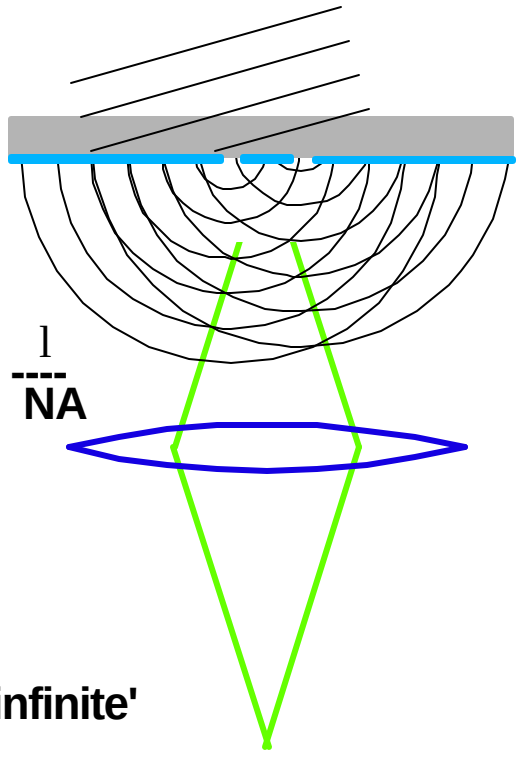
$$R_{min} = .25 \frac{\lambda}{NA}$$

$$DOF = \text{'infinite'}$$

$$Etch = \frac{0.5\,\lambda}{(n-1)}$$

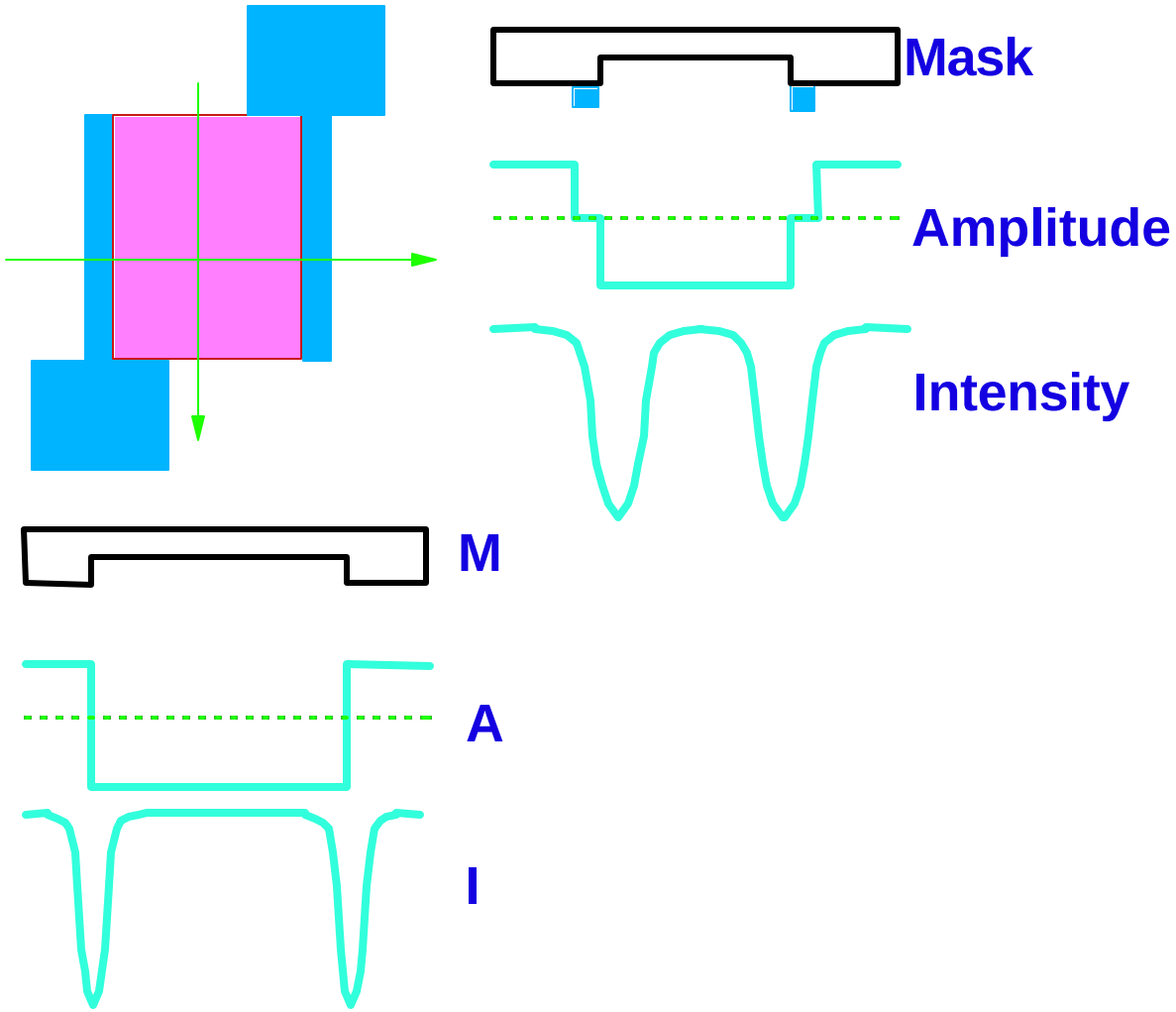
- complex mask
- double exposure

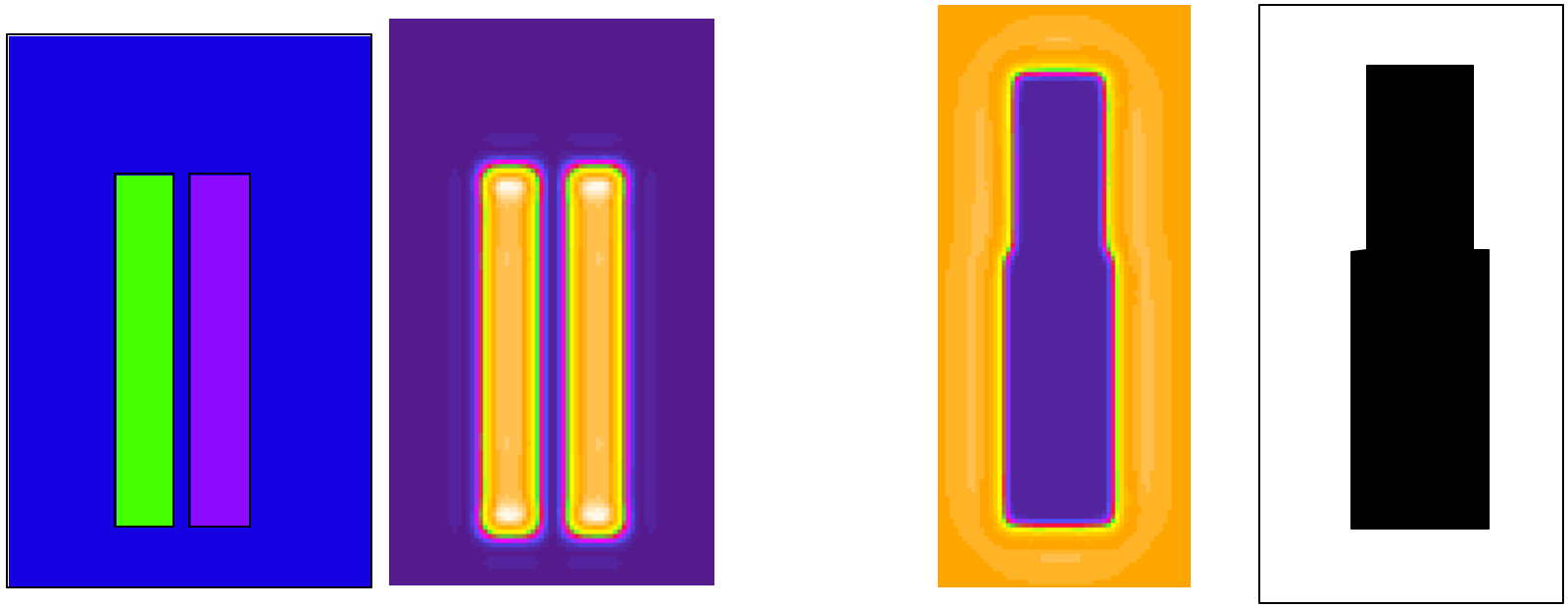
OAI



$$\sin\theta = \frac{0.5\,\lambda}{Pitch}$$

- intensity imbalance => attPSM
- pitch optimized => SRAF



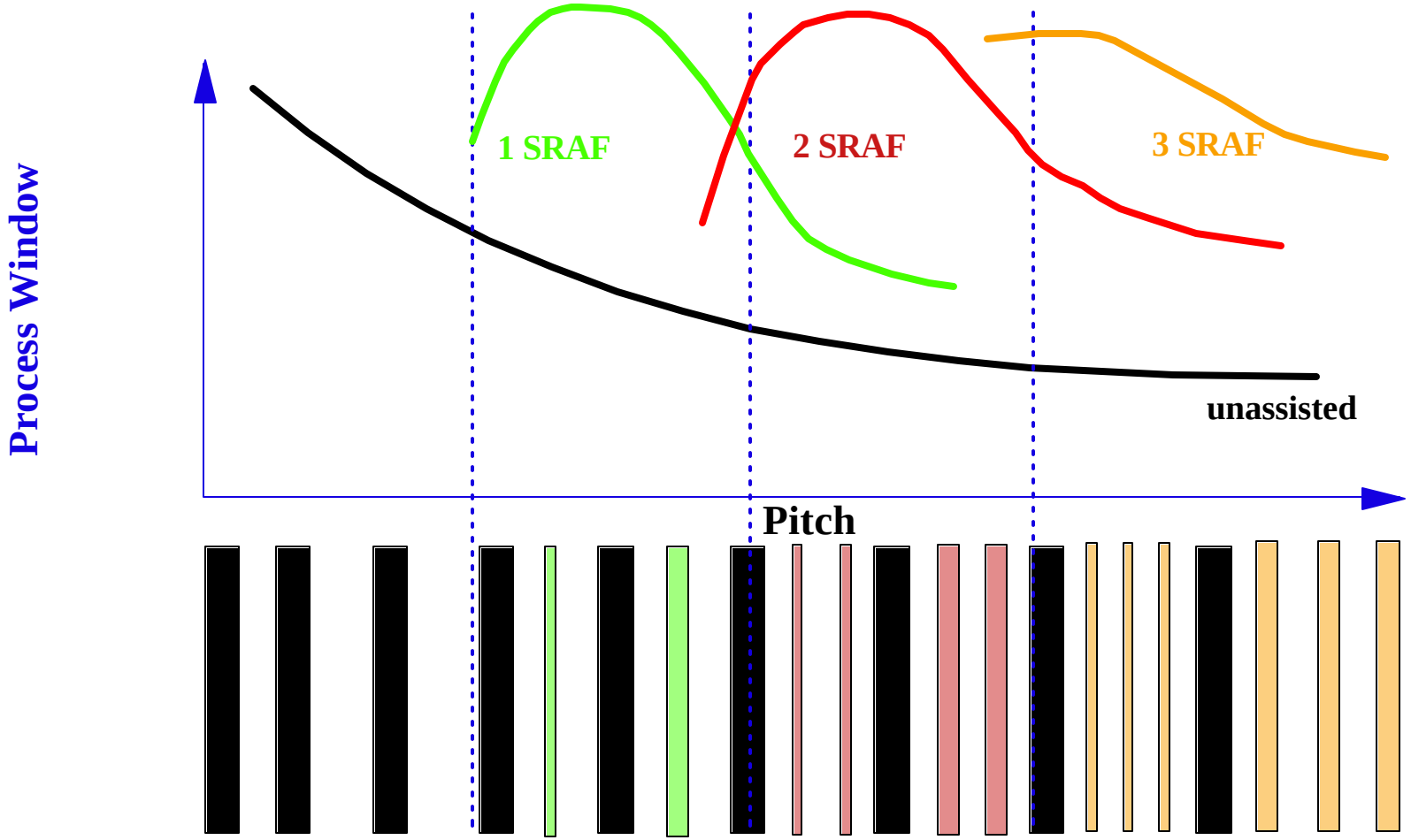


DF altPSM

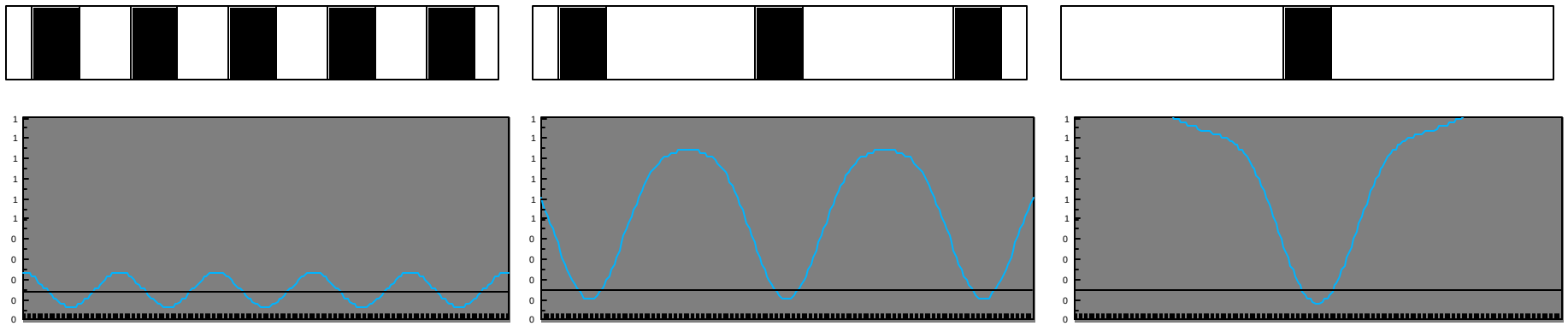
LF Binary Block

Sub-Resolution Assist Features

$$\sin\theta = \frac{0.5\,\lambda}{\text{Pitch}}$$

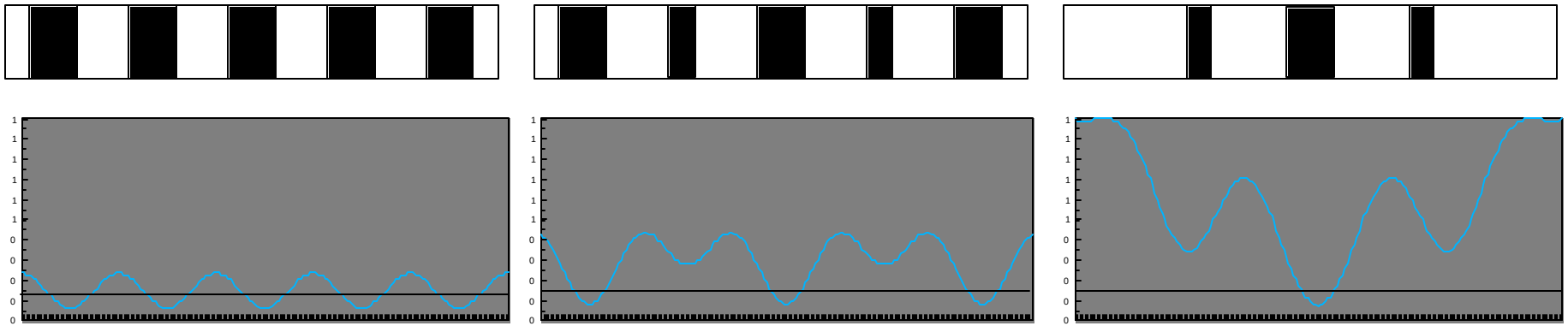


Standard



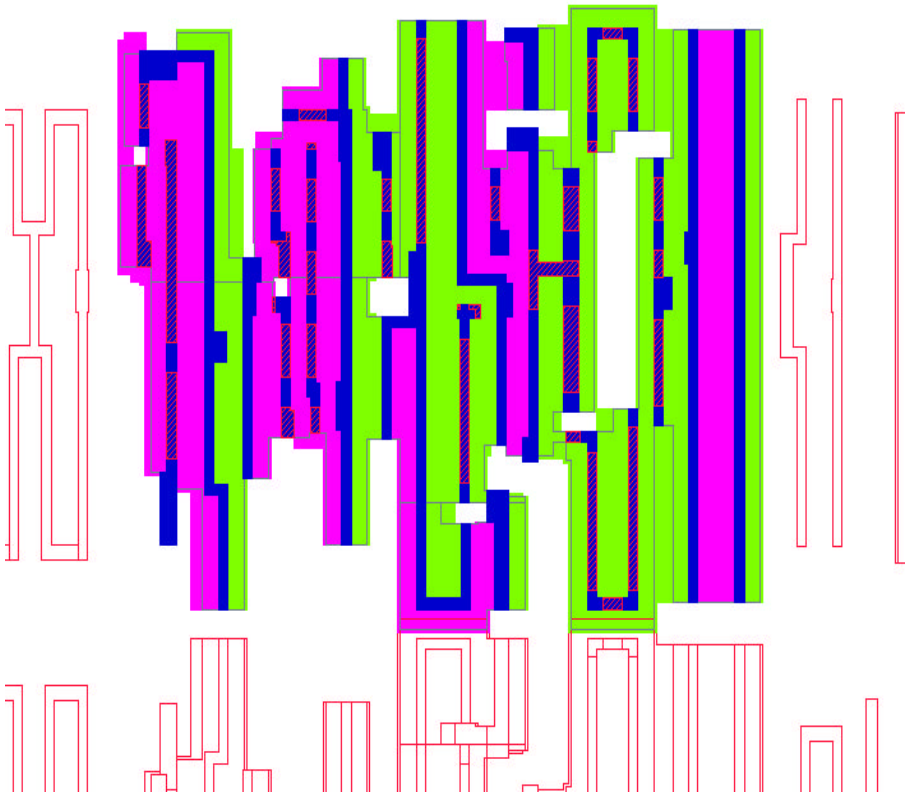
1:1 1:3 iso

with Assists

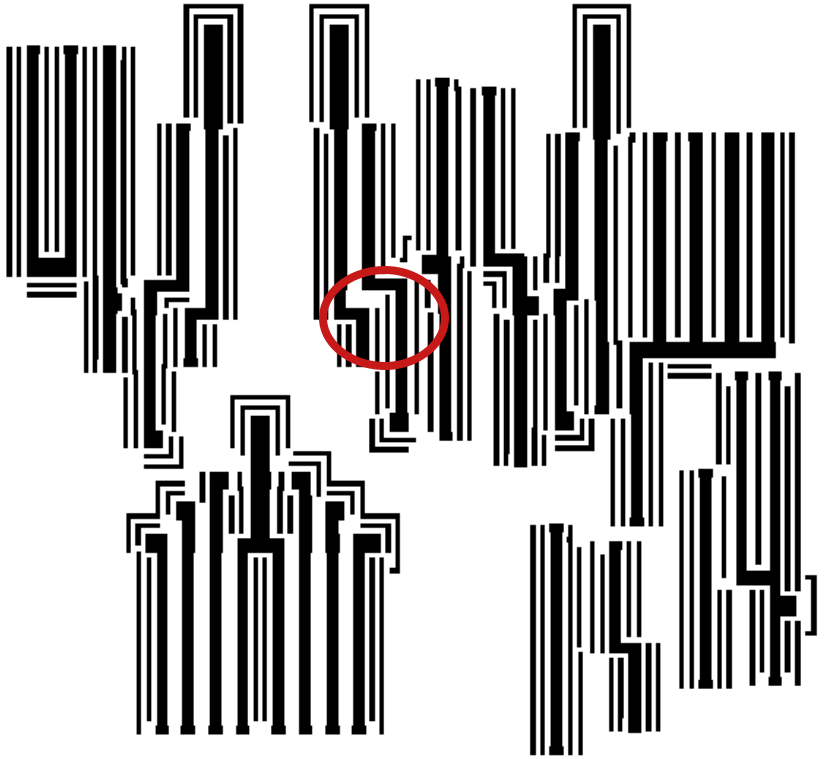


1:1 1:3 iso

altPSM Layout



sraf Layout



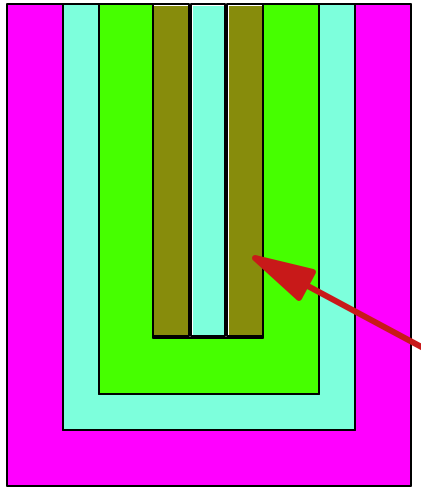
Strong-RET features can not be inserted into arbitrary layouts without RET-conflicts.

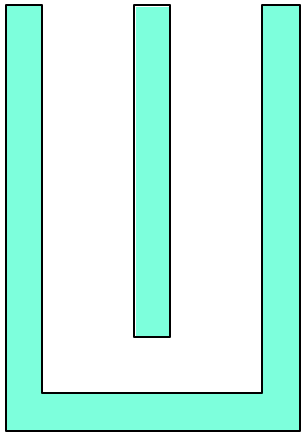
Seemingly 3 options:

1) smarter RET design tool
2) smarter RET approach
3) layout restrictions

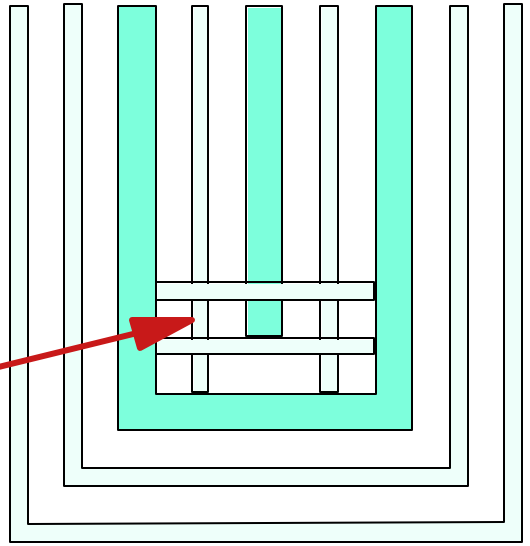
Smarter RET Solution to Avoid Conflicts

altPSM

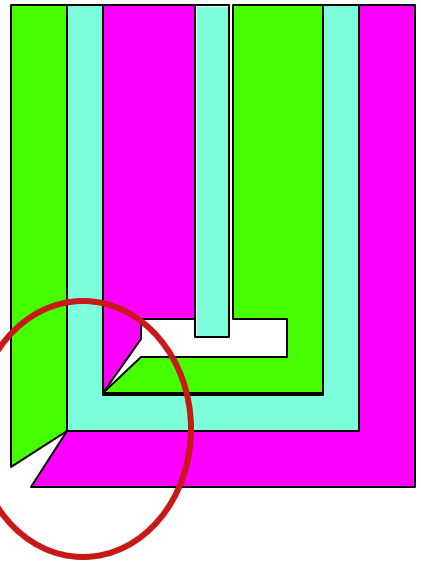




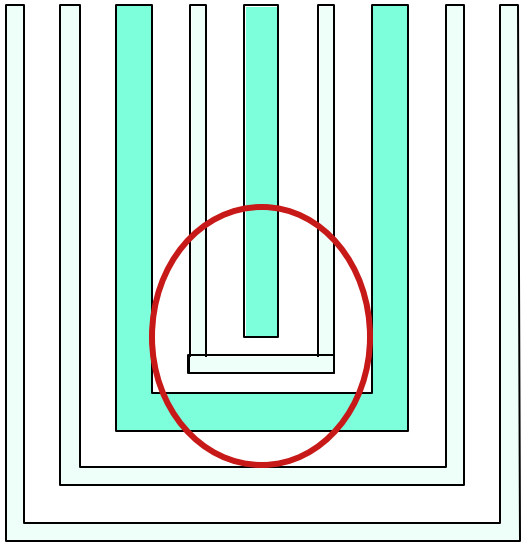
sraf



optimized RET features can not be added to arbitrary layouts



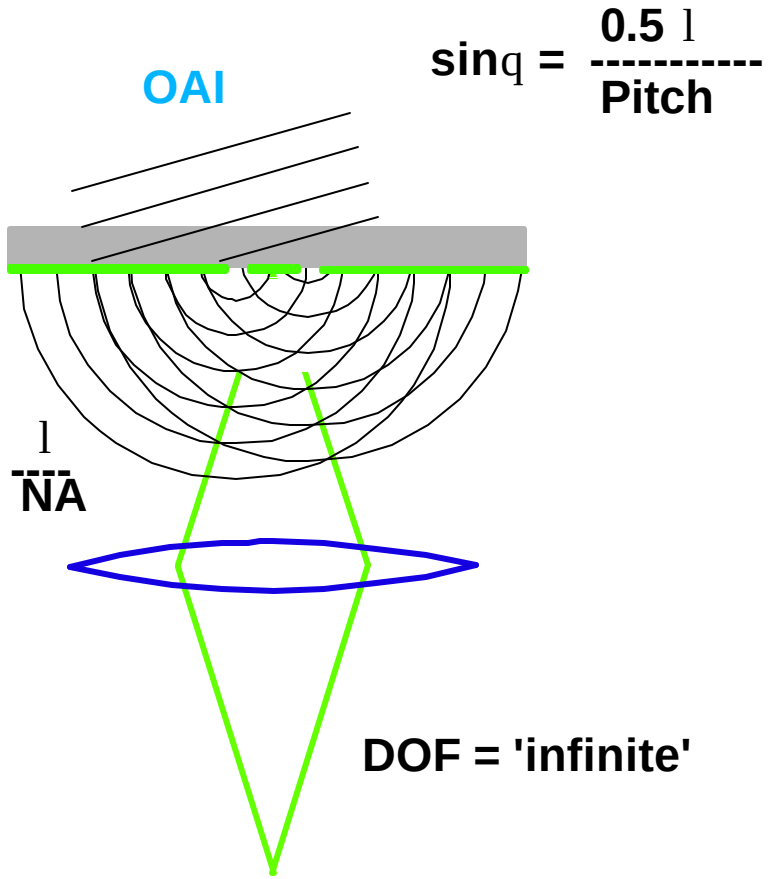
creative RET solutions that place RET features without layout restrictions trade lithographic performance for layout impact



layout restrictions are inevitable

Magic Cures to RET Layout Impact

recent champions in RET:
Double Dipole Lithography (DDL)
Chromeless Phase Lithography (CPL)



For both DDL and CPL, the resolution enhancement comes from OAI:

- **suffer intensity imbalance => attPSM**
  ..... at the extreme: 100% transmission == CPL
- **need optimized illumination => coherent OAI**
  ..... at the extreme: diPole == DDL
- **pitch optimized => SRAF remain!**

Net:
manufacturability issues change, layout concerns remain

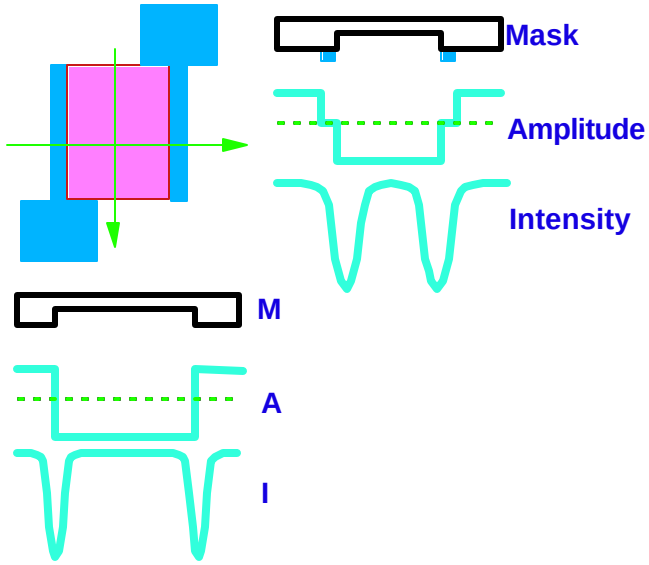
layout restrictions are inevitable

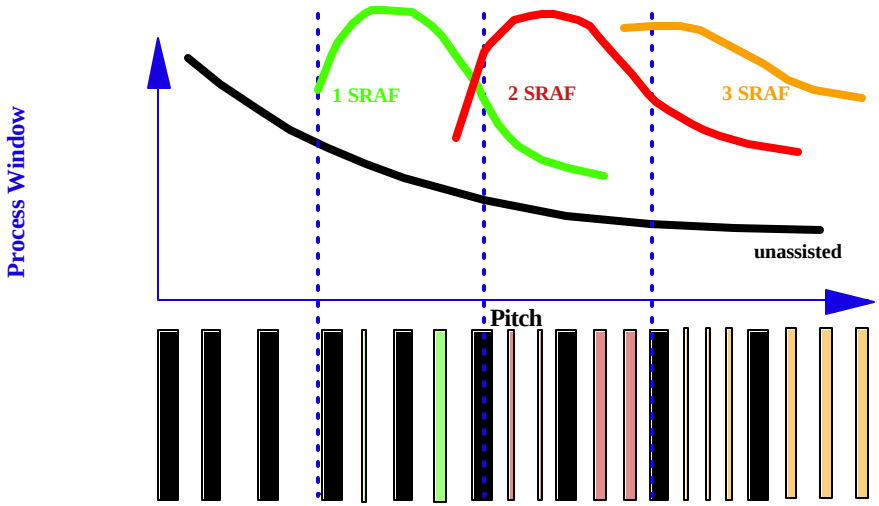
Strong-RET Summary

Strong-RET will allow us to push lithographic resolution closer to the k_1=0.25 limit to fill the gap between chip integration needs and exposure tool availability.

But:

- **strong RET require layout restrictions**
- **in most cases, these layout restrictions can not be enforced through 'conventional' design rules and DRC**

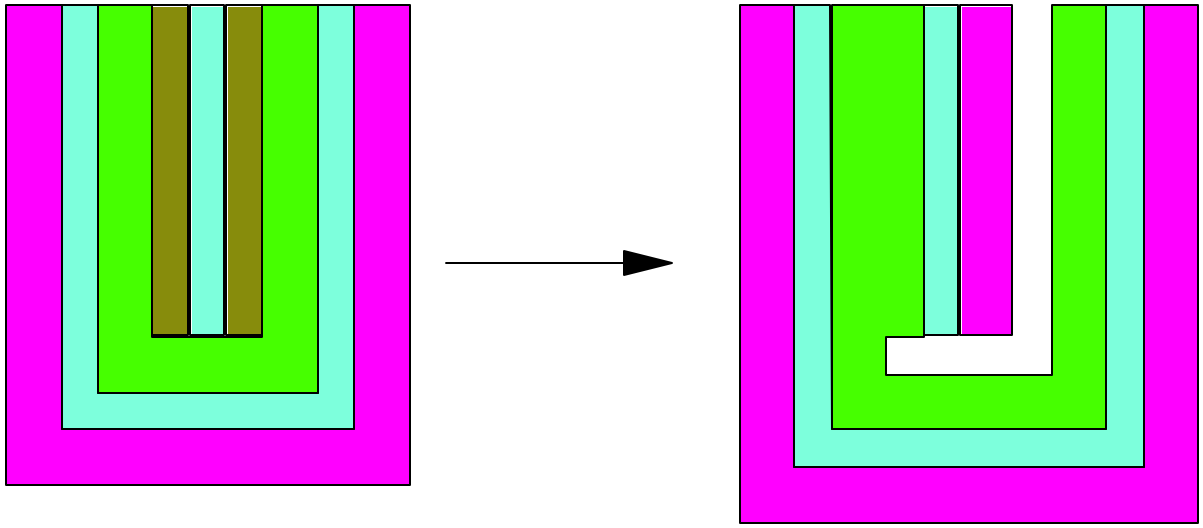




altPSM example:

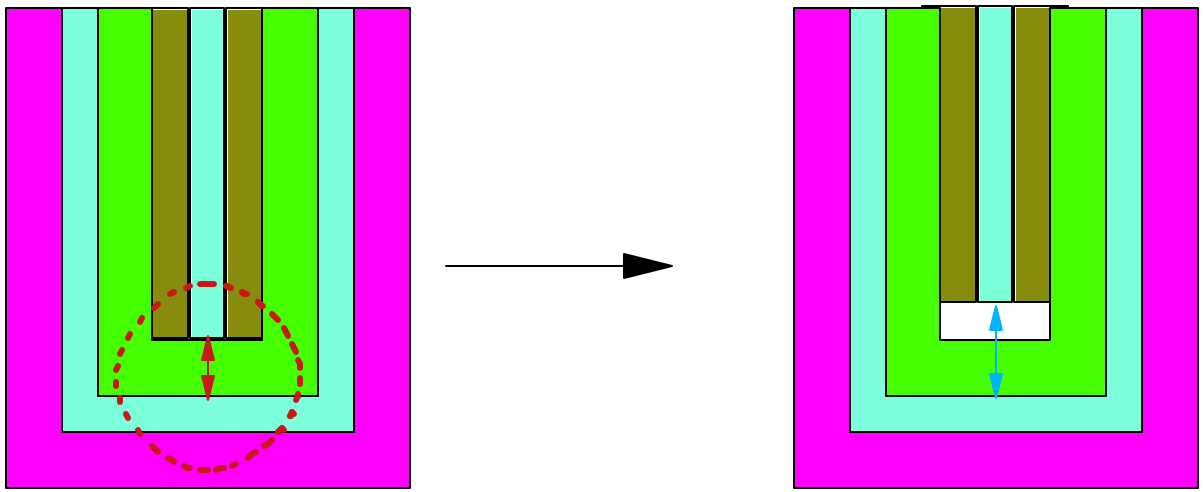
accurate design rules are very complicated:

....critical (i.e. needs RET) line-end surrounded by critical lines with lateral spacing of <(2*Phase-Width + Phase-Space) on both lateral sides and <(Phase-Width + Phase Space) at end...



....and very RET-parameter (i.e. process/fab) specific

simple (i.e. understandable) design rules are inadequate (misleading):
....critical-line-end to perpendicular citical-line space violation...

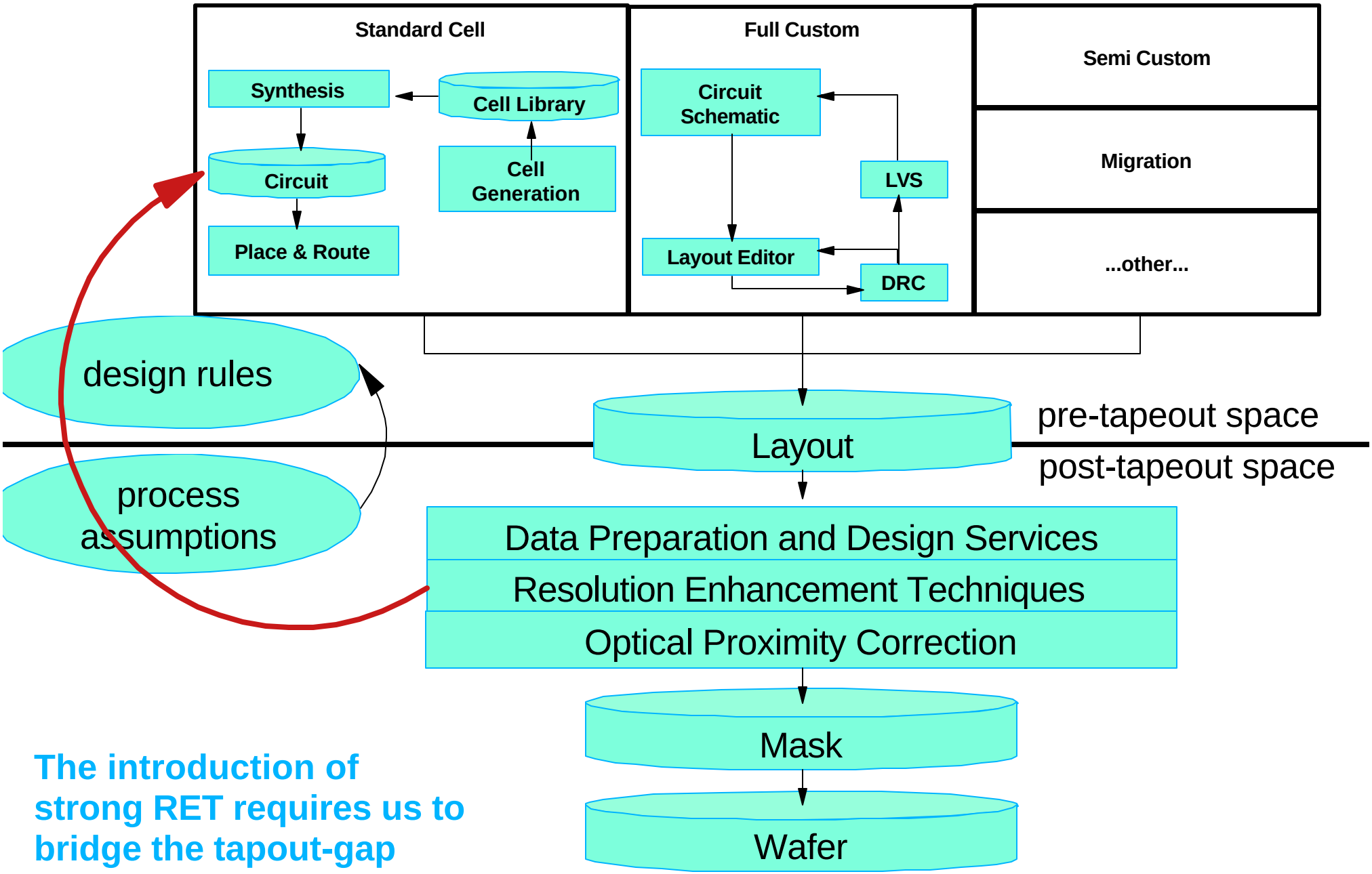


layout restrictions are inevitable
...and can not be enforced with conventional DRC

Summary So Far, Further Outline

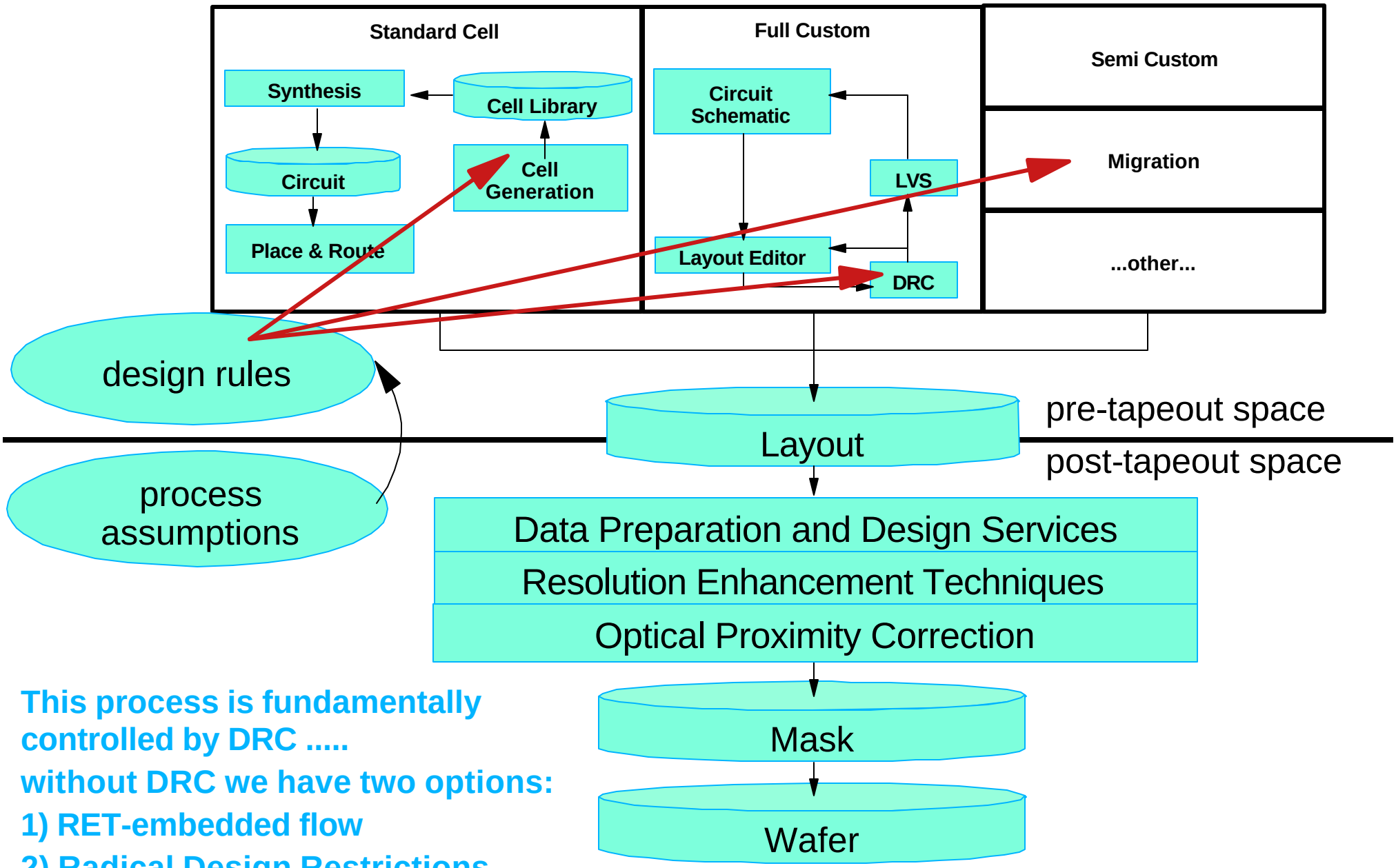
- **Problem: lithography is approaching a serious wall**
  - Passed the 'fundamental resolution limit' of k1 = 0.5
  - Mild-RET (post-tapeout and transparent to designers) insufficient for 65nm+
  - No lithography tooling solutions available on time!
- **Proposed Solution: strong-RET**
  - Issue 1: requires layout restrictions
  - Issue 2: conventional DRC not effective to cover these restrictions
- **Options to address issues**
  - Option 1: RET-embedded design flow
    - More complicated than conventional flow
      - RET-embedded cell design
      - RET-embedded placement and routing
    - RET-parameter specific
  - Option 2: radically-restricted rules
    - High impact on designers' actions (paradigm shift)
    - Significant Benefits
      - Simplified Methodology
      - RET-generic Layout Optimization
      - Improved Manufacturability in 2-beam Imaging Regime

RET: Impact and Opportunity



The introduction of strong RET requires us to bridge the tapout-gap

DRC dependence



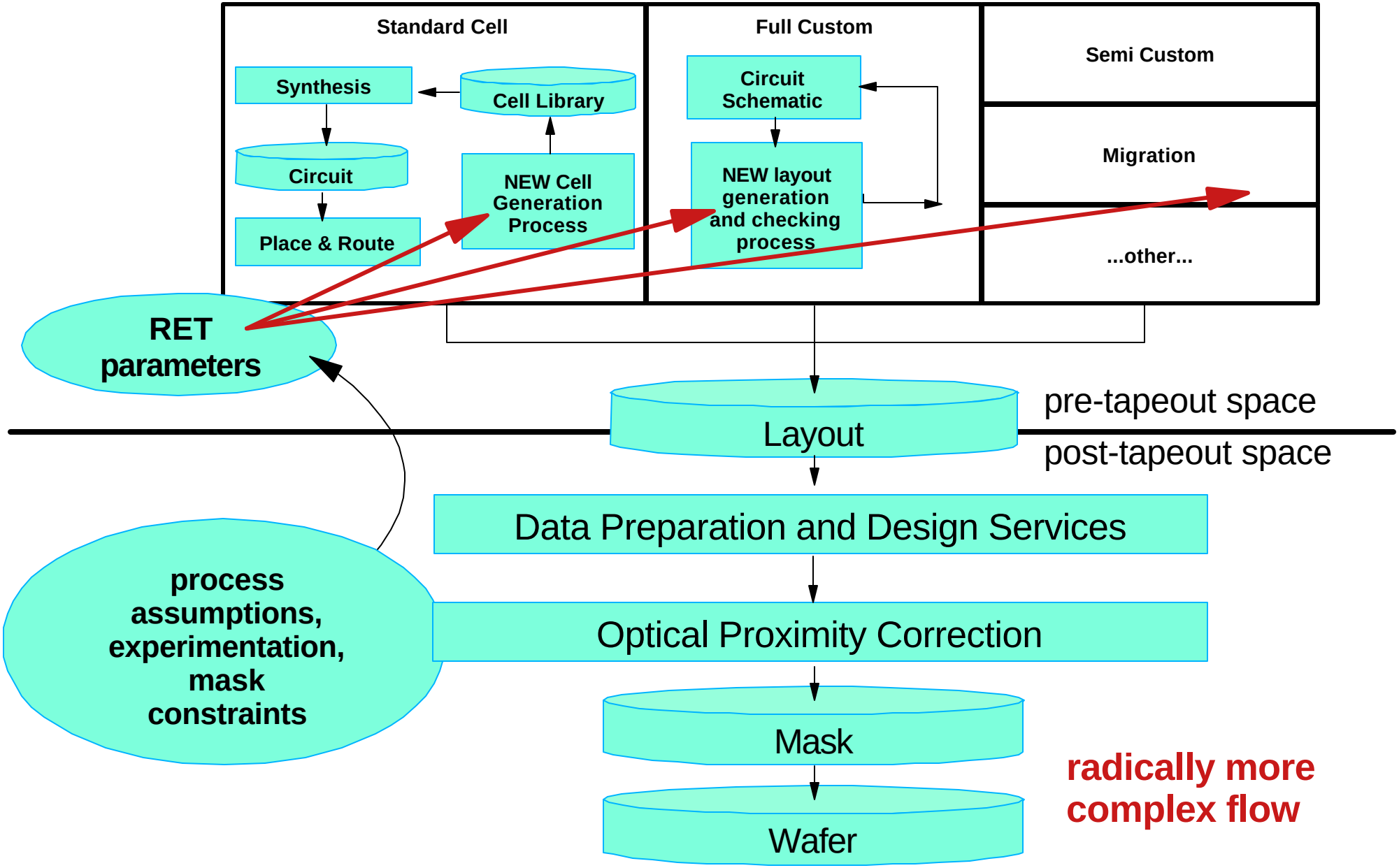
This process is fundamentally controlled by DRC .....

without DRC we have two options:

1) RET-embedded flow

2) Radical Design Restrictions

Option 1: RET-embedded design flow



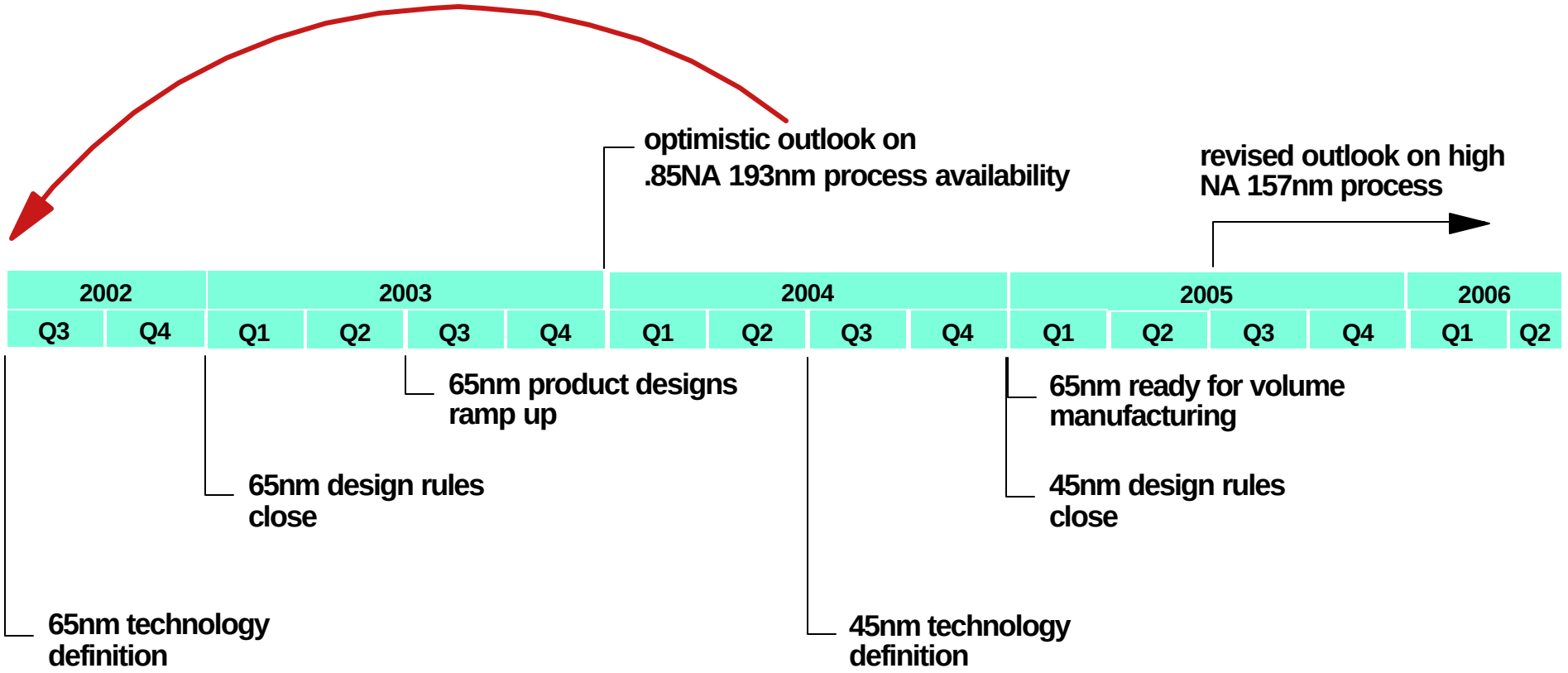
RET-embedded design flow challenges

Methodology Challenges

- 'abstract', non specific feedback on layout violations
- boundary conditions
- constrained placement and routing

Fundamental Parameter Challenges

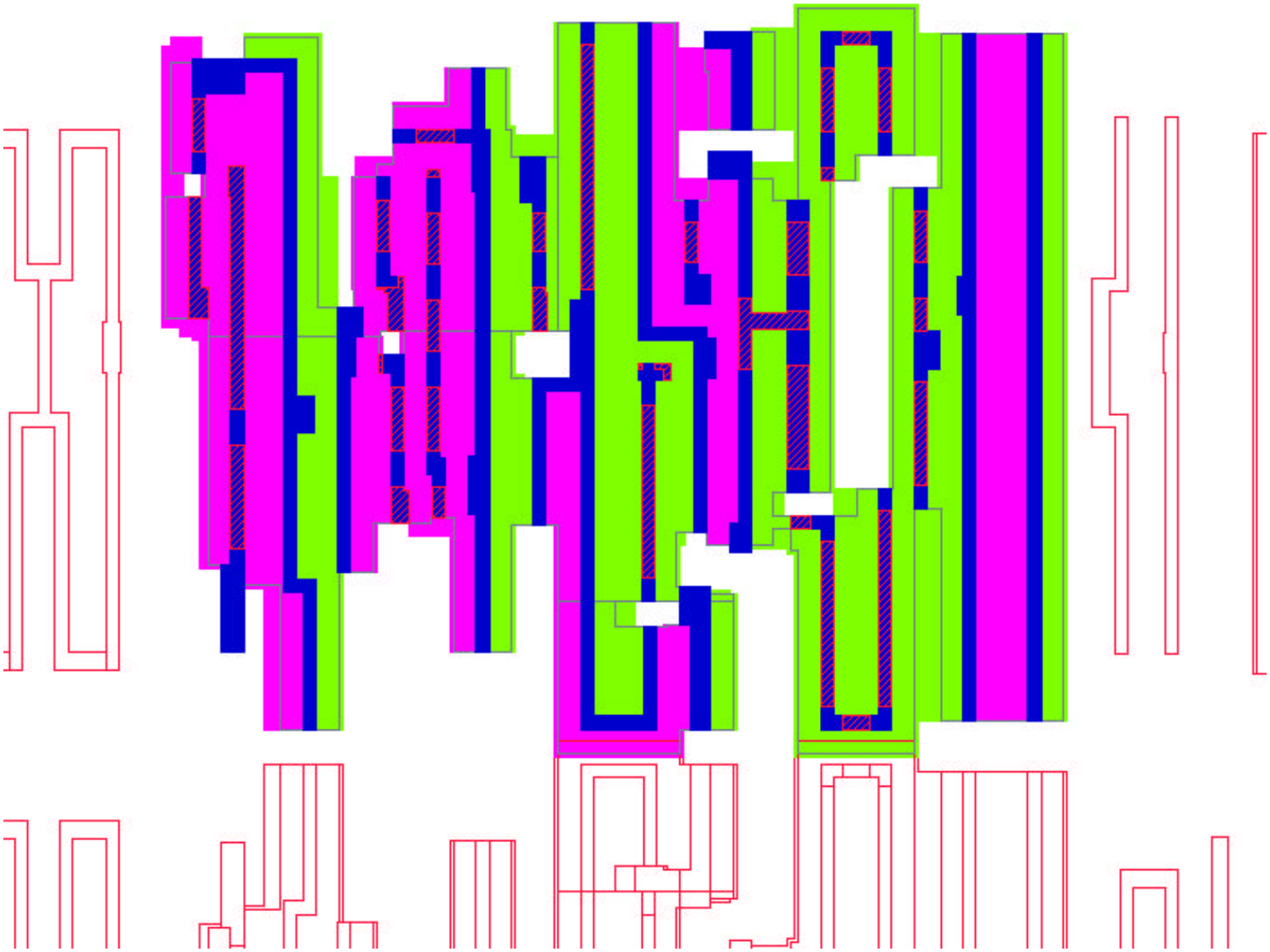
Parameter Challenges: Feed Process Assumptions Back in Time



RET-parameters are embedded in the design flow long before they are physically stable.

Parameter Challenges: Sample altPSM Layout

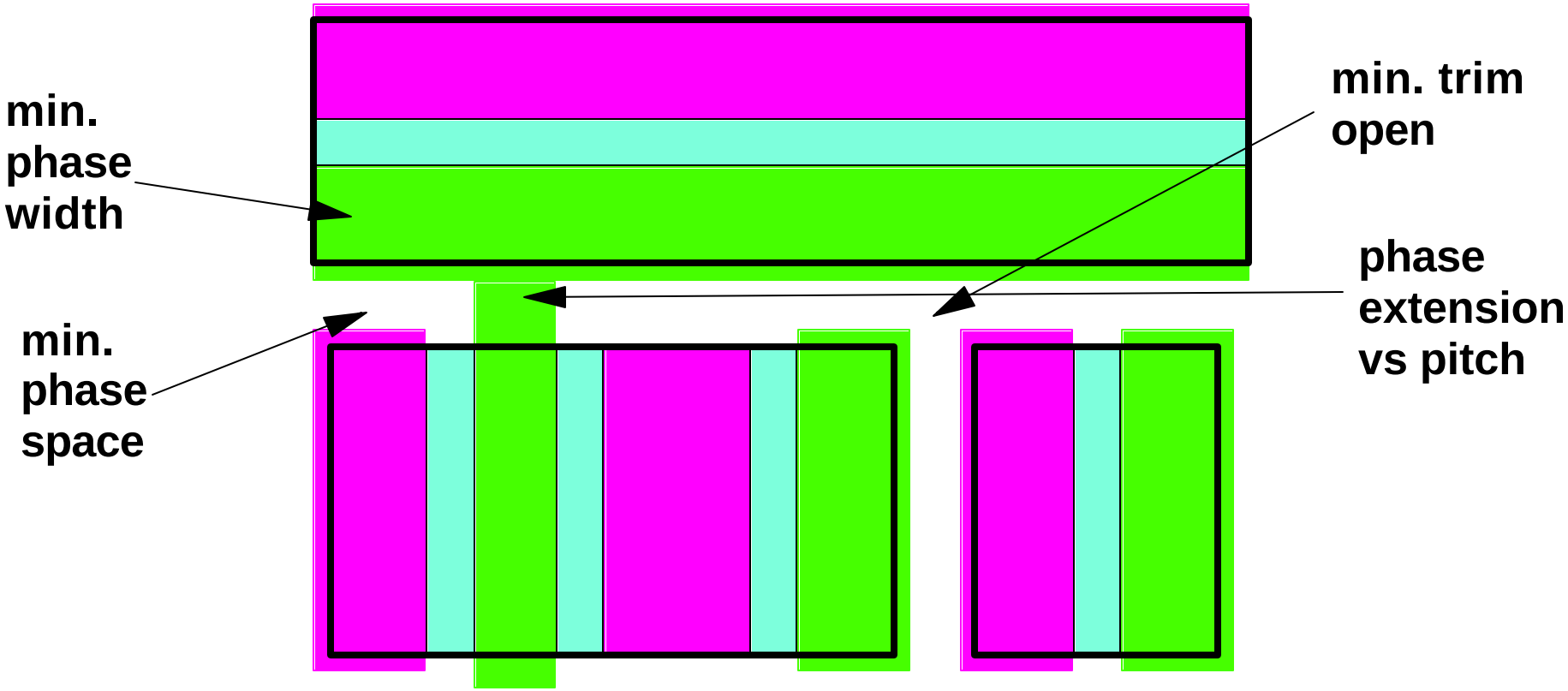
Detailed optimization of phase parameters leads to layout conflicts:



....tweak phase parameters to avoid as many conflicts as possible.

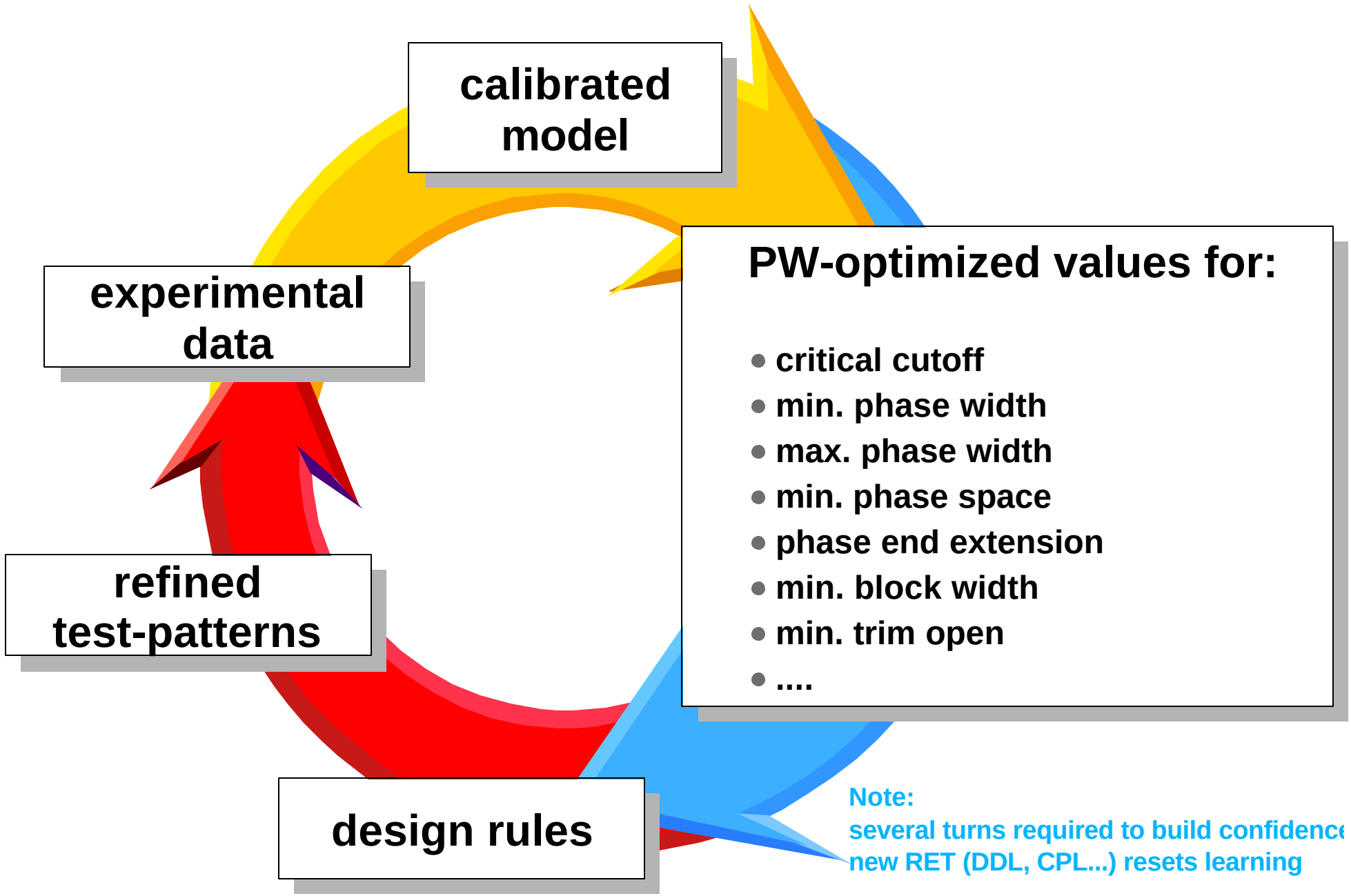
Parameter Challenges: Phase Parameters to Design Rules

Design Rule: minimum space between a critical line-end and a projecting critical line

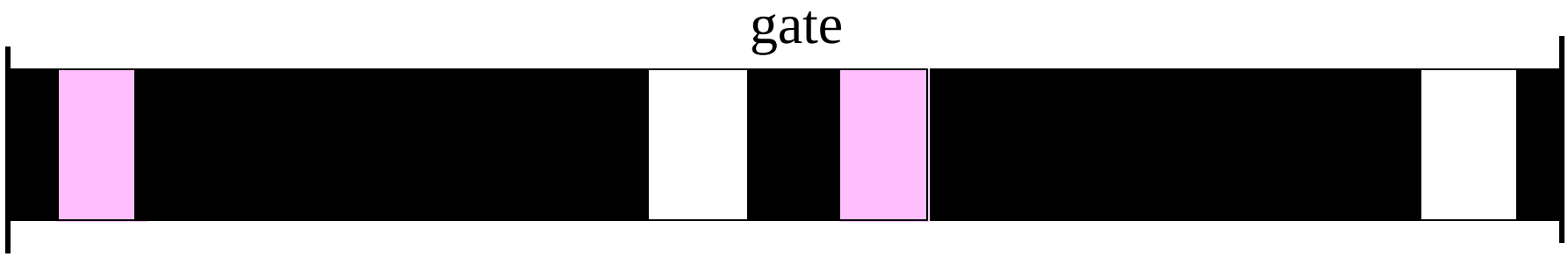


... becomes a function of many phase parameters

Parameter Challenges: Generation of Phase Parameters



Parameter Challenges: PW as a Function of Phase Parameters



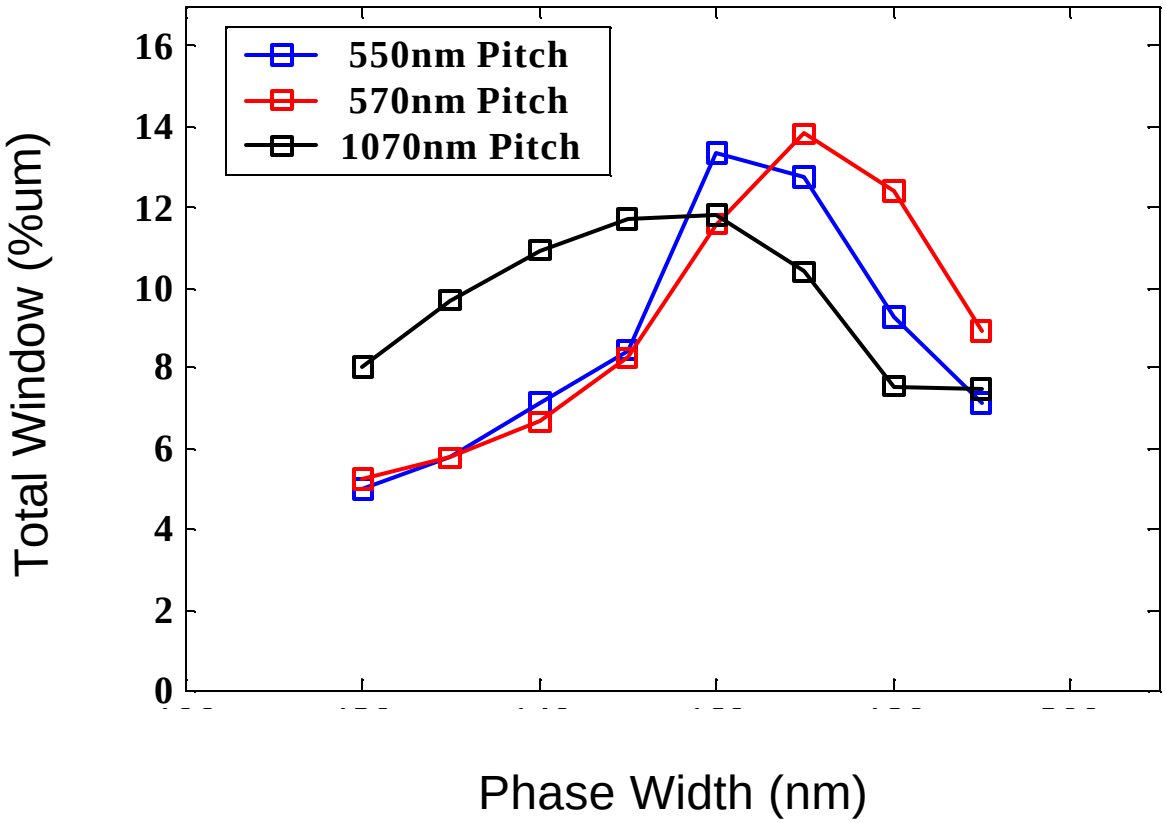
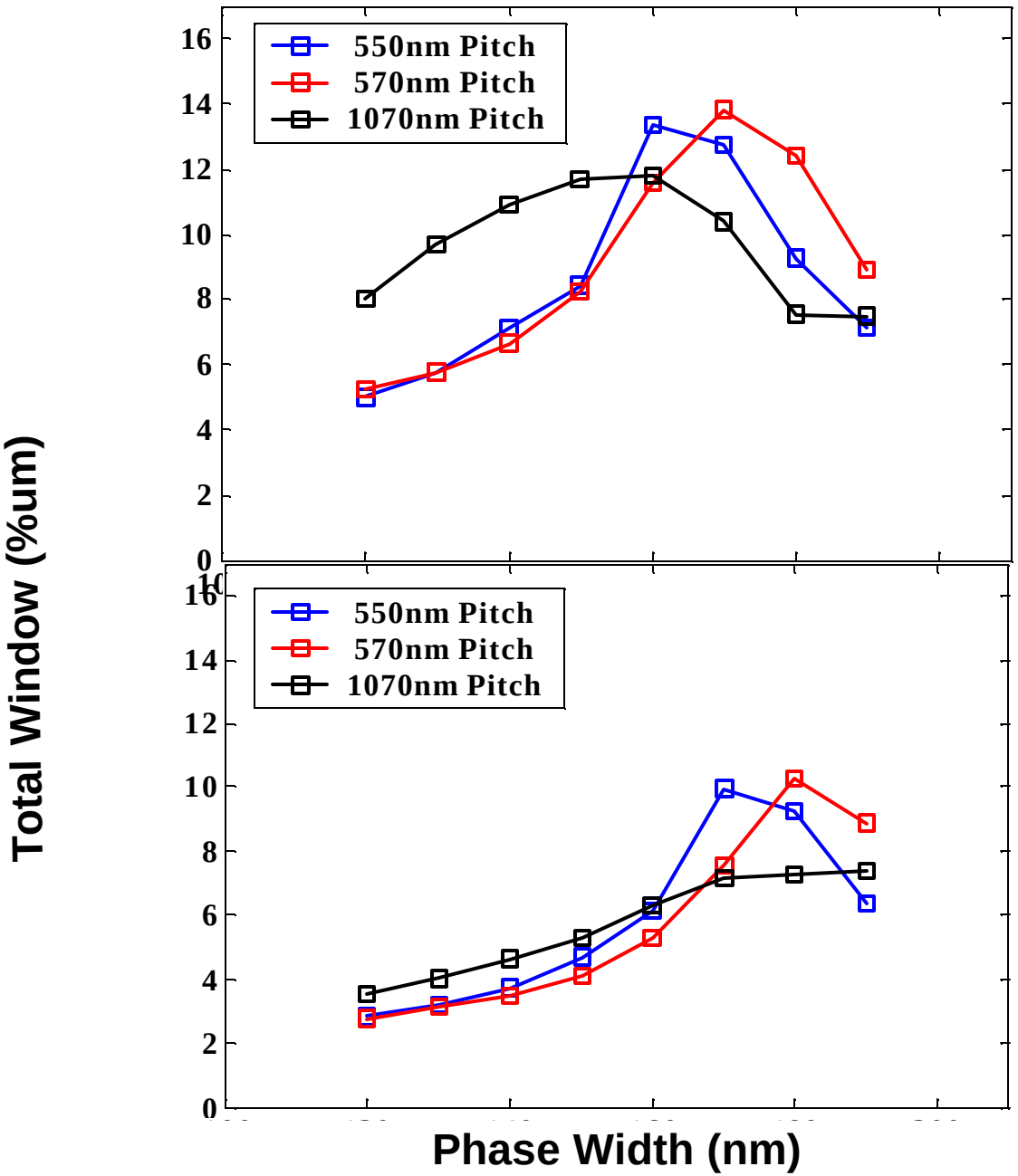


Fig. 10

Parameter Challenges: PSM Parameters vs Process Assumptions

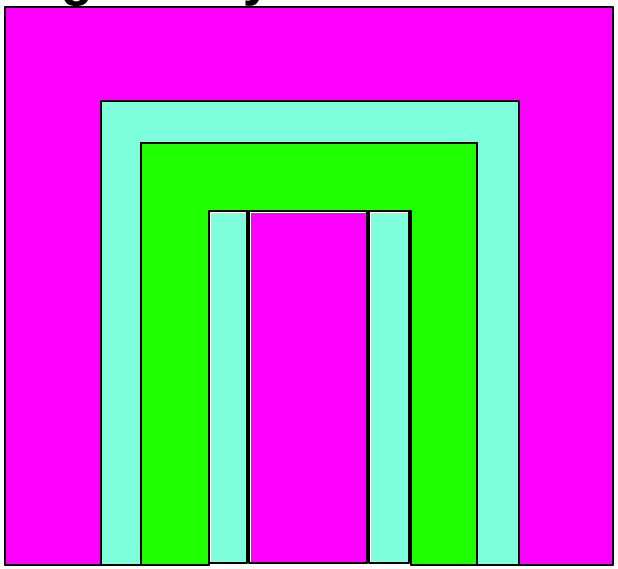


Aerial image simulation

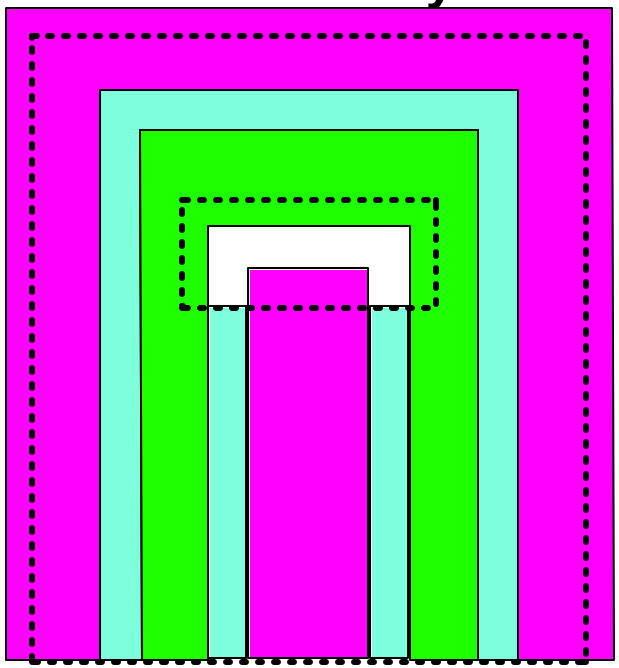
Simulation using calibrated lumped parameter resist model

Parameter Challenges: Impact of Detailed Layout Optimization

original layout with conflict



constrained layout

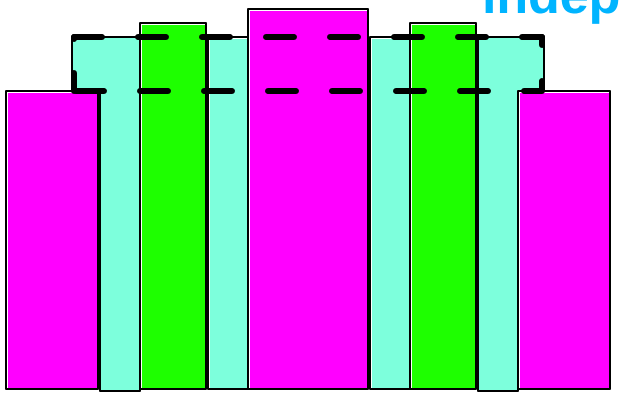


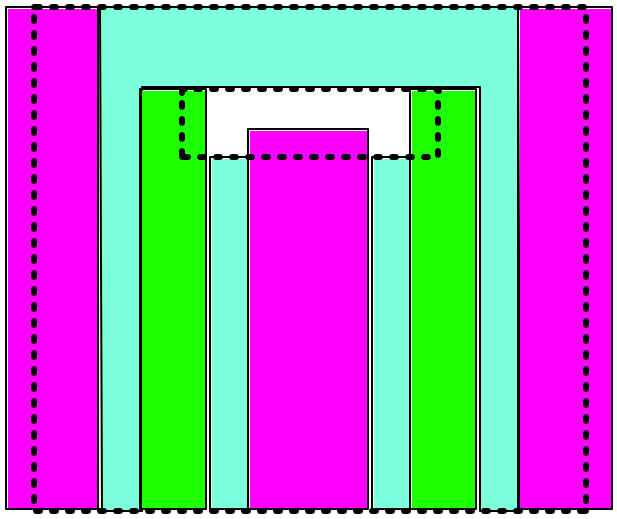
range of space impact =

aggressive: 1.7x

conservative: 3x

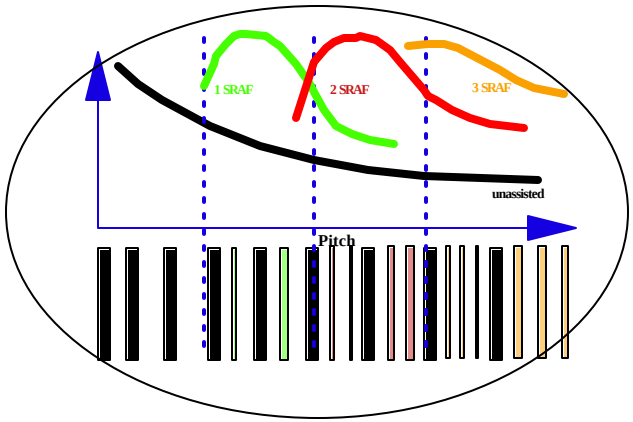
radically restricted layout:
critical in one orientation
independent of phase parameters





Parameter Challenges: Forbidden Pitch for SRAF?

Layout restrictions are not unique to altPSM, poor SRAF placement results in loss of manufacturability or process-window



most prominent layout restriction: "Forbidden Pitch"

Problem #1: "Pitch" is hard to define in many layouts

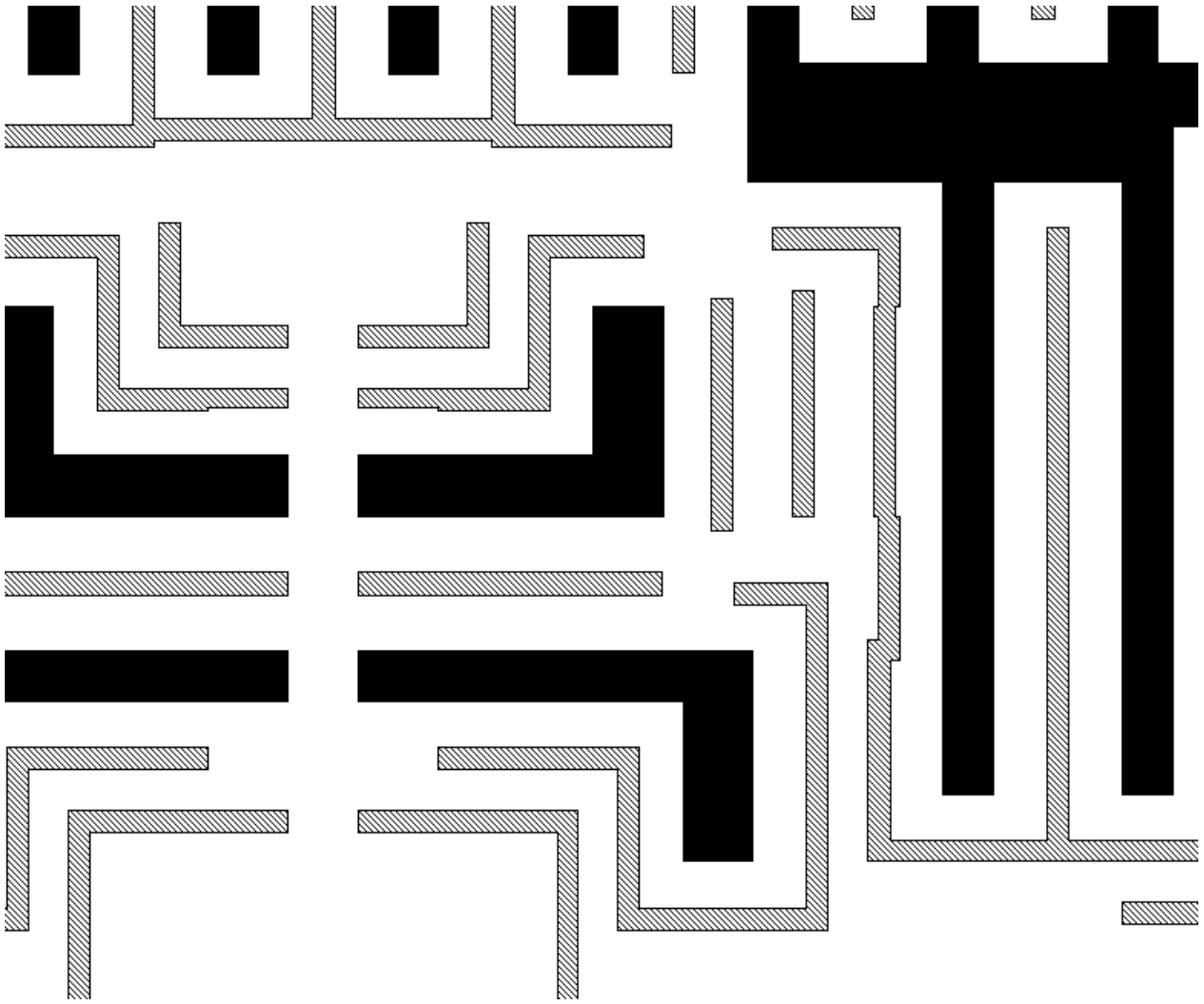
Parameter Challenges: Forbidden Pitch is not Absolute

Wavelength	193nm	193nm	193nm	193nm
NA	0.85	0.85	0.75	0.75
Illum. Angle (Mean Sigma)	0.95	0.95	0.8	0.8
Min. SRAF Size	40nm	50nm	40nm	50nm
Min. SRAF Space	70nm	100nm	70nm	100nm
160	FORBIDDEN	FORBIDDEN	OPTIMUM	OPTIMUM
170	FORBIDDEN	FORBIDDEN	OPTIMUM	OPTIMUM
180	FORBIDDEN	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
190	FORBIDDEN	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
200	FORBIDDEN	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
210	FORBIDDEN	FORBIDDEN	FORBIDDEN	FORBIDDEN
220	FORBIDDEN	FORBIDDEN	FORBIDDEN	FORBIDDEN
230	FORBIDDEN	FORBIDDEN	FORBIDDEN	FORBIDDEN
240	FORBIDDEN	FORBIDDEN	FORBIDDEN	FORBIDDEN
250	OPTIMUM	FORBIDDEN	FORBIDDEN	FORBIDDEN
260	OPTIMUM	FORBIDDEN	FORBIDDEN	FORBIDDEN
270	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
280	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
290	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
300	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
310	FORBIDDEN	FORBIDDEN	OPTIMUM	FORBIDDEN
320	FORBIDDEN	FORBIDDEN	OPTIMUM	OPTIMUM
330	FORBIDDEN	FORBIDDEN	OPTIMUM	OPTIMUM
340	FORBIDDEN	FORBIDDEN	OPTIMUM	OPTIMUM
350	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
360	OPTIMUM	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
370	OPTIMUM	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
380	OPTIMUM	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
390	OPTIMUM	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
400	ACCEPTABLE	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
410	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
420	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
430	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
440	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
450	ACCEPTABLE	FORBIDDEN	FORBIDDEN	FORBIDDEN
460	OPTIMUM	FORBIDDEN	OPTIMUM	FORBIDDEN
470	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
480	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
490	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
500	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
510	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
520	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
530	OPTIMUM	FORBIDDEN	OPTIMUM	OPTIMUM
540	ACCEPTABLE	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
550	ACCEPTABLE	FORBIDDEN	ACCEPTABLE	ACCEPTABLE
560	ACCEPTABLE	FORBIDDEN	ACCEPTABLE	ACCEPTABLE

160nm > Pitch > 560nm

Parameter Challenges: 2-d SRAF Constraints

Due to 'limited' understanding of SRAF in 2-d and multiple possible SRAF solutions ... 2-d layout optimization is very complicated



Note:

radically restricting layout to 'critical in one orientation' eliminates the problem

RET-embedded design flow challenges

Methodology Challenges

- 'abstract', non specific feedback on layout violations
- boundary conditions
- constrained placement and routing

Fundamental Parameter Challenges

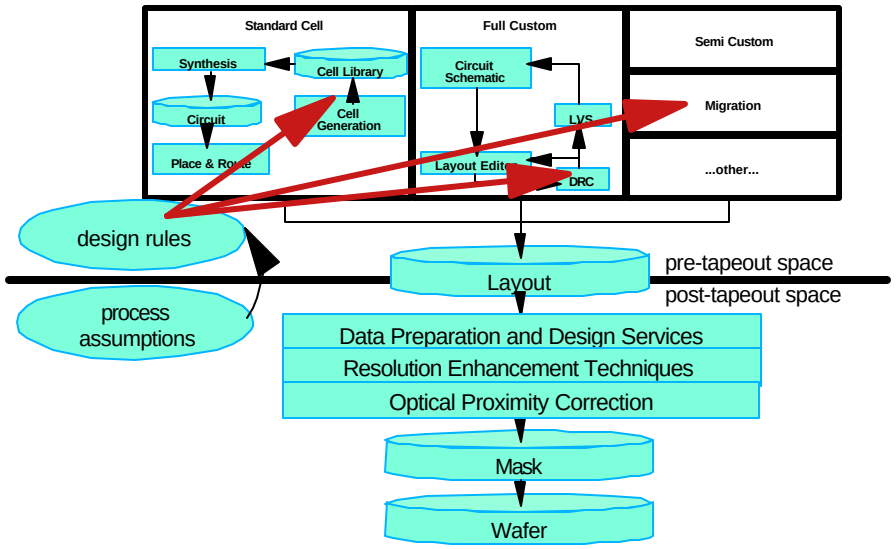
- RET-parameters are very process specific
- layouts need to be legalized long before processes are stable

This process is fundamentally controlled by DRC .....

without DRC we have two options:

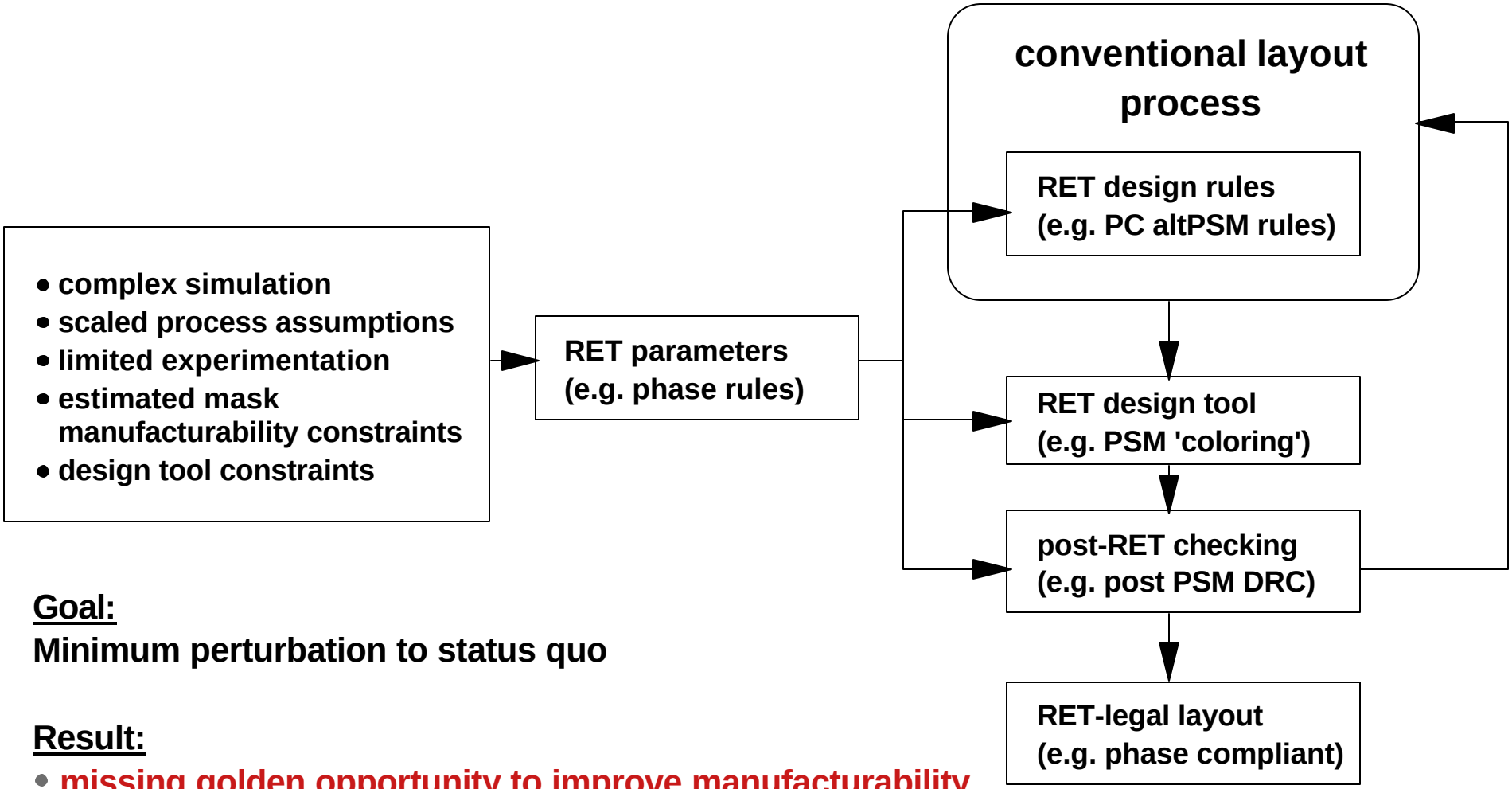
1) RET-embedded flow

2) Radical Design Restrictions



current 65nm design flow

A set of rules which completely guarantees phase-shiftability is too restrictive. Hence, even if a design passes DRC check of these rules, it must still run through the phase generation routine to verify that this routine completes without error.



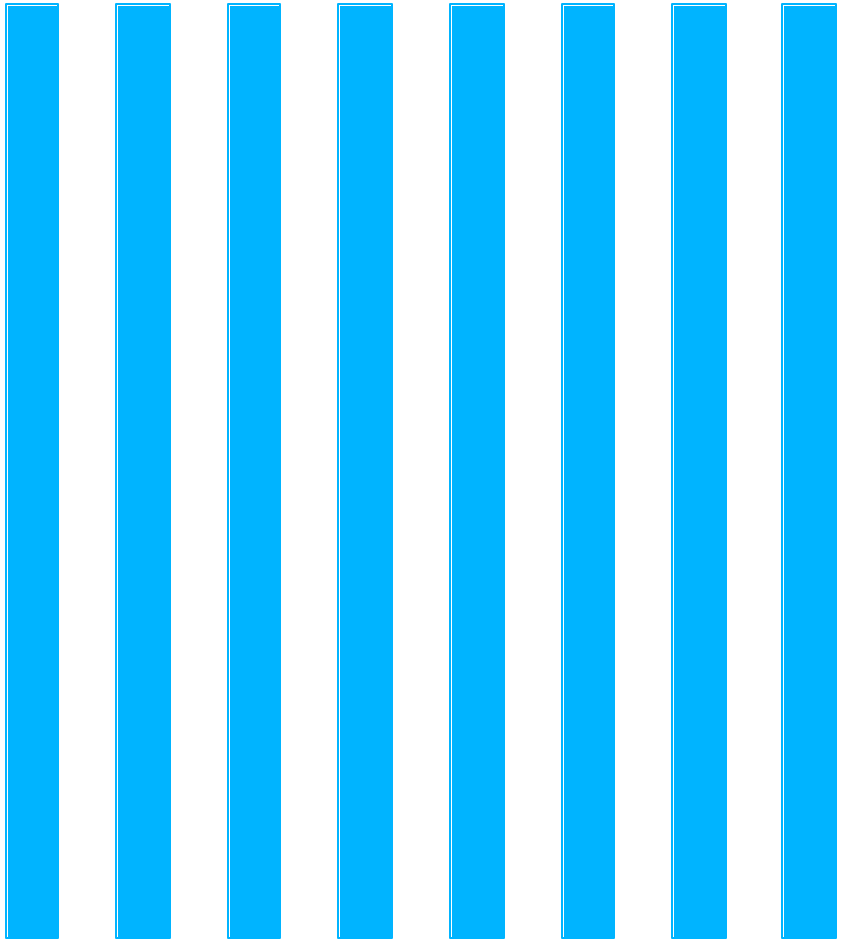
Goal:

Minimum perturbation to status quo

Result:

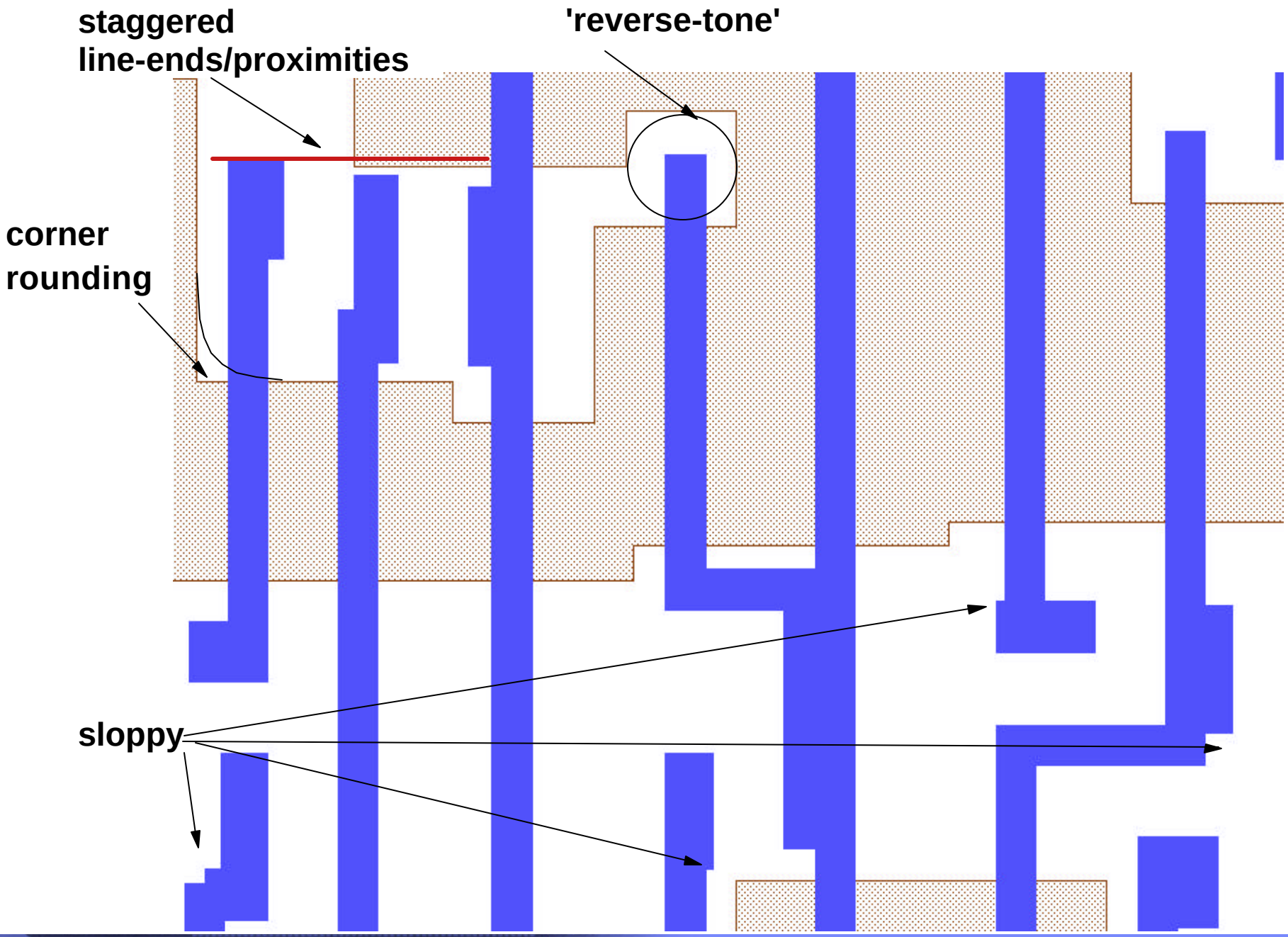
- **missing golden opportunity to improve manufacturability**
- **locking into one specific embodiment of a high risk RET**
- **know nothing about migration**

what litho can handle:



know how to simulate,
know how to optimize,
know how to print

what designers produce:

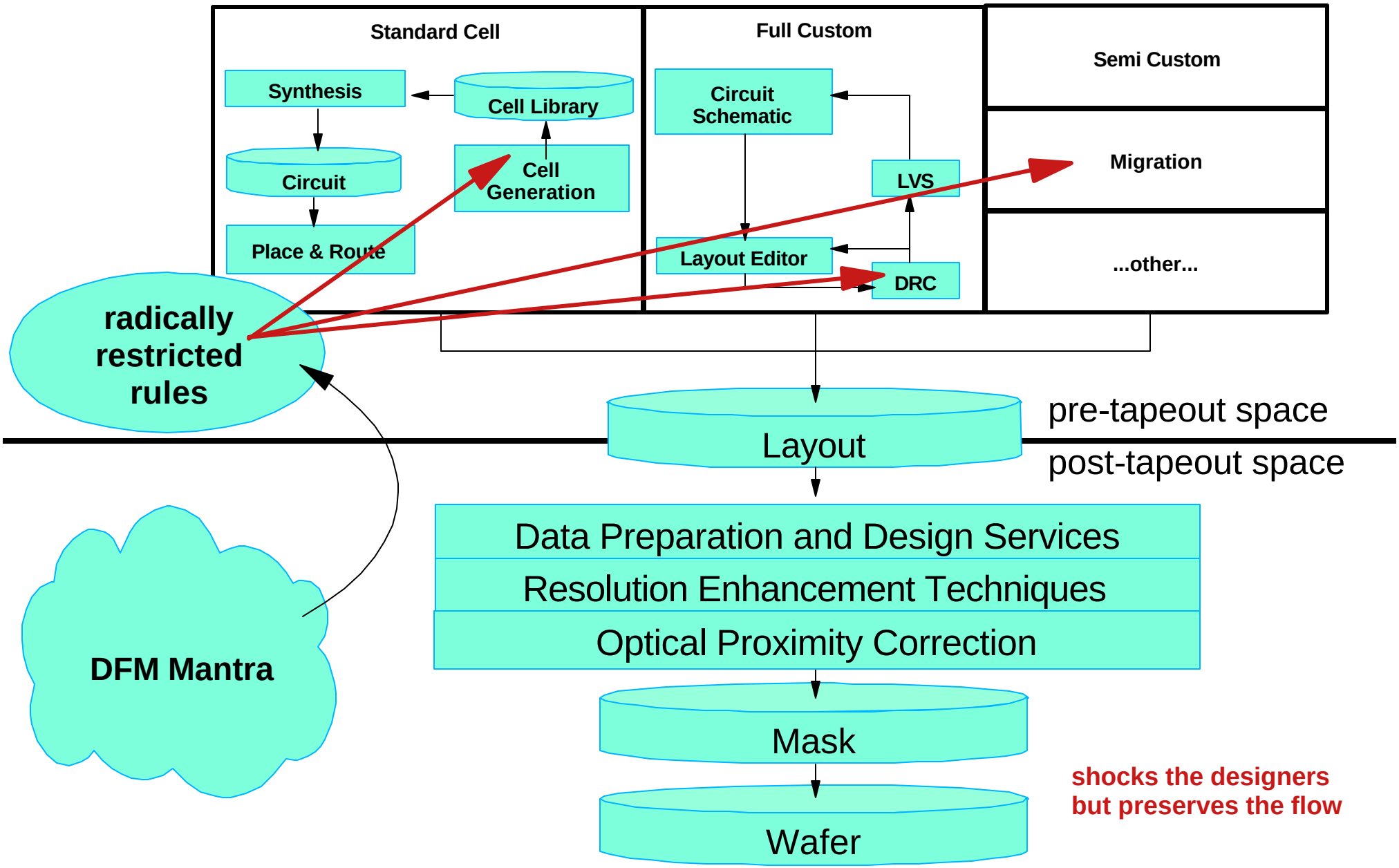


Design for Manufacturability Mantra

Design-rules, -tools, and -methodologies aimed at optimizing layouts for all future technology generations should:

- **generically enable lithographic resolution enhancement techniques**
- **improve manufacturability at extremely aggressive patterning resolution**
- **ensure migrateablility of designs into future technology nodes**
- **allow for density- and performance-competitive chip designs**
- **especially in the foundry market, address a broad spectrum of customer objectives with a single design and process solution**

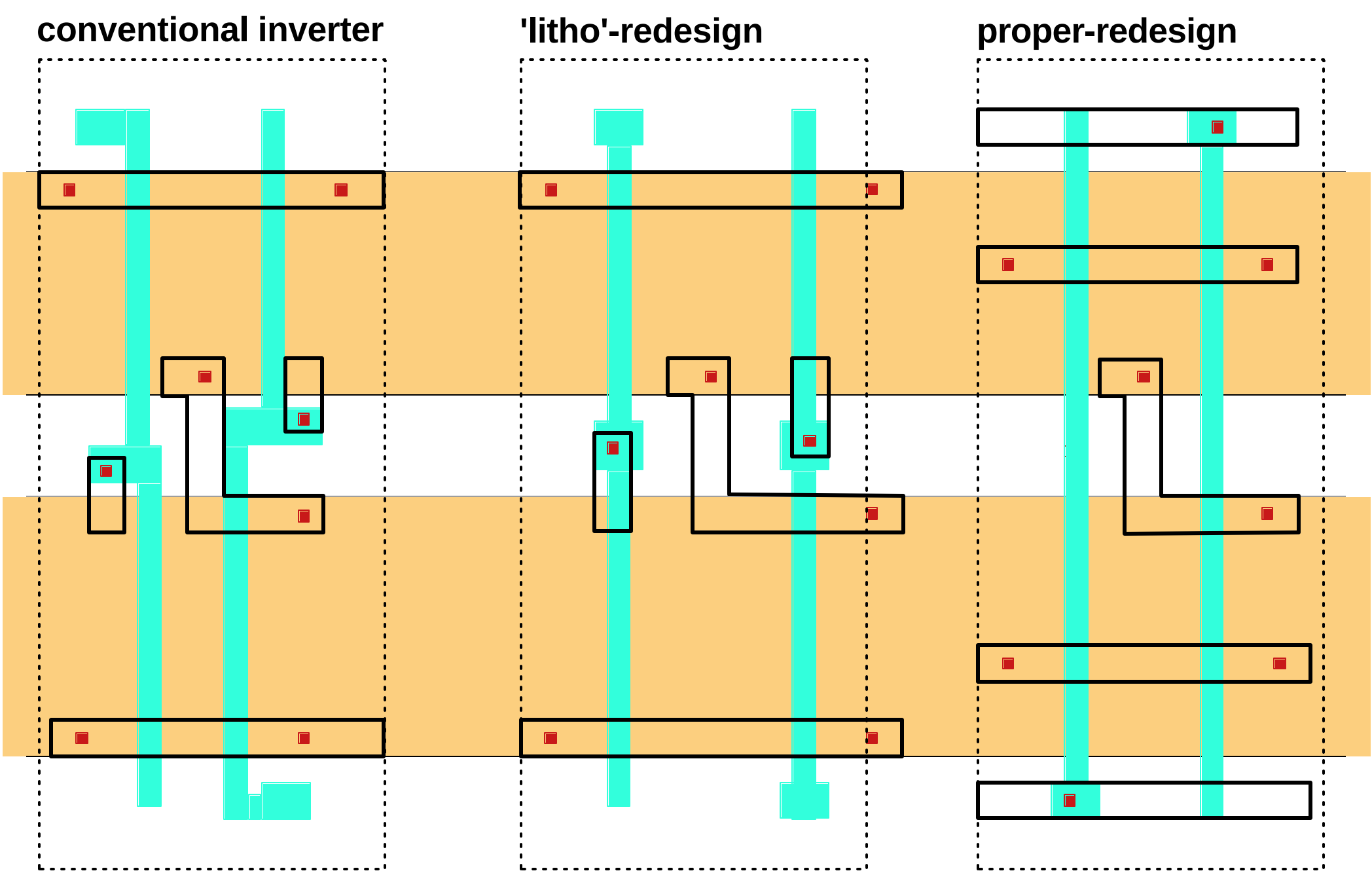
Option 2: DFM through RDR



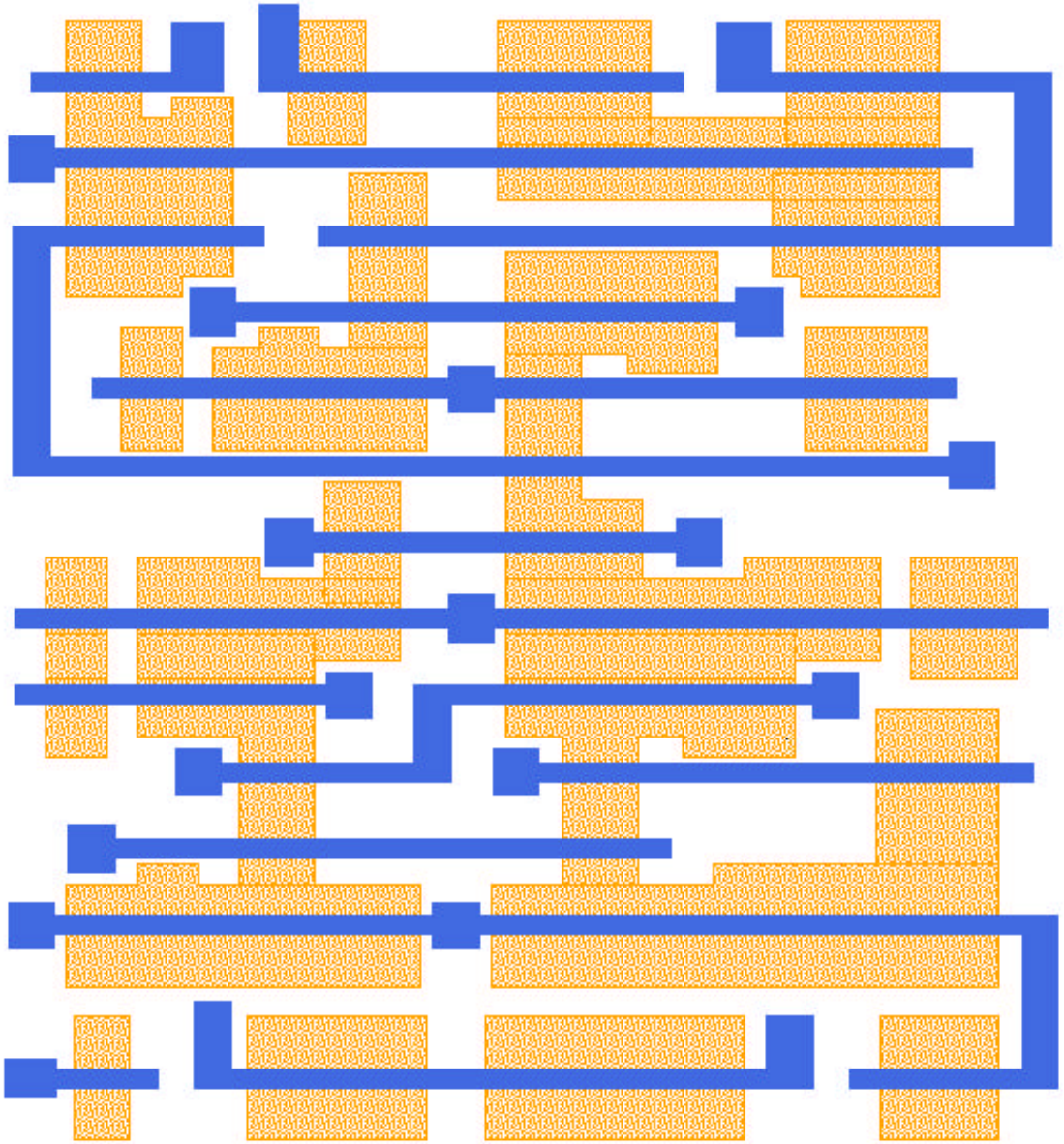
Proposal: understand and compromise

Litho	Design	Compromise
resolution fundamentally driven by pitch, smallest pitch drives litho-optimization	need smallest possible space between gates and devices at tight linewidth control	support integer multiples of contacted pitch at minimum dimension
abrupt or complex changes in proximity environment cause dimensional control problems	need tightest possible linewidth control on gates	run critical gates in one orientation, try to maintain constant proximity over length (width) of the gate, avoid bent gates (45s)
as diffracted orders are lost, corners will increasingly round ... move corners as far away from critical areas as possible	need to change device width between two gates at contacted space	allow corners in diffusion at 1/2 contacted space
at low k_1 details are lost, small jogs only add to datavolume and confusion	need DRC clean layouts	define spacings on related mask levels such that pitches align across critical levels, refine design rules to avoid artificial complexity

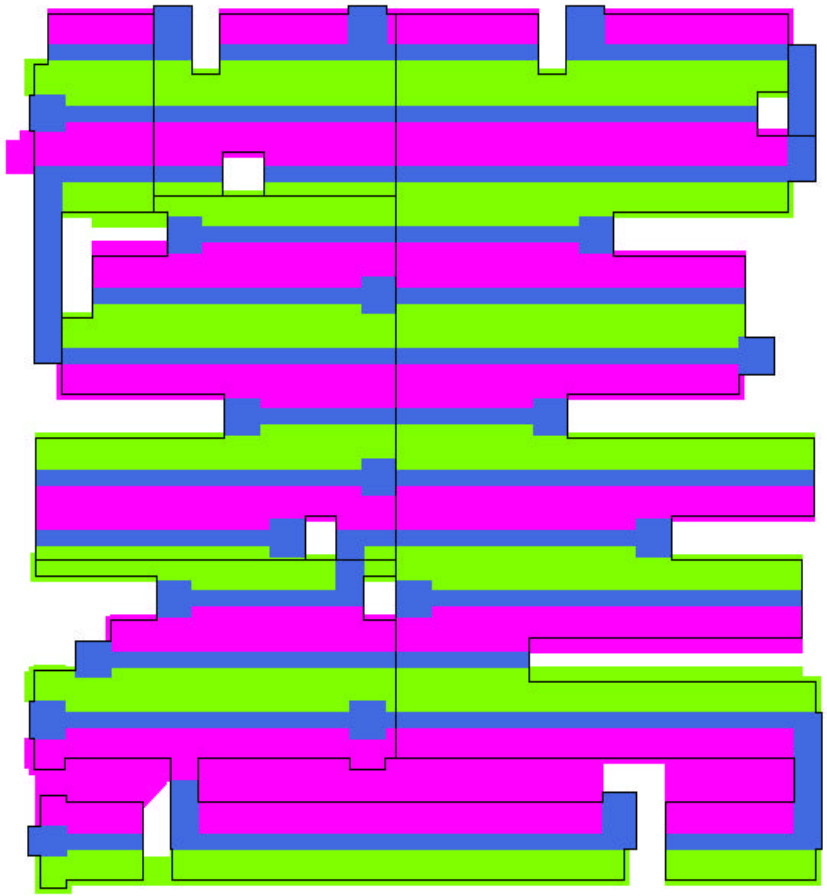
It's not just about density

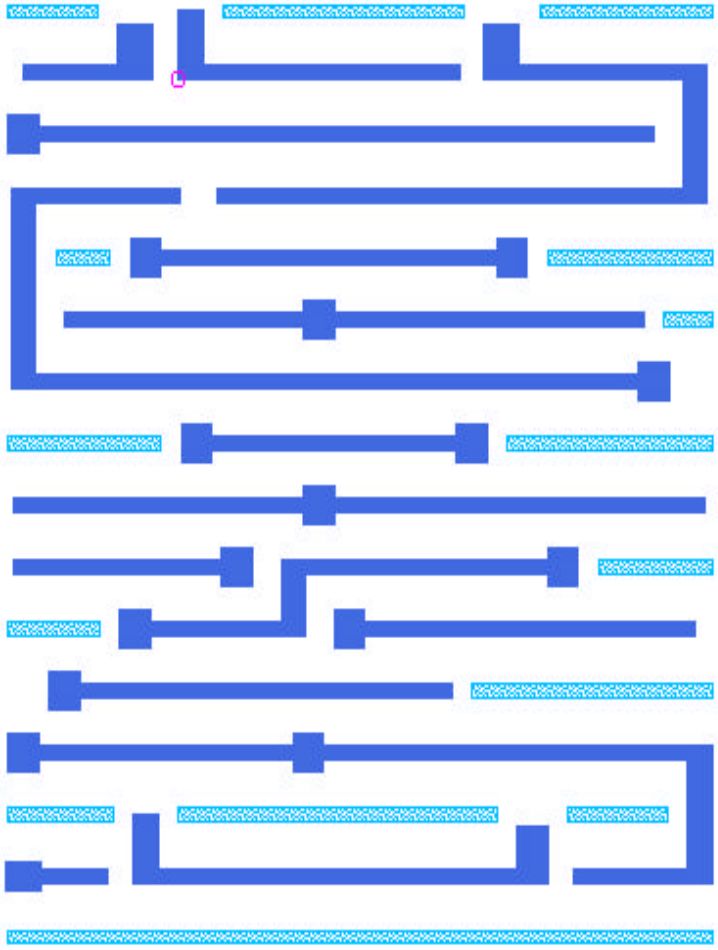


Feasibility study

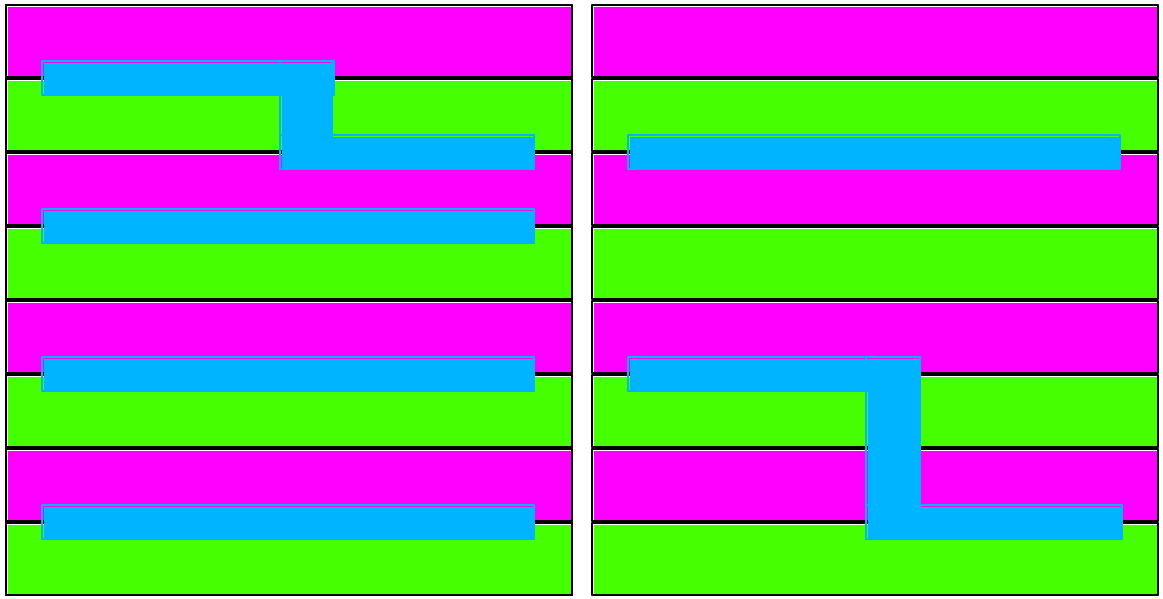


Generically RET compliant



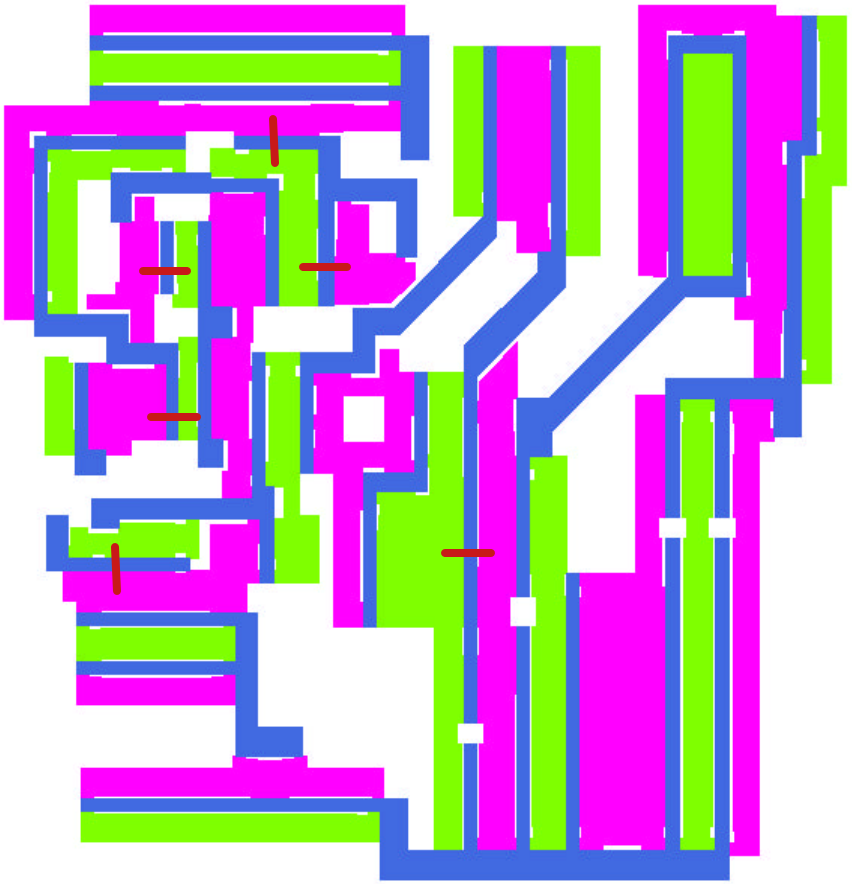


Generically place'able

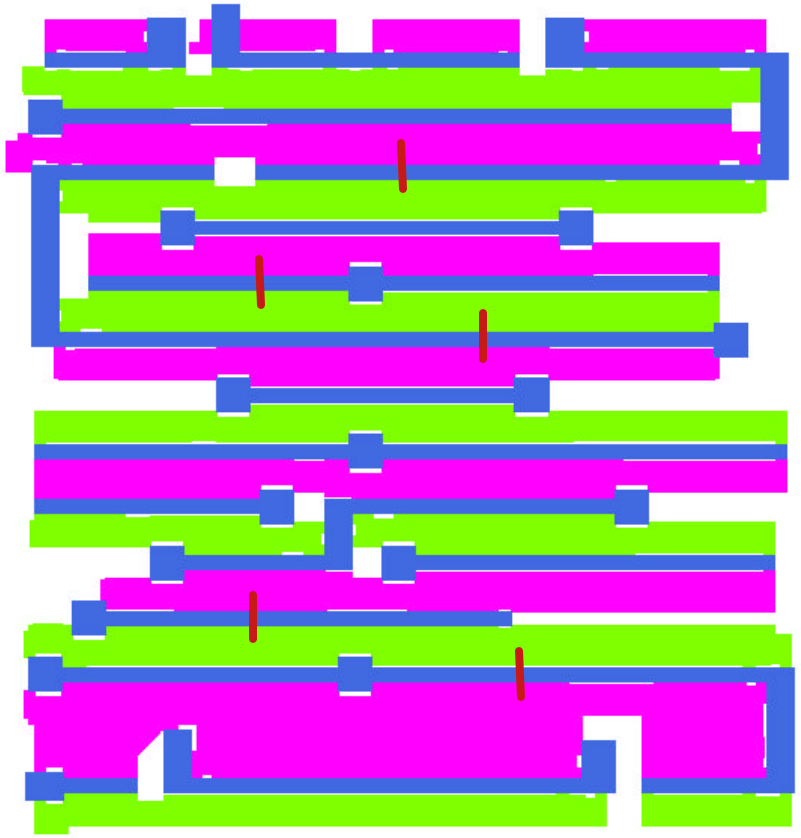


Across chip linewidth variation

'Conventional' Latch

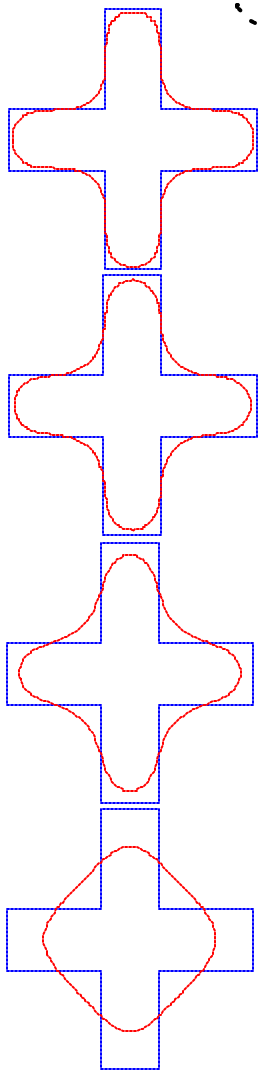


Manufacturable Latch



Working on performance improvement quantification….

Rayleigh constant for various technologies ... RDR close the plan



$R = k_1 \frac{\lambda}{NA}$

0.8
0.7
0.6
0.5
0.4
0.3

180nm node
130nm node
90nm node
65nm node
45nm node

conventional
introduce RET
widespread RET

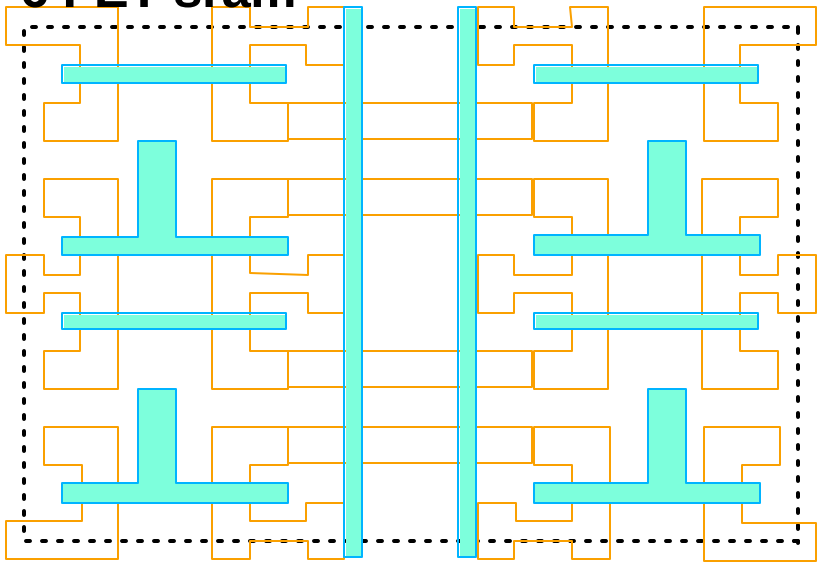
1997 1999 2001 2003 2005 2007

Wavelength
- 248 Dev.
- 248 Man.
- 193 Dev.
- 193 Man.
- 157 Man.
- 157 Dev.

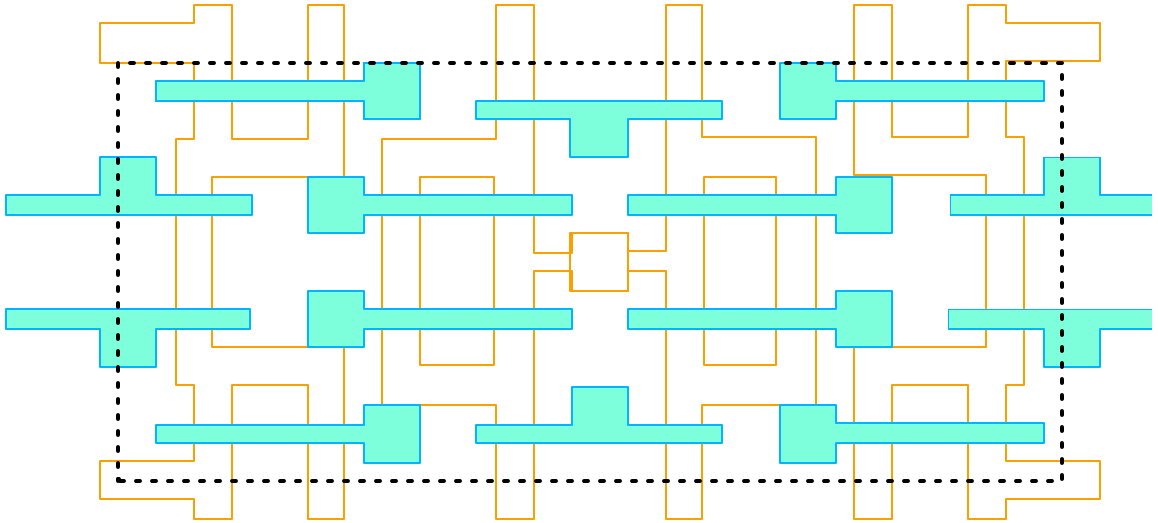
k_1 relief of pitch relaxation

...sure, but does it work for memory

schematic of conventional 6 FET sram



schematic of vastly more manufacturable 6 FET sram



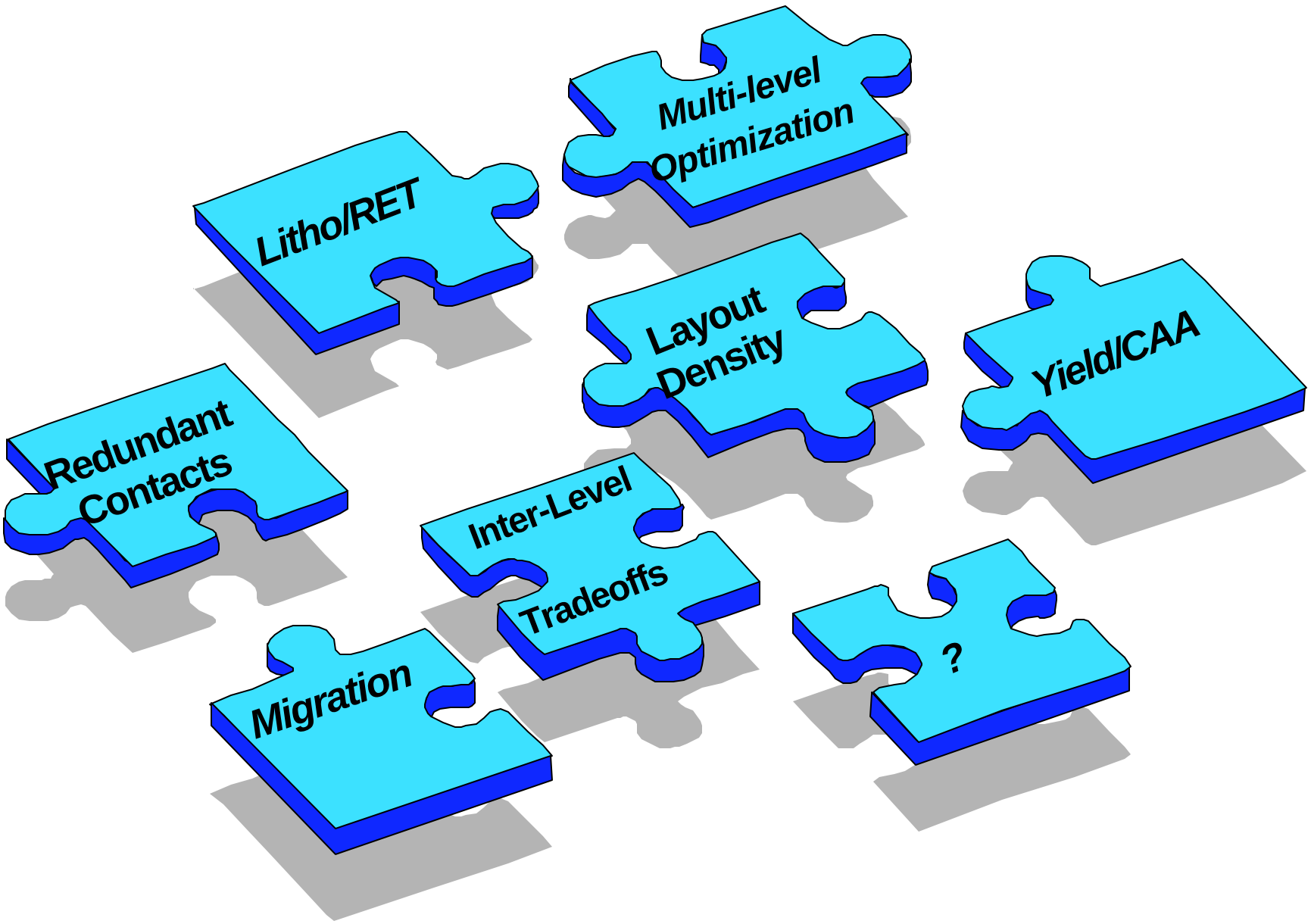
Poly level:

- generically RET compliant (migrateable)
- decreased dependence on complex OPC

claiming density impact is gross oversimplification (same area for 4 cells),

- lithographic benefit needs to be weighed against complex performance issues
- not all levels benefit as much as poly

Challenge: more pieces to the puzzle



Conclusion

Future technology nodes are critically dependent on flawless implementation of strong-RET.

All strong-RET require layout restrictions, prohibiting the reuse of existing layouts in these technology nodes.

Conventional design practices will be significantly perturbed by the need for strong RET.

The need to generate RET-compliant designs offers the opportunity to fundamentally improve chip layouts by adopting the DFM mantra and implementing radical design restrictions.

If we do everything right, we can accurately approximate 2-beam imaging ....that means we are patterning with 1 diffracted order of light

>>> gratings are good!

Catch-22 or Win-Win:

- **tight pitch requires strong RET**
- **strong RET require layout restrictions**
- **layout restrictions kill DRC-based design**
- **radical design restrictions are attractive alternative to RET-embedded layout**
- **radical design restrictions (relaxed pitch) lessen dependence on strong RET**