Invited Talk – ISPD 2025

Automatic Die-To-Die Routing With Shielding

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Outline

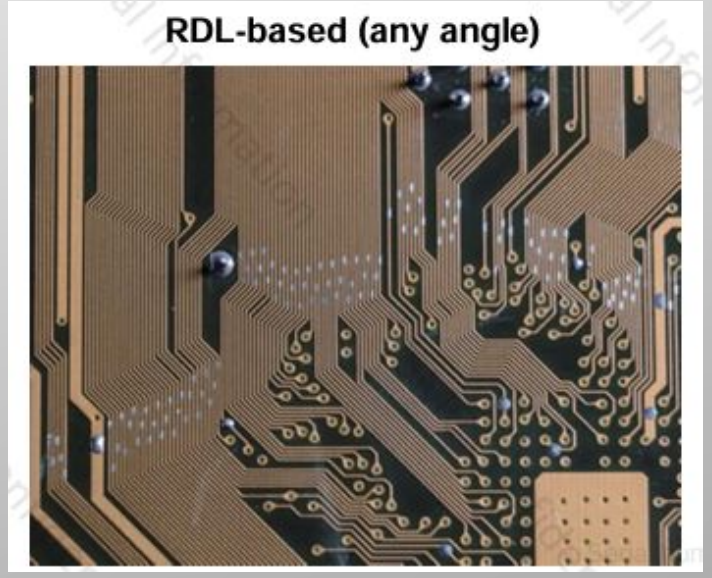
- An advanced packaging's bottleneck - routing
- Approaches for global wiring with space reservation for shielding
- To-dos: detailed wiring with teardrop rotation, and DRC rules

Acknowledgements

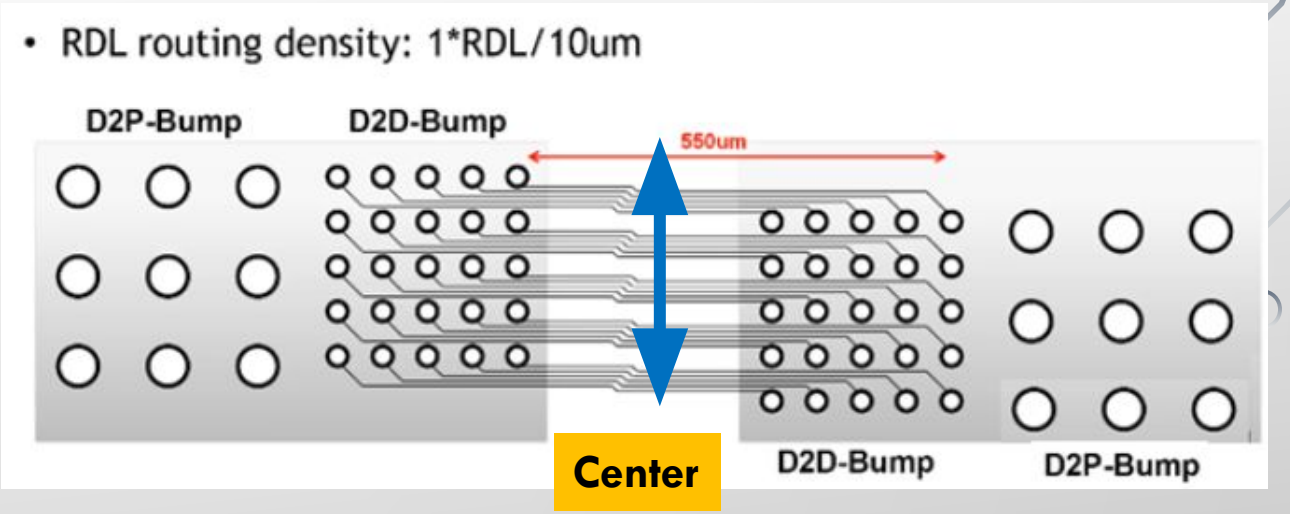
- Foundry-T
- National Science and Technology Council (Taiwan)

Routing – A Bottleneck In Advanced Packaging

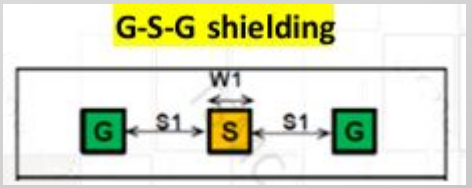
- 3D heterogeneous chiplet integration has become a hot area
- RDL (redistribution layer) routing covers tens-of-thousands signal connections with any-angle wiring and more design rules
- P/G routing and P/G plane with degassing are getting complicated
- Auto-routing capability is much needed

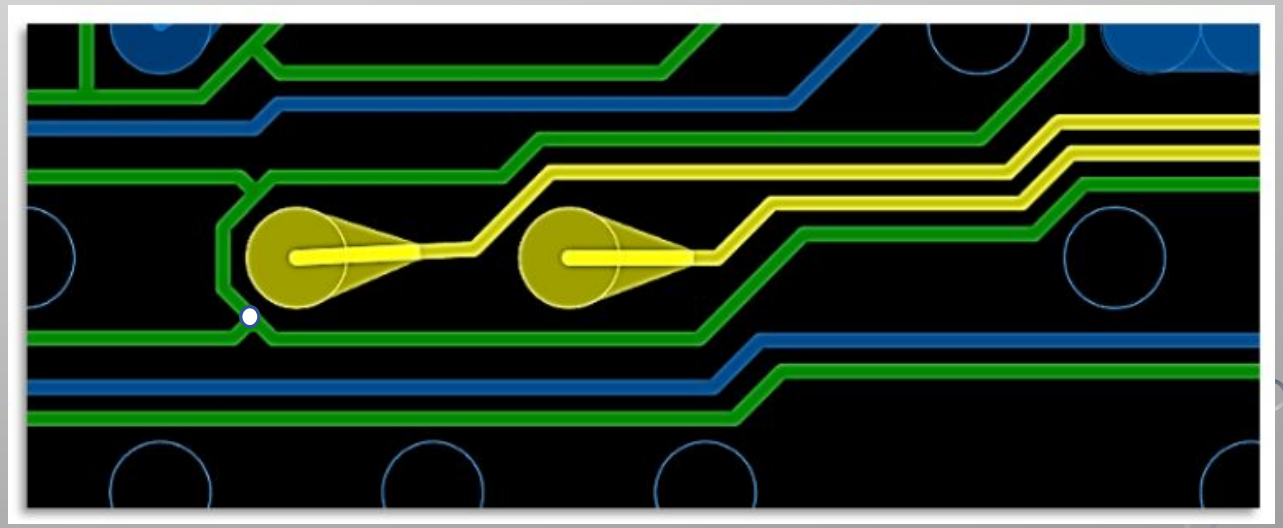


Die-To-Die Routing



- Trend – high density and shielding is a must for electrical performance
- How to generate good wiring results is not easy



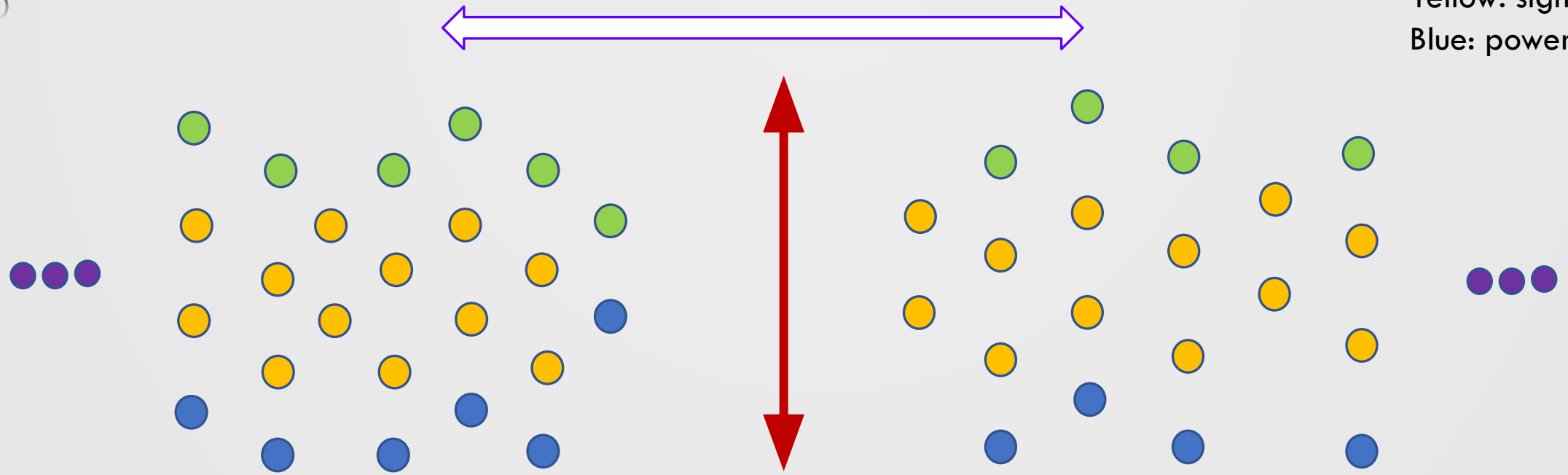


Green: ground wire
Yellow, Blue: signal wire

https://semiengineering.com/advanced-auto-routing-for-tsmc-info-technologies/
https://semiwiki.com/semiconductor-manufacturers/tsmc/287582-optimizing-chiplet-to-chiplet-communications/

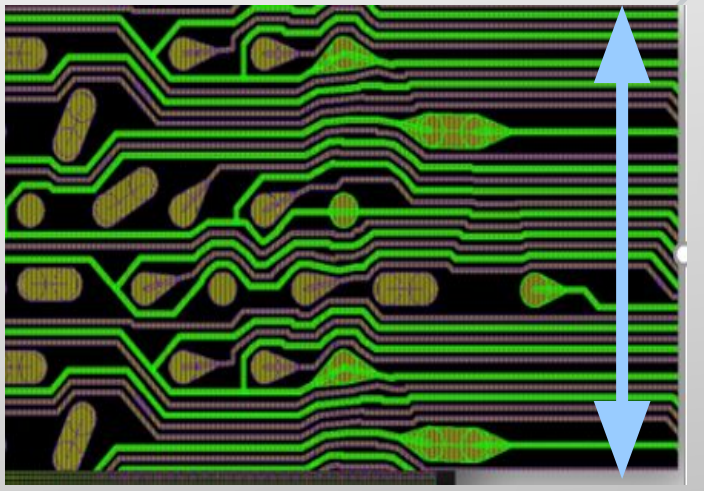
A Typical D2D Routing Problem – One Lane

Green: GND
Yellow: signal
Blue: power



1) Get number of nets to be connected and bump locations
2) All nets have 2 pins
3) Based on wire width, spacing, see how many wires can cross the center area (marked by red line).

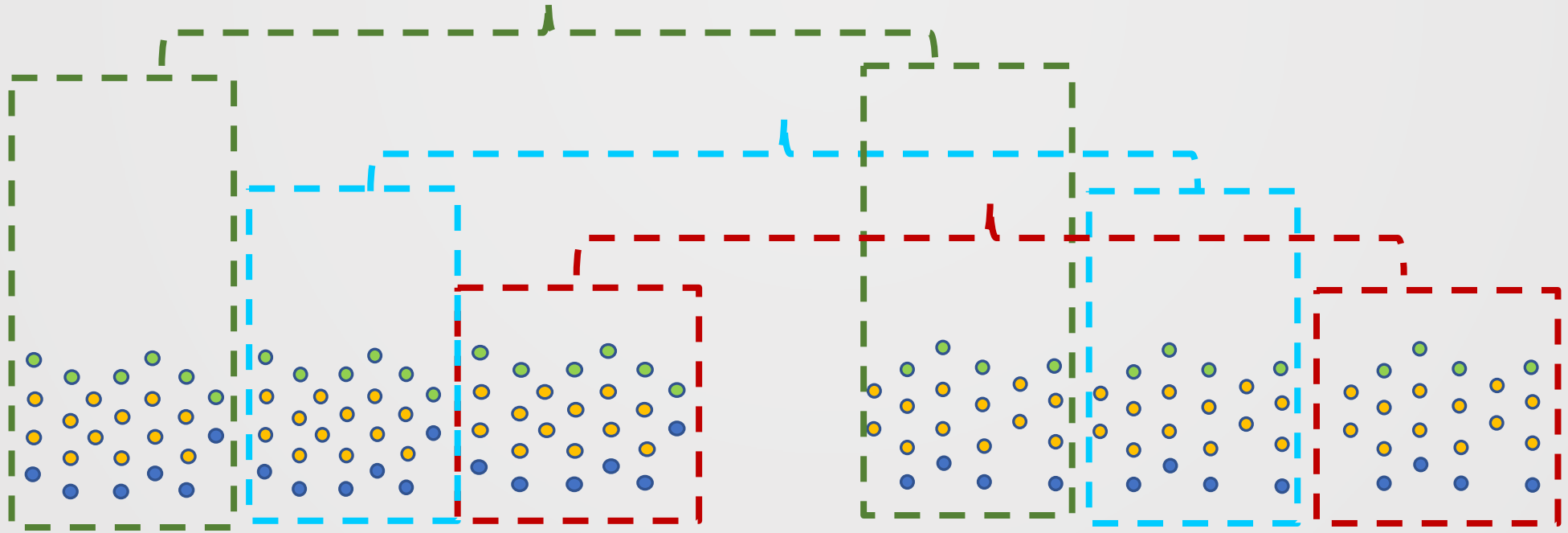
Routing Flow (1)



½ of # wires

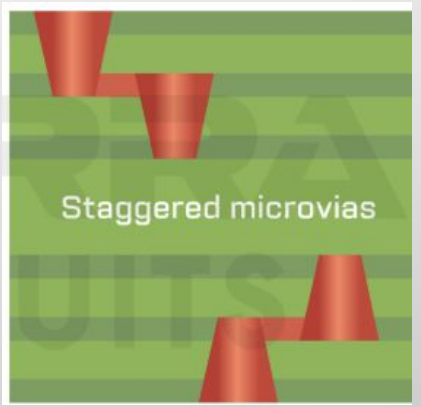
- Since GND shielding wires run almost side by side with the signal nets, we can estimate # nets able to cross the center area (i.e., half of # wires)
- Decide roughly number of layers needed
  - Assign nets to layers
  - For those nets to be routed at higher layers, they need to escape from lower layers
    - Need to consider non-via-stacking rules

Routing Flow (2): A Possible Way Of Layer Assignment

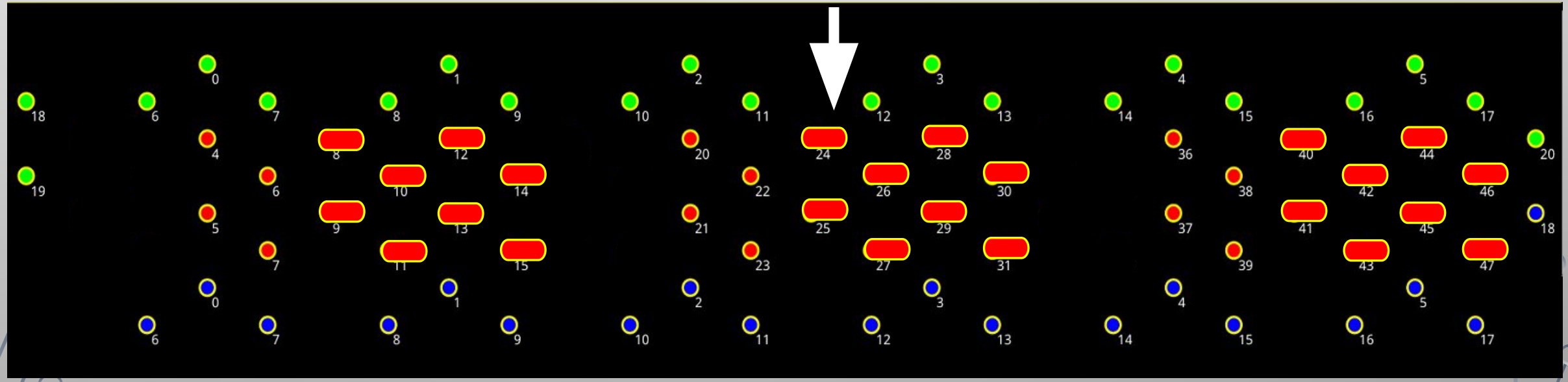


After finishing one layer, then we propagate the remaining connections to next higher layer. We can create a new sub-problem for layer L+1. When a bump "escapes" to higher layers, we need to consider the via-staggering rules.

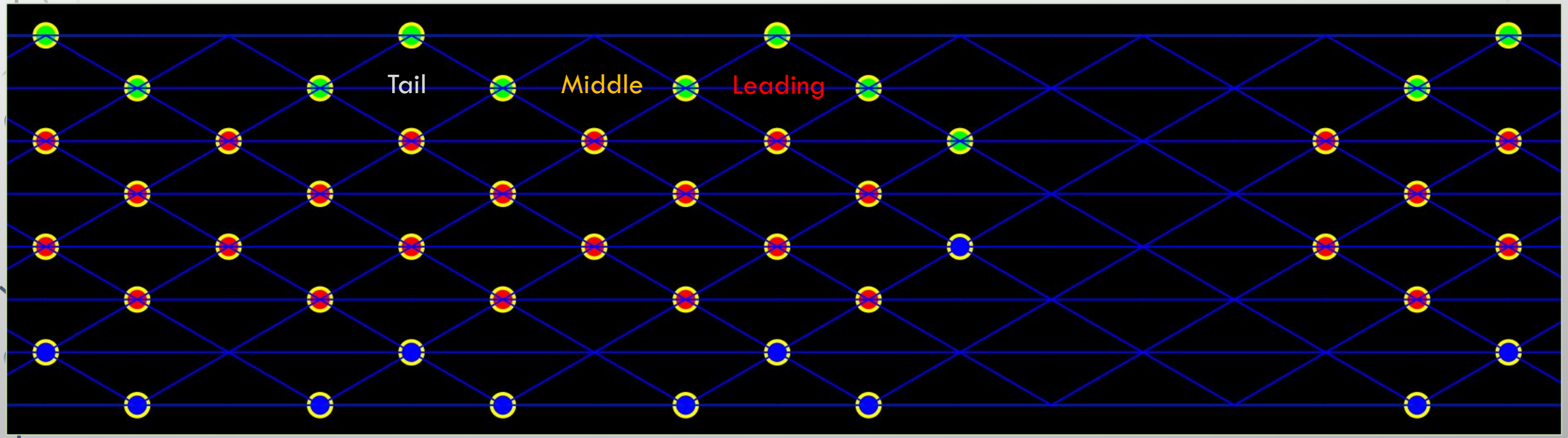
Impact Of Via-Staggering On Layer-2



Via offset
layer-N to layer-N+1



Routing Flow (3) : CDT (Constrained Delaunay Triangulation) & Global Routing Patterns

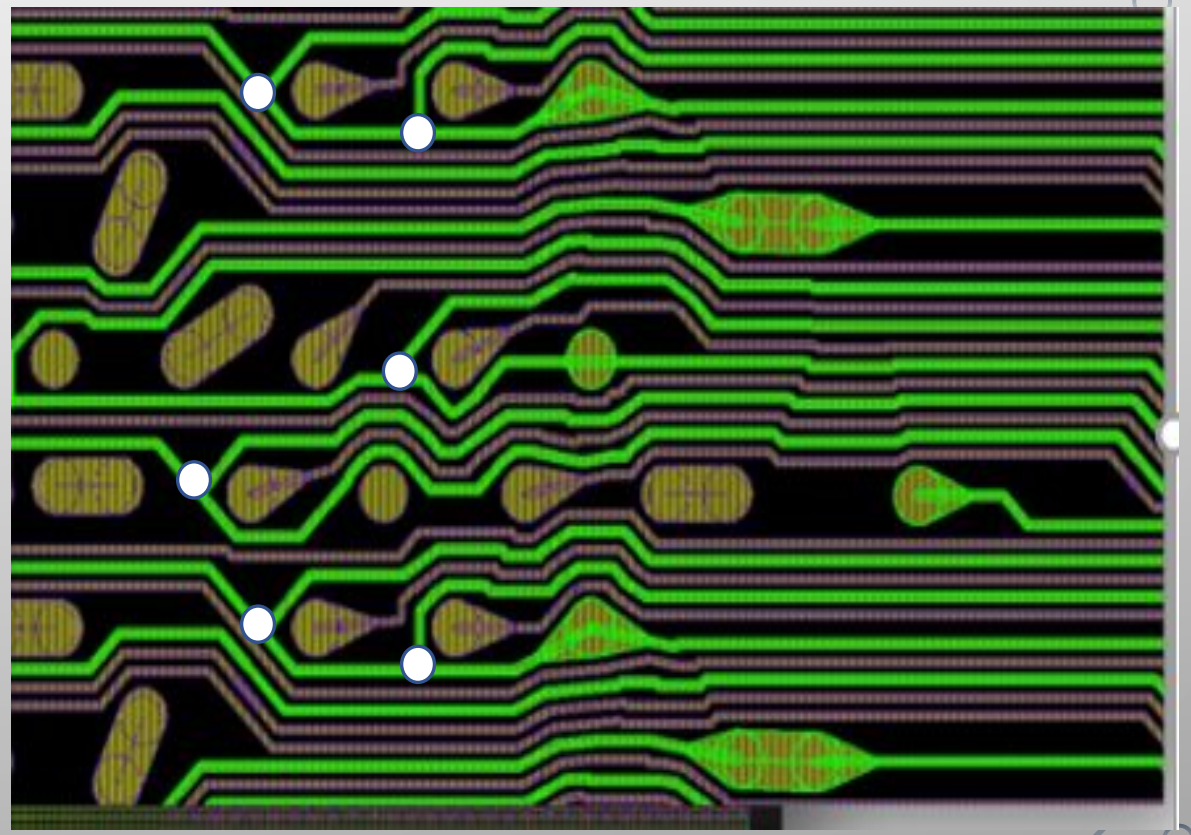


From the bump locations, we can see there are 4 rows for signal nets.
Each row we label bumps into 3 sub-groups: leading, middle, tail.
In each signal global wiring, short light green segments are for GND shielding.

Routing Flow (4): GND Shielding Wires

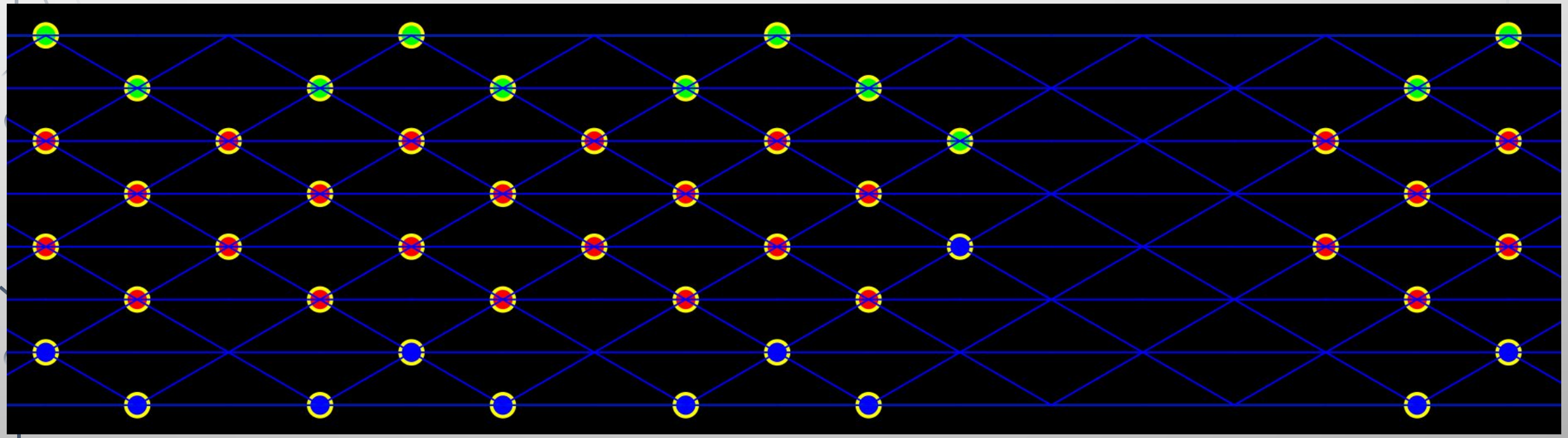
- When route GND wires, to achieve high shielding rate, we need to assign many branching points (as shown in white dot at the right).
  - Extra effort to devise the routing

Green: ground wire
Brown: signal wire



Global Route Sequence

Route VSS



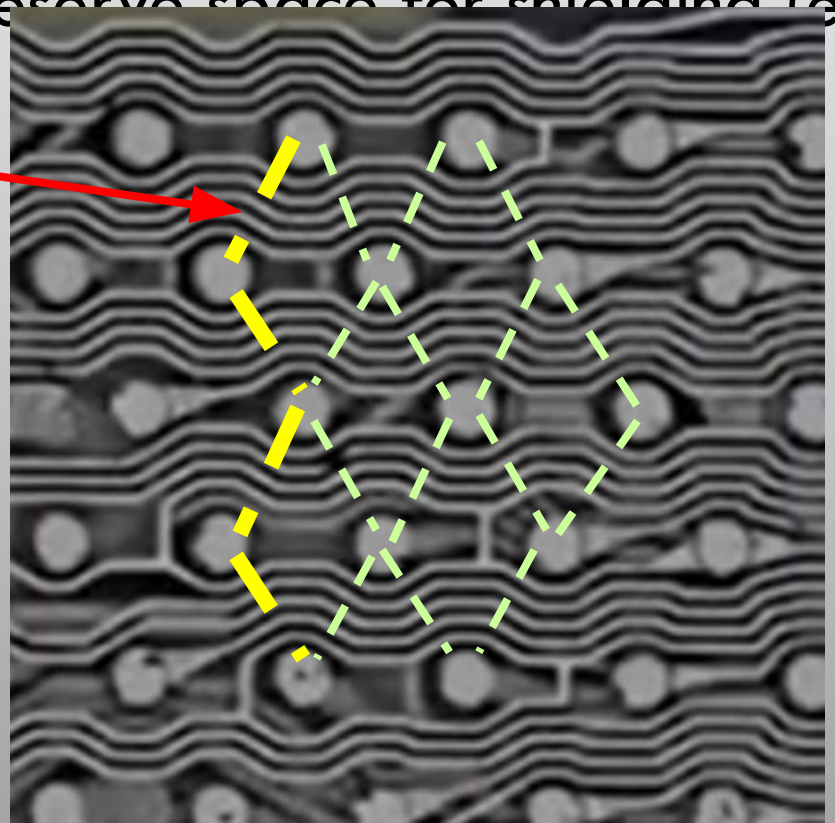
Route VDD

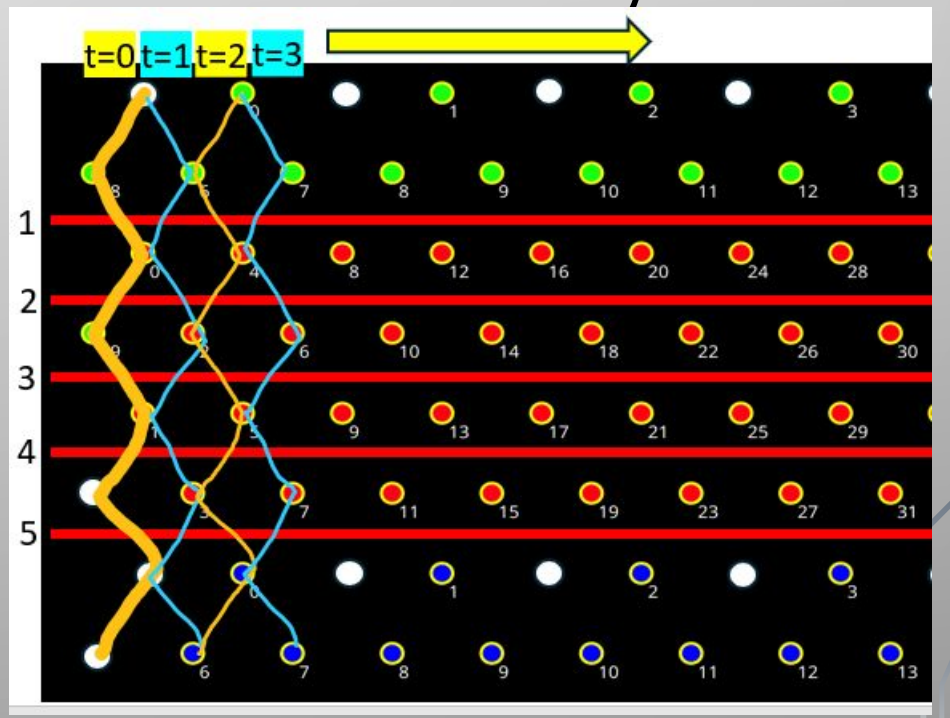
Connect VDD, GND bumps on two sides. If not enough wiring resource, we will leave some bumps open and escape to upper layers.
In each edge, if capacity is not fully used, extra GND wire is reserved.

Another Global Routing Approach

- Using skewed can line on each layer
- At each layer avoid crossing
- Reserve space for shielding (each edge allows at most 3 nets)

5 wires crossing an edge





Layer1_die1

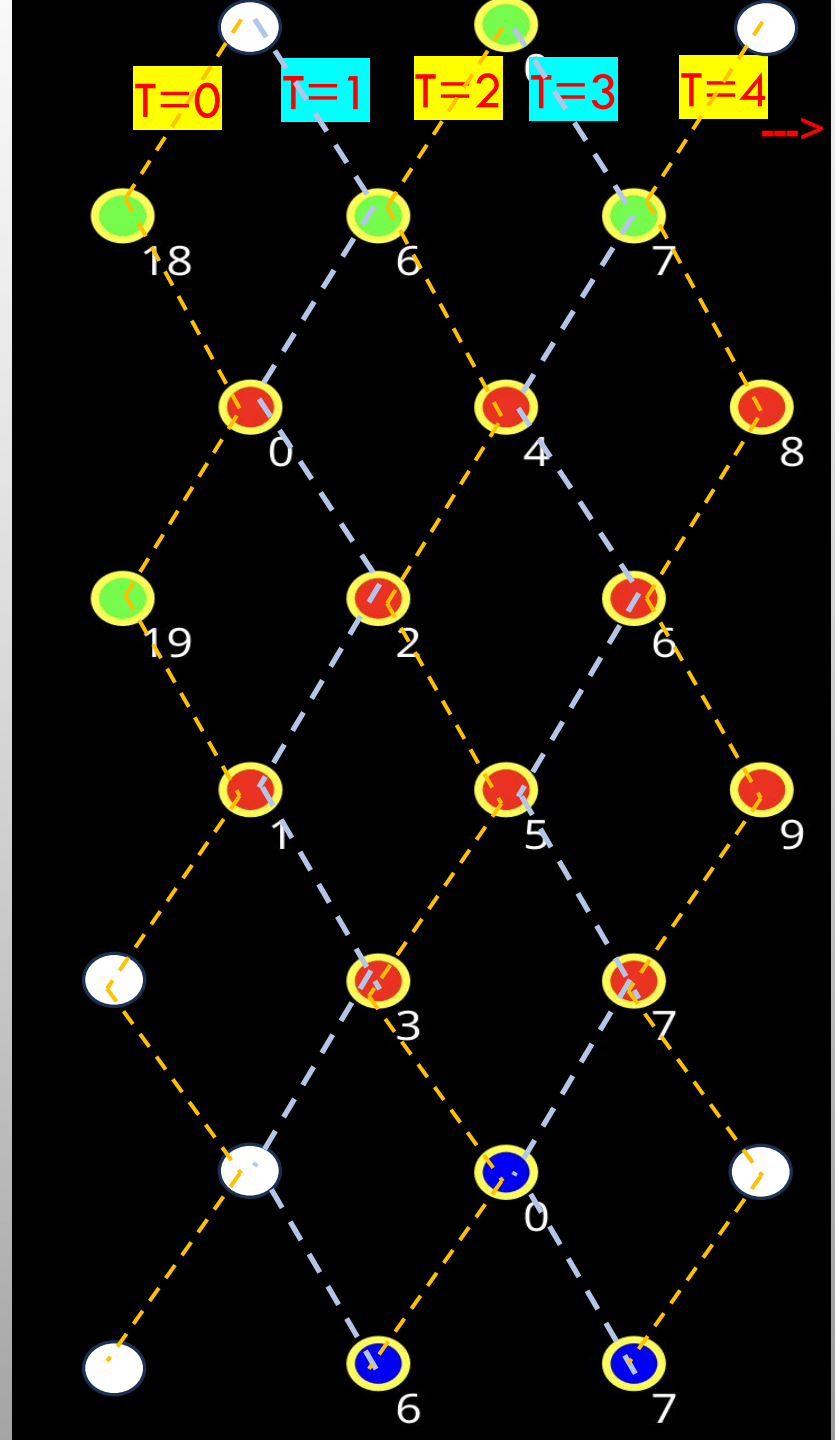
Group1(net0, net1, net2, net3)
Group2(net16, net17, net18, net19)
Group3(net32, net33, net34, net35)

For outer rows, wires prefer close to borders.

In the middle, such as net1, net2 prefer the center area.

Each edge allows at most 3 signal nets to go through.

When we global route group3, some rip-up-reroute is needed.



net2, net1take center

Summary

- In GR, the wiring order is created and GND shielding space is reserved
- Next we will work on detailed routing and DRC checker
  - Teardrop shapes will be rotated to avoid DRC errors