Integrated Design Ecosystem for Chiplets Heterogeneous Integration in Advanced Packaging Technology

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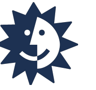
Semiconductor Industry Landscape



>$1T
Growing almost double by 2030

$600M
2022

$205M
2000

HPC
Automotive
Mobile
Healthcare
AI everywhere
IoT
Hybrid Work
Aerospace
Gaming

PC Era
Smartphone Era
Data Center Era
AI Era

2000
2005
2010
2015
2020
2025
2030

Source: Gartner 2023

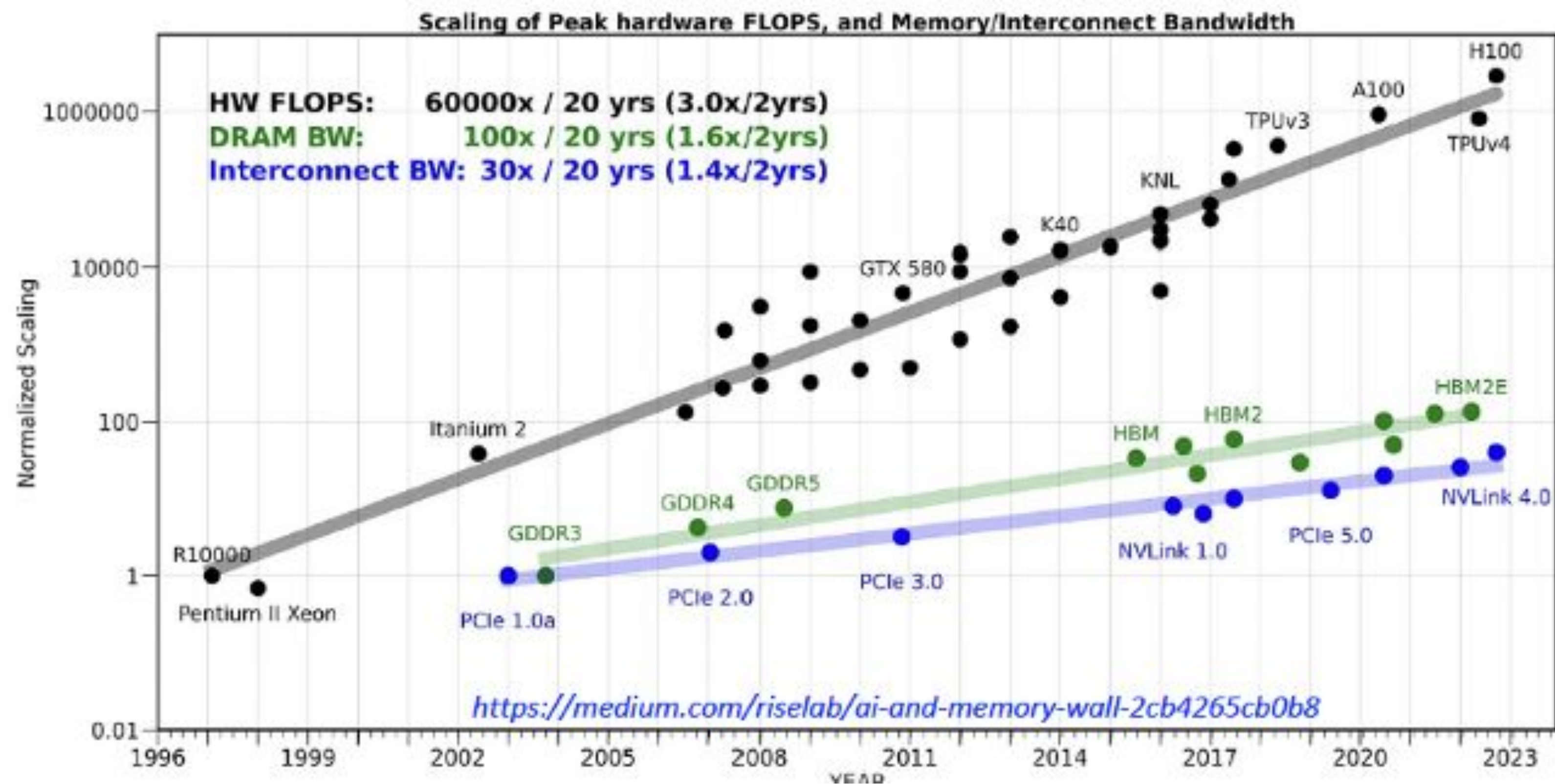
Scaling for AI Era

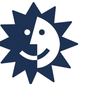
- *AI drives new architecture integration (Logic, Memory)*

NEW EFFICIENCIES

Mismatch between compute and bandwidth leads to low system utilization.

Optimizing new architecture and integration technologies



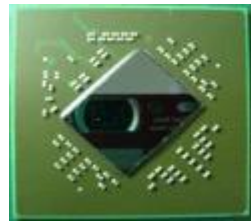


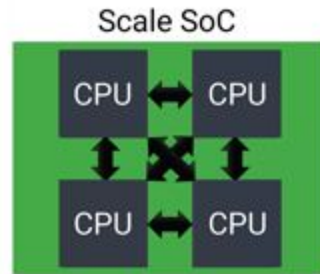
Chiplets and Heterogeneous Integration

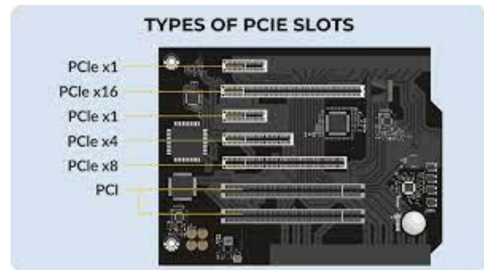
- Drivers for on-package Chiplets---IP reuse, higher performance, higher yield and Lower cost
- Chiplets---Disaggregation & Integration

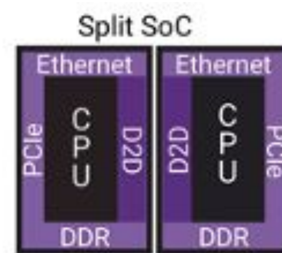
Monothetic Chip: Scale SoC & Homogenous one die in a package

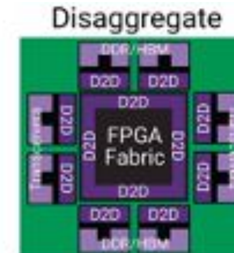
Chiplet: Split SoC & Heterogeneous multiple dies in a package

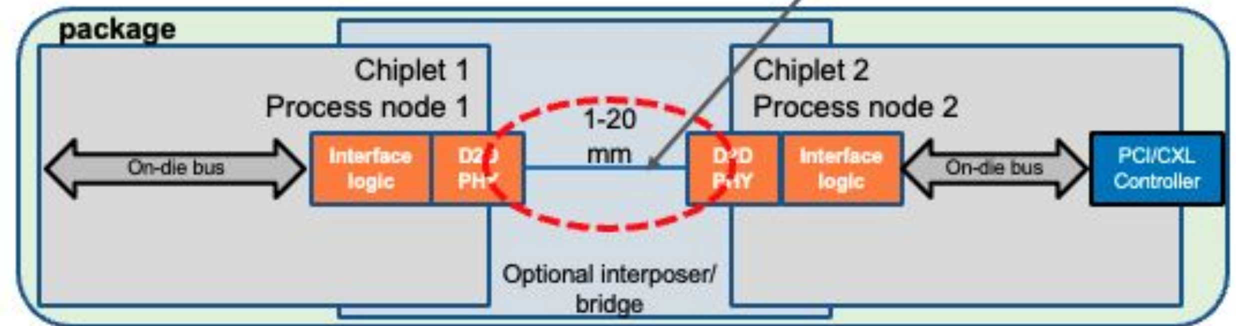








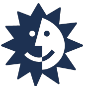




Off-package interconnect + simple package

On-package interconnect + more complex packages

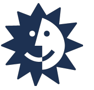
Chiplets – Complex Integration Workflow



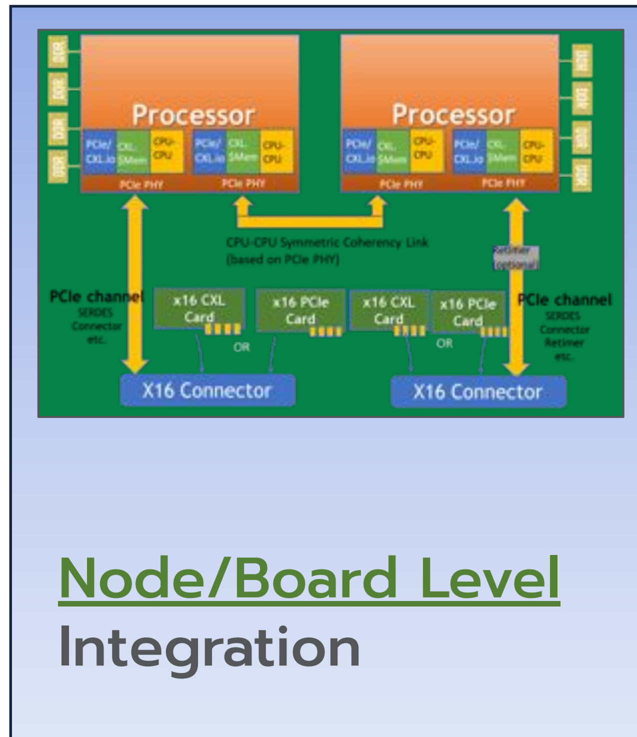
Key factors for more complex

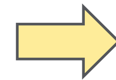
- Functional modularity
- Physical modularity
- Interconnect
- Packaging
- Test and operations
- Supply chain

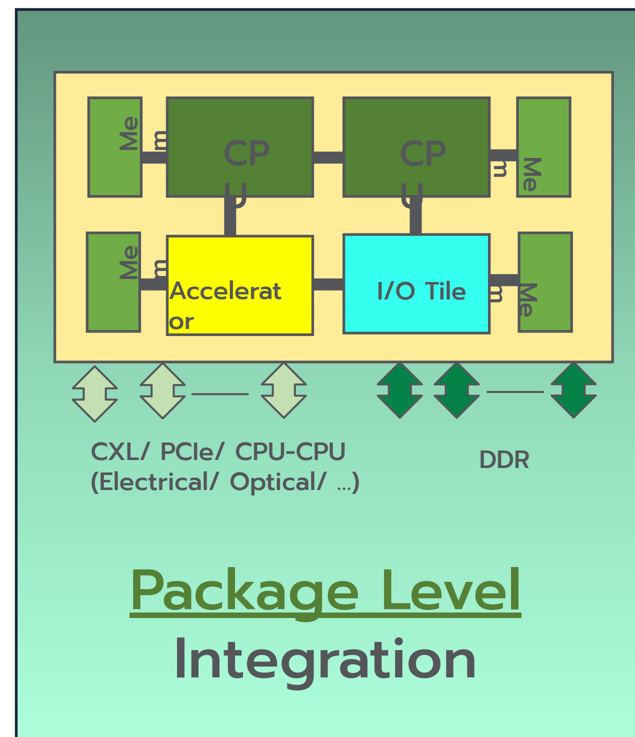
Chiplets Design Ecosystem

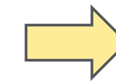


- Seamless Integration from Node/Board Package On-die
- Standardization for Chiplets D2D and interoperation (BoW, UCIe, OpenHBI)
- Same Software, IP, and Subsystem to build scalable solutions

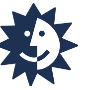








ASE Packaging Technology for Heterogeneous Integration



Performance

Density

Design Rule Improvement for Higher Performance

Wire Bond

Wire bond
(Dev in 1956)

Flip Chip
Ball Grid Array

Solder Flip Chip
(Dev 1964)

Fan-Out
Wafer Level
Package

Fan Out
Package
(Dev 2009)

2.5D
Through
Silicon Via

Cu Pillar Flip Chip
(Dev 2006)

VIPack Platform

FOSIP

FOPOP

FOCoS

FOCoS-B

2.5/3D
Enhanced

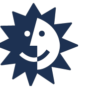
Co- SiPh

3D Advanced RDL Technology

Mobile - Networking - Compute - AI, Edge – Automotive - Industrial

1984-Now	1995-Now	2009-2021	2022 ~

ASE Integrated Design Ecosystem (IDE)



Cross platform integration

Database Exchange

Netlist

Layout

Cadence

Verification

Siemens

Mask

Database Exchange

PDK

Integrated Simulations

Auto-route

RDL/Si Interposer

Design & reliability enhancement

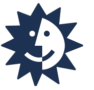
Die

Interposer

Fan-out HD RDL

Substrate

ASE Design Turkey Solution



Toolbox

FORDL Layout

Electrical

Thermal

Thermomechanical Stress

Material
(FORDL EBSD)

Robustness Testing
(FORDL Picoindenter)

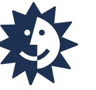
Assembly Process
(Corner Study + JMP)

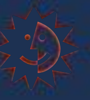
ASIC

HBM

DMY

Key Takeaways





Thank you