

# Invited: Toward an ML EDA Commons

Establishing Standards, Accessibility, and Reproducibility in ML-driven EDA Research

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# What can we learn from the success of AI?

## Open ecosystem and shared infrastructure

### AI Open Ecosystem and Shared Infrastructure

#### Collaborative Frameworks

 PyTorch  TensorFlow



**Hugging Face**

#### Pre-trained models

 LLaMA



deepseek

#### Community platforms

 kaggle  GitHub

#### Frameworks



ONNX



**Triton**

#### Datasets

 IMAGENET



COCO  
Common Objects in Context

# What can we learn from the success of AI?

## Beyond the infrastructure

### AI Open Ecosystem and Shared Infrastructure

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## ML Commons

### Benchmarks

- MLPerf
- AlgoPerf
- ....

### Data

- Datasets
- Croissant metadata

### AI Risk & Reliability

- MLCube
- MLCard

### Research

- Schema
- Algorithms
- Data-centric
- Science

# A case study in success

## ML Commons



Global collective engineering effort spanning industry and academia



Members and Affiliates

### Key principles:

- Grow AI markets and make the world a better place
- Get everyone involved
- Act through collaborative engineering
- Make fast but consensus-supported decisions
- Build a community that people want to be part of

MLPerf  
55,200+  
MLPerf results to-date across 6 benchmarks

Measure and improve the accuracy, safety, speed and efficiency of AI technologies

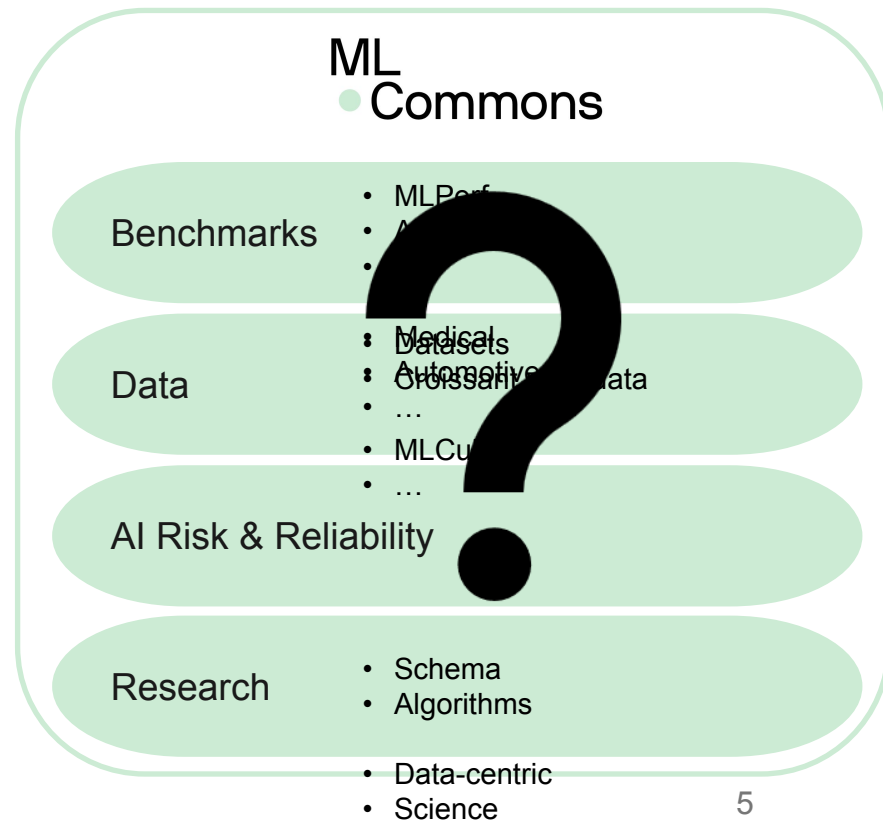
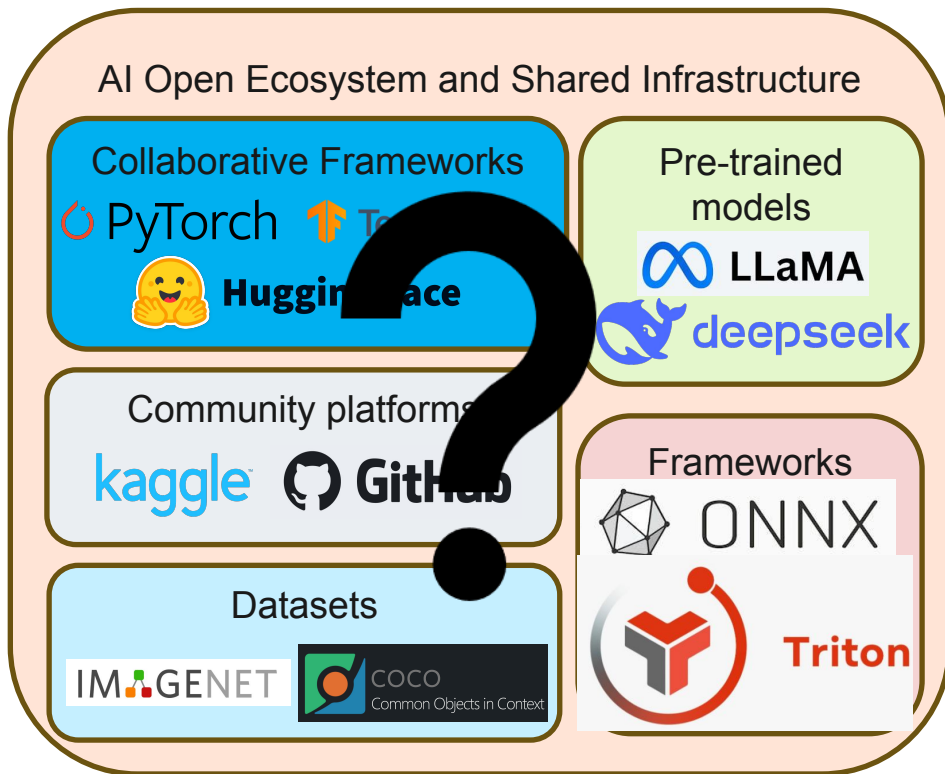
<https://mlcommons.org/>

### MLPerf breadth: $\mu$ Watts to MegaWatts

Scale	Evolution over time						
	2018	2019	2020	2021	2022	2023	2024
Training - HPC							
Training							
Inference - Datacenter							
Inference - Edge							
Inference - Mobile							
Inference - Tiny (IoT)							
Storage							
Automotive*							
AI Safety*							
Client*							

Targeting a diverse set of workloads that was built over time.

# What about ML EDA for physical design?



# This talk

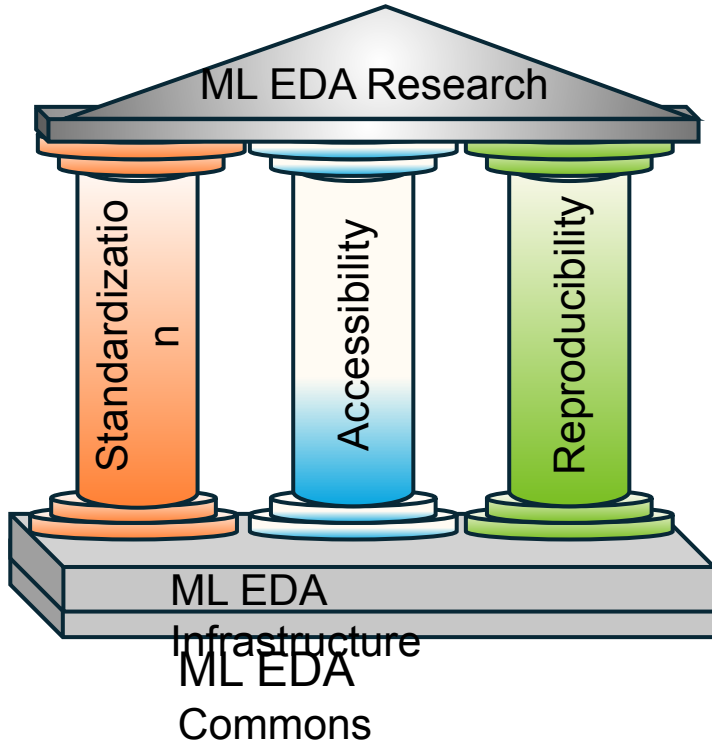
- Calls for the establishment of an **ML EDA Commons** to build ML EDA *infrastructure* and propel ML EDA research for the RTL-to-GDSII flow
- Highlights existing initiatives towards development of an *infrastructure* and identifies critical gaps in establishing an ML EDA Commons
- Outlines the scope and vision of an ML EDA Commons
  - Maturing and unifying ML EDA infrastructure
  - Establishing standards and governance
  - Prioritizing accessibility and reproducibility

# Agenda

- Vision of an ML EDA Commons
- Efforts toward ML EDA Commons
  - Infrastructure development efforts
  - Benchmarks and standardization efforts
  - Accessibility and reproducibility efforts
- Governance and roadmap
- Conclusion

# A vision for an ML EDA Commons

## The pillars of an ML EDA commons



- Foundations: ML EDA infrastructure
  - Datasets, models, proxies, contests, etc.
  - Python APIs with open-source tools, libraries
- Pillar: Standardization
  - Benchmarks and metrics
  - Data formats standardization and taxonomy
- Pillar: Accessibility
  - Open datasets and models
  - Open-source tools and flows
- Pillar: Reproducibility
  - Contests and leaderboards
  - Artifact and community evaluations

# Road to an ML EDA Commons

## Components of an ML EDA Commons

Nascent

Mature

Ongoing individual-driven infrastructure development efforts:

Benchmarks and metrics

Datasets

Contests

Tools & flows

Tools & flows

Tools & flows

Tools & flows

Proxies

Components of an ML EDA Commons:

Governance & standards

Consortium of stakeholders

Formats & quality

Sustenance

Accessibility & reproducibility

Cloud infrastructure

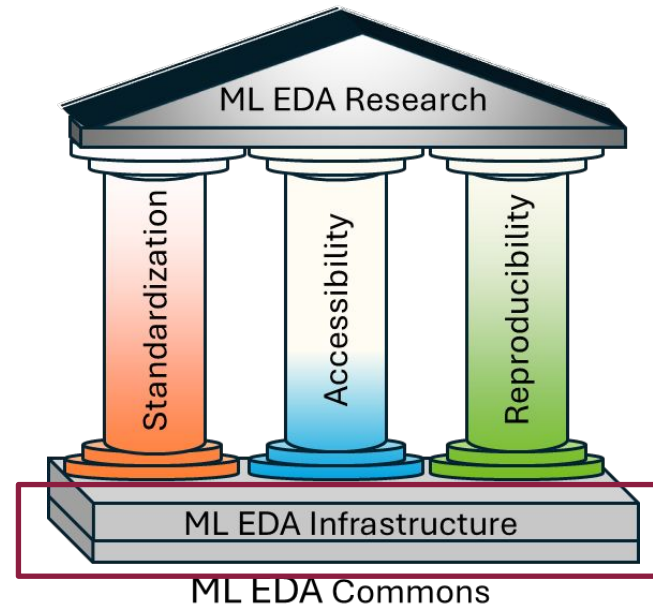
Open-source

Research artifacts

ML EDA infrastructure

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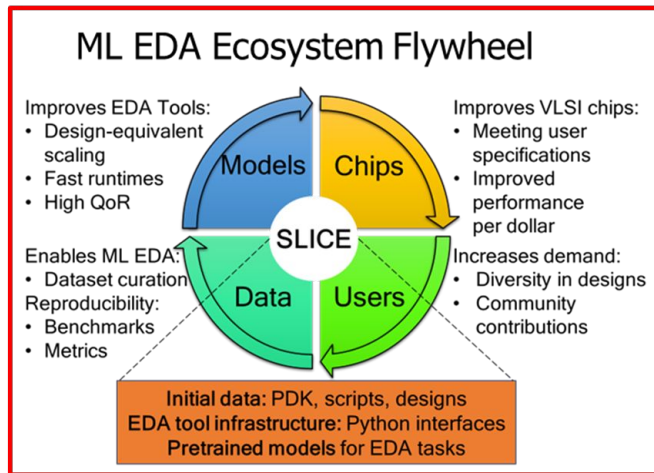
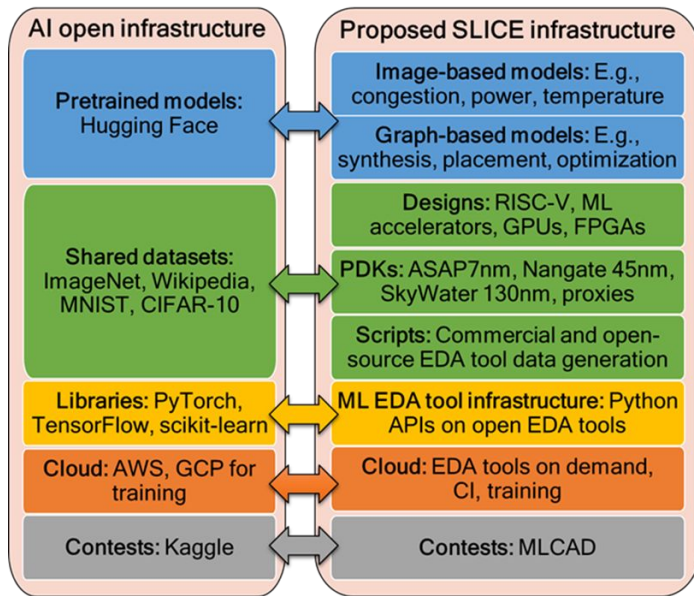
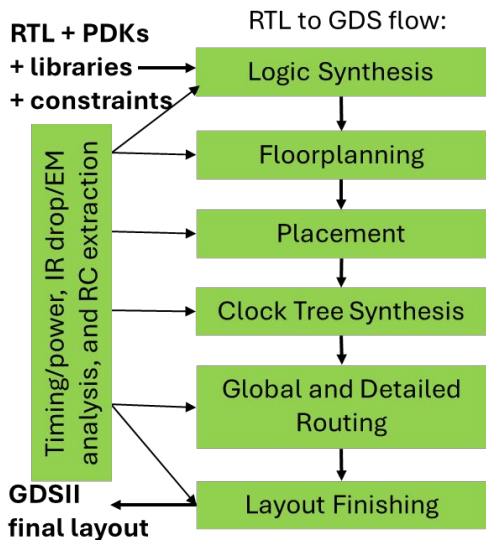


# Shared open infrastructure development efforts

## ML EDA Infrastructure: SLICE for RTL2GDS flow

<https://slice-ml-eda.github.io/>

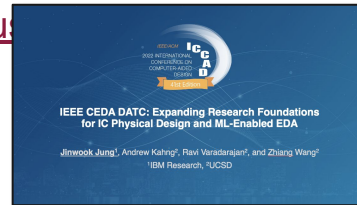
### Learning from the ML Community



# Open flows and design enablement efforts

## IEEE DATC Efforts

- A member technical committee of IEEE Council on EDA (CEDA)  
<https://iee-ceda.org/technical-committee/dadc>
- Since 2016, DATC has maintained Robust Design Flow (RDF) for RTL2GDSII
  - An academic reference RTL-to-GDS design flow incorporating numerous contest-winning point tools and the OpenROAD tool chain, to preserve and integrate leading research codes



- Other efforts:
  - Advancing benchmarks and baselines for ML enablement

V. A. Chhabria et al., "Strengthening the Foundations of IC Physical Design and ML-EDA Research", ICCAD 2024

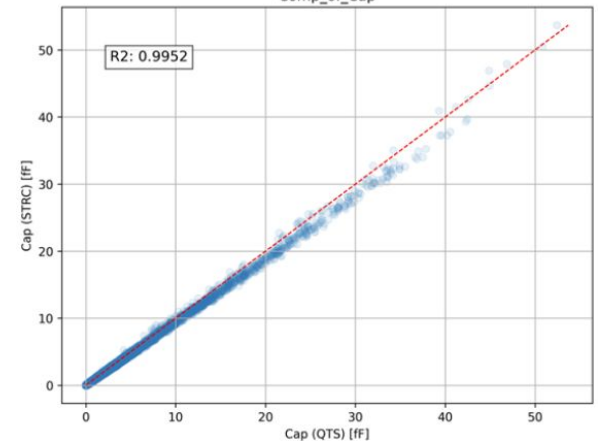
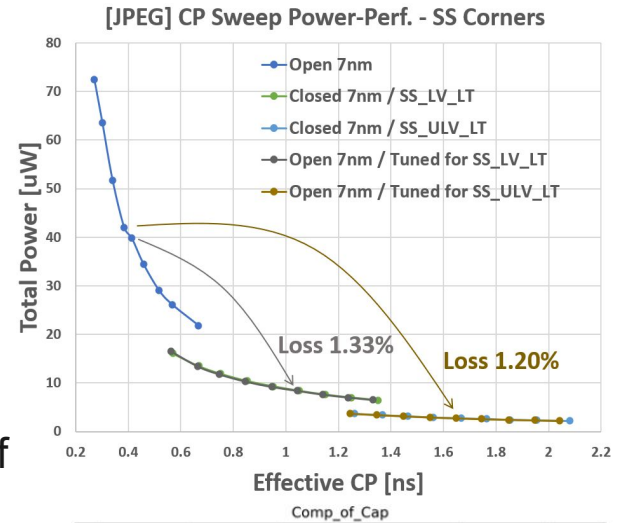
- Leaderboard using Metrics2.1 and autotuning and calibration

# Efforts towards open data via proxies

## PDK Proxies

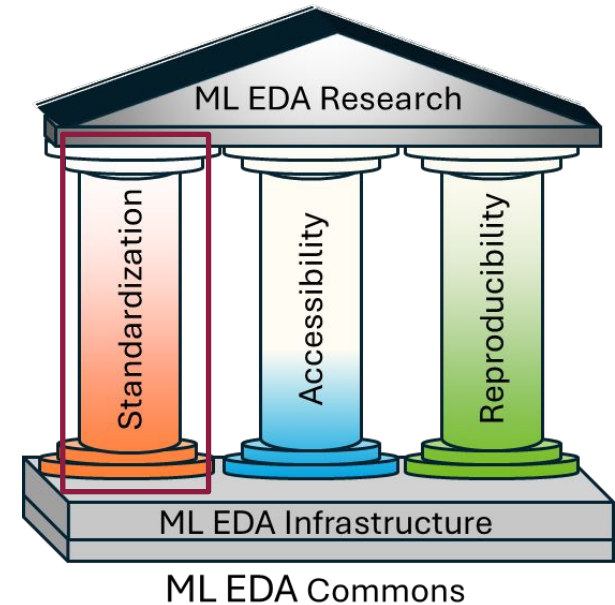
- Calibration of proxy design enablement
  - RDF-2023: autotuning flow to narrow gap between ASAP7 and commercial 7nm
  - RDF-2024: additional scaling factors enable matching of multiple PVT corners  
(<https://github.com/ieee-ceda-datc/Robust-Design-Flow>)
- Expansion of NanGate45 research enablement
  - NanGate45 (FreePDK45) was released with only Cadence enablement
  - Recently: TLUPlus is developed and made public for Synopsys users

V. A. Chhabra et al., "Strengthening the Foundations of IC Physical Design and ML EDA Research", ICCAD 2024



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# Efforts toward establishing benchmarks

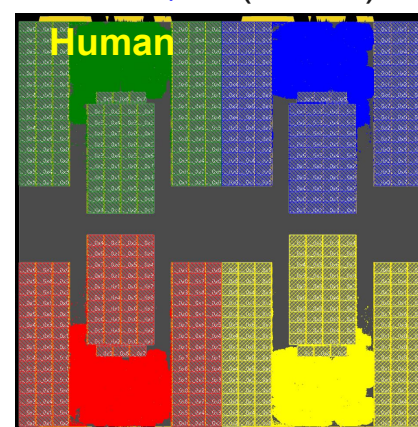
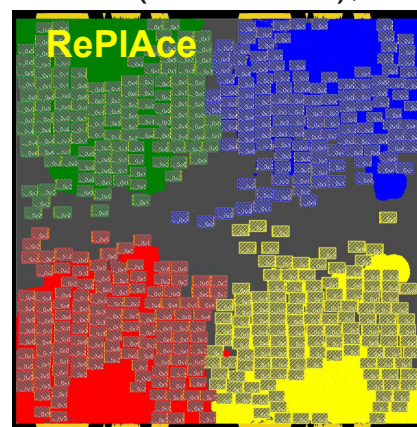
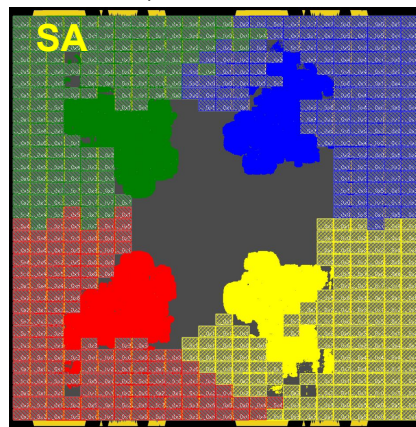
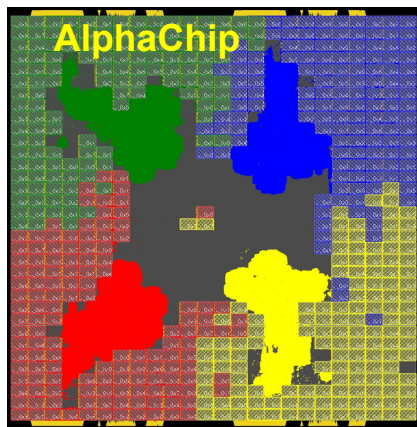
## Expansion of Modern Floorplan Benchmarks

- **MemPool Cluster** has been enabled on MacroPlacement
  - 1,296 macros, 10.5M instances
- Protobuf to LEF/DEF converter has been added
  - Protobuf is used in Google AlphaChip / Circuit Training (CT)

<https://github.com/TILOS-AI-Institute/MacroPlacement>

### CT-Ariane-X4 (Xflip-Yflip version): macro placement solutions

Gate-level detailed placement  
from macro placement (Finch) v21.1  
(NG45)



**AlphaChip** = Circuit Training (AlphaChip) fine-tuned from Google's pre-trained checkpoint  
**CT-Ariane-X4** has 532 macros, 332K instances (scaled from Google's Ariane protobuf)

# Leaderboard and calibration efforts

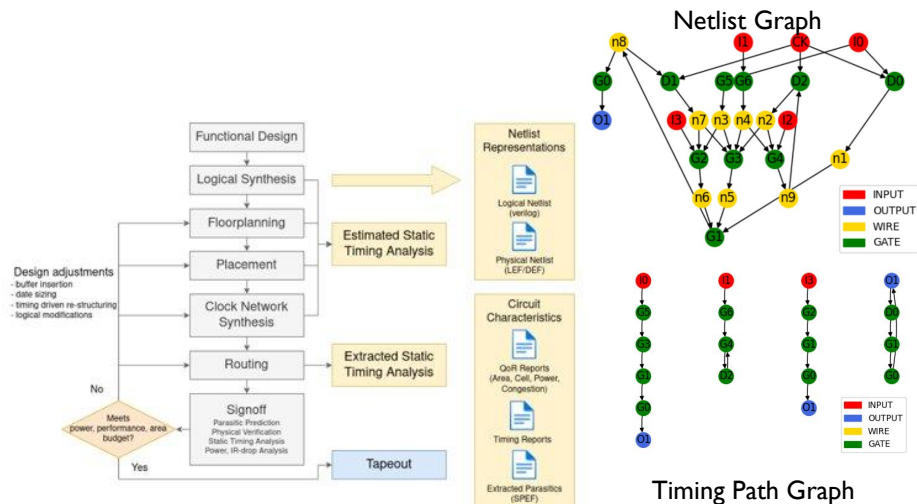
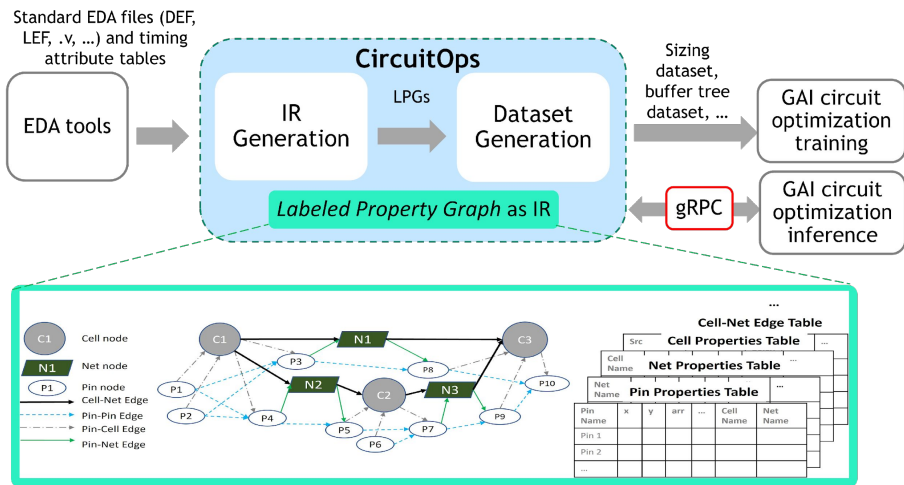
## IEEE DATC-driven efforts

- Revisited the Autotuning studies from METRICS2.1
  - Added newly enabled knobs of OpenROAD such as:  
(i) ENABLE\_DPO, (ii) TNS\_END\_PERCENT
  - Extended autotuning studies to find the **best implementations** in terms of power and area using an unnamed commercial tool flow
  - Also added results from **hybrid flow**
- Leaderboards in RDT enabled unnamed commercial tool, P&R using **Hybrid flow data (OR\*)** indicates, e.g., room for improvement in Yosys
  - All results evaluated using Open RCX and OpenSTA
  - Tracking progress in the rapidly evolving OpenROAD
  - Standardized baseline to easily plug, assess new EDA algorithms

Case	Goal	Tool	EffCP (ns)	Diff (%)	Area ( $\mu\text{m}^2$ )	Diff (%)	Power (mW)
IBEX	Perf	Comm	1.123	NA	68843	NA	794.9
		OR	2.313	106.0	44825	-34.9	92.0
		OR*	1.654	47.3	47969	-30.3	473.9
	Area	Comm	4.273	NA	22331	NA	39.3
		OR	4.346	1.7	37699	68.8	50.4
		OR*	4.134	-3.3	28077	25.7	56.6

# Establishing standard formats for ML EDA

## CircuitOps and EDA Schema



<https://github.com/NVlabs/CircuitOps>



<https://github.com/drexel-ice/EDA-schema>

Liang et. al "CircuitOps: An ML Infrastructure Enabling Generative AI for VLSI Circuit Optimization," ICCAD 2023.

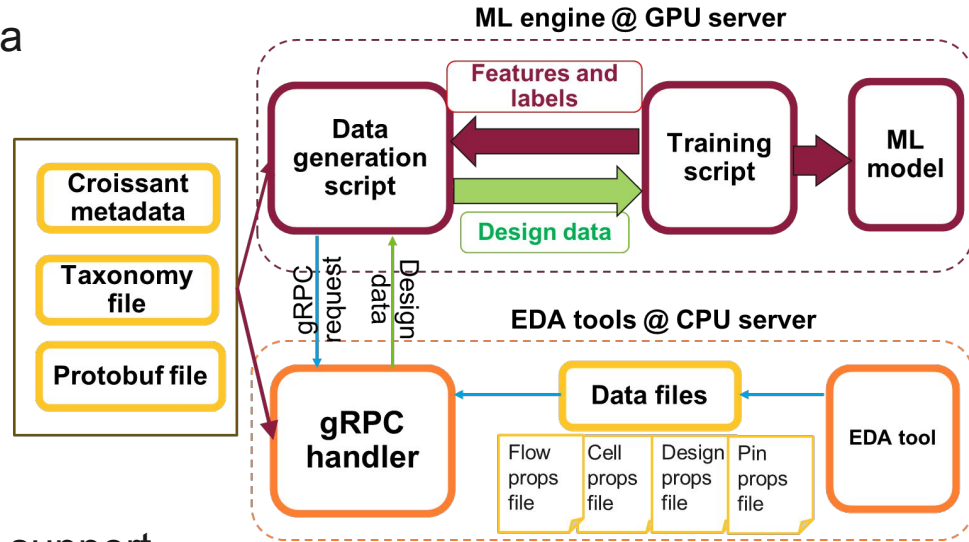
Pratik Shrestha et. al. "EDA-schema: Graph Datamodel Schema and Dataset for Design Automation," GLSVLSI 2024.

# Establishing standard formats for ML EDA

## Si2 ML EDA Schema Effort

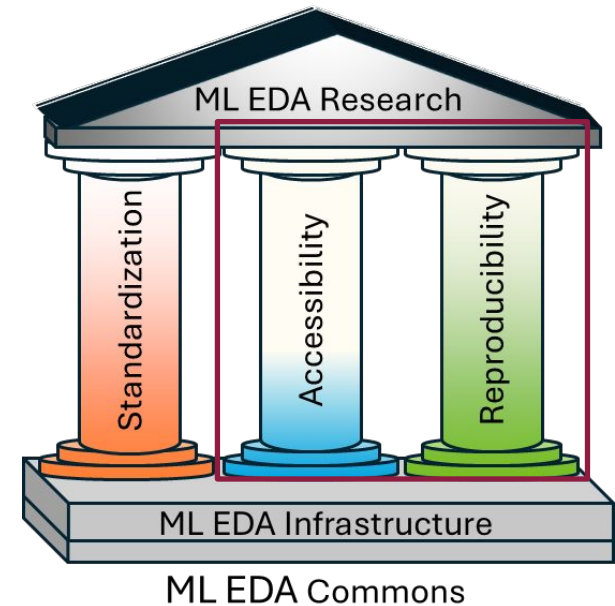
Components of the proposed ML EDA schema

- Taxonomy
  - Standard EDA taxonomy definition
  - Resource description framework
- Croissant Metadata
  - MLCommons proposed standard file format for describing datasets
- Communication across servers
  - gRPC and protobuf files
- Currently being developed to support the applications EDA schema and CircuitOps support



# Agenda

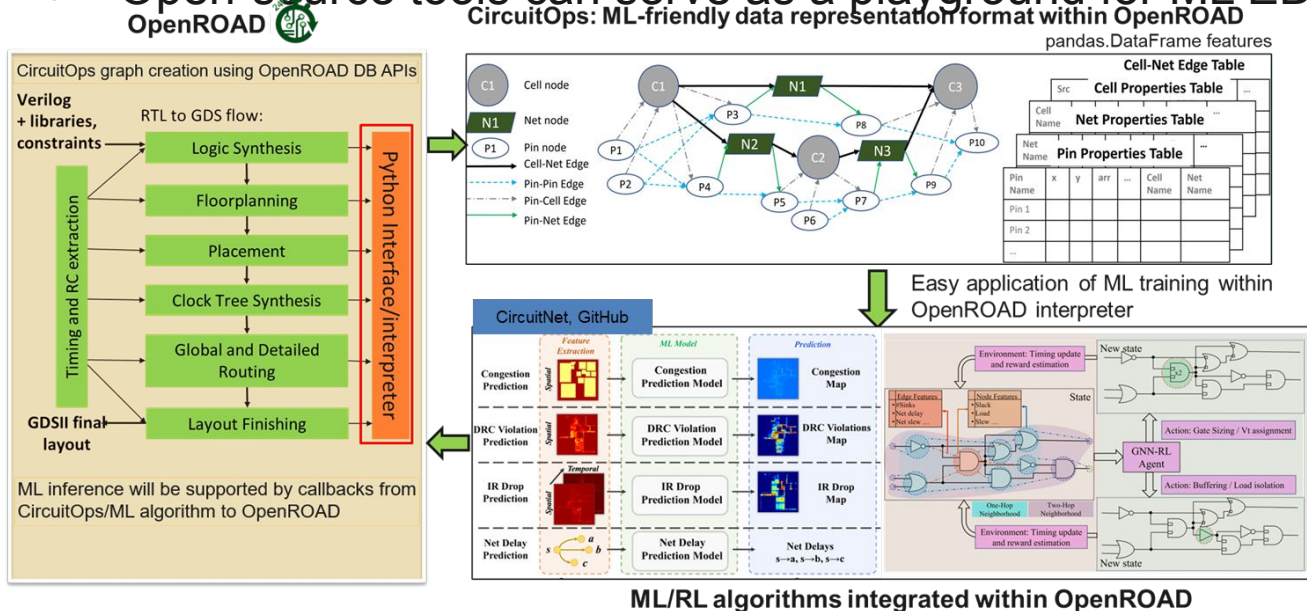
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# Efforts towards accessible ML EDA research

## Critical role of open-source for accessibility

- Lower the barriers to entry
- Proxies (PDKs, tools, IP, and design) are critical for accessibility
- Open-source tools can serve as a playground for ML EDA research



V. A. Chhabria et al., "OpenROAD and CircuitOps: Infrastructure for ML EDA Research and Education," VTS 2024.

# Efforts toward reproducible research

## Artifact evaluation at MLCAD 2024

- Artifact evaluation badges area available from IEEE and ACM to encourage reproducible research
- MLCAD 2024 tailored ACM badge awarding criteria for ML EDA research  
<https://github.com/ml-eda/artifact-evaluation>
- Criteria to be revised with inputs from IEEE CEDA DATC and ACM for MLCAD2025 to encourage:
  - Artifact availability with meaningful data
  - Use of proxies to demonstrate key ideas of papers for functionality
  - Hosting ML EDA research reproducibility challenges with incentives inspired by:  
<https://reproml.org/>

<https://www.acm.org/publications/policies/artifact-review-and-badging-current>

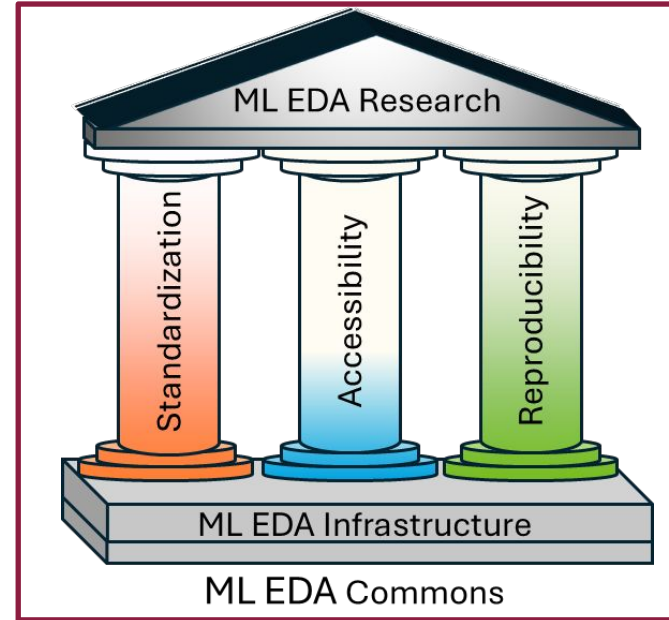


<https://ieeexplore.ieee.org/Xplorehelp/overview-of-ieee-xplore/about-content#reproducibility-badges>



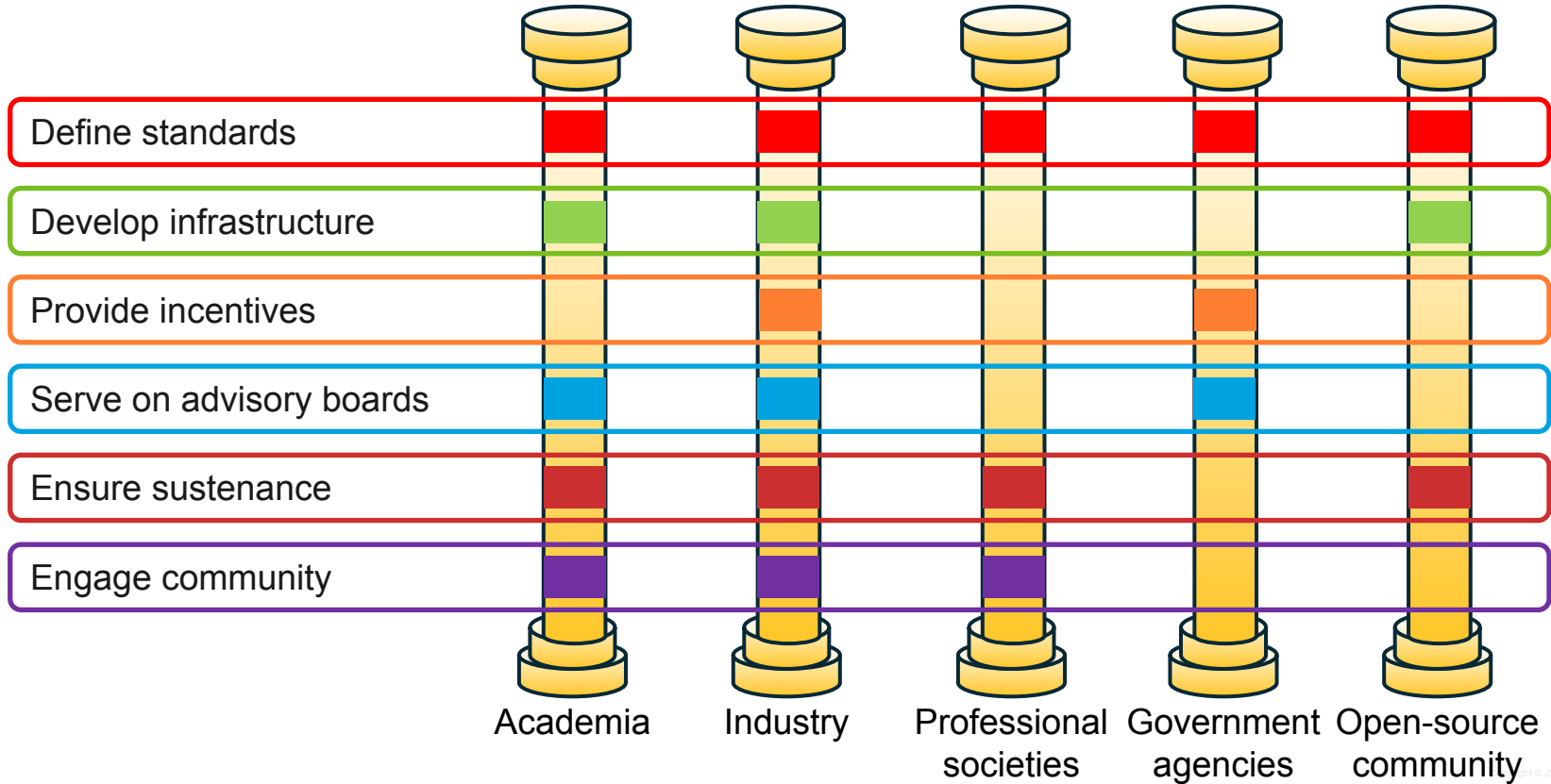
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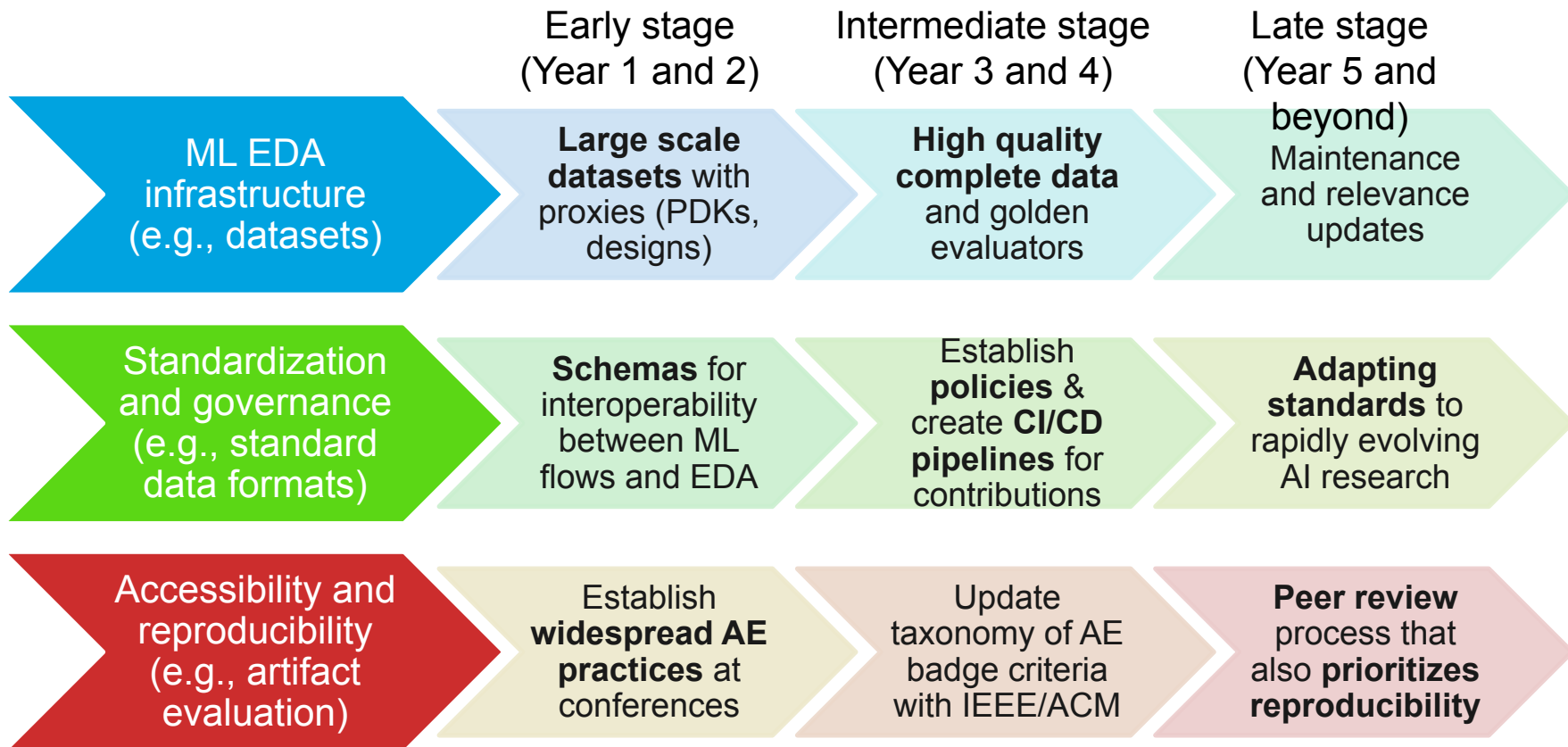


# Governance

## Key stakeholders and roles

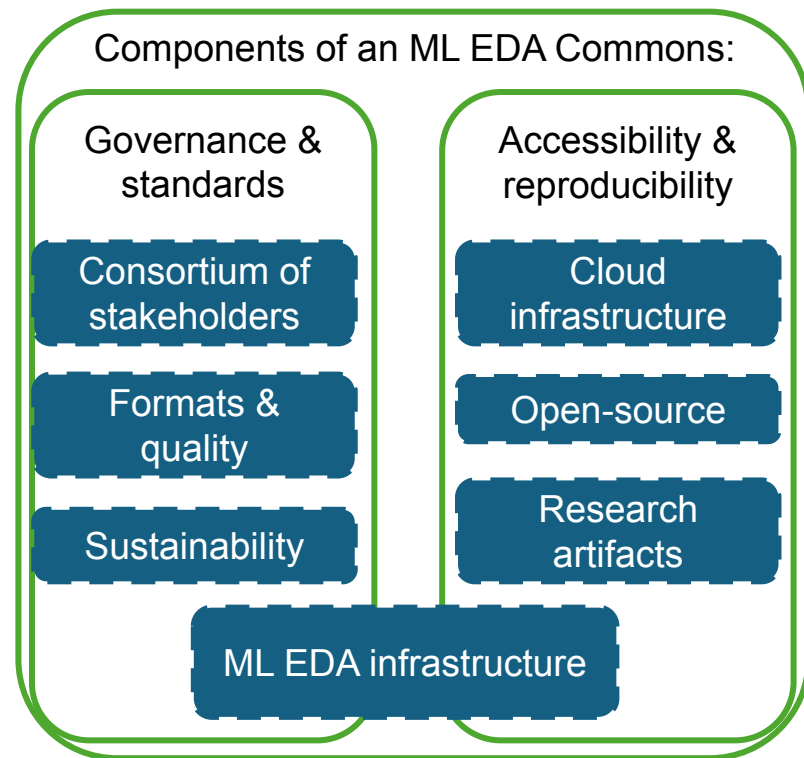


# Steps to establish the Commons



# Conclusion

- Aims to bridge the divide between the open culture of ML research and the closed EDA domain to accelerate innovation in ML EDA
- Components of an ML EDA Commons
  - ML EDA infrastructure
  - Governance and standards
  - Accessibility and reproducibility
- **Journey ahead requires sustained and expanded effort**
  - **Involvement from key stakeholders**
  - **Changing mindset of researchers, establishing incentives for researchers**



# Acknowledgements

- Ioannis Savidis (Drexel Univ.)
- Ivan Kissiov (Siemens)
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- Sayak Kundu (UCSD)
- Zhiang Wang (UCSD)
- Dooseok Yoon (UCSD)
- Vikram Gopalakrishnan (ASU)
- Bing-Yue Wu (ASU)
- Pratik Shrestha (Drexel Univ.)

- SLICE Team

# Backup Slides

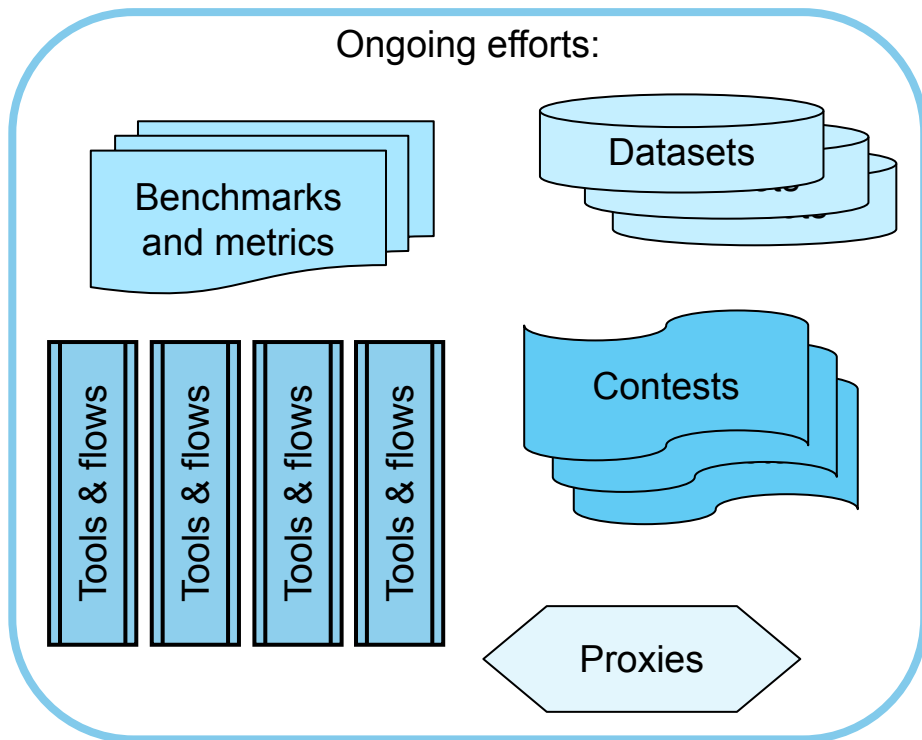
# Road to an ML EDA Commons

## Individual-driven efforts

Nascent

Mature

Ongoing efforts:



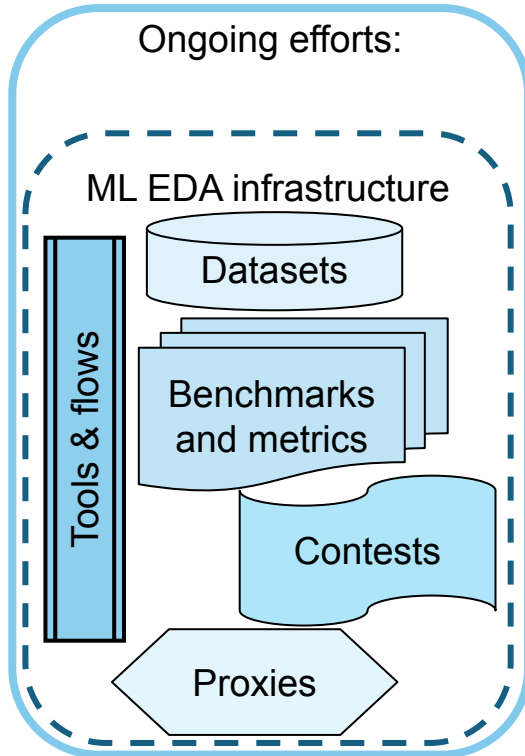
- Benchmarks
  - IWLS 2005, IBM power grid 2008 benchmarks, MacroPlacement etc.
- Datasets
  - VerilogEval, CVDP, FloorSet, BeGAN benchmarks etc.
- Tools and flows
  - OpenROAD, ORFS, yosys, etc.
- Contests
  - ICCAD, MLCAD, ISPD, ICLAD contests etc.
- Proxies
  - PDKs (ASAP7, NG45) and designs

# Road to an ML EDA Commons

## Need for unified efforts

Nascent

Mature

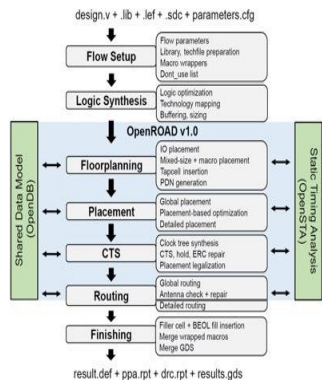


Unified ML EDA infrastructure is critical to

- Identify gaps in existing infrastructure (e.g., what parts of the flow, what can have large impact, gaps in design enablement)
- Establish interoperability via standardization
- Establish and maintain datasets and benchmarks with complete enablement for the entire physical design flow
- Drive contests and live leaderboards on those benchmarks and datasets
- Establish meaningful well-maintained proxies

# Establishing standard formats for ML EDA

## CircuitOps



IR (LPG)  
generated by  
interacting with  
OpenDB

CircuitOps

Operating on AI  
and  
parallel-friendly  
LPG

Dataset for  
task 1

AI Engine 1

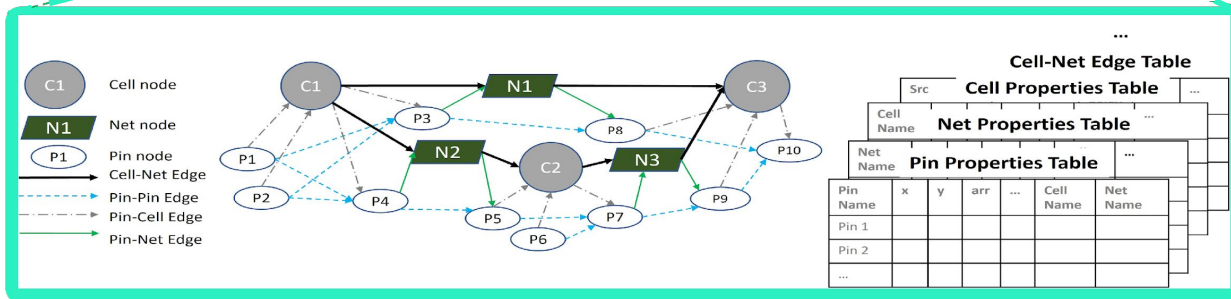
...

Dataset for  
task i

AI Engine i

...

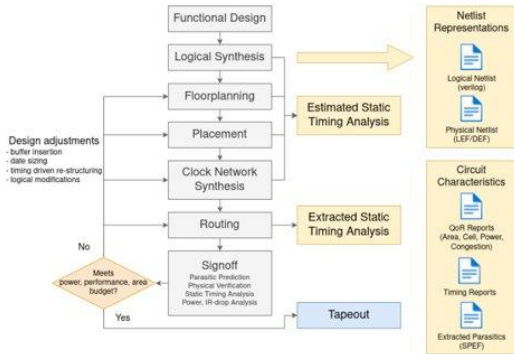
OpenROAD



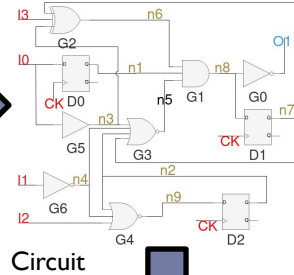
Liang et. al "CircuitOps: An ML Infrastructure Enabling Generative AI for VLSI Circuit Optimization," ICCAD 2023.

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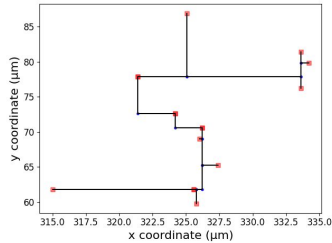
## EDA schema



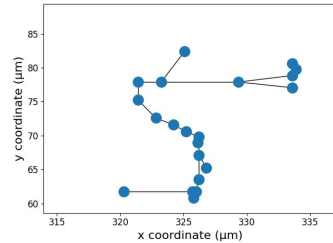
Physical design automation flow and corresponding netlist and circuit data formats



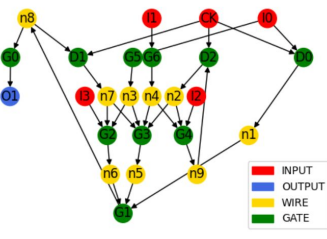
Circuit



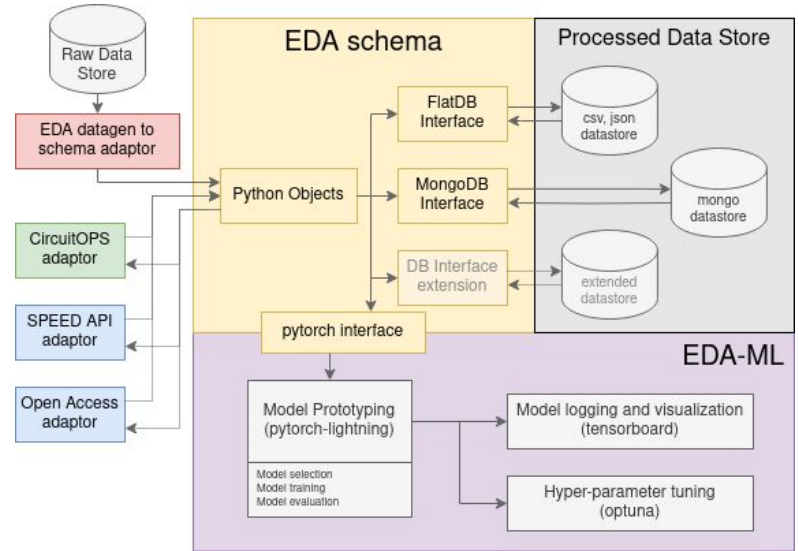
Interconnect Graph



Netlist Graph



Timing Path Graph



Prof. Ioannis Savidis  
[is338@drexel.edu](mailto:is338@drexel.edu) EDA-schema:  
 Graph Datamodel Schema and  
 Dataset for Design Automation