



ISPD'25 Contest: Performance-Driven Large Scale Global Routing

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NVIDIA

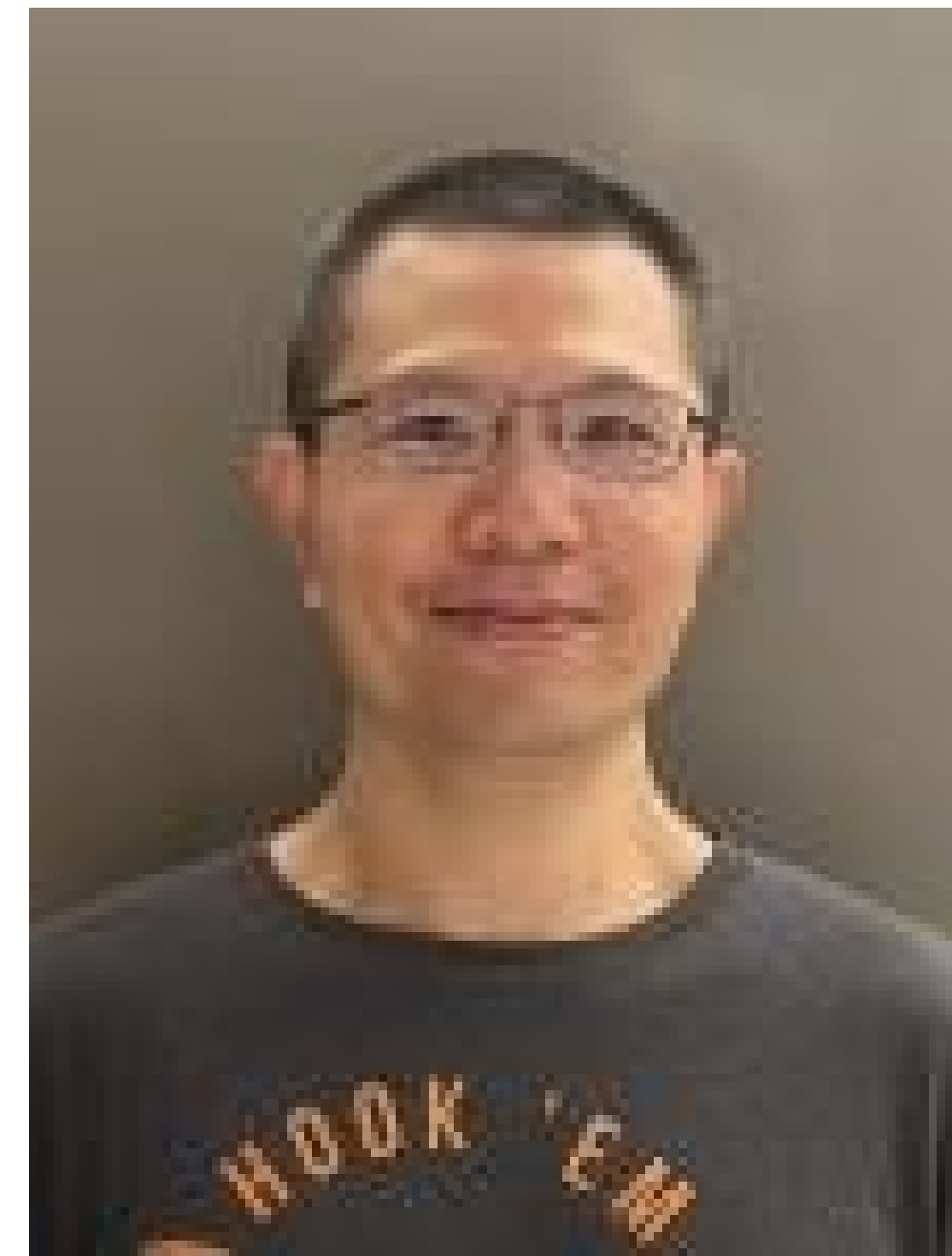
Contest Organizers



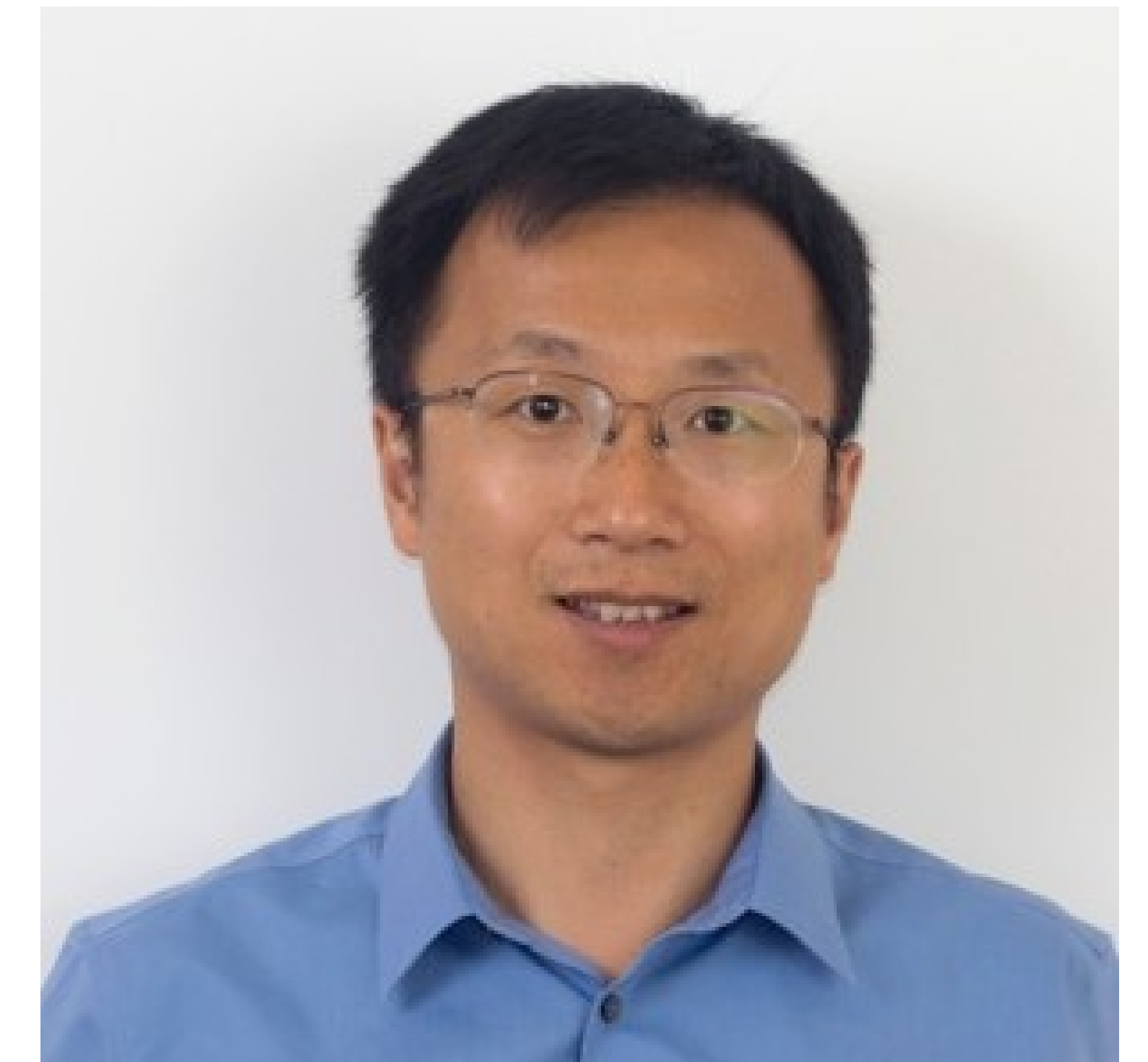
Rongjian Liang
Problem formulation & Evaluation



Anthony Agnesina
Benchmarks



Wen-Hao Liu
Problem formulation



Haoxing (Mark) Ren
High-level guidance

Motivations

- Global routing has significant impact on PPA
- ISPD'24 contest focuses on scalability, but its simplified evaluation metrics introduce **inaccuracies in performance modeling**
- **Performance-driven global routing** is required at various applications

Table 1: Application of global routing across various VLSI design stages.

Global Router Usage	Design Size	Runtime Requirement	Congestion Resolving Effort	Global Router Features	Goals
Logic Synthesis	20M–100M	fast	low	routability estimation, timing estimation	guide physical-friendly netlist
Physical Planning	20M–100M	fast	low	routability estimation, timing estimation	partition design, I/O planning, timing budgeting
Placement	1M–5M	fast	low	routability estimation, timing estimation	guide routability- and timing-aware placement
Optimization	1M–5M	medium	medium	timing-driven topology, buffering-friendly topology, incremental update	guide routability-aware optimization
Guide Detailed Routing	1M–5M	long	high	timing-driven topology, power-driven	guide high-quality DR result

Problem Formulation

- Input
 - Industry files:
 - LEF, LIB, DEF, SDC
 - Simplified files:
 - A 3D routing space defined using a GCell grid graph (.cap file)
 - Net information (.net file)

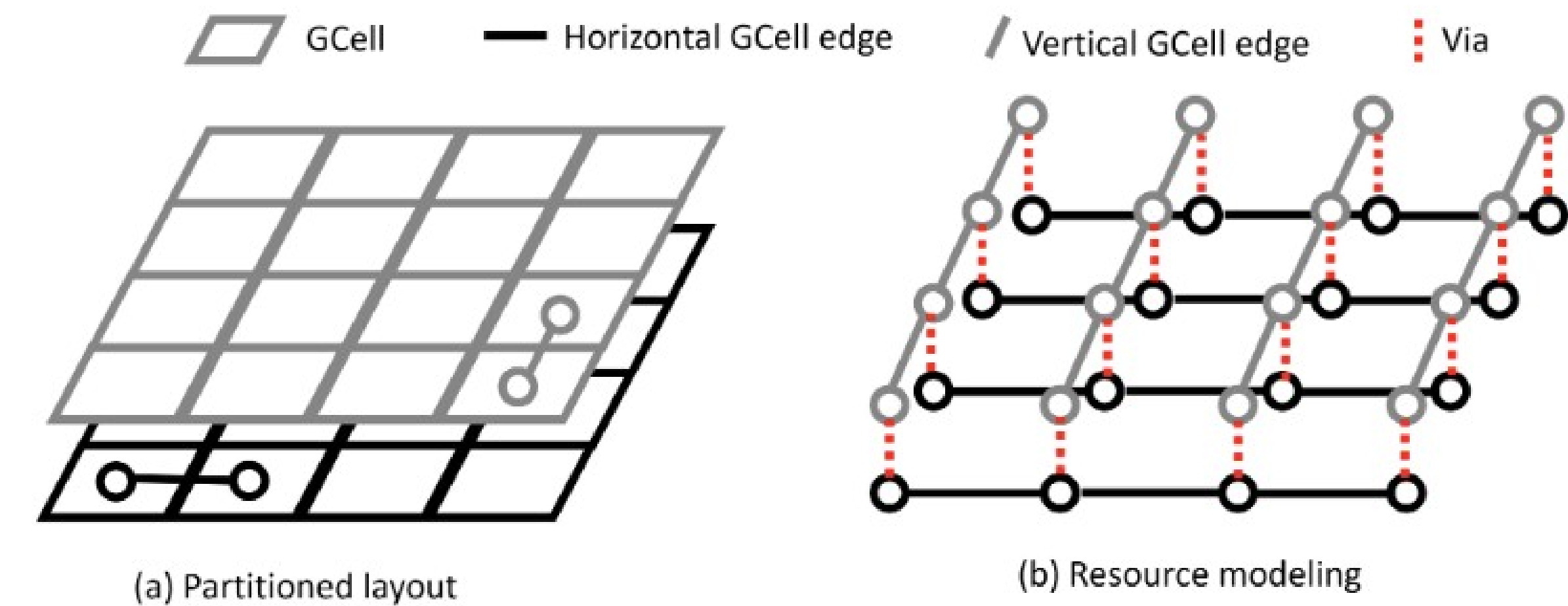


Figure 1: Illustration of a GCell grid graph.

- Output
 - Routing guide on the Gcell grid graph
- Objectives:
 - A concrete path for each net
 - Optimize timing
 - Minimize power
 - Minimize overflow

Net name

Net0

(

x_l y_l z_1 x_h y_h z_2

270 13230 M4 270 13230 M5

270 13230 M5 270 13230 M6

270 13230 M4 810 13230 M4

810 13230 M4 810 13230 M3

810 13230 M2 1350 13230 M2

1350 13230 M2 1350 13230 M1

)

Benchmark Suit Characteristics

- The benchmarks derived from [1]
- The benchmarks are synthesized using the nangate45nm technology and cell libraries
- The benchmarks are divided into two sets
 - One placed layout from each design for testing (public)
 - Another placed layout from each design for final ranking (blind)
- Simplifications for the contest
 - Power and ground nets are removed
 - Clock tree routing is not considered

[1] C.-K. Cheng, A. B. Kahng, S. Kundu, Y. Wang and Z. Wang, "Assessment of Reinforcement Learning for Macro Placement", Proc. ISPD, 2023

Benchmark Suit Characteristics (Cont.)

Testcase (visible)	w1	w2	w3	w4	N_{endpoint}	{N_net}	GCell graph dimensions
ariane	-10	-100	300	3e-7	20218	123900	10x761x761
bsg	-10	-100	25	4e-8	214821	736883	10x1384x1384
NVDLA	-0.05	-0.5	25	1.5e-7	45925	199481	10x1120x1120
mempool_tile	-1	-10	300	7e-7	13350	136120	10x428x428
mempool_group	-1	-10	20	3e-8	347869	3274611	10x1611x1610
mempool_cluster	-1	-10	0.3	5e-9	1082397	12047279	10x3175x3175

Testcase (blind)	w1	w2	w3	w4	N_{endpoint}	{N_net}	GCell graph dimensions
ariane	-0.2	-2	100	0.0000004	20218	105924	10x646x646
bsg	-0.1	-1	50	0.00000002	214915	768239	10x1384x1384
NVDLA	-0.01	-0.1	100	0.0000001	45925	157744	10x1120x1120
mempool_tile	-3	-30	100	0.000001	13350	135814	10x386x386
mempool_group	-0.5	-5	3	0.00000004	347869	3218496	10x1611x1610
mempool_cluster	-0.4	-4	2	0.00000001	1082397	12168735	10x3719x3719

Evaluation Metric

$$\textit{scaled_score} = \textit{original_score} \cdot (1 + \textit{runtime_factor} + \textit{np})$$

$$\begin{aligned} \textit{original_score} = & w_1 * (WNS - WNS_{ref}) \\ & + w_2 * \frac{TNS - TNS_{ref}}{N_{endpoint}} \\ & + w_3 * (TotalPower - TotalPower_{ref}) \\ & + w_4 * OverflowScore \end{aligned}$$

$$\textit{OverflowCost}(c, d, l) = \textit{OFWeight}[l] \cdot e^{s(d-c)} \quad s = \begin{cases} 0.5 & \text{if } c > 0, \\ 1.5 & \text{if } c = 0, \end{cases}$$

$$T = 0.02 \cdot \log_2 \left(\frac{\textit{GRouter_Wall_Time}}{\textit{Median_Wall_Time}} \right)$$

$$\textit{runtime_factor} = \min(0.2, \max(-0.2, T))$$

OpenROAD-Based Timing Evaluation

- SDC: timing constraints
- LIB: NLDM timing models used in NanGate45
- Global routing solution: RC extraction

OpenROAD-Based Power Evaluation

- LIB: power models
- Activity: probabilistic activity propagation
- Components: leakage, internal and switching

Ranking

- Rank each team for each benchmark. Smaller scores -> better ranking
- Prune out the worst ranking number, and then average the remaining rankings for each team
- The team with the smallest averaged ranking number wins the contest

Evaluation Platform

- RAM: 200 GB
- CPU Cores: 8 cores
- GPUs: 1 NVIDIA GPU

Participation Statistics

- 46 initial registrations
 - Asia
 - Europe
 - America
 - Others (unknown affiliations)
- 12 final submissions

Prizes

- 1st place: \$1000 + one NVIDIA GPU of similar value
- 2nd place: \$500 + one NVIDIA GPU of similar value
- 3rd place: \$250 + one NVIDIA GPU of similar value

Contest Results

	ariane	bsg	NVDLA	MP_tile	MP_group	MP_cluster	Avg_ranking
A	4	7	3	2	2	4	3
B	3	1	6	6	1	5	3.2
C	1	5	2	4	10	6	3.6
D	7	2	4	5	5	3	3.8
E	9	3	5	8	4	1	4.2

Results on Mempool_cluster

Results on mempool_cluster (visible)

	runtime	WL	via	congestion	tns	wns	internal	switch
A	414	1.25e9	3.58e8	2.43e8	-42564	-0.22	12.1	11.0
B	1038	1.24e9	3.17e8	2.14e8	-50372	-0.29	12.2	11.1
C	672	1.24e9	4.65e8	3.35e8	-39516	-0.20	12.2	10.7

Results on mempool_cluster (blind)

	runtime	WL	via	congestion	tns	wns	internal	switch
A	468	1.15e9	3.47e8	2.37e8	-59713	-0.27	12.0	10.4
B	1018	1.14e9	3.03e8	1.92e8	-62460	-0.31	12.0	10.5
C	726	1.14e9	4.20e8	2.90e8	-59534	-0.28	12.0	10.1

Team A: fast runtime, balanced metrics

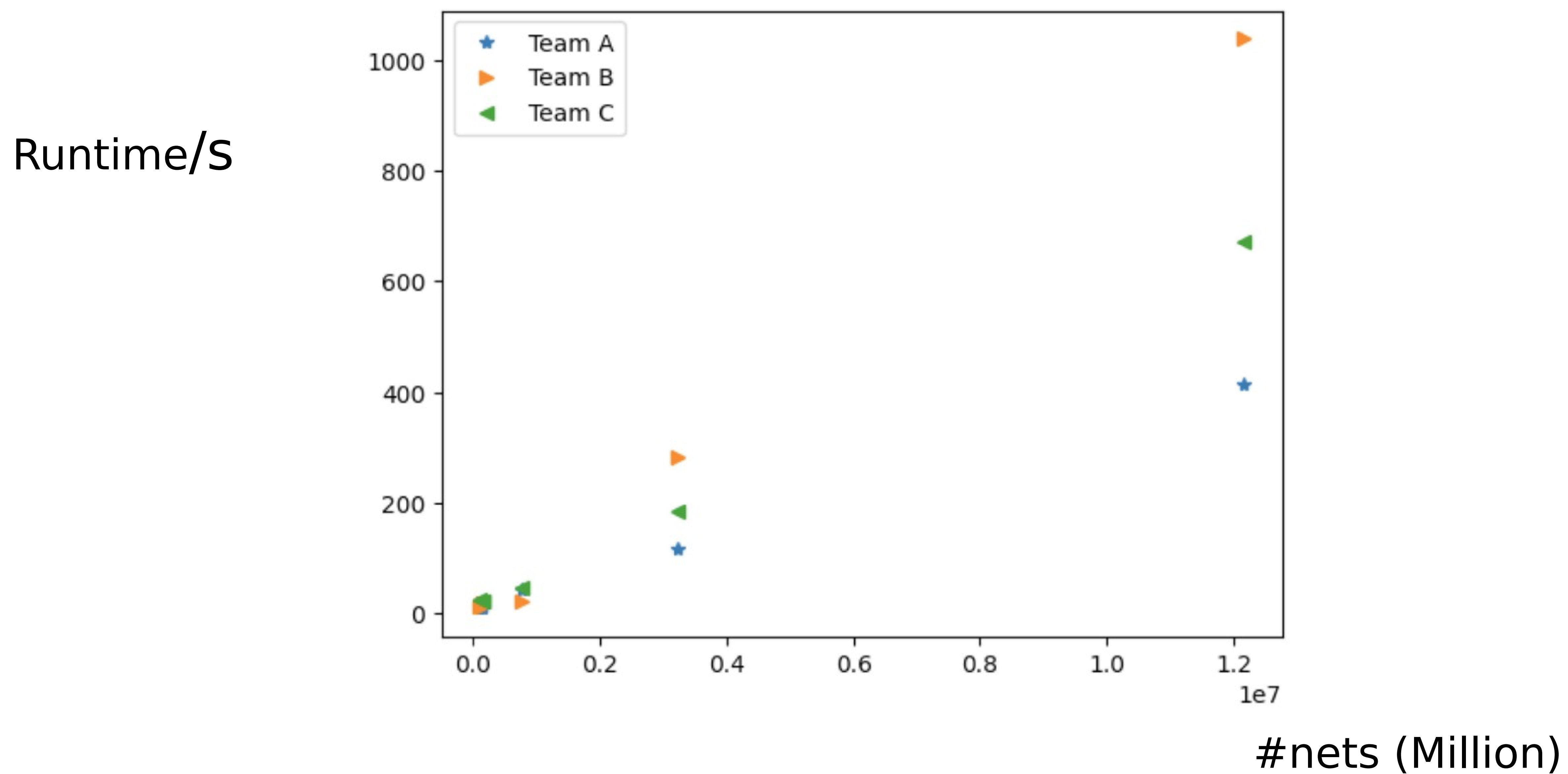
Team B: longer runtime, reduced congestion, worse timing

Team C: congested, more via counts, good timing and power

Results Analysis - GPU Usage

Team	Use GPU?
A	Y
B	Y
C	Y

Results Analysis - Runtime Scalability (Main Track)



Runtime performance: Team A > Team C > Team B

Acknowledgment

- David Chinnery - Siemens Digital
- Gracieli Posser - Cadence
- Matt Liberty - OpenROAD
- Hsin-Tzu Chang - National Taiwan University
- **All the contestants for your participation and feedback!**



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HONORABLE MENTION

GODW Router

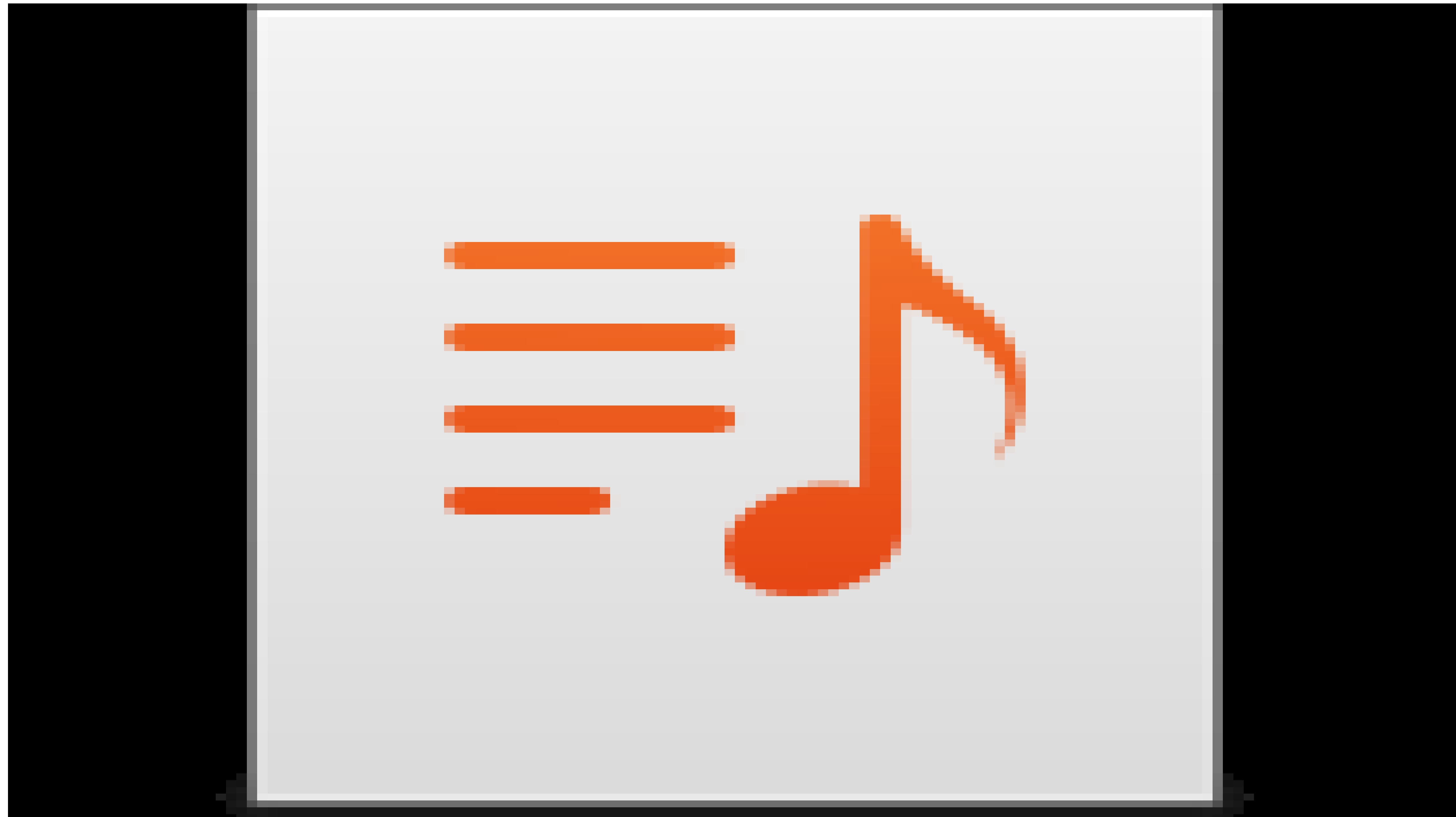
Jinghui Zhou, Xinglin Zheng, Hao Gu, Youwen Wang,
Ziran Zhu, Jun Yang
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GODW Router





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HONORABLE MENTION

LX Router

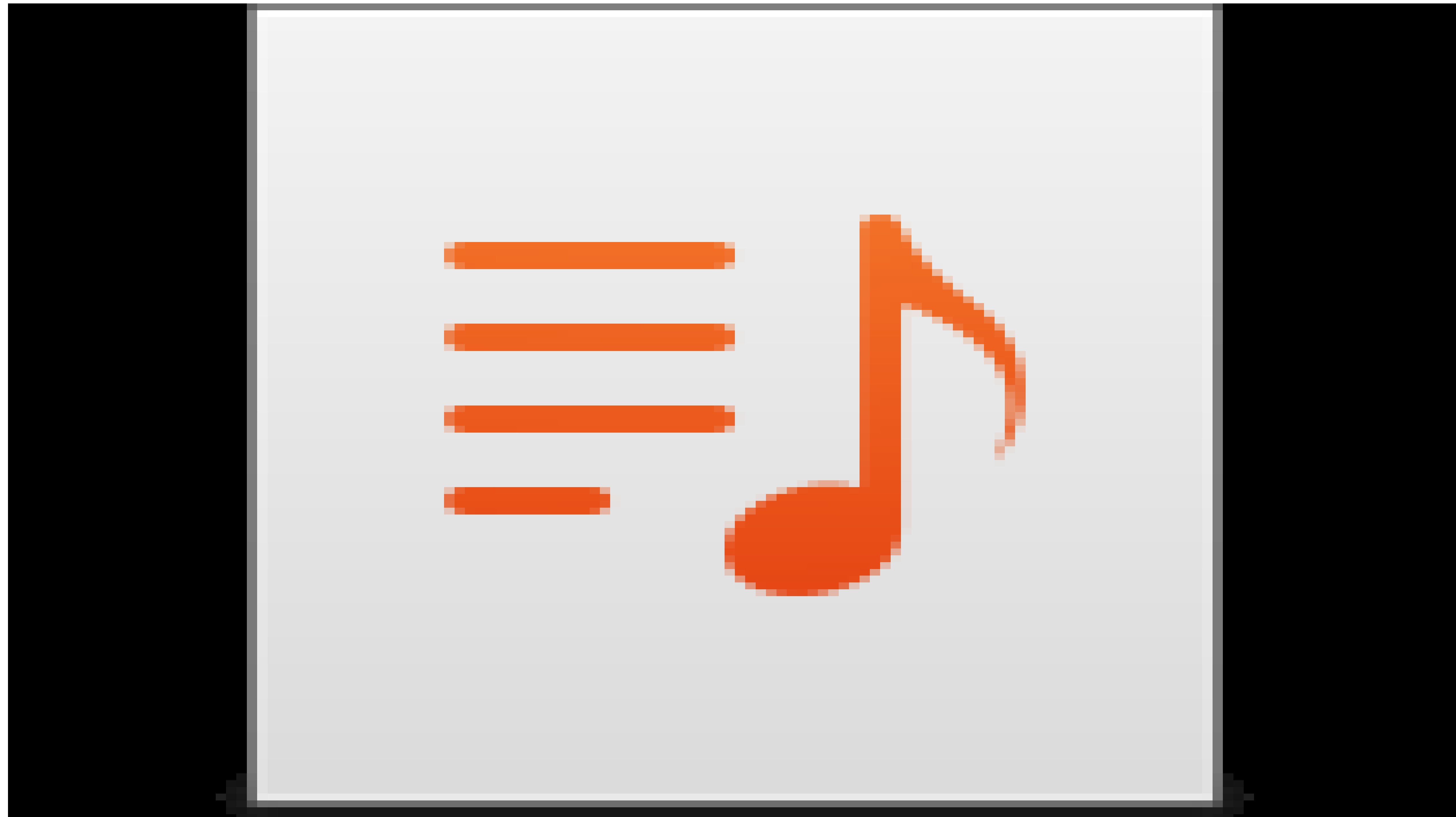
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LX Router





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THIRD PLACE

It's MyRoute!!!!

Chuyu Wang, Zecheng Xu, Boxiang Song, Zhiang Wang,
Keren Zhu

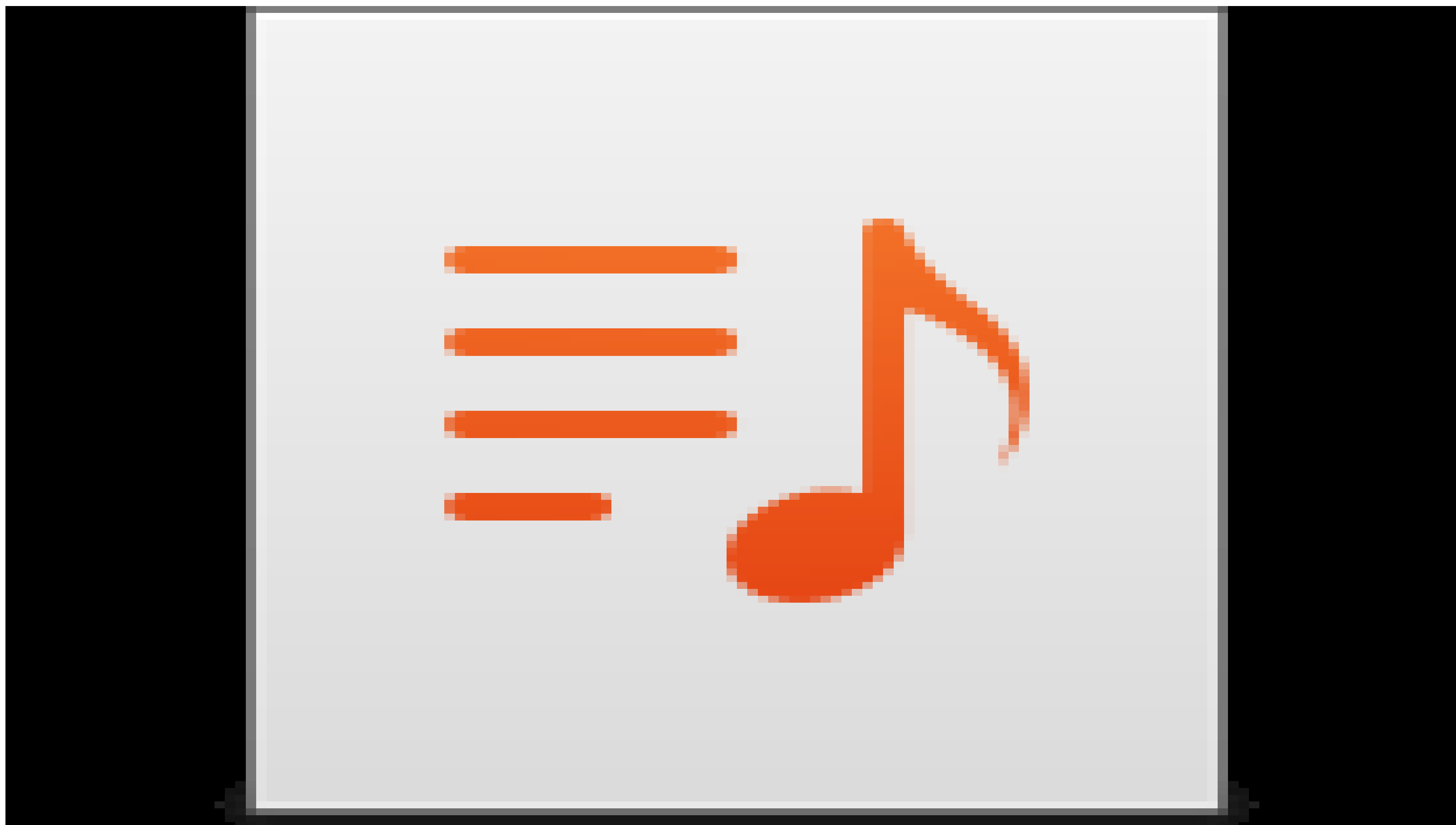
Fudan University, Wuhan University,
University of California San Diego

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It's MyRoute!!!!





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SECOND PLACE

RL-Route

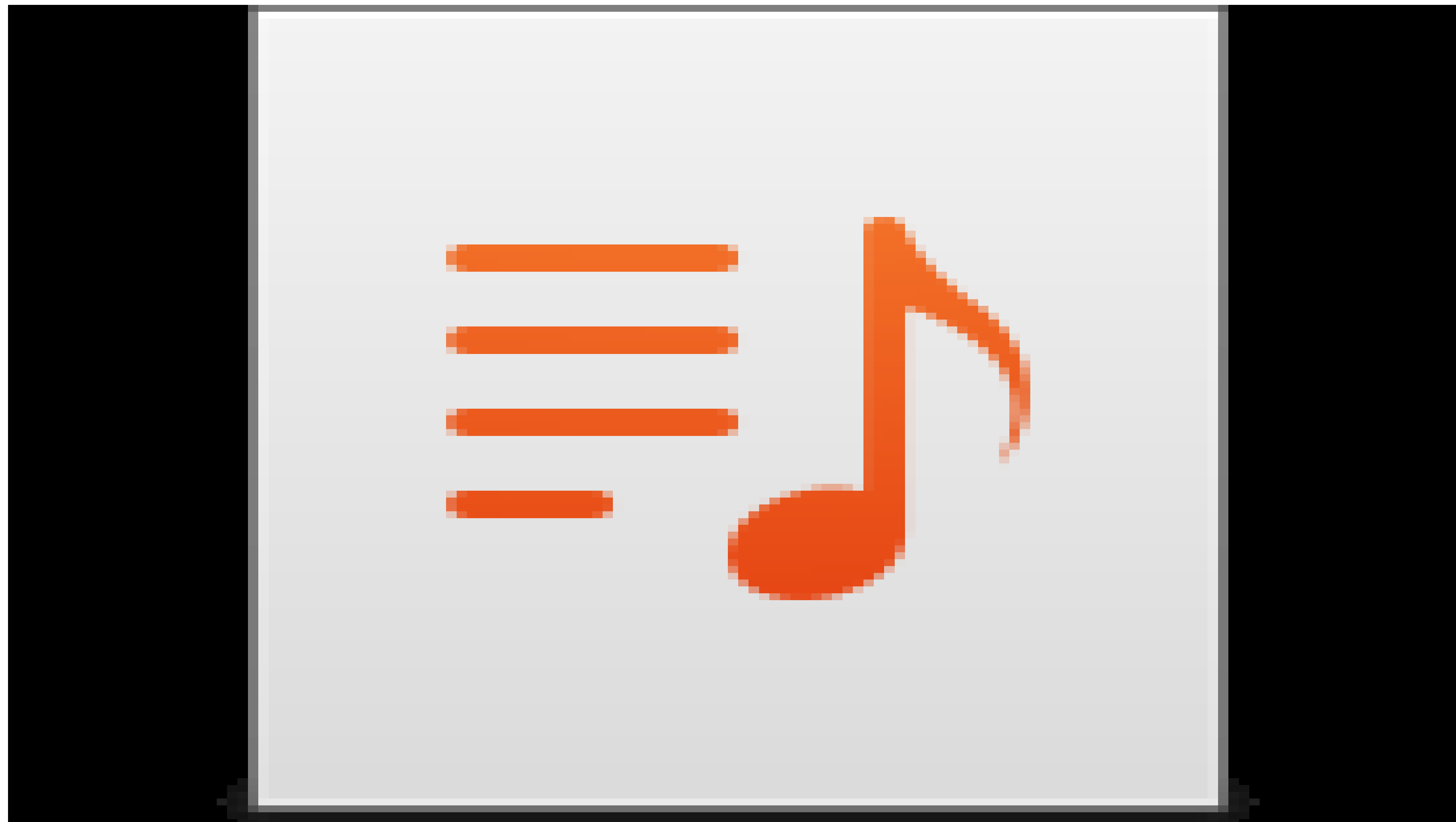
Liang Xiao, Qinkai Duan, Qinkai Duan, Leilei Jin,
Jinwei Liu, Tsung-Yi Ho, Evangeline F.Y. Young
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University of Science and Technology, Hong Kong
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RL-Route





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FIRST PLACE
Team Hippo

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Peking University

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Stephan Held
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ISPD 2025

Rongjian Liang, Wen-Hao Liu,
Anthony Agnesina, Haoxing Ren
NVIDIA

Team Hippo



Last Notes

- Thanks again to all the contestants for their participation and for their patience in enduring the delays and mistakes throughout the contest...
- We hope this marks the beginning, not the end, of their journey in exploring performance-driven global routing. We will be releasing the blind testcases, along with a larger testcase containing approximately 50 million cells for further study



Thank you! ☐