Powering Innovation That Drives Human Advancement

Next Generation Power Integrity Concepts and Applications for Physical Design

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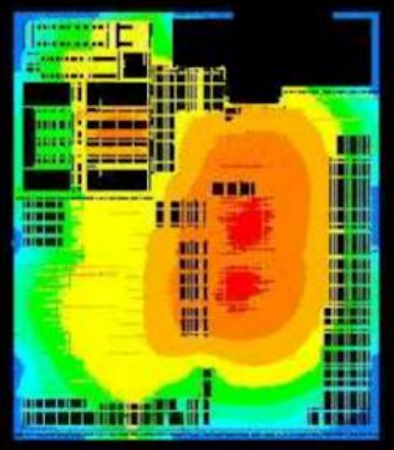
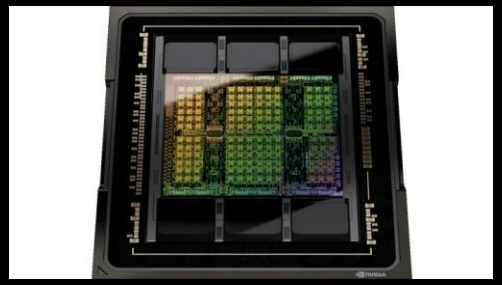
Ansys

Power Integrity

- Billions of instances/nodes
- Use of HBMs, GPUs, 3D-IC becoming the norm
- Power Integrity already 1st order problem





r/vlsi_enthusiast • 2 yr. ago
Freddy_lang

Ever Heard of IR Drop in VLSI Design? Let's Explore!

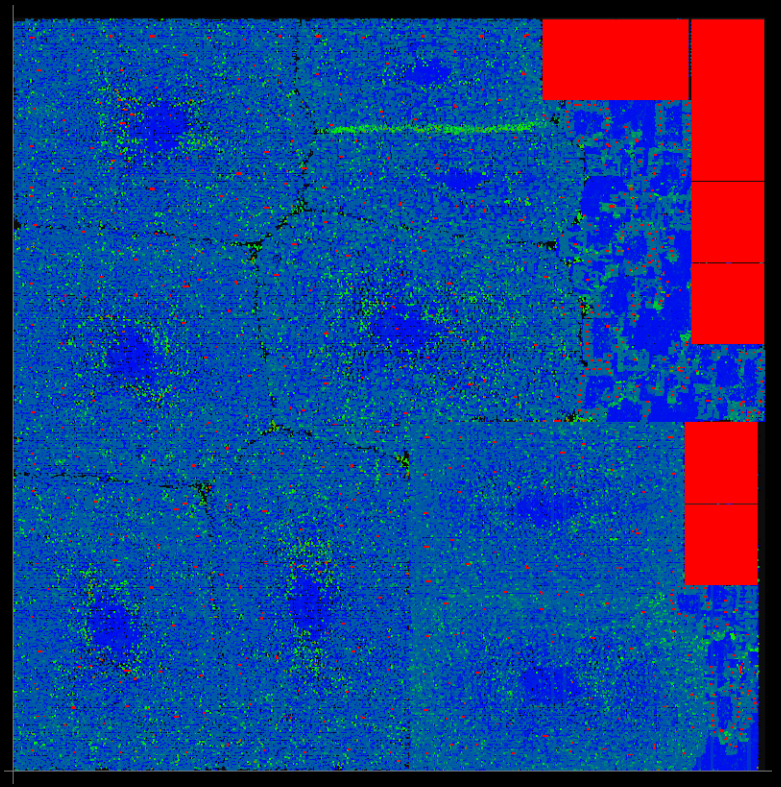
1.Timing Violations: The voltage drop caused by IR drop can lead to variations in gate delays, disrupting the precise timing requirements of various paths within the circuit.
2.Functional Errors: Voltage drops can cause logic behavior deviations, resulting in functional errors and unpredictable outcomes.
3.Reduced Noise Margins: Voltage fluctuations might reduce the distinction between logical '1' and '0,' making circuits susceptible to noise-induced errors.
4.Electromigration: As current density escalates in wires, it can lead to electromigration – a process where metal atoms migrate, potentially causing wire thinning and eventual failure.
5.Thermal Effects: The resistance-induced current generates heat. Poor heat dissipation can lead to localized overheating, affecting both reliability and performance.

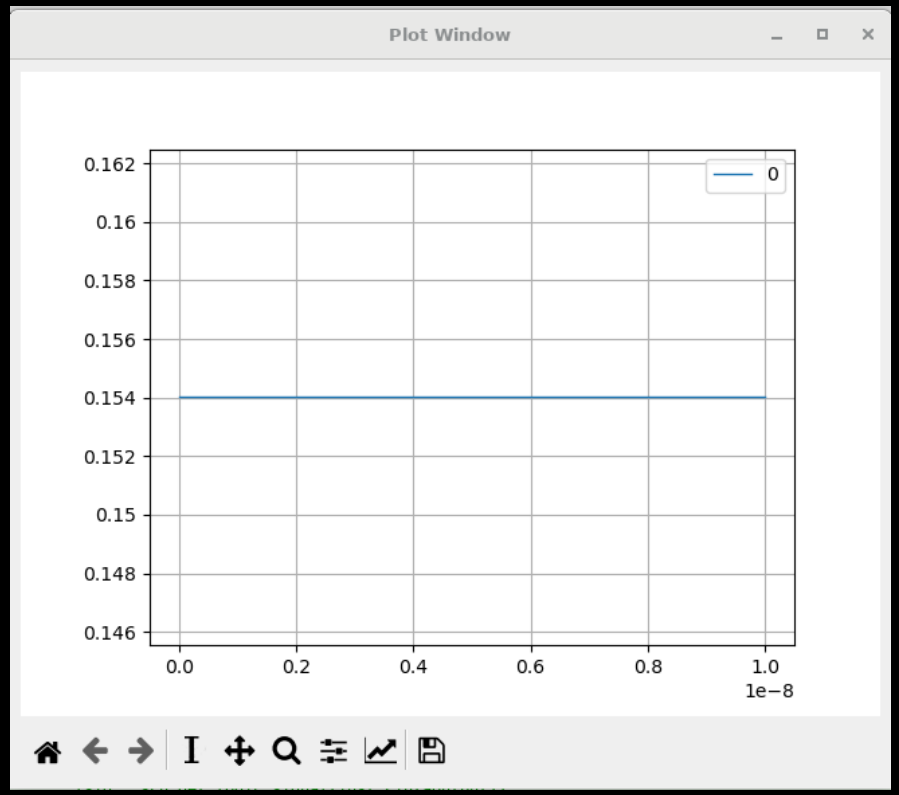
State of Art PI Sign-Off is RedHawk-SC

- Analyzing the IR-drop
- Vectored flow: Switching gates known (FSDB, VCD), input and states known
- Vectorless flow: Input vectors generated realistically.
  - Example: In each clock cycle, ~10% of gates can switch (power constraint)

- State of the art tool is RedHawk-SC
- Handles all sizes of designs, blocks, 3D-Ics
- Linearly Scaling up to 1000s CPUs
- Still taking long time to perform conventional PI Sign-off

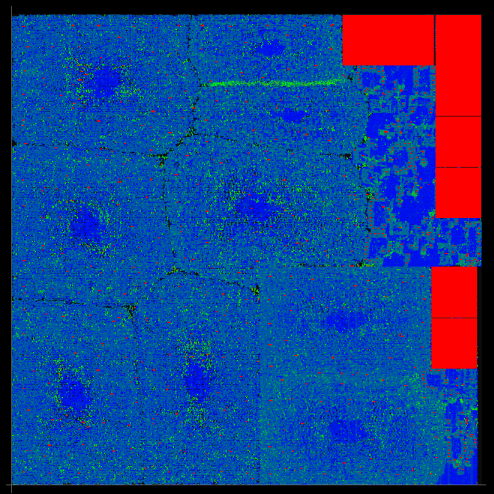
A bit of History / Voltage Drop Evolution

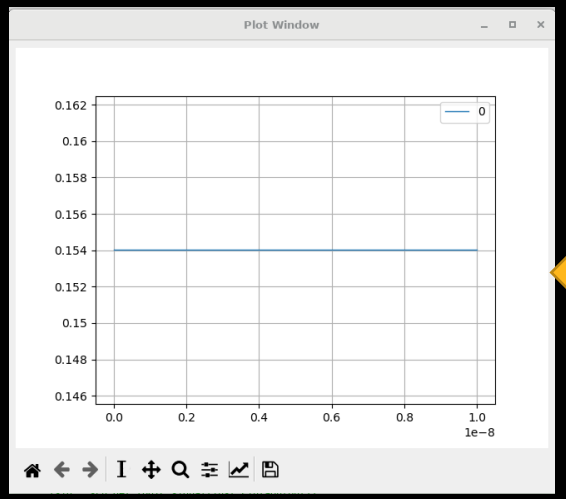




Analysis Type	Temporal	Local/spatial
Static	averaged activity	averaged activity

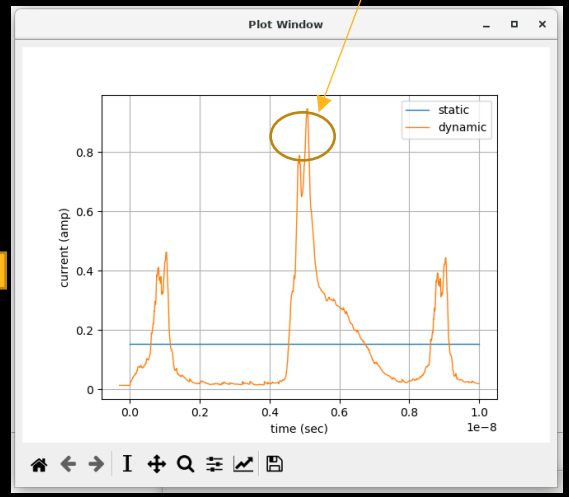
Voltage Drop Evolution





Time avg

Escapes in Static



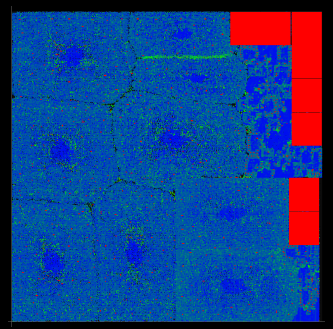
Analysis Type	Temporal	Local/spatial
Static	averaged activity	averaged activity

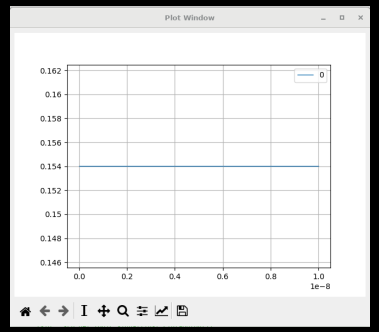
Approaches to mitigate

- Peak current based Static

Issue:-
Unrealistic drop numbers

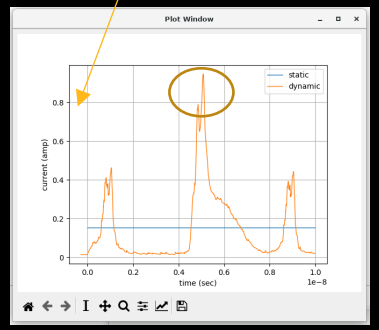
Voltage Drop Evolution





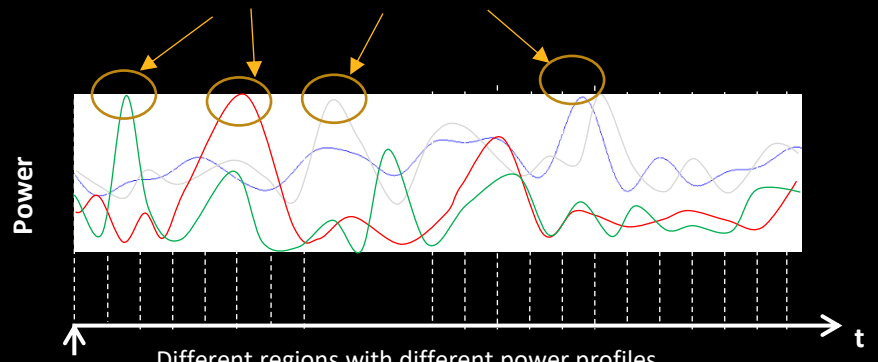
Time avg

Escapes in Static



Spatial avg

Potential escapes in transient

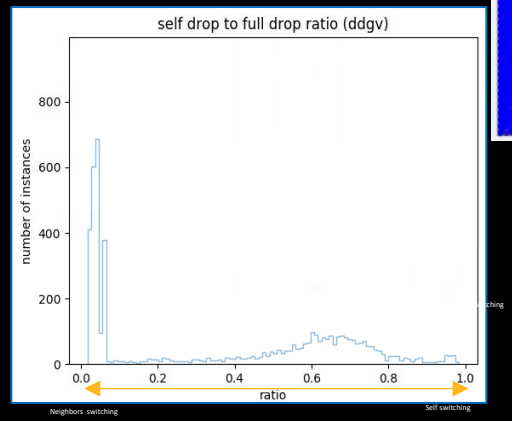


Different regions with different power profiles

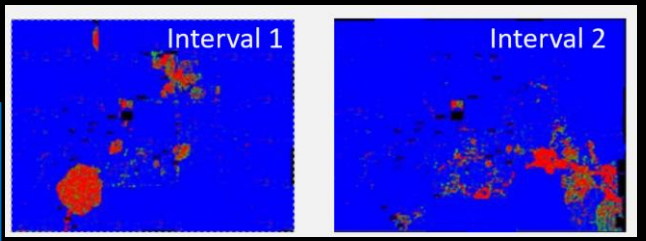
Analysis Type	Temporal	Local/spatial
Static	averaged activity	averaged activity

Approaches to mitigate

- Higher power/activity
- Annotate peak activity per region
- Multiple transient runs
  - LPV, NPV, FSDB
- Multi cycle at the cost of long runtimes,
  - Low noise coverage

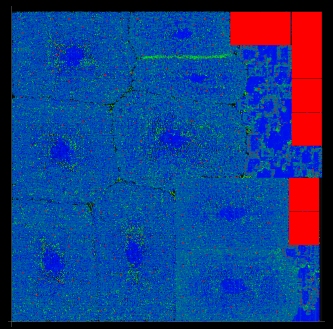


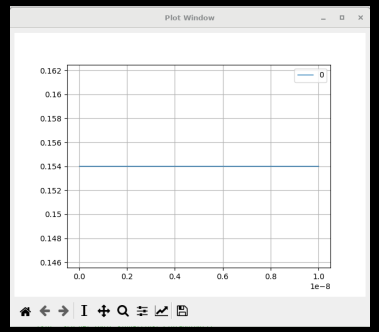
Contribution to drop



Different regions highlighted with different runs

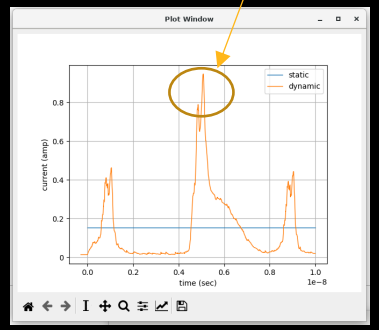
Voltage drop evolution





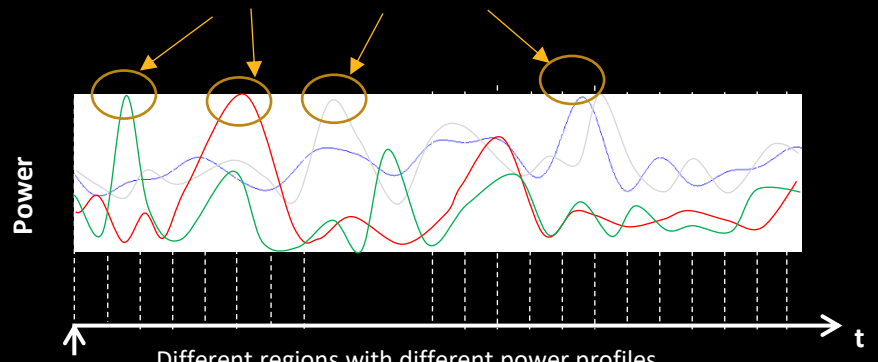
Time avg

Escapes in Static



Spatial avg

Potential escapes in transient



Different regions with different power profiles

Analysis Type	Temporal	Local/spatial
Static	averaged activity	averaged activity
Transient	Peak activity	averaged activity

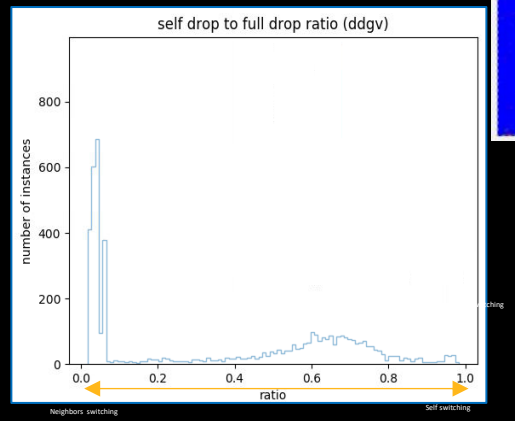
Approaches to mitigate

- Higher power/activity

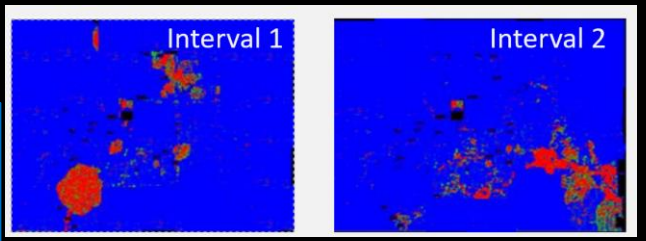
Issue:- unrealistic Drop numbers

- Multiple transient runs
  - LPV, NPV, FSDBs
- Multi cycle

Issues:- Long runtimes, low noise coverage

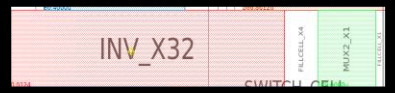


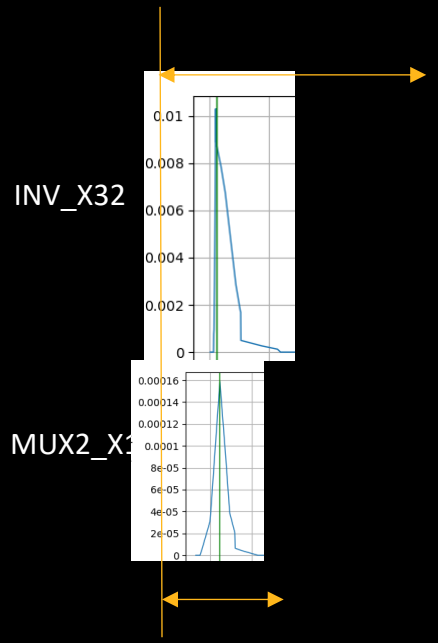
Contribution to drop



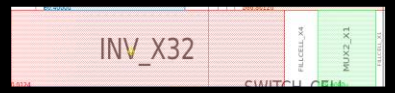
Different regions highlighted with different runs

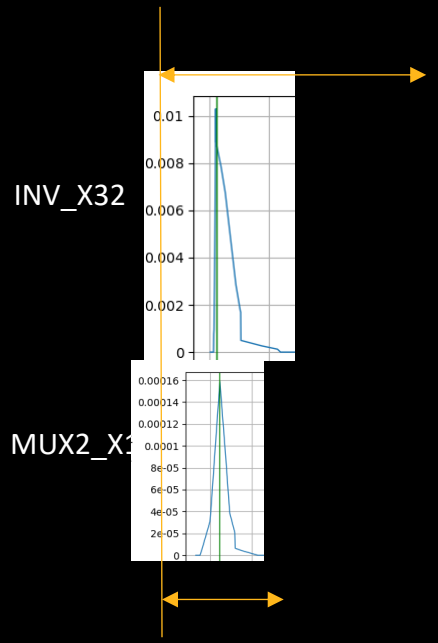
Timing alignment





Timing alignment





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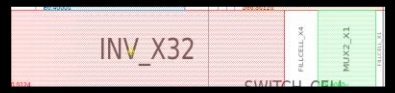

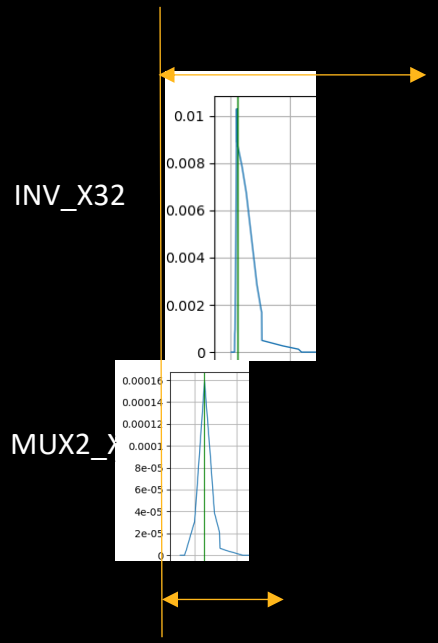

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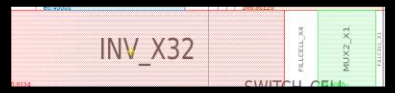

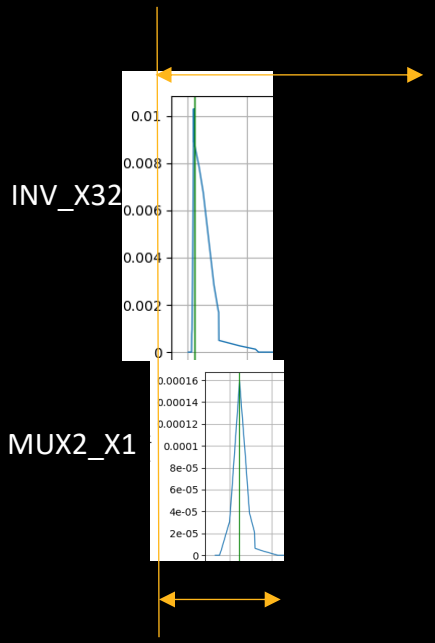

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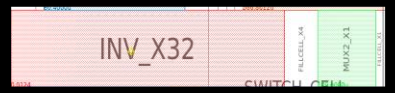
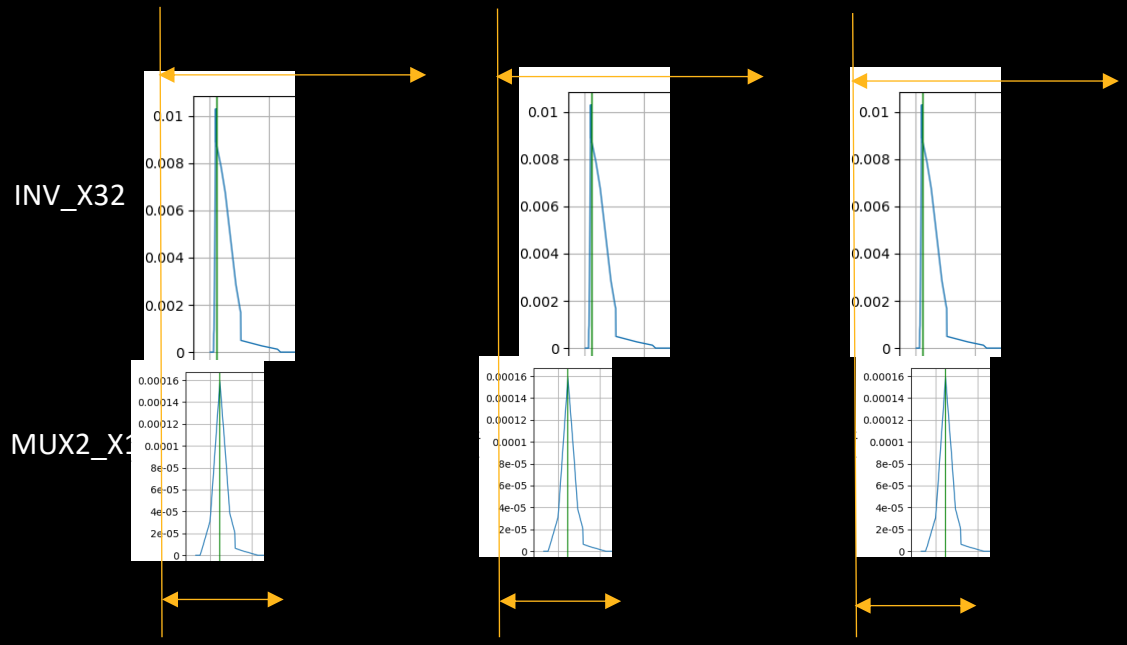
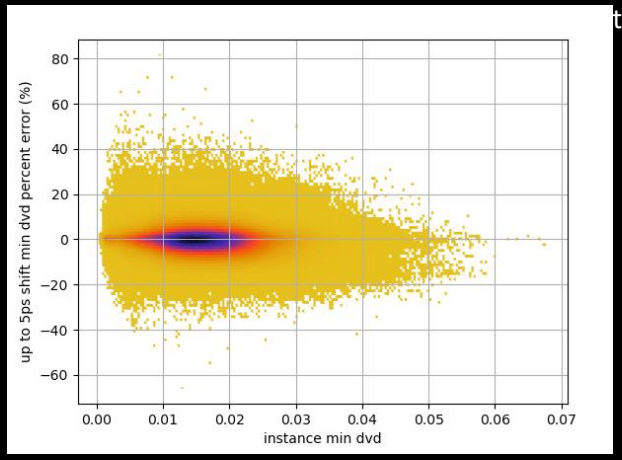


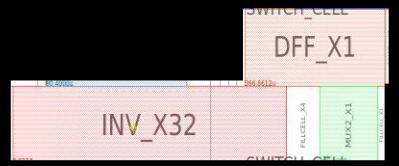


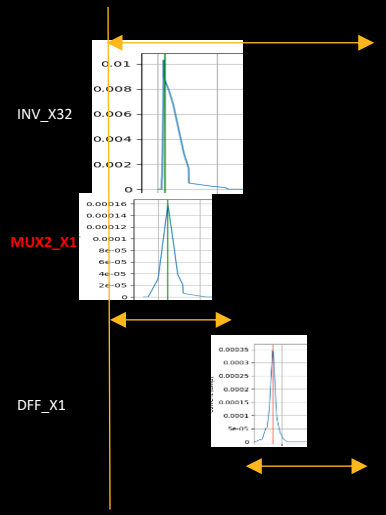
ts by +-30%

- Small changes in the event times can change voltage drop numbers



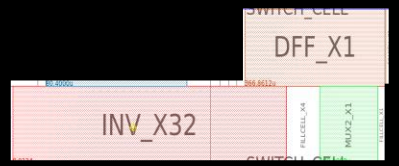
Aggressor Coverage issue

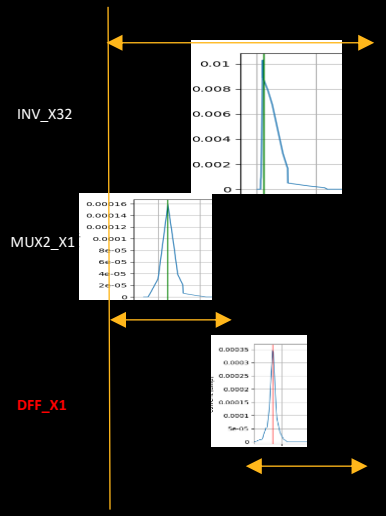




Cycle 1

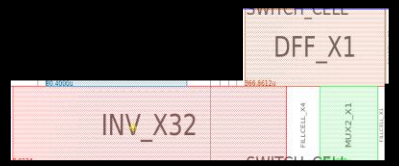
Aggressor Coverage issue

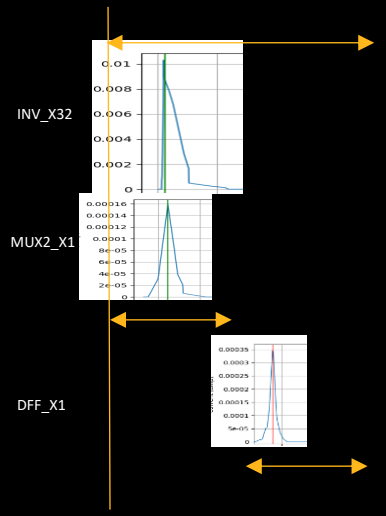


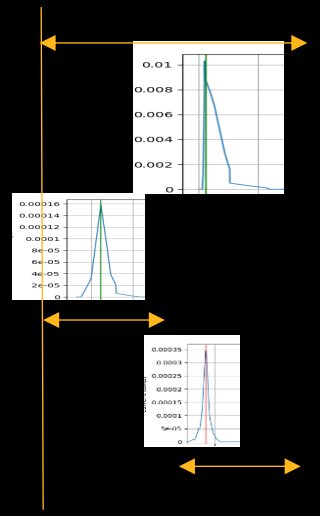


Cycle 2

Aggressor Coverage issue







Transient

Cycle 1

Inst 1

Cycle 2

Inst 2

Transient:-

- Solving each cycle is sequential
- Each Cycle will have 100s of time steps
  - Each timestep will involve solving the complete PG network
  - This can really take hours depending on the size of the design

Limitations of Transient Simulation for Voltage Drop

- Coverage is limited for local switching noise
  - Impossible number of cycles to get the needed coverage
- Runtime is high
  - Timestep needs to be small (< 5ps) and run most be done long duration
- Results are very sensitive to inputs
  - Time step, peak noise alignment
- Transient should do for what it does well
  - Chip + Package, upper metal layer effects, dynamic EM, specific vectors
  - Impact on common routing resources of many instances switching
  - ROM creation – needs a transient ScenarioView that meets target power

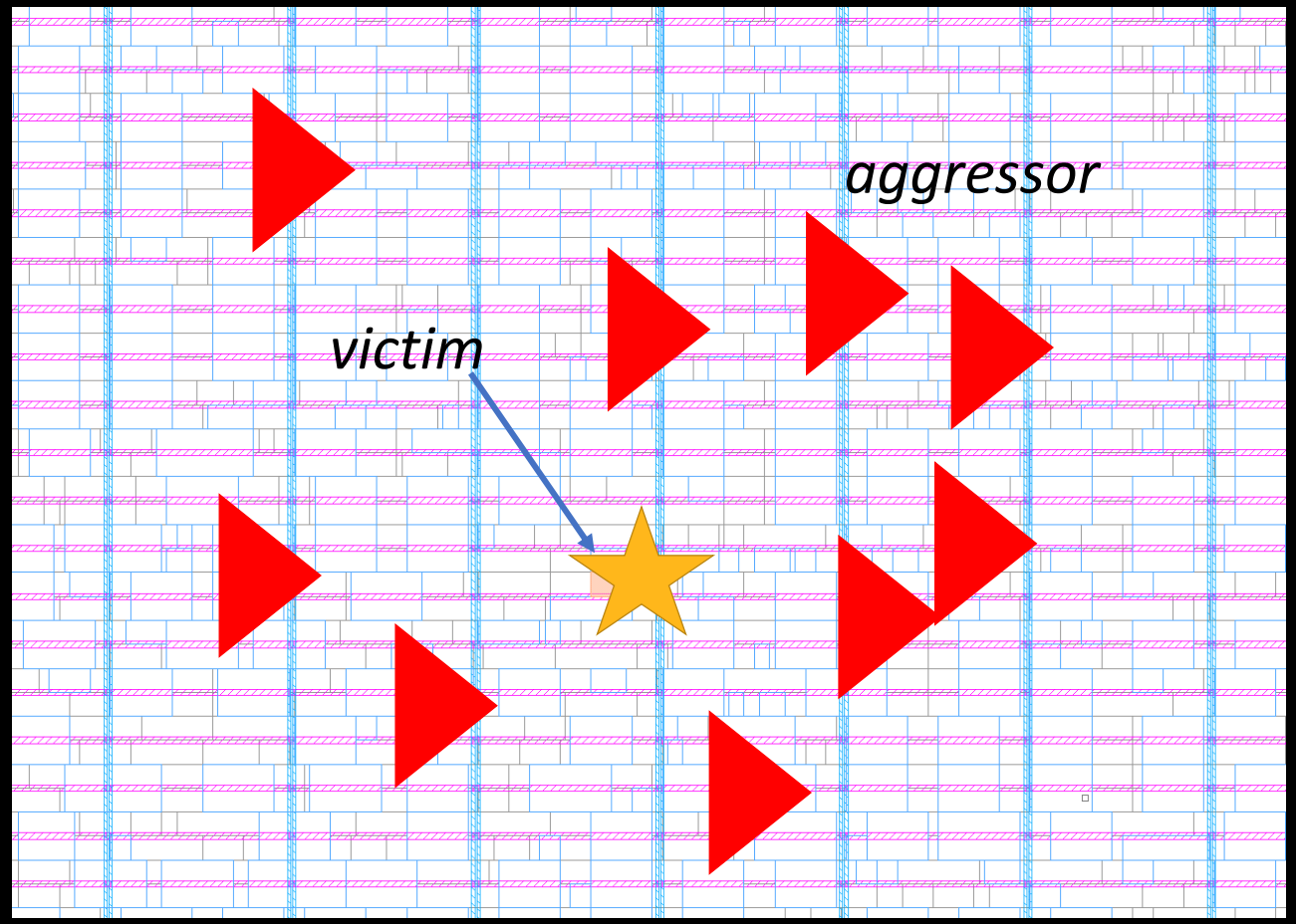
Redhawk-SC SigmaDvD

- The most recent technology revolution
  - 100% victim coverage with large numbers of simulations
  - Complete understanding of each component of instance noise for debug and ECO
  - Aggressor focus: Which aggressors impact victim voltage drops

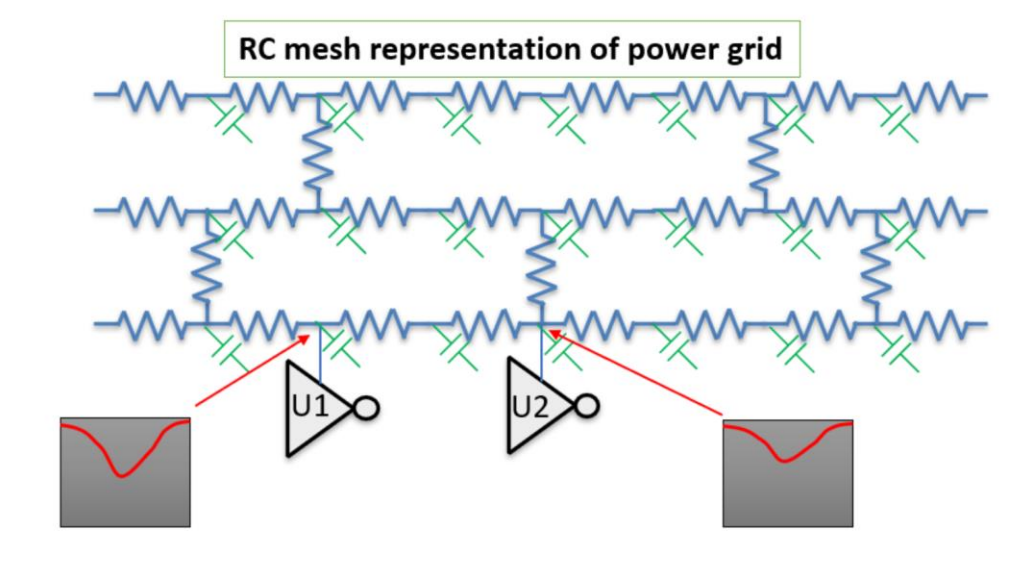
- Various Applications
  - IR/ECO
  - IR/STA
  - IR/Physical Design
  - IR/Dynamic Simulation with Enhanced Coverage

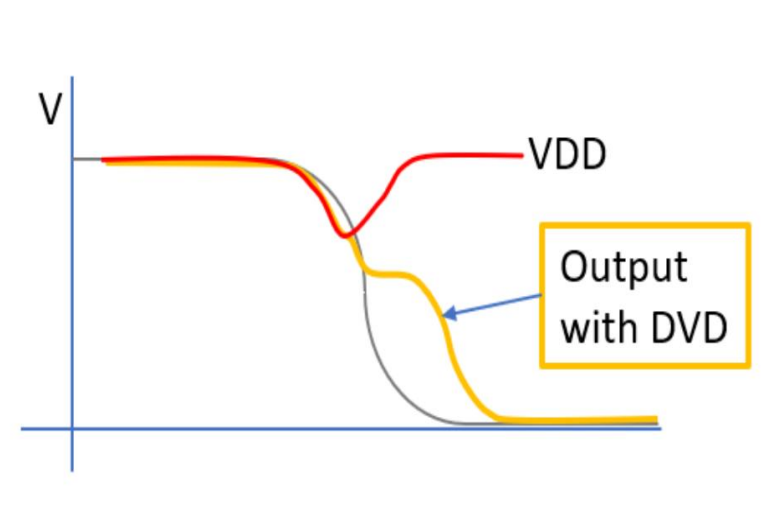
Back to basics, why and how IR occurs?

- Problem Statement:
- What is a realistic voltage drop on a given instance pin, under typical operation of the design that will limit the functionality?



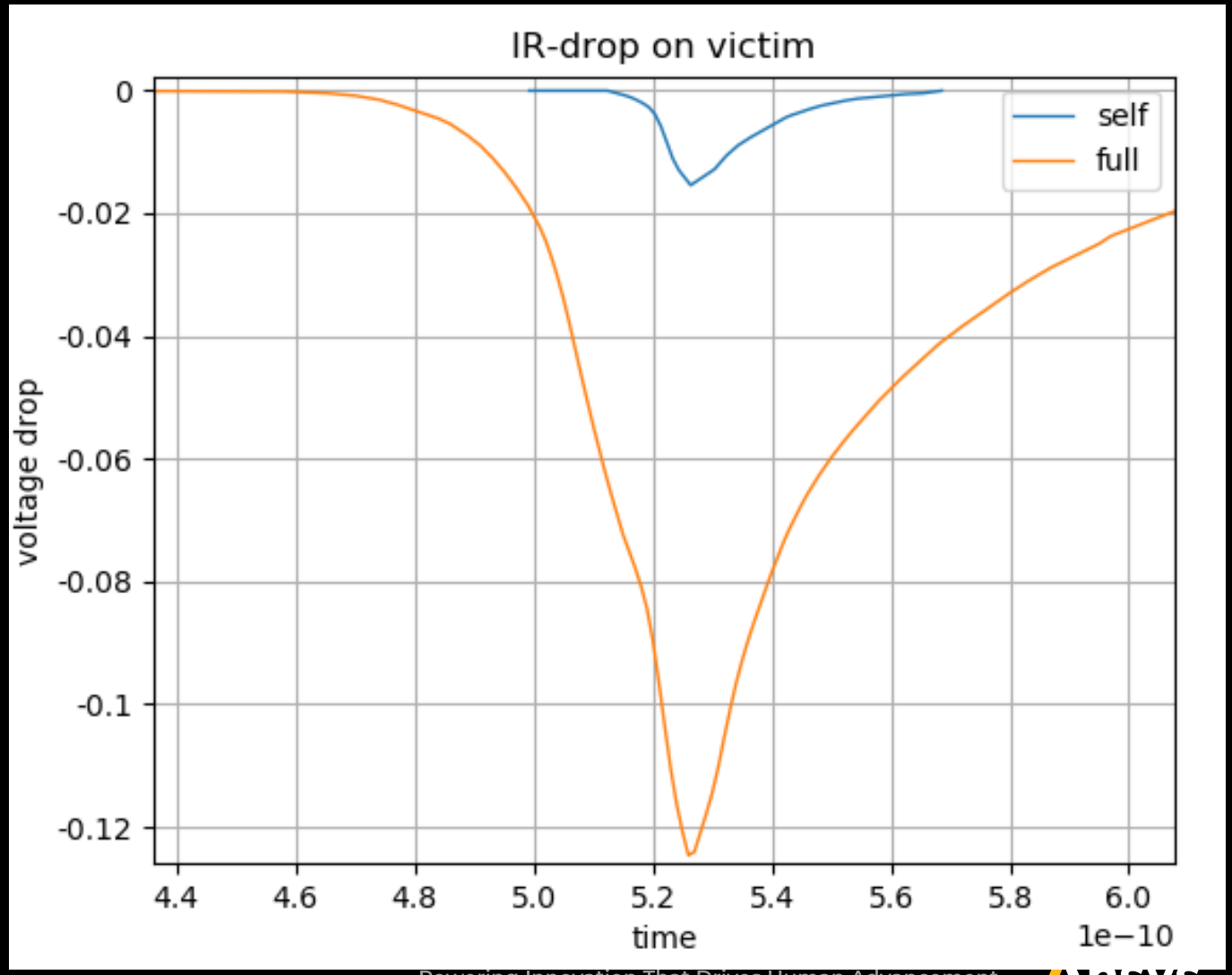
Circuit Model





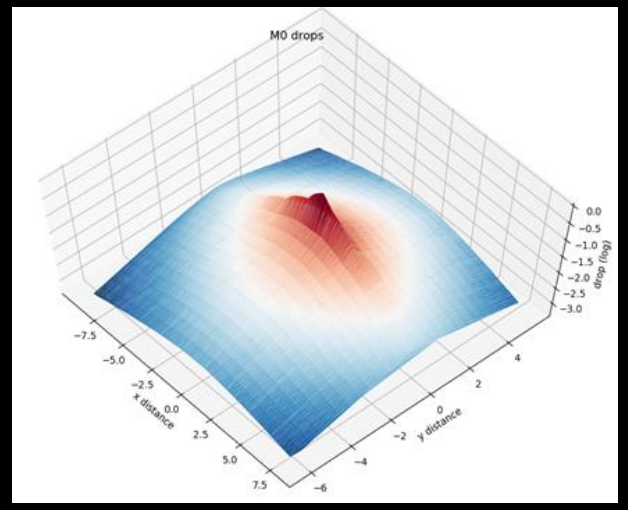
Is Self IR drop enough?

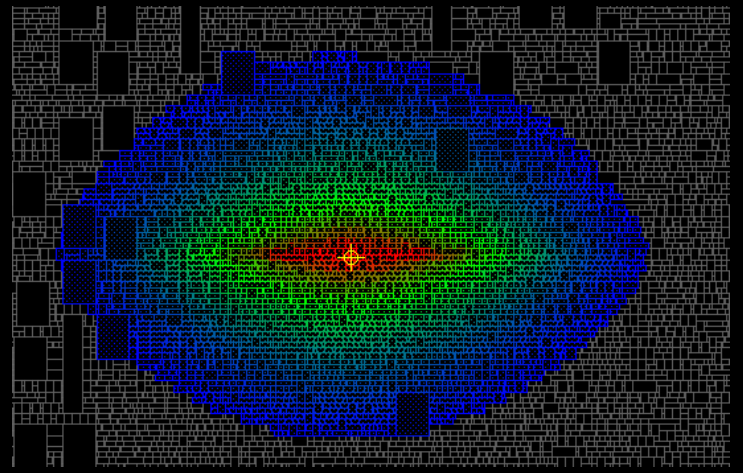
- Only the victim switched (rest of design quiet)
  - self-drop: 15mV
- Victim and *all* aggressors switched at the same time (aligned).
  - full-drop: 124mV
- 8x larger than self
  - All aggressor switching at the same time is
  - Probable
  - Low Likelihood

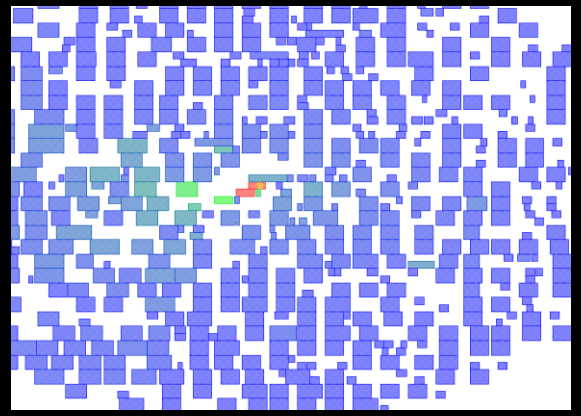


Decomposing Voltage Drop

- Local effects of an aggressor
- Impedance effects
  - Self-resistance
  - Cross-resistance (PGImpact)
  - The effect to victim from an aggressor instance
    - Overlapping in time and switching behavior

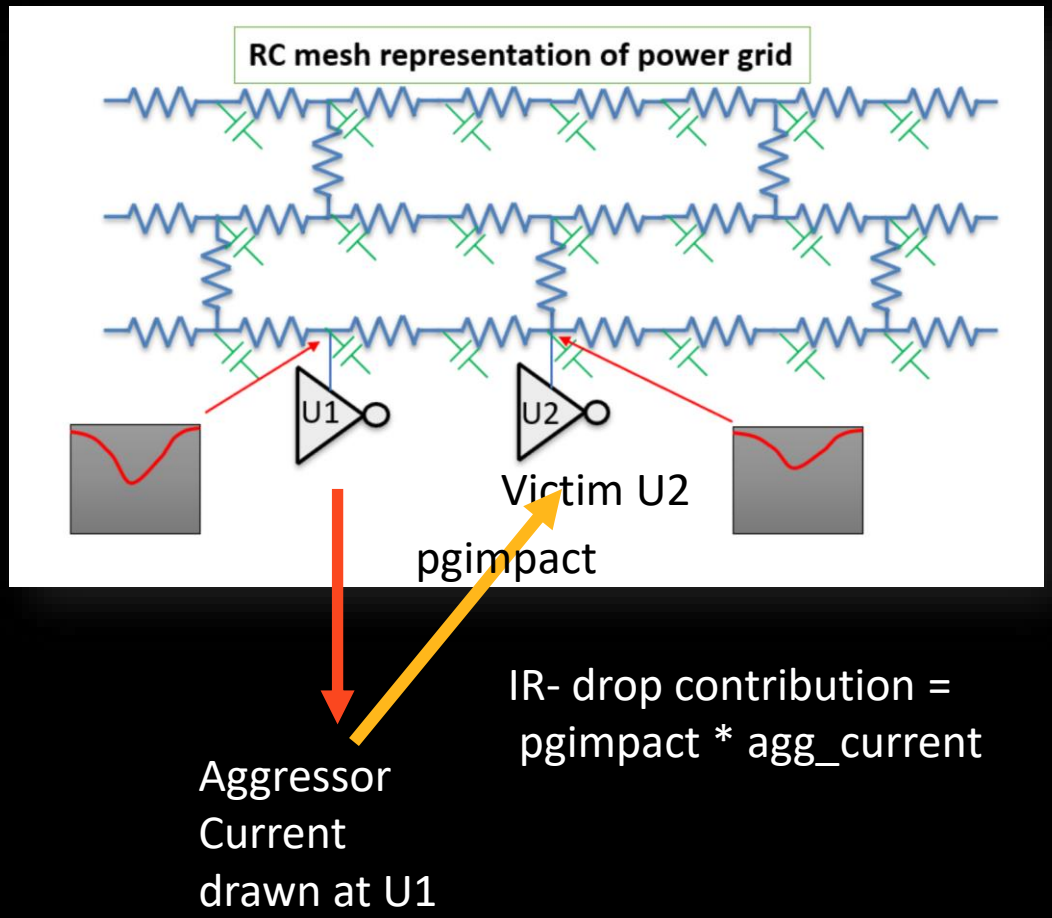




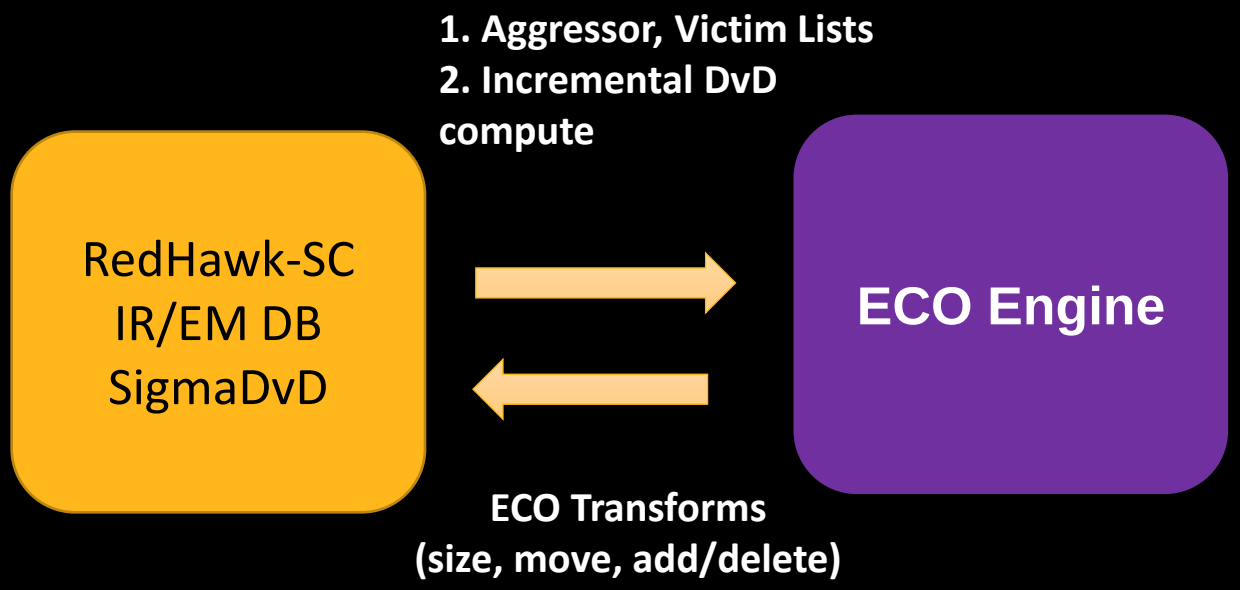


SigmaDvD Concepts

- Effective Resistance
  - IR drop due to self-switching
- PGImpact: Trans-impedance
  - IR drop due to aggressors switching at the time of victim
- Risk/Likelihood concepts
  - Can the aggressors switch w/ victim
  - Likelihood of switching along with victim
    - P(aggressor@t0 | victim@t0) = ?
- SigmaDvD voltage metrics
  - Local voltage drop limits of victim and chosen aggressors



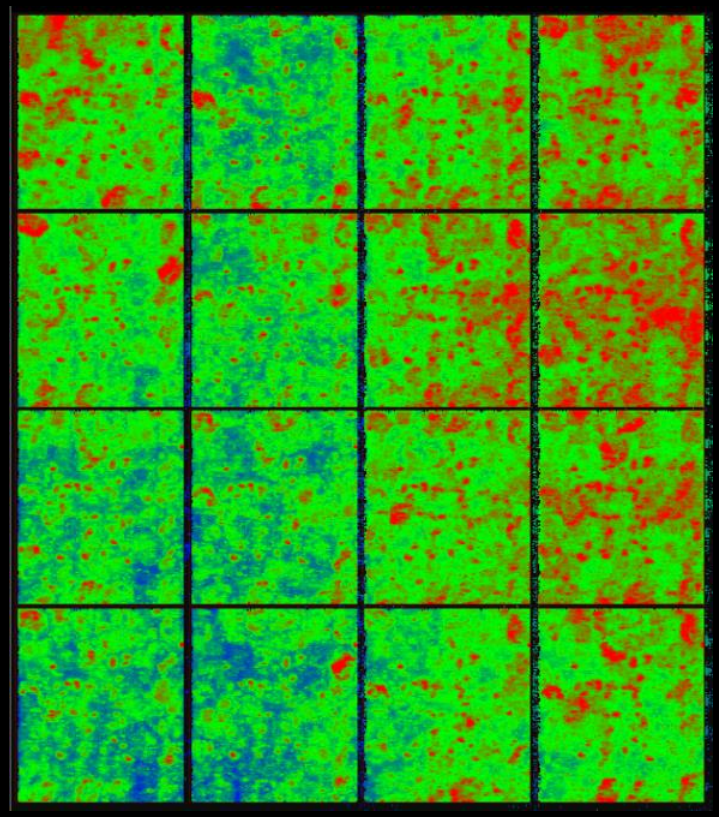
IR Aware Engineering Change Order (ECO)



- **Prioritize DvD violations to fix**
- **Incremental what-if queries**
  - Each ECO change will remove and add drop contributions

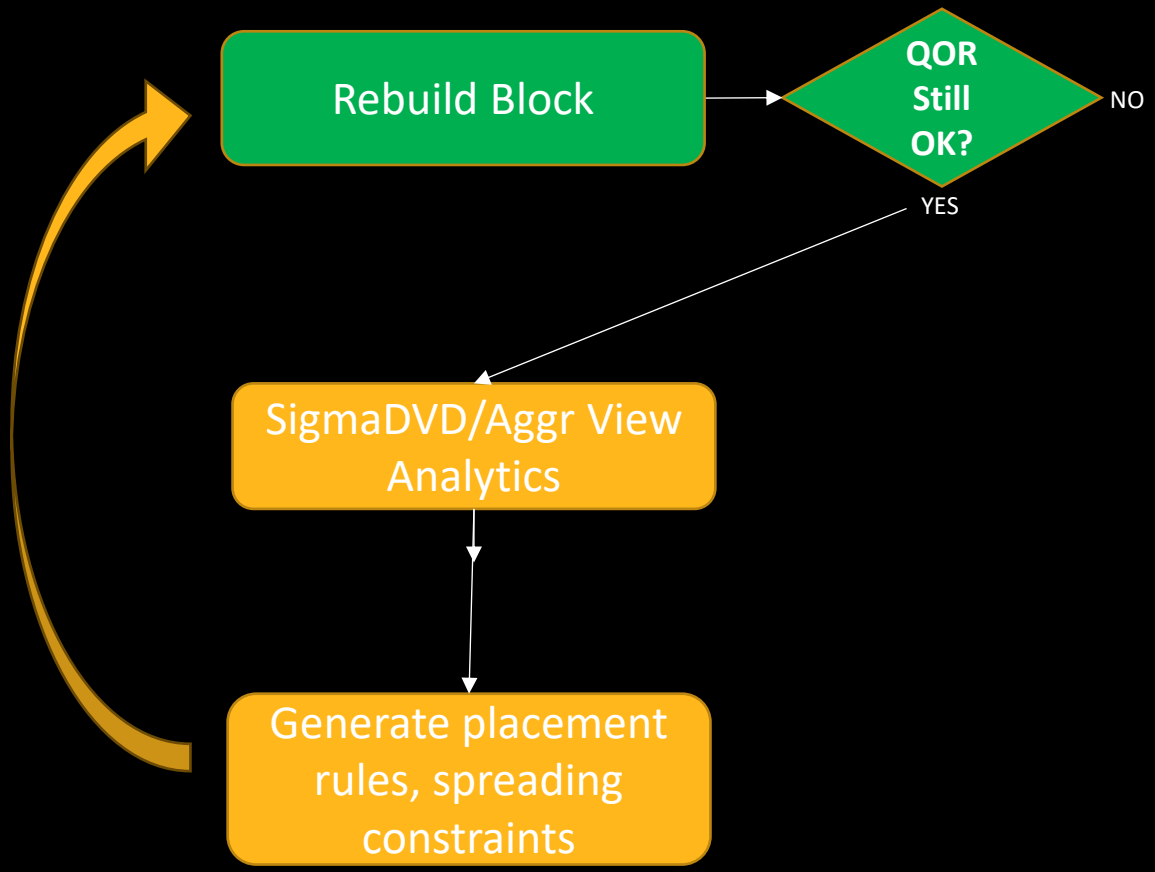
Decomposing Local And Regional IR drops

- Same dies
- Same power profiles
- Why seeing different hotspots
- Deduce Local IR-drop contributions
- Regional variability



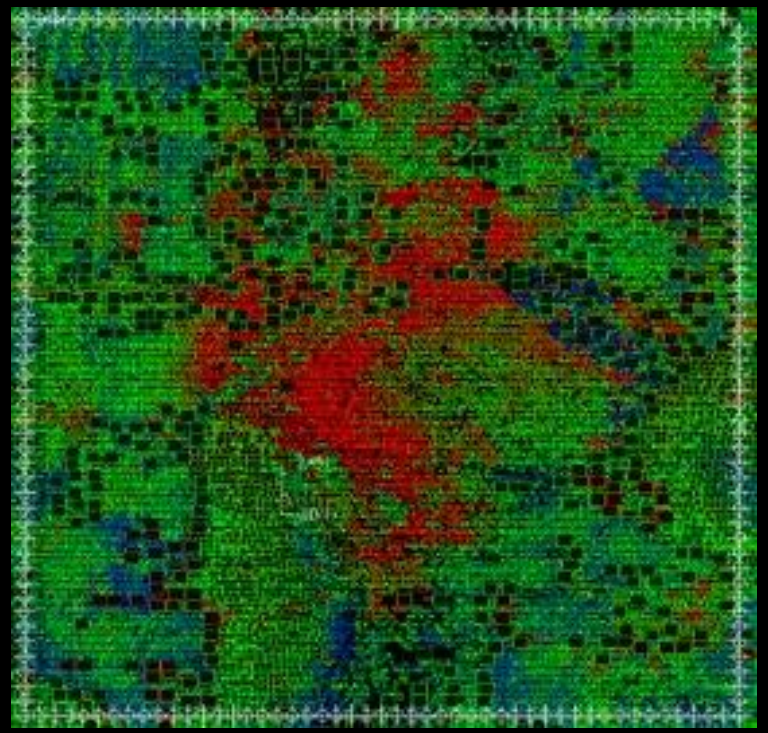
IR aware Placement

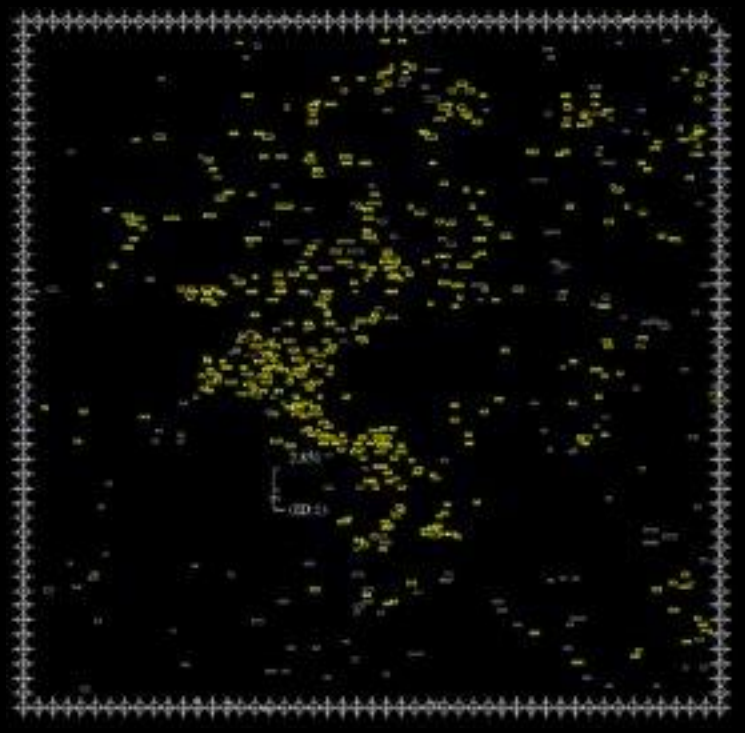
Analyze the design, generate placement rules to improve DVD, rebuild the block, repeat. Monitor timing and QoR



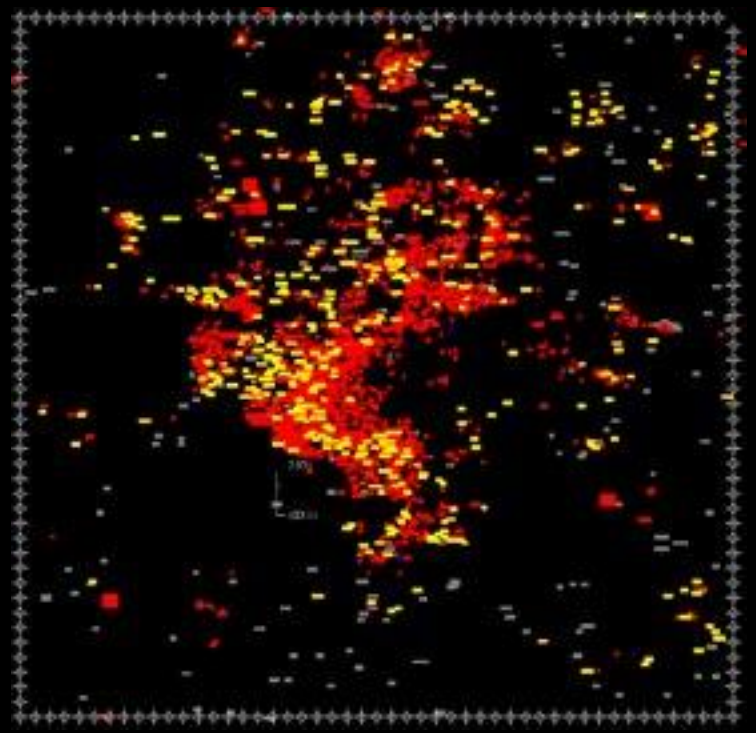
IR aware Physical Design (Aggressor Clustering)

- IR failures typically happen in clusters



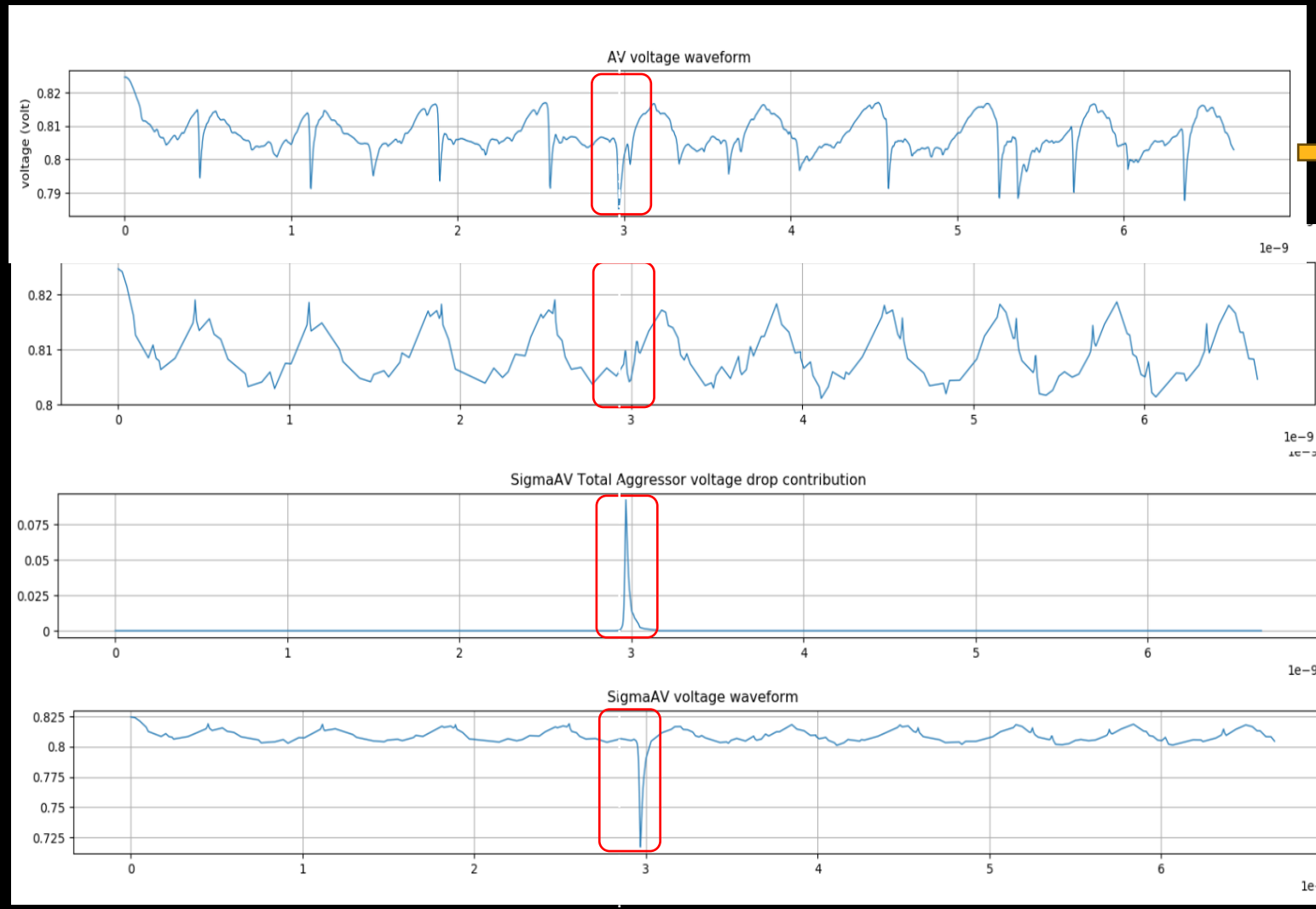


Identify worst aggressor cells



High density of aggressor cells are the root cause

Sigma-Enabled Transient Analysis for Enhanced Coverage



V(victim), self-switching but some aggressors may be missing, or mis-aligned

V(victim) - existing aggressor contributions

DeltaV(victim) due to total aggressor voltage impact

V(victim) + DeltaV that will have pessimistic voltage impacts

Conclusion

- IR-Drop a major problem
- SigmaDvD offers an excellent analytics platform
- AI/ML applications
- Many potential Physical Design applications
  - Yet to be explored