GEORGIA TECH CAD

INVITED: MODELING AND DESIGN METHODOLOGY FOR BACKSIDE INTEGRATION OF VOLTAGE CONVERTERS

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MOTIVATION

TOWARDS FUNCTIONAL BACKSIDE INTEGRATION

Problem	
Solution	Decouple power-delivery-network to backside (BS-PDN)
	Integrate voltage regulators (IVR) in backside back-end-of-line (BEOL)

Fig 1: Technology scaling trends[1]

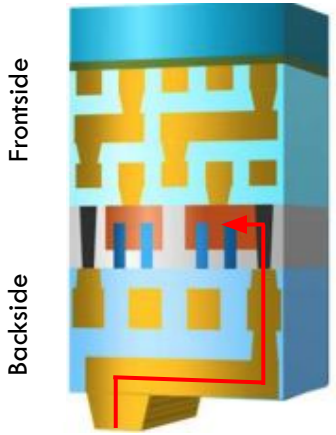


Fig 2: Backside power delivery[2]

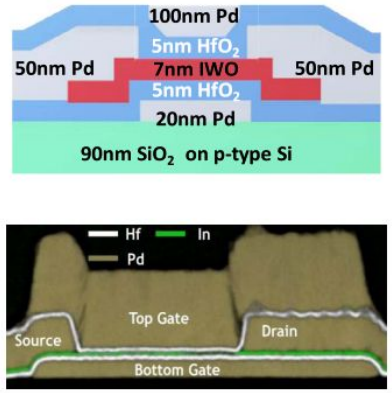


Fig 3: BEOL IWO devices[3]

[1]"Chip roadmap for the next decade - Easybuyic.com." Accessed: Mar. 06, 2025. [Online]. Available: https://www.easybuyic.com/wapshop/ArticleDetails?ArticleId=2087

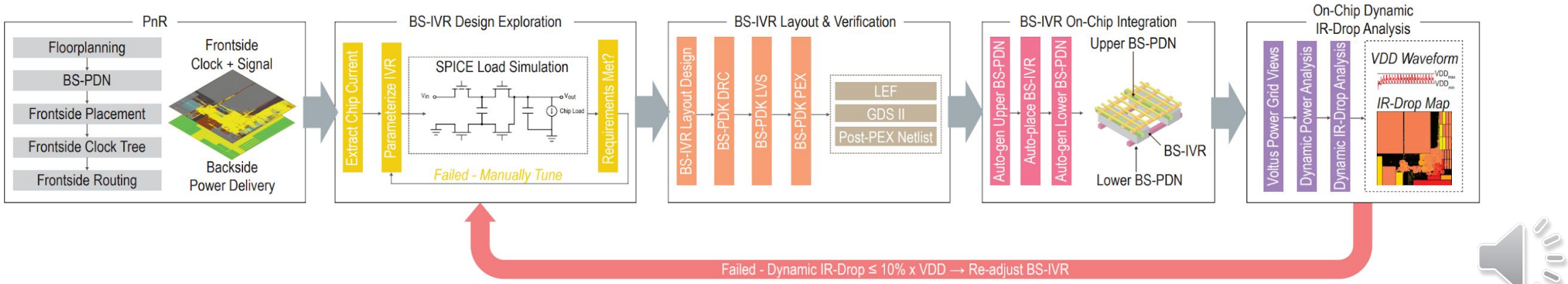
[2]W. Hafez *et al.*, "Intel PowerVia Technology: Backside Power Delivery for High Density and High-Performance Computing," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2023, pp. 1–2. doi: 10.23919/VLSITechnologyandCir57934.2023.10185208.

[3]W. Chakraborty, H. Ye, B. Grisafe, I. Lightcap, and S. Datta, "Low Thermal Budget (<250 °C) Dual-Gate Amorphous Indium Tungsten Oxide (IWO) Thin-Film Transistor for Monolithic 3-D Integration," *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5336–5342, Dec. 2020, doi: 10.1109/TED.2020.3034063.

MOTIVATION

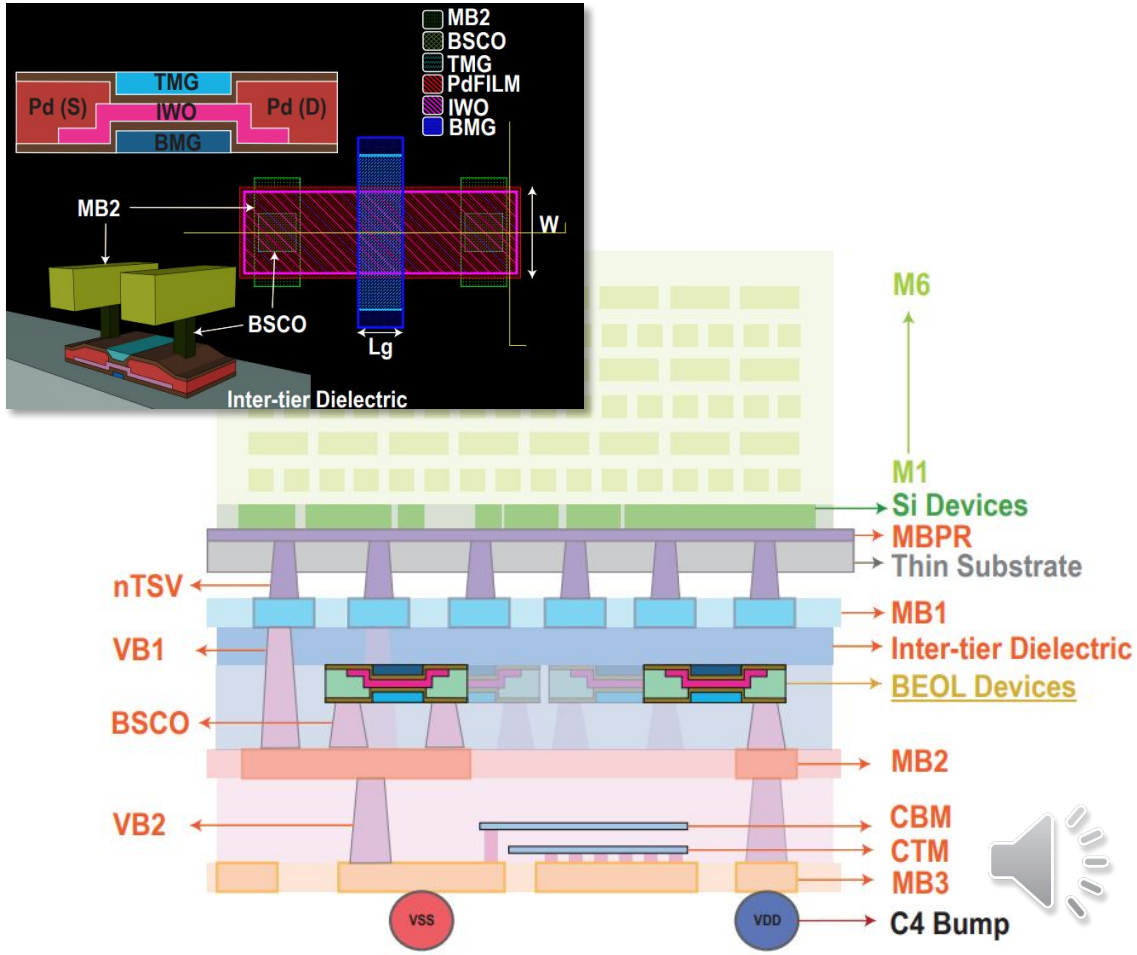
OVERVIEW

- Proposed and characterized BS-IVRs with BEOL IWO transistors
- Developed backside process design kit (BS-PDK) for functional backside
- Established end-to-end EDA flow for dynamic power integrity analysis with IVRs



IWO BEOL DEVICES

Amorphous Tungsten-Doped Indium Oxide Thin-Film Transistor (IWO TFT)	
Location	BEOL
Process Temperature	< 250°C
Functionality	N-type device
Modalities	Enhancement / Depletion
Application	Monolithic 3D Integration
Gate Structure	Dual Gate
Contacts	Palladium (Pd)
Channel	IWO *Oxygen vacancies in channel analogous to donors in MOSFETs*
Mobility	>20 cm^2 x s / V



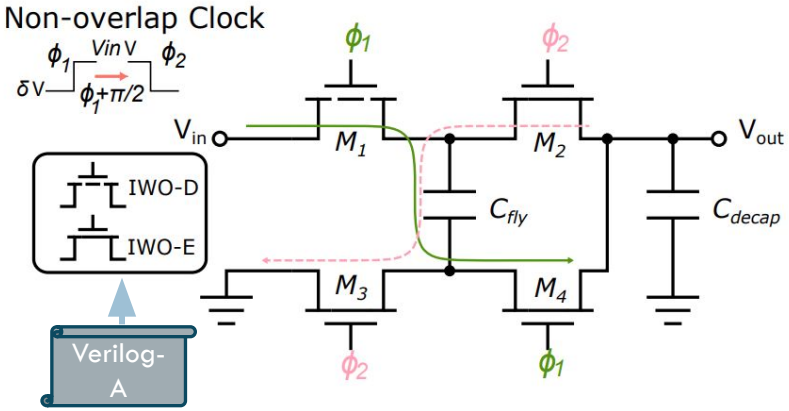
METHODOLOGY

BACKSIDE IVR DESIGN AND EXPLORATION

- $V_{in} = 1.4\,V$, $V_{out,target} = 0.7\,V$
- Maximize $\Rightarrow \eta = \frac{P_{out}}{P_{in}} = \frac{I_{load}V_{out}}{I_{in}V_{in}}$
- Minimize $\Rightarrow V_{p2p} = \max(V_{out,steady-state}) - \min(V_{out,steady-state})$

$$\min(V_{out,steady-state}) > 0.7\,V$$

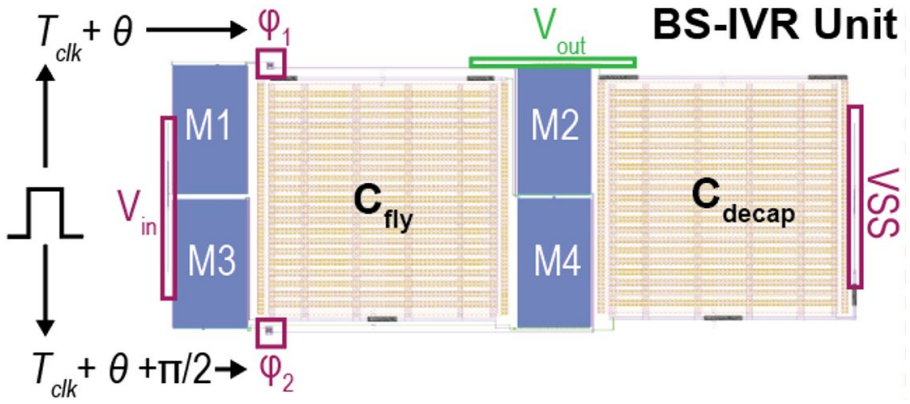
Device	Parameter	Baseline	Optimized
Top	# *IVR units*	1	10
IWO-E/-D	W_{total}	7500 μm	1400 μm
	L_g	50 nm	50 nm
	# $fingers$	50	50
$C_{fly}, C_{decoupling}$	W	150.76 μm	50.75 μm
	L	150.76 μm	50.75 μm
	$C_{density}$	33 $fF/\mu m^2$	33 $fF/\mu m^2$
	C	750 pF	85 pF

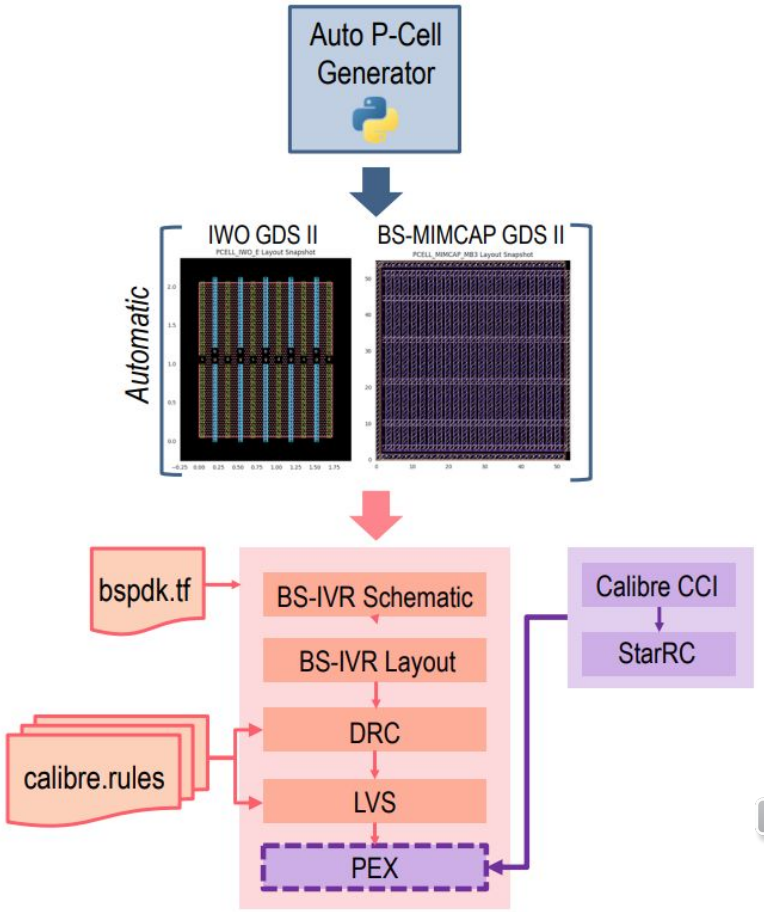


METHODOLOGY

THE BACKSIDE PROCESS DESIGN KIT

- Backside design rules follow commercial 65nm technology
- Automatic generation of GDS-II of IWO & MIM devices
- Manual layout design and tuning

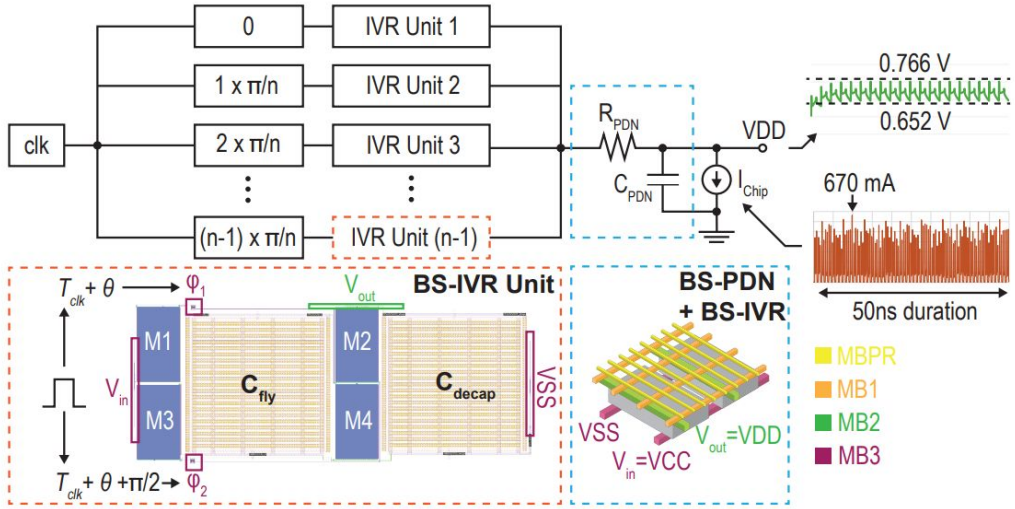


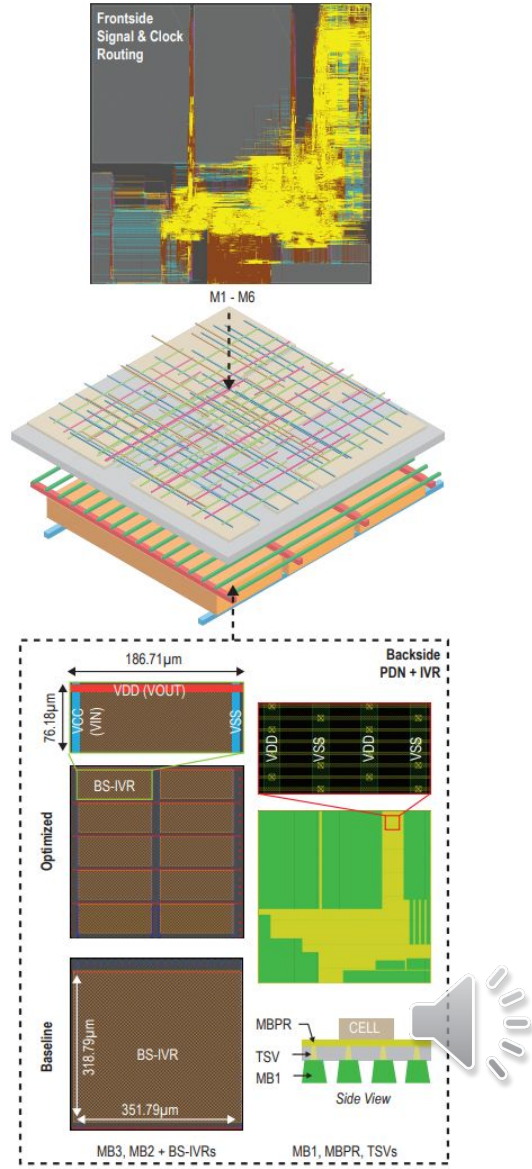


EXPERIMENTAL RESULTS

BS-IVR ON-CHIP INTEGRATIOI

- OpenPiton Benchmark: open-sourced single-core RISC V CPU
- 3nm in-house PDK with buried power rails for P&R
- BS-IVR physically co-design with BS-PDN
- Parallel IVR units with interleaved clock signals improves reliability





EXPERIMENTAL RESULTS

POWER, PERFORMANCE, AREA COMPARISON

Metrics	BS-PDN	BS-IVR - Baseline	Δ%	BS-IVR - Optimized	Δ%
# BS-IVR Units	-	1	-	10	-
BS-IVR Unit Footprint (mm^2)	-	0.112	-	0.0142	-
BS-IVR Operating Freq. (MHz)	-	400	-	400	-
BS-IVR Input Voltage (V)	-	1.40	-	1.40	-
BS-IVR Min. V_{out} (V)	-	0.58	-	0.65	-
BS-IVR Unit Target Efficiency (%)	-	60	-	60	-
BS-IVR Unit Power Density (W/mm^2)	-	0.52	-	3.02	-
Full-Chip Footprint (mm^2)	0.128	0.128	-	0.128	-
# Cells	279,507	279,507	-	279,507	-
Eff. Freq. (GHz)	0.9462	0.9495	+0.35%	0.9502	+0.42%
Dyn. Worst On-Chip VDD Droop (mV)	63.00	122.2	-48.36%	33.64	+46.60%
Total Dynamic Power (mW)	99.89	99.89	-	99.89	-

- End-to-end power integrity simulation takes **~5min**
- Baseline BS-IVR case showcases challenges of IVR on-chip power integrity
- Optimized BS-IVR solution has **6x** improved power density and **2x** improved dynamic VDD droop

CONCLUSION

- We propose novel fully integrated backside BEOL IVR using IWO devices
- We design and verify with our novel BS-PDK from DRC □ LVS □ PEX
- We establish a complete end-to-end EDA flow co-designing BS-IVR with BS-PDN and analyzing dynamic on-chip power integrity
- Future Work:
  - Rigorously analyze off-chip and on-chip power integrity impacts of fully frontside and backside BEOL IVRs
  - Analyze thermal integrity impacts of introducing BEOL switching devices in backside / frontside

THANK FOR LISTENING! Q&A

BACKGROUND

SWITCHED-CAPACITOR DC-DC CONVERTER

	Inductor-based	Capacitor-based
Pros	Better load regulation	Fully integrable
	High efficiency	High efficiency
Cons	Not fully integrable	Challenging high load regulation
	Inductors cause high EMI	Prone to greater voltage ripple