ISPD'25 Lifetime Achievement Session
Honoring Prof. Jason Cong

Shaping the Future of Interconnected Physical Design

David Z. Pan

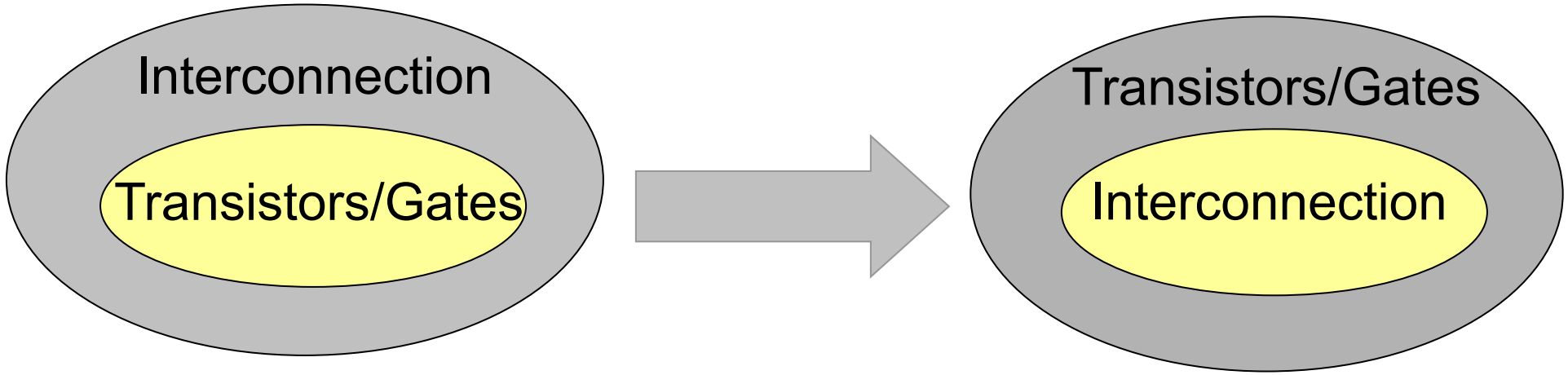
The University of Texas at Austin

History 101 of Physical Design

- Born in early 1960's (board layout)
- Passed teenage in 70's (standard cell place and route)
- Entered early adulthood in 80's (over-the-cell routing)
- Declared dead in late 80's !!!
- **Found alive and kicking in 90's**
- Physical Design (PD) is a dominant force in the overall design cycle
  - Due to the deep submicron scaling & interconnect dominance
  - Expand vertically with logic synthesis/HLS, interconnect optimization, planning, DFM/DTCO, signoff Design and Manufacturing Closure
  - IC implementation tool is about 1/3 of the overall EDA market

Interconnect-Centric Design

- In early 1990s, Prof. Jason Cong advocated paradigm shifting



- Many seminal papers □ key for modern design closure

An Interconnect-Centric Design Flow for Nanometer Technologies

JASON CONG, FELLOW, IEEE

Invited Paper

Proc. of IEEE 2001

2000 SRC Technical Excellence Award

"Interconnect Estimation, Planning and Synthesis for Deep Sub-micron Designs"

My PhD Thesis and First Papers

- My PhD Thesis under Prof. Cong "**Interconnect** Synthesis and Planning for High-Performance VLSI" (2000)
- Before working with Jason, I was a PhD student at UCLA Atmospheric Sciences – in the same building as CS (Boelter Hall)
- B.S. in Physics to Physical Design ☺
- My first two papers ICCAD'97

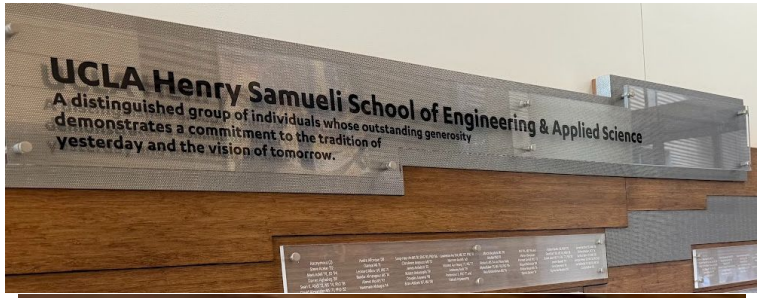
Interconnect Design for Deep Submicron ICs

Jason Cong*, Zhigang Pan, Lei He, Cheng-Kok Koh and Kei-Yong Khoo
Computer Science Department
University of California, Los Angeles, CA 90095 †

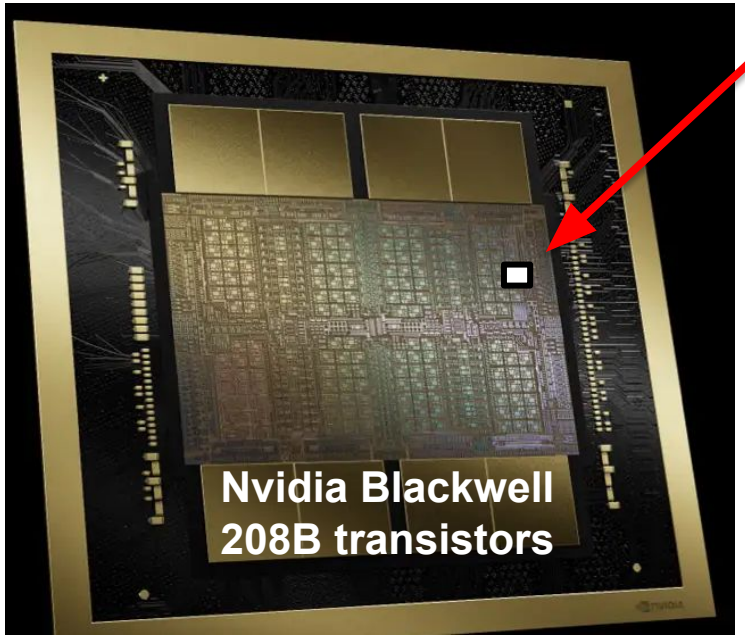
GLOBAL INTERCONNECT SIZING AND SPACING WITH CONSIDERATION OF COUPLING CAPACITANCE

Jason Cong, Lei He, Cheng-Kok Koh, and Zhigang Pan
Department of Computer Science
*University of California, Los Angeles, CA 90095 **

Taken 02/18/25



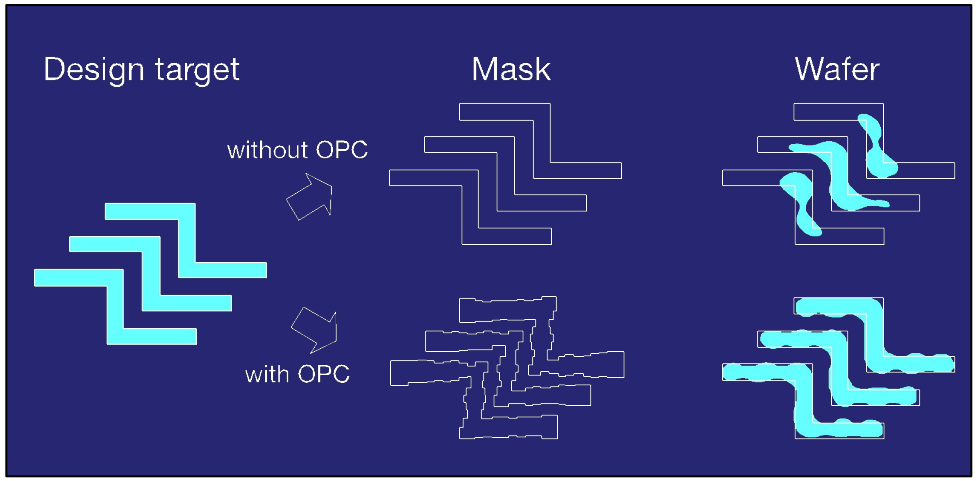
Nanometer IC Design/Manufacturing Complexity



Divide and conquer, e.g., O(M) cells per partition

Turn-around time for 1 iteration of backend flow may take days for one partition!

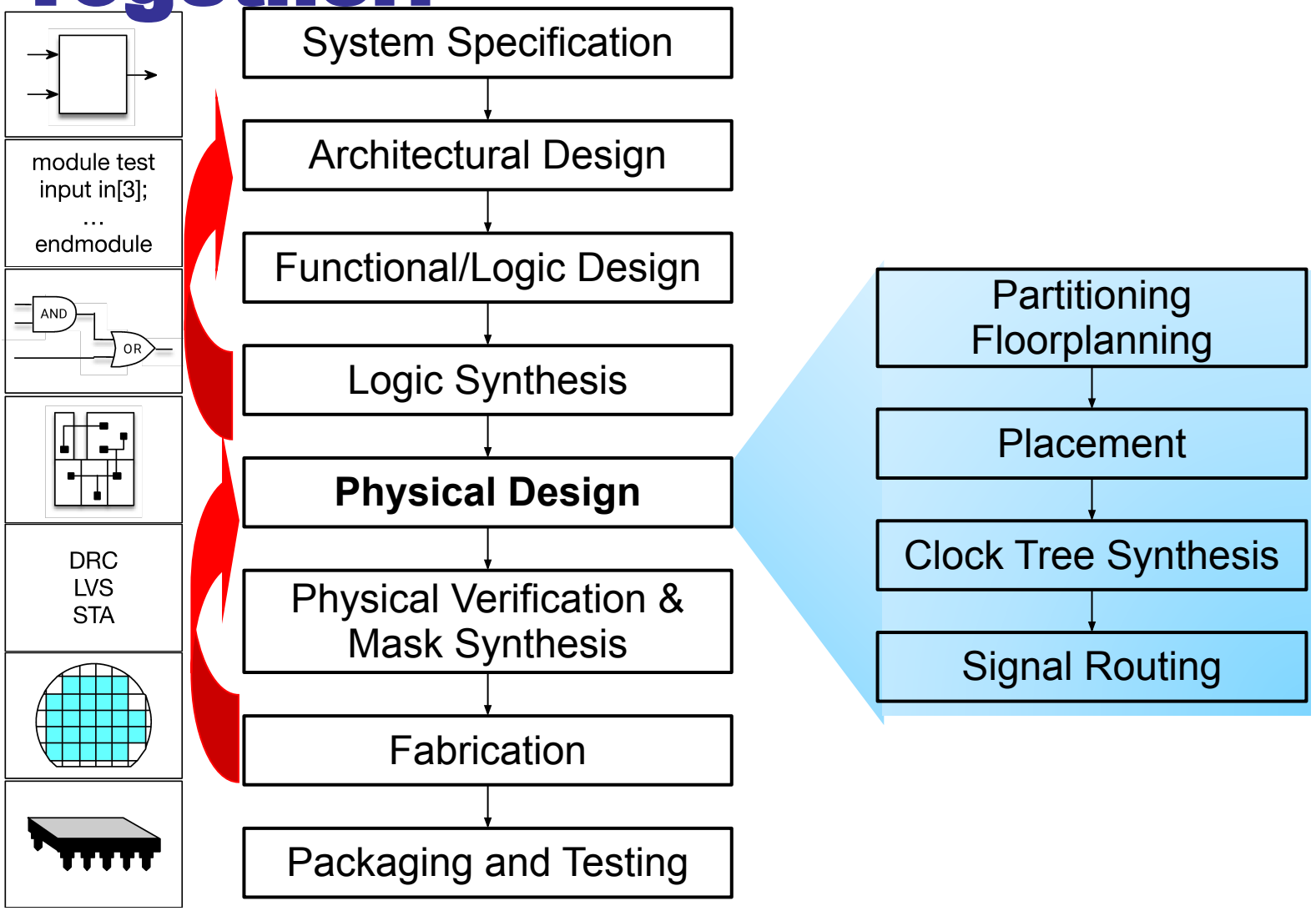
Nvidia spent $10 billion (!) to develop Blackwell



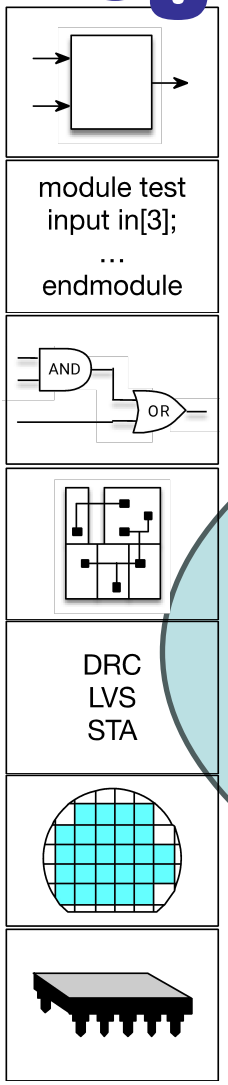
What you see (at design) is not (necessarily) what you get (at fab)

EDA/PD is the backbone of all modern chip designs!

Everything Needs to Work Together!



Everything Needs to Work Together!



System Specification

Architectural Design

Functional/Logic Design

Logic Synthesis/Opt.

Physical Design

Physical Verification & Mask Synthesis

Fabrication

Packaging and Testing

Interconnected Physical Design

Placement Driven Synthesis

Placement

Clock Tree Synthesis

Signal Routing

Interconnect Planning

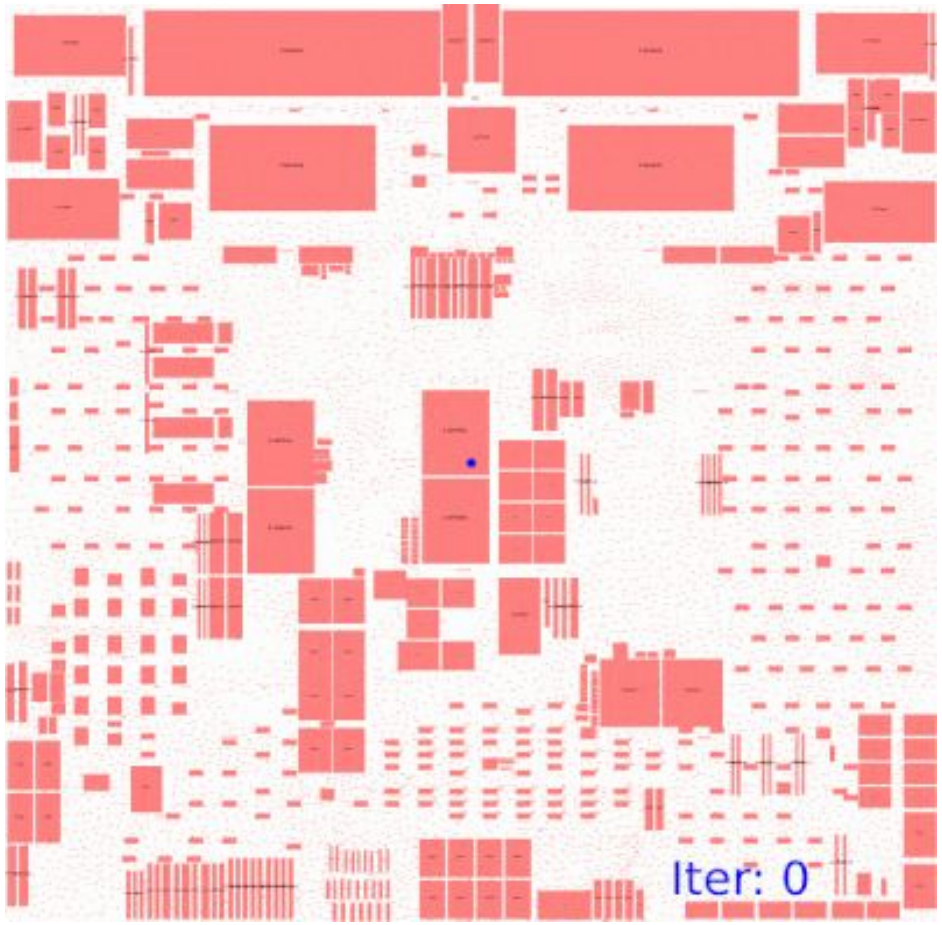
Interconnect Optimization

PPA Design Closure

DFM Closure

Placement and Physical Design Closure

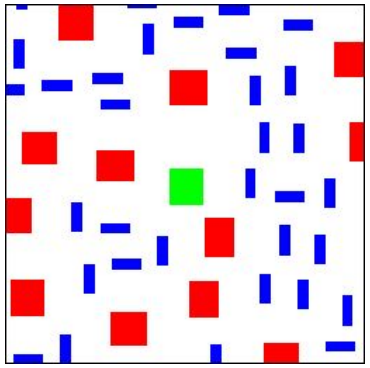
- A classical NP-hard problem!
- Modern huge designs: many billions of transistors, 100M+ cells, and hundreds of macros
- Plays a **central** role in modern IC design closure
  - Largely determines interconnects
  - Driving physical synthesis (buffering, sizing, congestion, …)



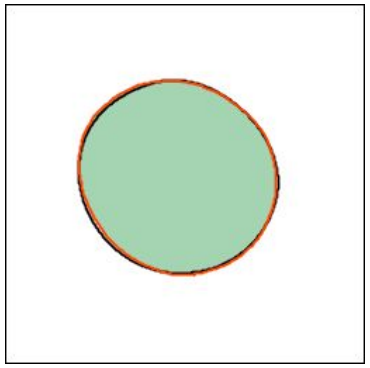
LithoGAN: End-to-End Lithography Modeling

Question: Without going through litho-simulations, can we directly get printed images?

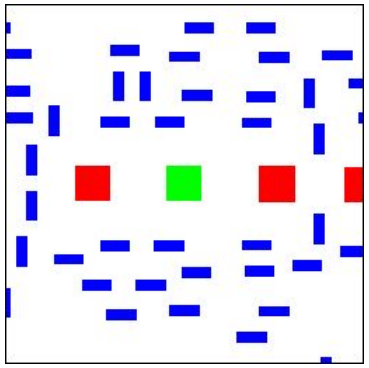
- Our work LithoGAN [Ye+, DAC'19 Best Paper Finalist] is **the first** to use GAN for end-to-end litho-image modeling
- LithoGAN is **1800x** faster than rigorous simulations, with acceptable error (in consultation with industry)



Input



LithoGAN output



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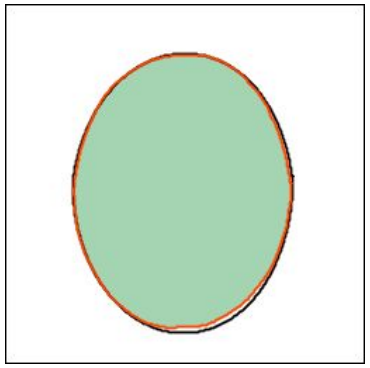
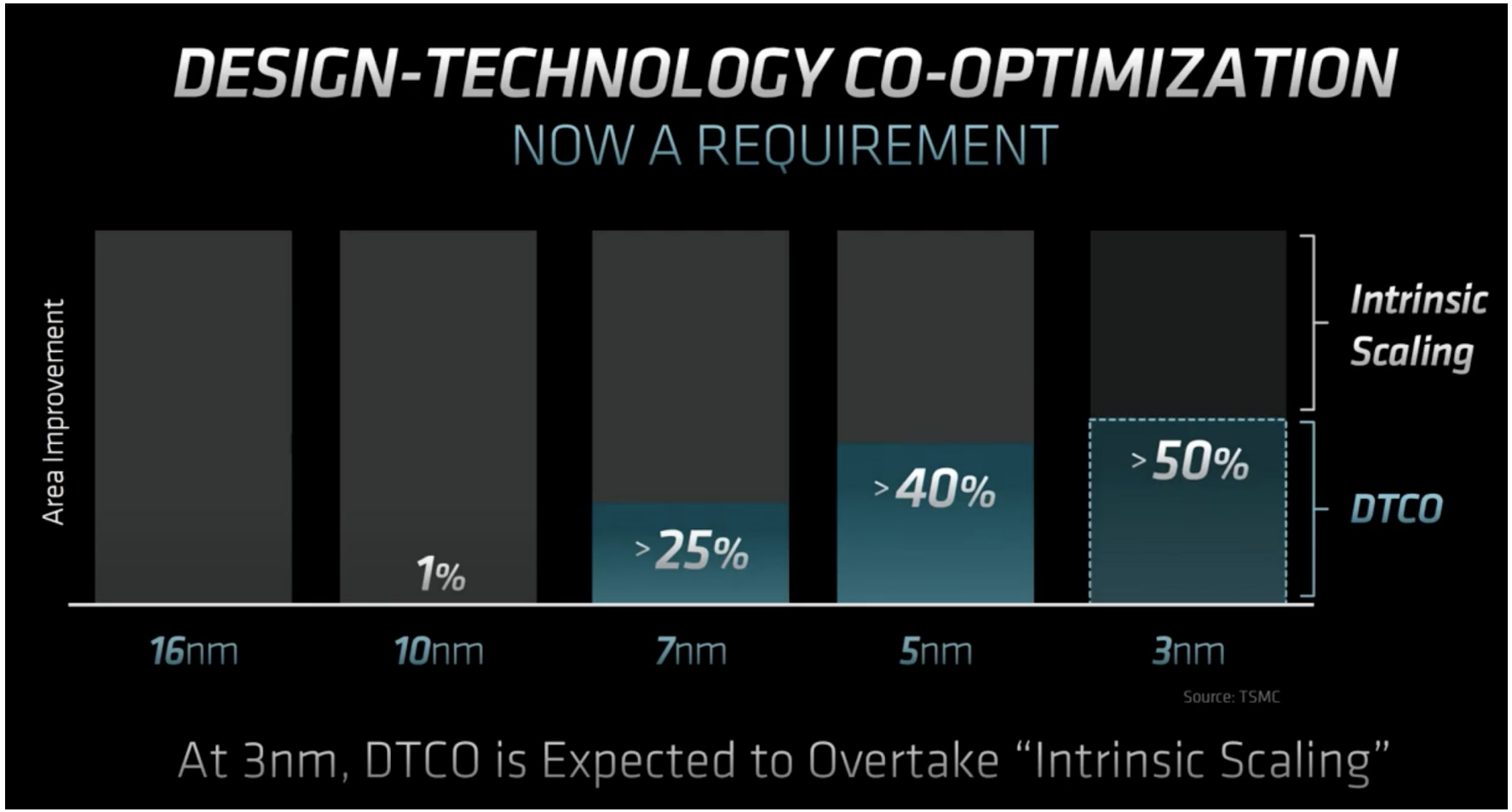


LithoGAN output

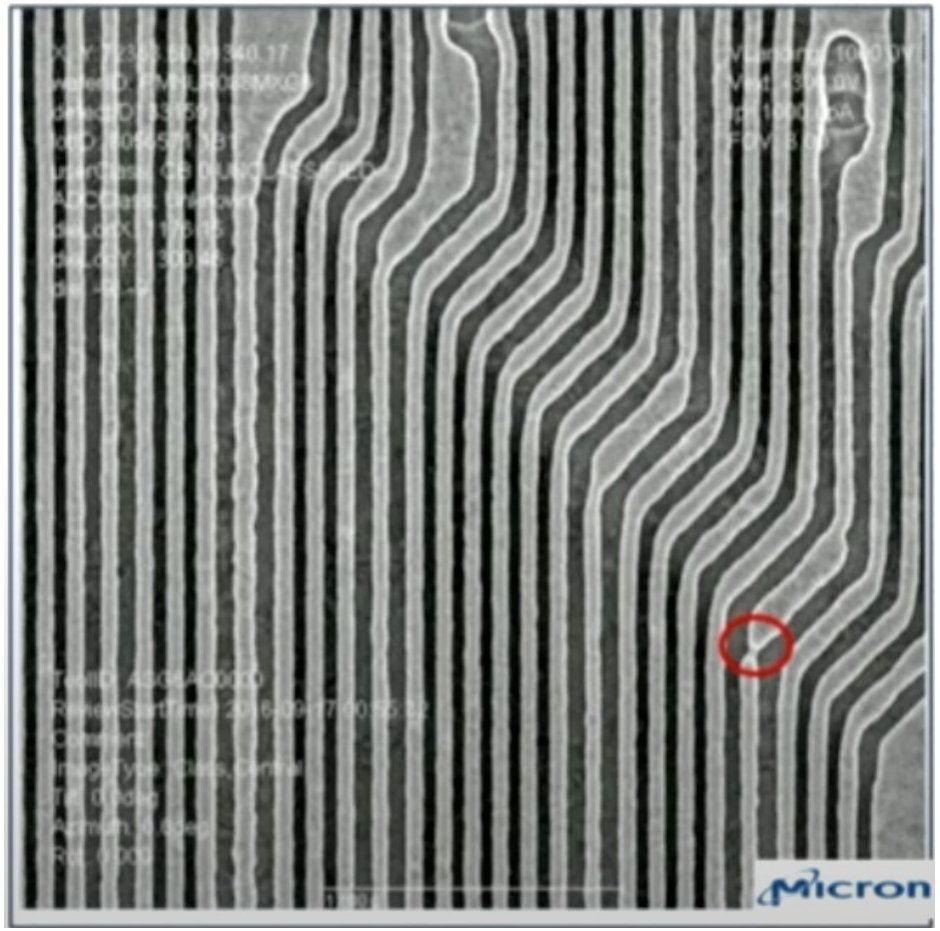
Push for Extreme DTCO (and STCO)

- Mark Papermaster (AMD CTO) DAC 2022 Keynote

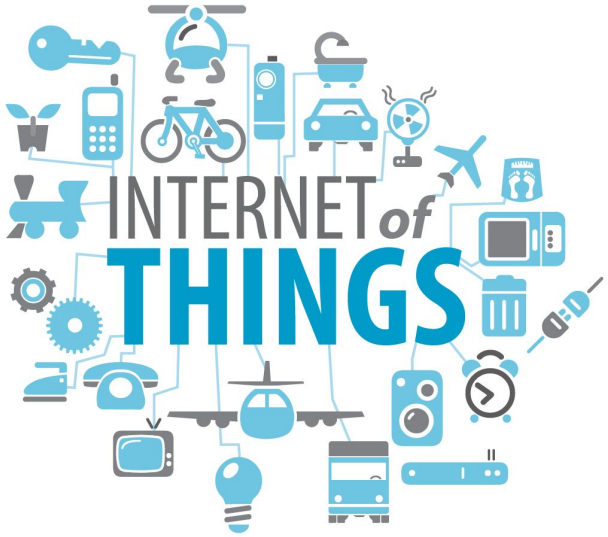


Push for Extreme DTCO

- Designer's intent or dream: free form as long as they can be fabricated
  - They care about PPA, etc.
- Curvilinear mask is happening
  - Real printed image on wafer is never truly rectangular anyway!
- How abut curvilinear design for extreme DTCO?
  - Litho-GAN like Digital Twins can help bridge the gap



Growing Analog IC Demand



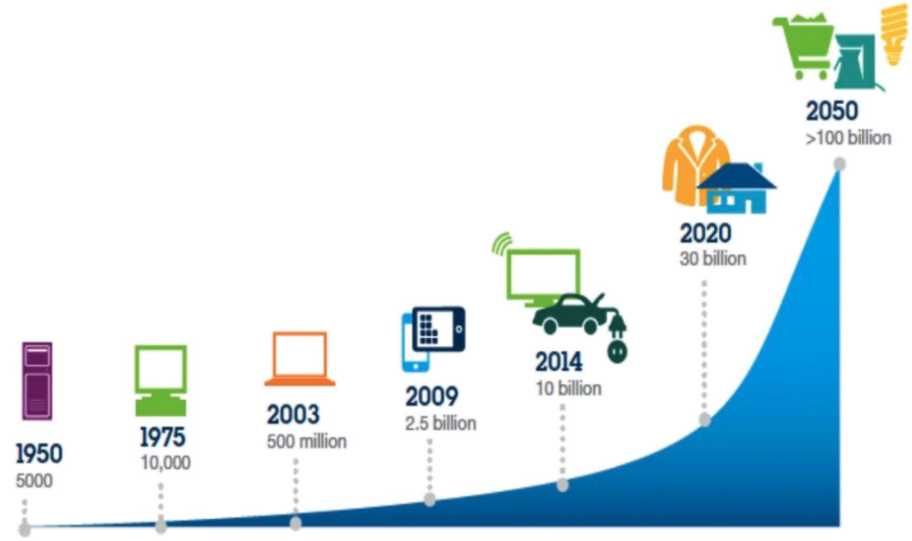
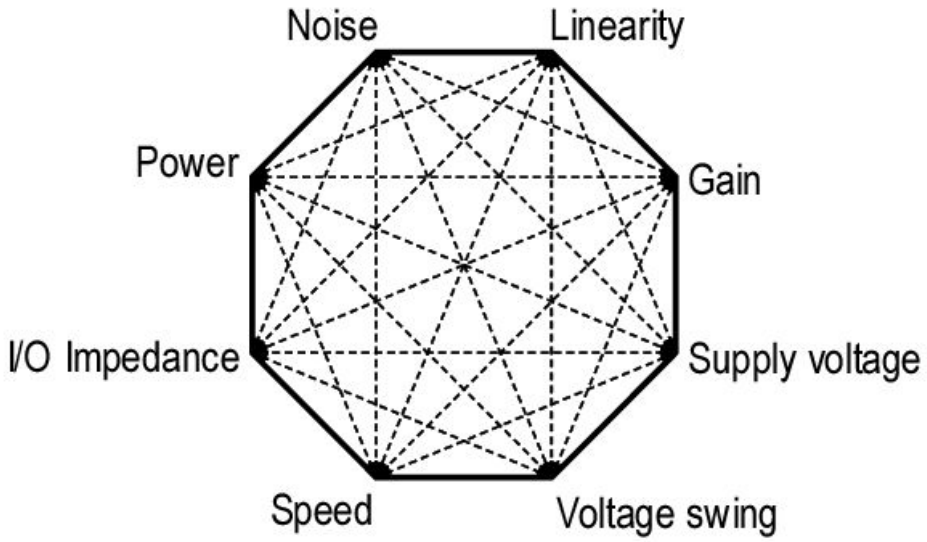
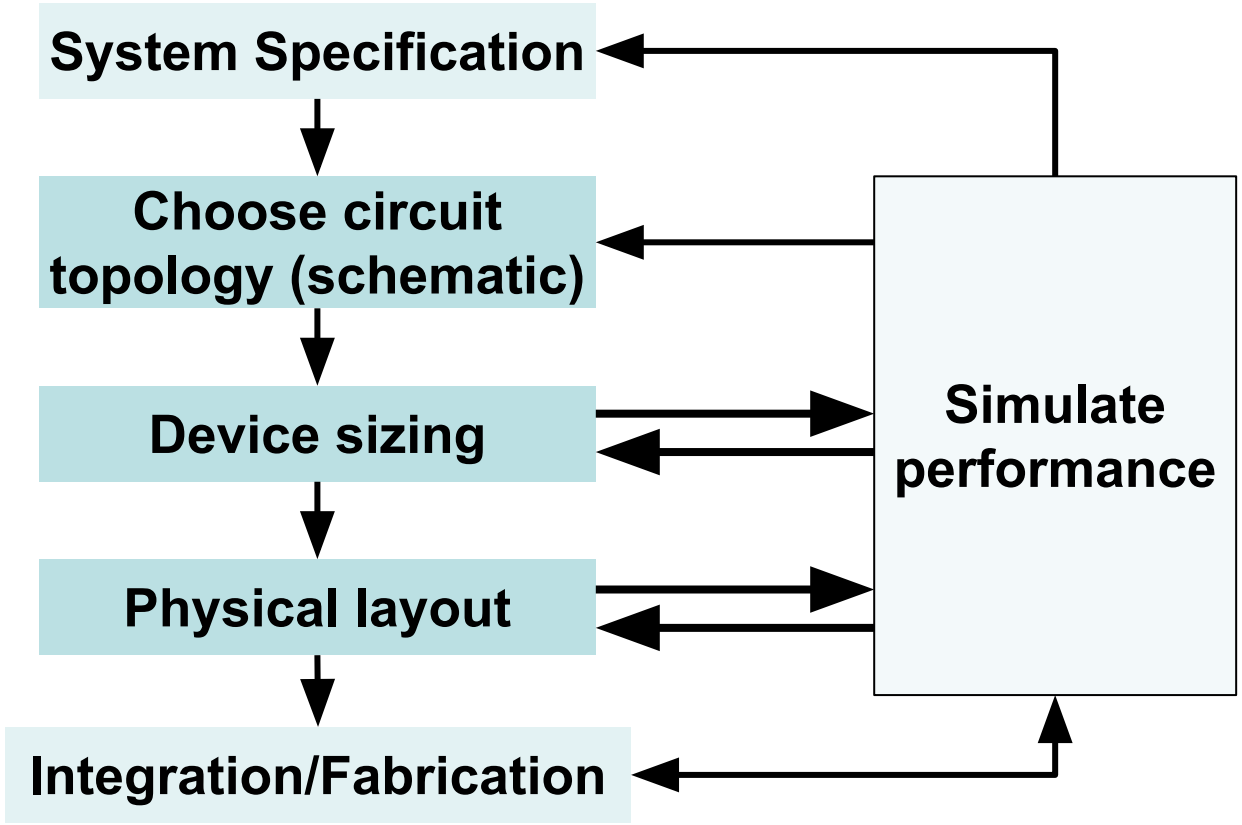


Image Sources: IBM, Ansys, public technology

Analog IC Design is Hard

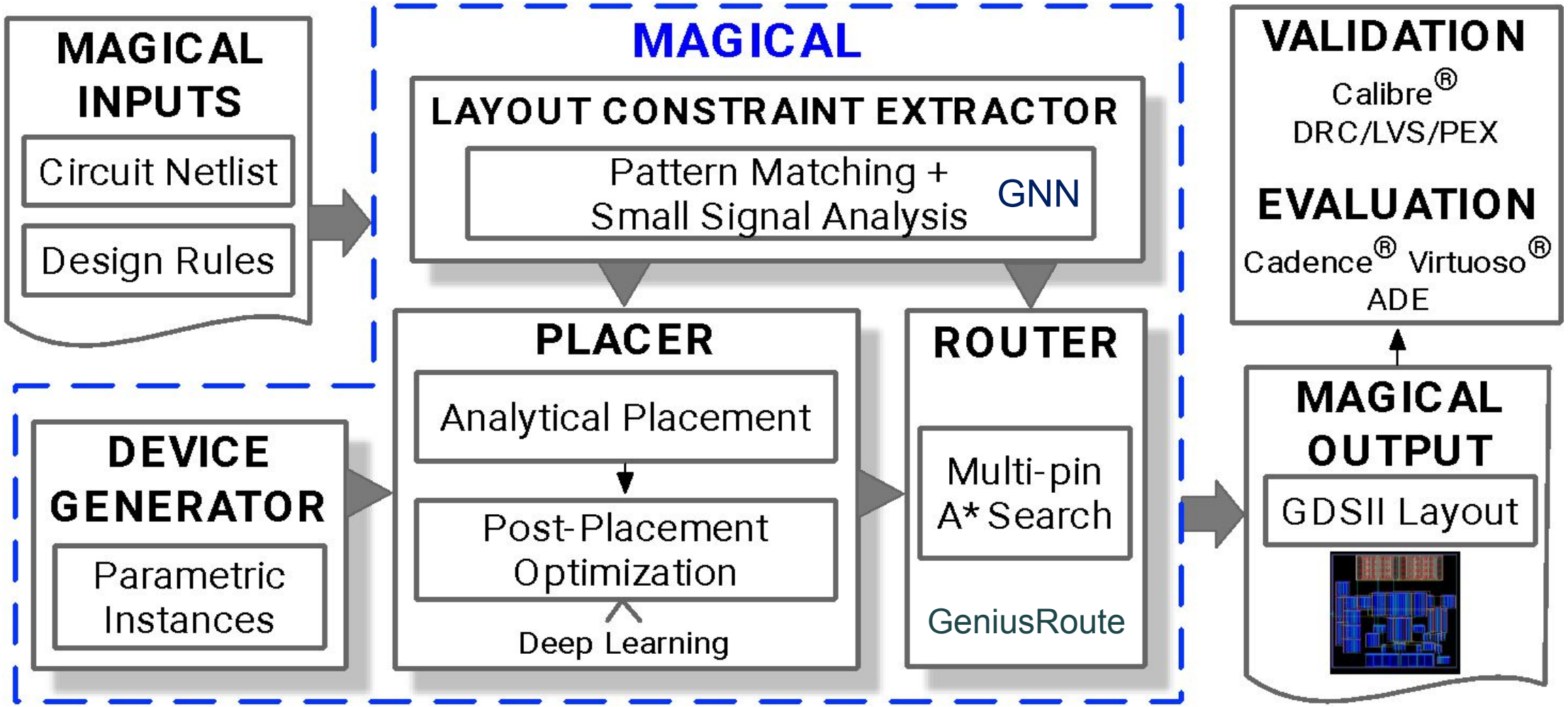


[Razavi, Design of Analog IC]



- Many design specs to juggle
- Heavily rely on designer experience
- Tons of simulations

MAGICAL Layout Automation System

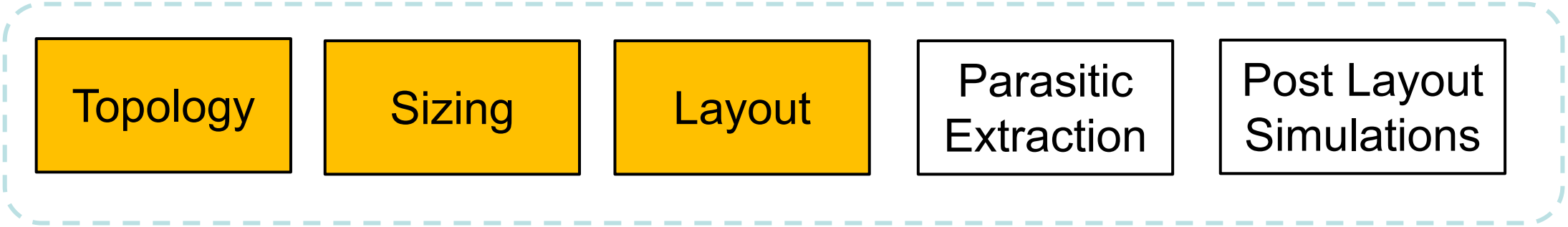


- 20+ papers; open-sourced;
  3 tape-outs proven at TSMC40

https://github.com/magical-eda/MAGICAL

Fork 53 | Starred 221

End to End Analog Design Automation

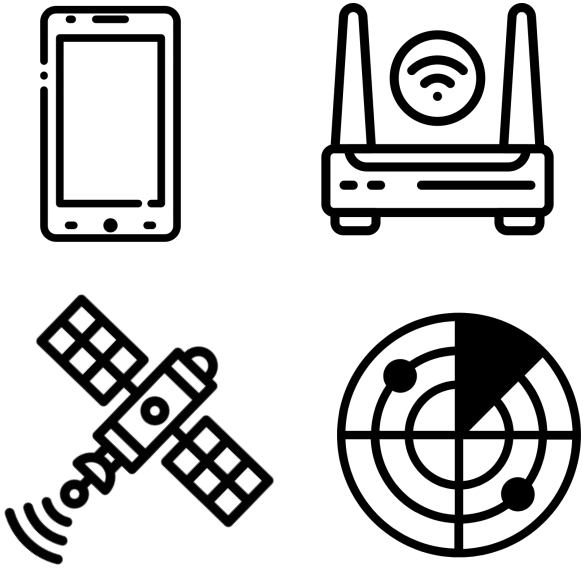


- The overarching goal: an end-to-end analog DA flow?
- **Analog "S&PR" like RTL to GDSII for digital?**

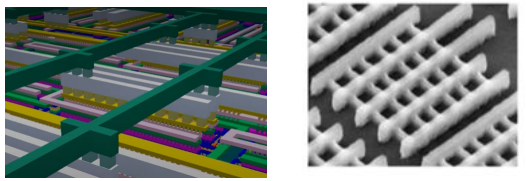
- Multi-fidelity ML guided layout-aware sizing [Budak+, ICCAD'23]
- ML-guided sized topology generation/synthesis [Poddar+, DATE'24]
- LLM for analog design: AnalogCoder [Lai+, AAAI'25 oral]

RFIC (Radio Frequency Integrated Circuit)

- RFIC components are fundamental in wireless systems
- RFIC = actives + passives (often occupying most core chip area)

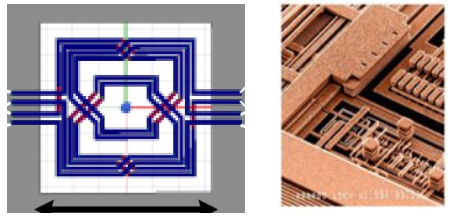


[Behzad Razavi, RF Microelectronics]



Active Components

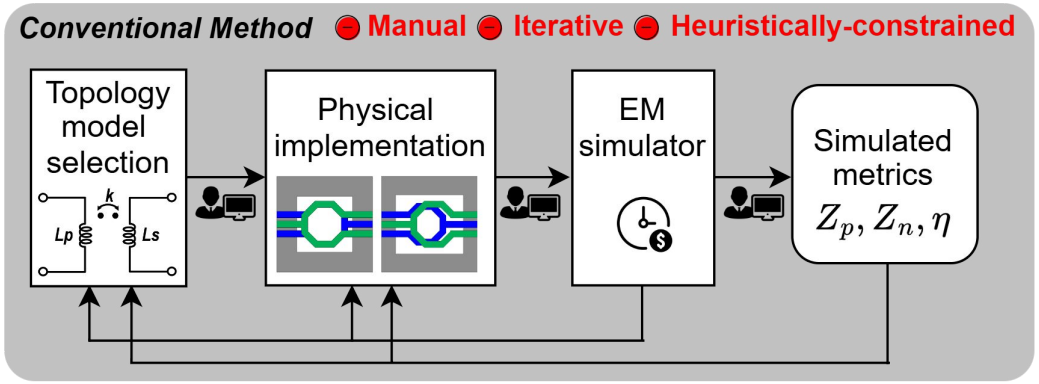
Passive Components

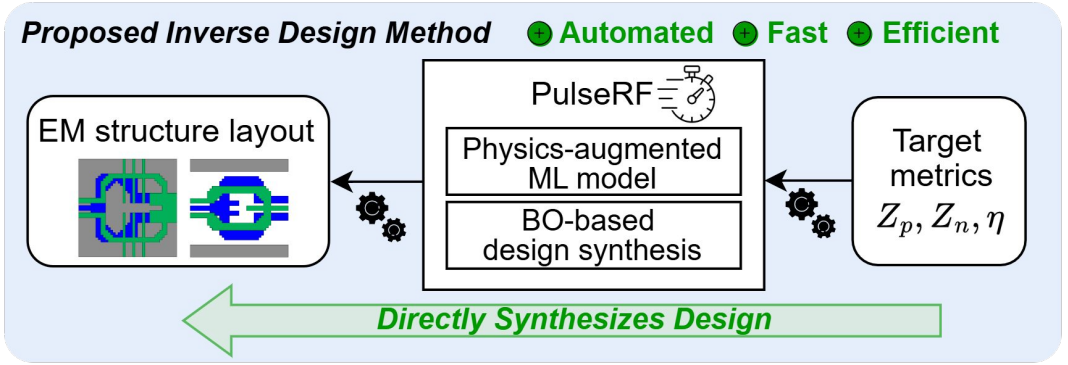


The majority of RFIC design efforts are on passive design, to balance many different objectives: loss, bandwidth, impedance transformation ratio, interface mismatch, …

PulseRF for RFIC Passive Design

- Conventional vs. our PulseRF approach [Chae+, ICCAD'24]





☹ Slow simulation restricts the number of optimization iterations possible

☹ Optimization is confined to a limited set of topology templates

☺ Physics-augmented ML model for fast design evaluation

☺ Bayesian optimization-based inverse design

1st NSTC Jump Start R&D Program: AIDRFIC

Natcast

- **Active**: leverage analog DA
- **Passive:** PulseRF++
- Just scratched the surface!
- **75+ team competed => 3 winning teams**
- **UT Austin team** “GENIE-RFIC: Generative ENgine for Intelligent and Expedited RFIC Design”

NATCAST ANNOUNCES ANTICIPATED AWARDEES, APPROXIMATELY $30 MILLION INVESTMENT THROUGH FIRST NSTC R&D JUMP START PROJECT

October 18, 2024

AIDRFIC awards will propel AI-driven RFIC design innovation, enhance U.S. global competitiveness in semiconductor R&D

WASHINGTON, D.C., October 18, 2024 – Natcast, the purpose-built, non-profit entity designated by the Department of Commerce to operate the National Semiconductor Technology Center (NSTC) established by the CHIPS and Science Act of the U.S. government, today announced three anticipated awardees and approximately $30 million in funding through the Artificial Intelligence Driven RF Integrated Circuit Design Enablement (AIDRFIC) program, the first NSTC R&D Jump Start project. The anticipated awards will revolutionize RFIC design by integrating artificial intelligence (AI) and machine learning (ML) technologies, addressing one of the U.S. semiconductor industry’s most pressing design productivity challenges and strengthening U.S. leadership in broadband, 5G, and next-generation radio-frequency hardware.

Natcast has selected three anticipated proposal teams for award. These teams are led by Keysight Technologies, Princeton University, and the University of Texas at Austin, respectively, and comprise top experts from academia and industry. Projected awards will range from $7.5 million to $10 million each, with projects expected to commence in 2025 and last 30 months. The success of these projects will

3DHI of Everything

- Digital/FPGA, analog, RF, photonics, emerging memory, …
- A lot of “mismatches” and “multi-physics” (thermal, stress, …)
- All kinds of AI-driven EDA tools needed for modeling, optimization, and STCO (system-technology co-optimization)
- NAPMP NOFO of $1.6B to fund 5 R&D areas including EDA

TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC

By Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim

Communications of ACM, Jan. 2014 Research Highlights

Jul 18, 2024

UT’s Texas Institute for Electronics Awarded $840M To Build a DOD Microelectronics Manufacturing Center, Advance U.S. Semiconductor Industry

Interconnected Physical Design

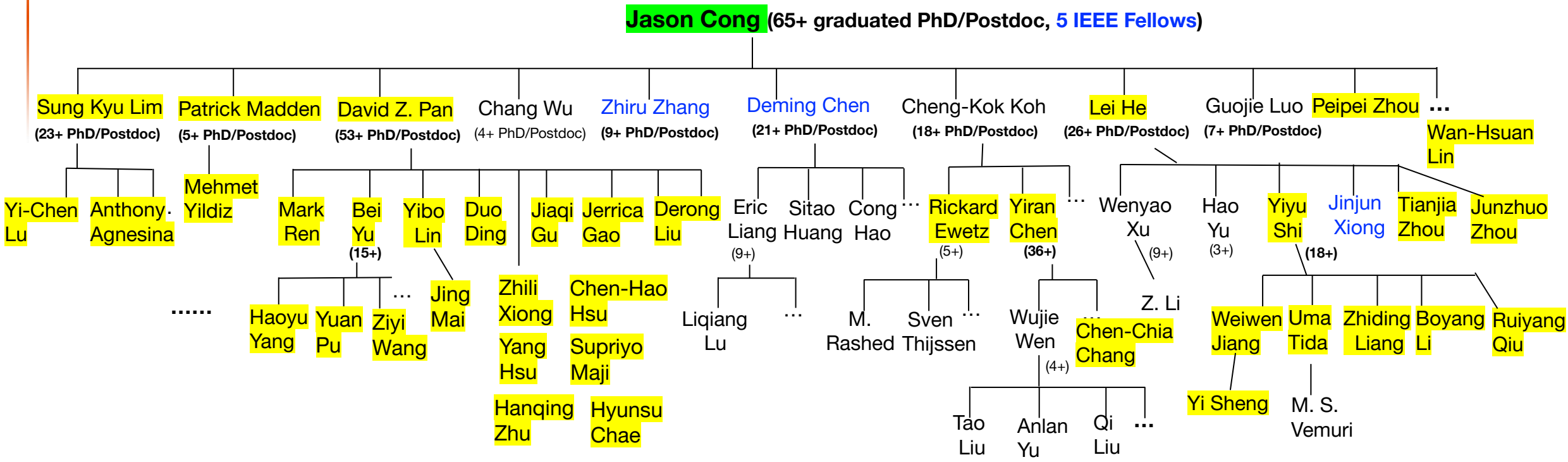
- Prof. Jason Cong has played an instrumental role in shaping the future of "interconnected physical design"
- Through his research group at UCLA + academic descendants

- Classical physical design + interconnect optimization/planning
- Move up with physical aware synthesis
- Move down with DFM/DTCO
- From digital to analog/RF, and emerging technologies
- AI/ML EDA everywhere for QoR and productivity
- ……

Prof. Jason Cong's Academic Family Tree

- 320+ PhDs/postdocs *graduated* in Prof. Cong's academic tree (Cong-tree)
  - **Among them, 80+ professors, 10+ startup co-founders, and many industry leaders (Cadence, Synopsys, Siemens EDA, AMD, Nvidia, Apple, Google, …)**
  - **8 IEEE Fellows, 2 ACM Fellows, …, and many rising stars!**

Prof. Jason Cong's Academic Family Tree



- **38 of them are here today for the Commemoration/Banquet!**

ISPD Trivia: Top 25 Authors per DBLP

8/25 top ISPD authors from Cong-tree!

- Andrew B. Kahng (44)
- David Z. Pan (35)
- Charles J. Alpert (29)
- Martin D. F. Wong (26)
- Evangeline F. Y. Young (26)
- Jiang Hu (26)
- Chris C. N. Chu (25)
- Jason Cong (25)
- Yao-Wen Chang (24)
- Sachin S. Sapatnekar (24)
- Igor L. Markov (21)
- Chung-Kuan Cheng (20)
- Gi-Joon Nam (18)
- Iris Hui-Ru Jiang (18)
- Malgorzata Marek-Sadowska (17)
- Cheng-Kok Koh (16)
- Lei He 0001 (16)
- Sung Kyu Lim (15)
- Majid Sarrafzadeh (14)
- Haoxing Ren (14)
- Jens Lienig (13)
- Patrick H. Madden (12)
- Cliff C. N. Sze (12)
- Patrick Groeneveld (12)
- Bei Yu 0001 (12)

https://dblp.org/db/conf/ispd/index.html

Prof. Cong's ISPD Legacy

- From 2002 to 2024, total 23 ISPD BPAs □ 8 by Cong-genealogy authors (35%)
  - 2024 C-T. Ho, A. Chandna, D. Guan, A. Ho, M. Kim, Y. Li and Haoxing Ren: "Novel Transformer Model Based Clustering Method for Standard Cell Design Automation"
  - 2020 W. Ye, M. Alawieh, Y. Watanabe, S. Nojima, Y. Lin, David Z. Pan, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning"
  - 2017 H. Zhang, F. Zhu, H. Li, E. Young, Bei Yu, "Bilinear Lithography Hotspot Detection"
  - 2014 S. Roy, P. Mattheakis, L. Masse-Navette, David Z. Pan, "Clock Tree Resynthesis for Multi-corner Multi-mode Timing Closure"
  - 2013 H. Xiang, M. Cho, H. Ren, M. Ziegler, R. Puri, "Network flow based datapath bit slicing"
  - 2011 K. Yuan, David Z. Pan, "E-Beam Lithography Stencil Planning and Optimization with Overlapped Characters"
  - 2006 J. Xiong, V. Zolotove, Lei He, "Robust Extraction of Spatial Correlation"
  - 2005 T. Chan, J. Cong, K. Sze, "Multilevel Generalized Force-Directed Method for Circuit Placement"

ISPD'25 BPA candidates all from Cong-tree (Mark Ren and Bei Yu): 9/24=38%

Congratulations Jason!

We are so grateful to have you as our dear advisor, and lifetime mentor & friend!