Innovation in Times of Technology Disruption

A Tribute To Jason Cong And His Contributions To Physical Design Automation

How I Met Jason

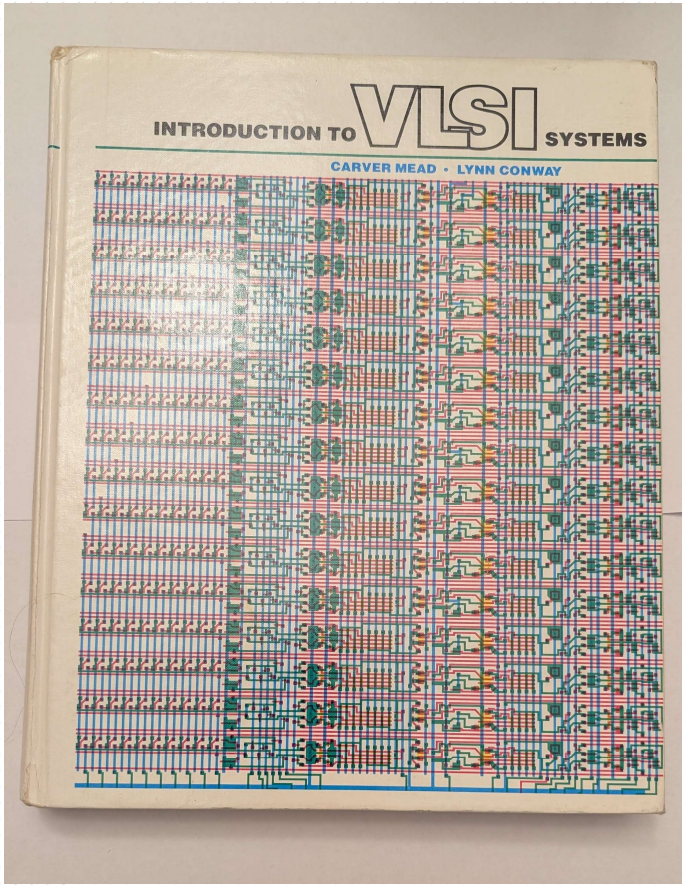
- Jason Was an Intern at Xerox PARC in 1987
- Dave Liu, Jason's PhD Advisor

Disruptive Innovation

- A Lens To View Jason's Contributions To EDA
- Well Studied Business School Topic. Disrupts Industries With Better, Cheaper Offerings
- Times Of Great Innovation And Creativity
- Recent Examples: The Internet And E-commerce
- Jason Is A Master At Finding New Solutions To New Problems
- Trace Three Disruptive Events In EDA and Highlight Jason's Contributions

Mead And Conway's Structured VLSI Design

- Before: Domain of Large Companies, Physicists and Engineers
- Democratized VLSI Design. Made Accessible to Many More People
- Standardized Design Rules, Methodologies, Nomenclature
- DARPA and Others Greatly Increased Funding to Industry and Universities
- Buzz Led to Early CAD Companies: Daisy, Mentor, Valid



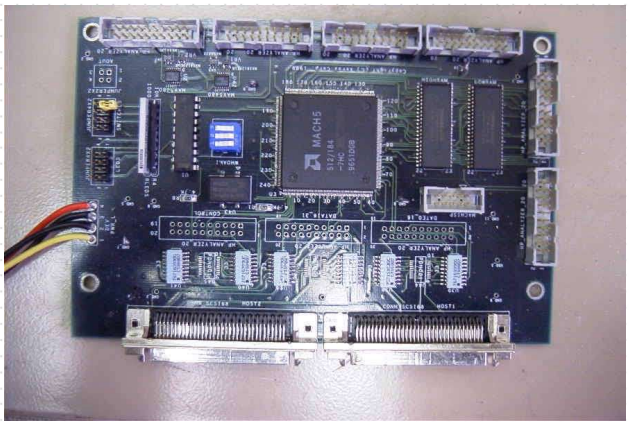
Jason's Response to Disruption

- CAD Companies Didn't Know How to Use University Research
- Mead And Conway Created A Disconnect with Universities
- Jason Found Outlets By Founding Four Companies
  - Aplus Design – Architecture evaluation and FPGA physical synthesis
  - AutoESL – RTL code from behavioral specification in C/C++
  - Neptune Design Automation – Fastest, most scalable physical design tools of its era
  - Falcon Computing Solutions – Compilation tools and accelerators for FPGAs for big data

Another Disruption: Field Programable Gate Arrays

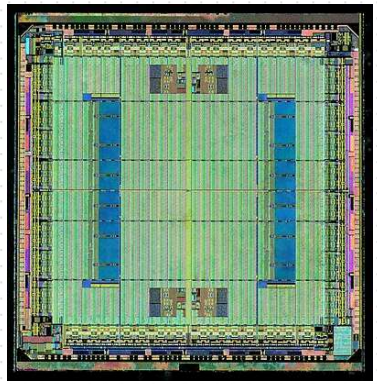
- **Revolutionized Electronic Design: Combines Hardware Performance and Software Flexibility**
- **Enabled Rapid Innovation. Low Volume Shops Could Better Compete**
- **Allowed Design Flexibility, Rapid Prototyping, High Performance**

Xerox PARC Dolphin Processor Board, 1982



Xerox PARC: Airjet Paper Mover Controller, 1990

Jason's Contributions to FPGA Design Automation



Wikipedia: Xilinx Spartan FPGA, Package and Die

- **Depth-Optimal Mapping (FlowMap)**
  - Optimized mapping logic onto FPGAs. Foundation of modern FPGA logic synthesis tools
- **Cut-Enumeration and Boolean Matching**
  - Advanced mapping techniques. Greatly improved efficiency and performance
- **High-Level Synthesis**
  - Opened FPGAs to a whole new group of designers. Designers could start from C/C++ code rather than hardware description languages
- **Interconnect Optimization**
  - Improved circuit placement, timing closure and performance

A Third Disruption: Interconnect Centric Design

- As transistor sizes shrunk, the relative impact of interconnects increased
- In Deep Sub-micron Designs, Interconnection Causes New Problems
  - Timing closure issues: Unreliable performance
  - Increased power consumption
  - Poor signal integrity
  - Difficult to optimize performance

Harry Pregerson Interchange. When interconnection is the problem.

Jason's Contributions to Interconnect Centric Design

- **Interconnect Planning and Optimization**

  Improved performance and reliability by addressing delay, noise and power consumption

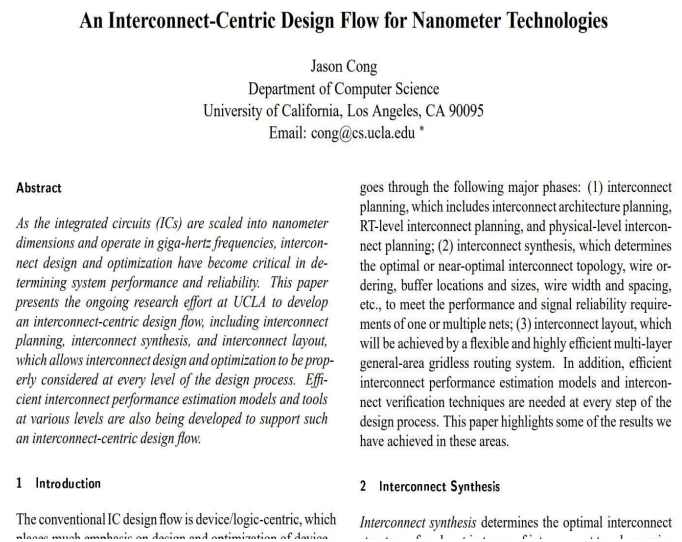
- **Interconnect Performance Estimation Models**

  Created models for accurate interconnect performance estimation. Enabled better planning and optimization

- **Topology Generation and Optimization**

  Developed methods for topology generation, buffer insertion and wire sizing

- **His Innovations Have Been Widely Adopted by The EDA Industry**



An Interconnect-Centric Design Flow for Nanometer Technologies

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Abstract

As the integrated circuits (ICs) are scaled into nanometer dimensions and operate in giga-hertz frequencies, interconnect design and optimization have become critical in determining system performance and reliability. This paper presents the ongoing research effort at UCLA to develop an interconnect-centric design flow, including interconnect planning, interconnect synthesis, and interconnect layout, which allows interconnect design and optimization to be properly considered at every level of the design process. Efficient interconnect performance estimation models and tools at various levels are also being developed to support such an interconnect-centric design flow.

1 Introduction

The conventional IC design flow is device/logic-centric, which

goes through the following major phases: (1) interconnect planning, which includes interconnect architecture planning, RT-level interconnect planning, and physical-level interconnect planning; (2) interconnect synthesis, which determines the optimal or near-optimal interconnect topology, wire ordering, buffer locations and sizes, wire width and spacing, etc., to meet the performance and signal reliability requirements of one or multiple nets; (3) interconnect layout, which will be achieved by a flexible and highly efficient multi-layer general-area gridless routing system. In addition, efficient interconnect performance estimation models and interconnect verification techniques are needed at every step of the design process. This paper highlights some of the results we have achieved in these areas.

2 Interconnect Synthesis

Interconnect synthesis determines the optimal interconnect

Jason's Awards

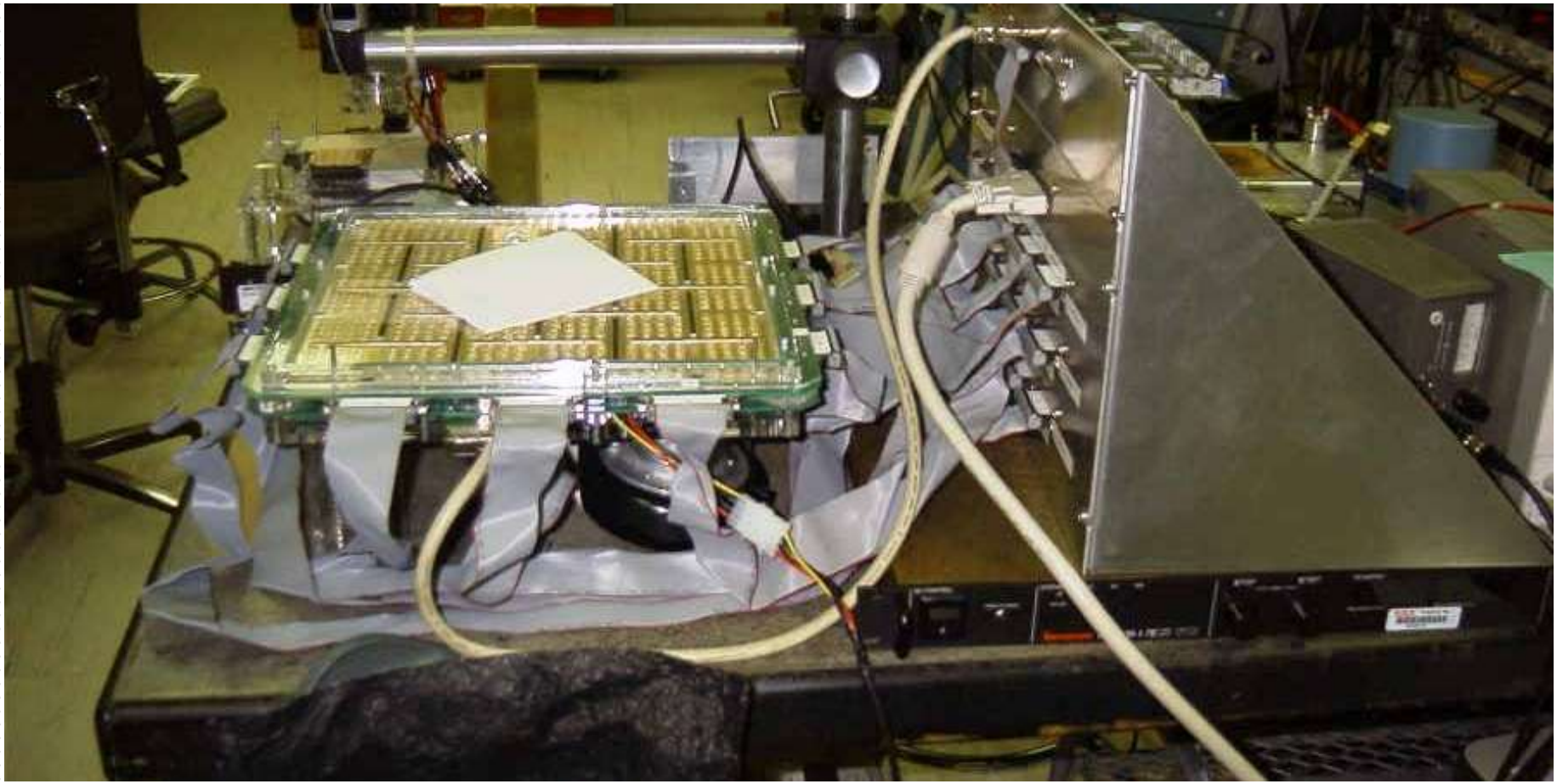
- 2000 IEEE Fellow, 2008 ACM Fellow
- 2010 IEEE CAS Technical Achievement Award
- 2011 ACM/IEEE A. Richard Newton Technical Impact Award
- 2016 IEEE CS Technical Achievement Award
- 2017 Member of the National Academy of Engineering
- 2020 Fellow of the National Academy of Inventors
- 2022 IEEE Robert N Noyce Metal
- 2024 ESDA/IEEE CEDA Phil Kaufman Award
- 18 Best Paper Awards

And Many More. See https://vast.cs.ucla.edu/people/faculty/jason-cong

In Summary

- Jason Has Profoundly Impacted The EDA Industry
- Certainly, Deserves This Lifetime Achievement Award
- I Have Watched Jason's Extraordinary Accomplishments With Pride and Pleasure Over The Years
- I Am Proud To Know Jason And Count Him A Friend
- Thanks For Including Me In Jason's Lifetime Achievement Award Ceremony

Airjet Paper Mover System



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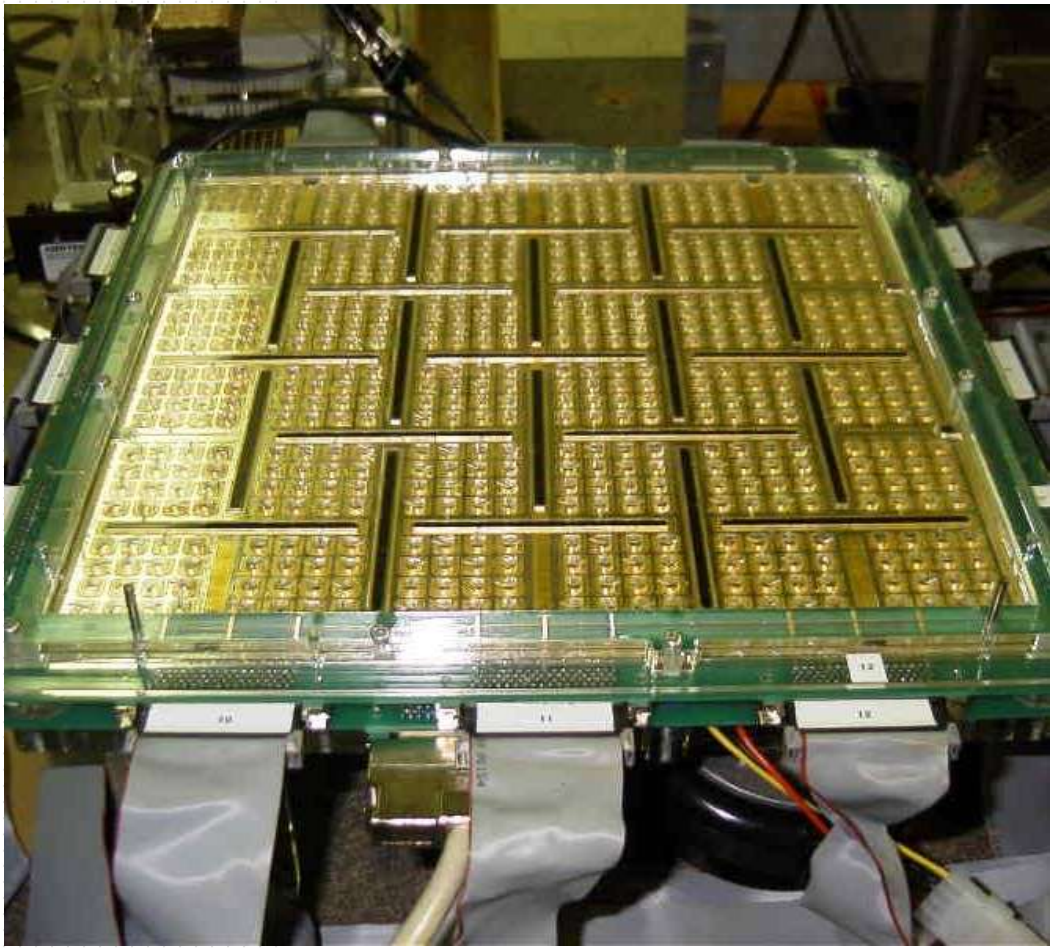

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