Scalable CFET Cell Library Synthesis with A DRC-Aware Lookup Table to Optimize Valid Pin Access

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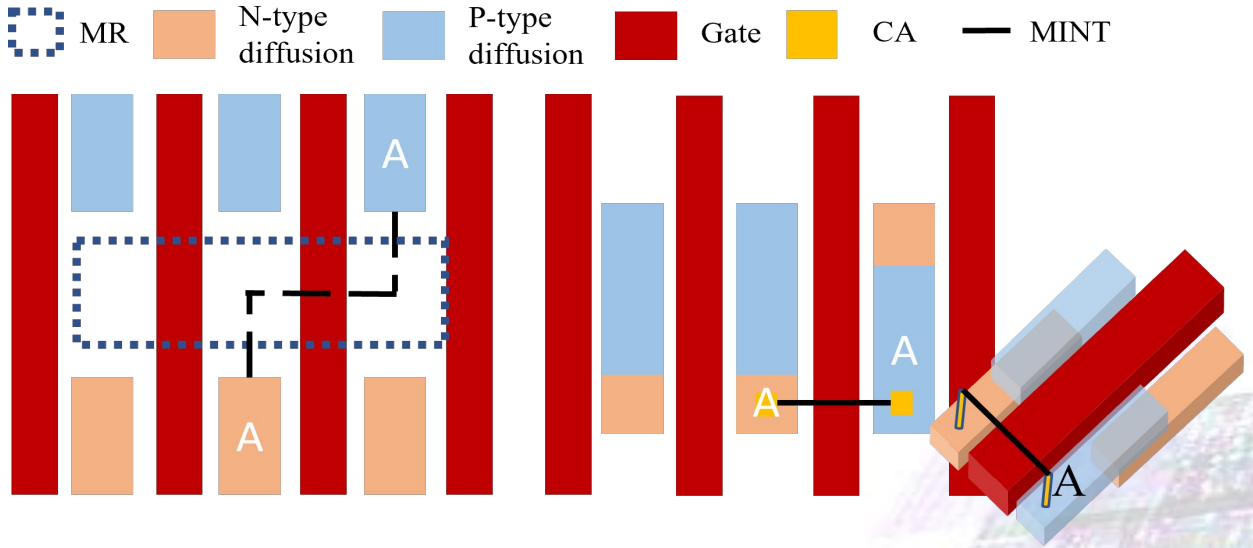
Introduction to CFET stack structure

- Benfit
  - Smaller cell area
  - Flexible M0 layer
- Challenge
  - Reduced routing track
  - Pin accessibility



Benefit of CFET stacking structure. (a) traditional standard cell needs vertical wiring. (b) stacking CFET standard cell does not require the vertical wiring.

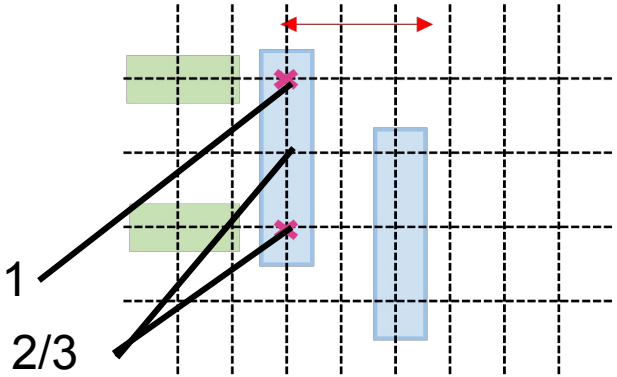
Contribution

- The proposed balanced DRC-aware RPA optimization effectively expels invalid access points by considering the potential DRC caused by blockage and cell pin location.
- Achieves a speed improvement of 100 times compared to the state-of-the-art, while maintaining or surpassing the quality of the generated cells. This advancement enables the synthesis of high-driving-strength cells and complex cell designs.
- Achieves significant improvements in block-level P&R: a 27% reduction in wire length, a 12% reduction in via usage, and a remarkable 99% decrease in DRC violations.

Motivation

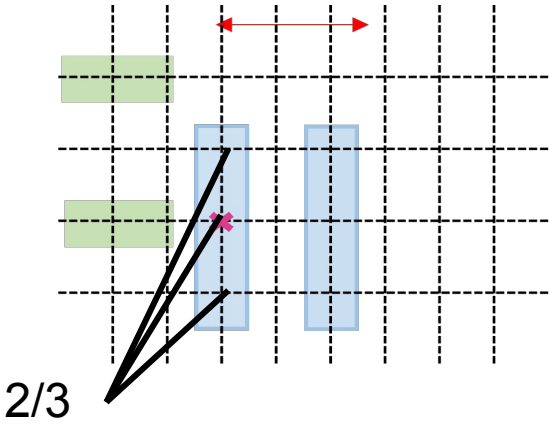
- RPA was proposed by “Pin accessibility-driven cell layout redesign and placement optimization” to estimate the pin accessibility of a pin.
- However, RPA cannot identify the invalid access point due to potential DRC.

RPA:1 + 2/3*2 = 7/3



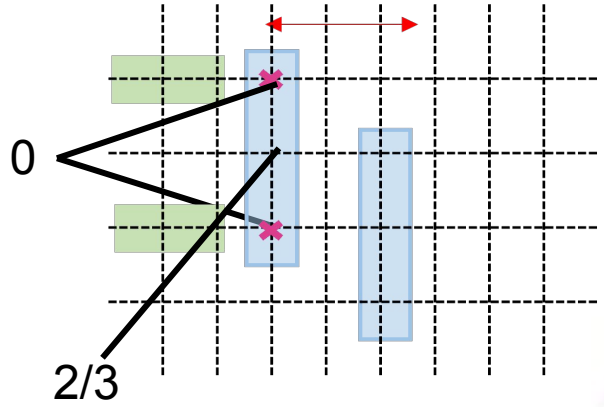
(a)

RPA: 2/3 * 3 = 2



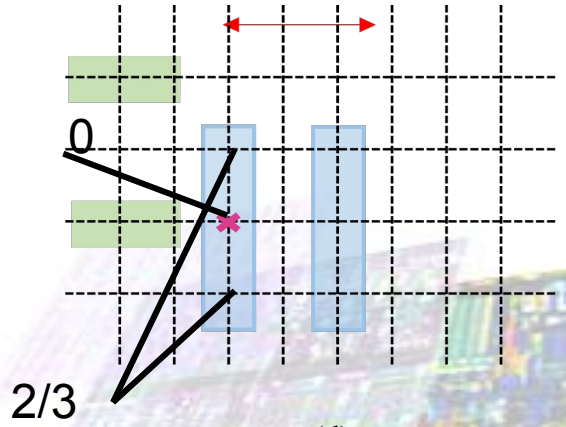
(b)

DARPA: 2/3



(c)

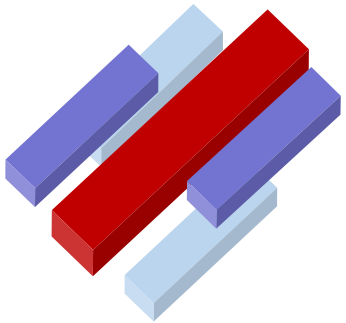
DARPA: 2/3 * 2 = 4/3

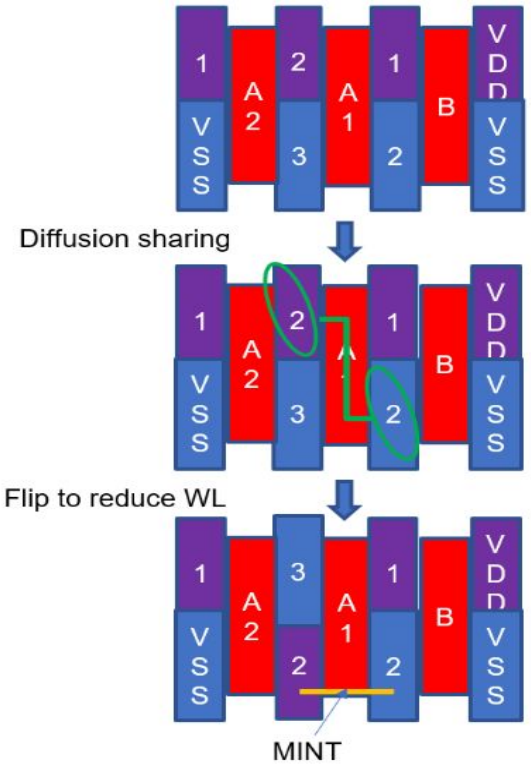


(d)

Methodology

- 2 Stages Flow





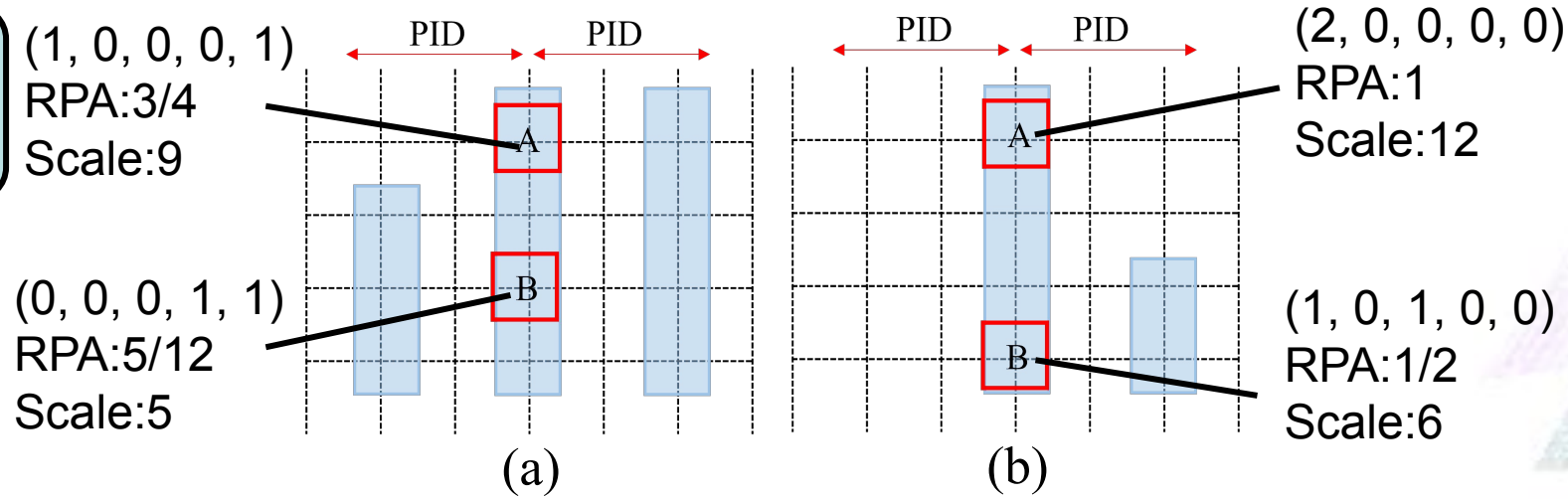
Placement:
- Contact Poly Pitch (CPP)
- Minimum Required Track
- Poly connection density (PCD)

CA allocation by router(SMT based router):
- M2 track
- Balanced-DRC-aware RPA (BDARPA)
- Total Weighted WL

Methodology

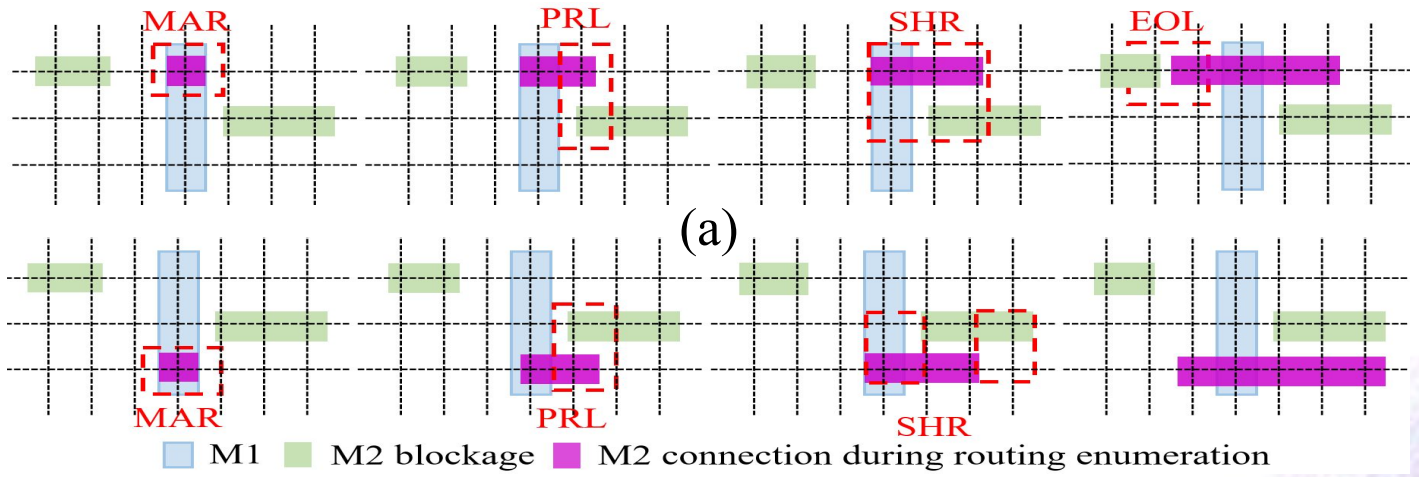
- RPA Lookup Table
  - It is a challenge to optimize RPA for different pin combinations
  - We encode a pin's 2 neighbor (left and right) to a binary vector of length Track + 1, each element *ni* represent #neighbor with length i. *n0+n1+..+nT = 2*, only O(T^2) combinations are calculated
  - we scale the RPA value to integer for each encoded vector to make it possible to speed up.

left A len = 0
right A len = 4
n0 = 1, n4 = 1



Methodology

- DARPA by Simulating Pin Access
  - If the access point trigger DRC violation then set it's DARPRA to 0
  - if the access point is legal, then it's DARPA is RPA
  - We use a simulation space to check DRC for access point w/o adding metal in final synthesis



Examples of DARPA. (a) The access point is deemed invalid by the DRC enumeration; (b) the access point is deemed valid by the DRC enumeration.

Methodology

- Balanced DARPA (BDARPA) Scheme
  - Define DARPA indicator to speed up optimization

$$\mu_{darpa}(n, \delta_{thr}) = \bigvee_{p \in \mathcal{CD}_{pin}(n)} darpa(p) \geq \delta_{thr} \ , \forall n \in \mathcal{N}_{IO}$$

  - Use incremental optimization to make sure each I/O pin is well optimized
    - make last result a hard constraint of next iteration

$$Max \sum_{n \in \mathcal{N}_{IO}} \mu_{darpa}(n, \delta_{thr}), \ \forall \delta_{thr} \in \{12, 24, 36, 48\}$$

Experimental Result

- Efficiently synthesize high-driving strength cells within a short timeframe.
- Enables the synthesis of MBFF within a week.

TABLE 2. CFET SDC COMPARISON.

Cell type/ #Cell	#CPP Ours/[7]	#M2 T Ours/[7]	Total time Ours/[7]	Speed upAvg	Speed up range
AND/3	19/19	0/0	3/67	21	18-23
AOI/2	19/20	1/1	26/483	19	7-40
BUF/4	30/30	0/0	2/68	36	18-45
DFFHQN/1	15/16	0/0	4/6832	1627	1627
FA/1	14/14	2/2	41/6653	160	160
INV/4	23/23	0/0	1/24	22	9-28
NAND/4	48/48	0/0	36/3043	84	22-99
NOR/4	48/48	0/0	11/1991	188	22-270
OAI/2	20/20	0/1	14/665	49	12-65
OR/3	19/19	0/0	3/179	69	31-92
XNOR/1	11/11	1/1	4/977	238	238
XOR/1	11/11	1/1	3/135	45	45
Avg.	9.2/9.3	0.17/0.2	5/704	106	7-1627

TABLE 3. HIGH DRIVNG SDCS AND MBFF.

Name	CPP	#M2 Track	M2 WL	Time (s)
AND2x16	20	0	0	4.9
OR2x16	20	0	0	6.6
BUFx24	30	0	0	6.6
XOR2x16	26	1	4	14.4
XNOR2x16	26	1	42	15.8
DFFHQNx8	24	1	4	14.5
DFFLQNx8	24	1	8	18.4
MBFF2x2	31	1	8	79.6
MBFF4x2	57	2	44	2453.9
MBFF8x2	111	2	126	68840.9

Experimental Result

- Achieve a good reduction in wire length by 27%, a decrease in via count by 12%, and a remarkable 99% reduction in DRC violations on average throughout the block-level placement and routing process.

TABLE 4. P&R RESULT COMPARISON.

Circuit	#DRC Ours/[7]/Reduction	WL [7]	#Via [7]
B15	0/5/100%	1.18	1.12
B17	17/425/96%	1.67	1.10
B18	0/698/100%	1.44	1.16
B19	0/118/100%	1.30	1.11
Avg.	4/311/99%	1.27	1.12

Conclusion

- The experimental results demonstrate that our synthesis methodology is highly scalable and yields cell layouts that are either equivalent to or superior to those generated by [7], but in a more efficient manner. Furthermore, in the P&R stage, we achieve a significant 99% reduction in DRC violations on average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