

Electromigration Assessment in Power Grids with Account of Redundancy and Non-Uniform Temperature Distribution

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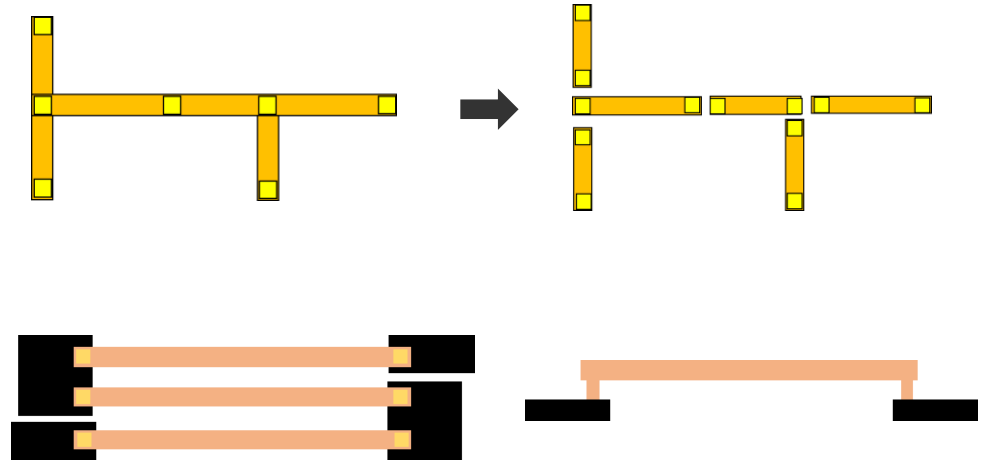
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Outline

- New approach to EM assessment based on IR drop analysis
- Modeling EM stress evolution in interconnect trees and voiding models
- Experimental validation of temperature-aware EM model with grid-like structure
- Validation of EM assessment flow with real silicon power/ground grid degradation data
- Conclusions

Traditional Circuit-Level EM Assessment

- Decompose an interconnect layout into individual segments.
 - Calculate MTTF for each segment
 - The expected lifetime of the overall system is determined from the failure probability of the individual wire segments
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- Motivation for new development: traditional EM design rules are mostly conservative and can result in grid overdesign
 - Correct EM prediction model is required for development of power grid fixing capabilities

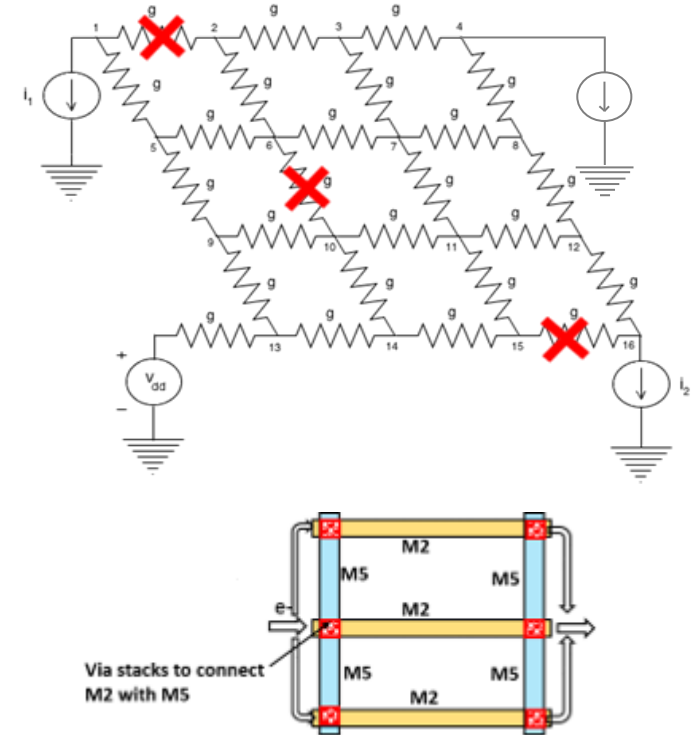


$$MTTF = \frac{A}{j^n} \exp\left(\frac{E_a}{k_B T}\right)$$

$$j_{MAX} = j_{test} \left(\frac{MTTF_{test}}{MTTF_{TARGET}} \right)^{\frac{1}{n}} \exp\left\{ \frac{E_a}{k_B} \left(\frac{1}{T_{use}} - \frac{1}{T_{test}} \right) \right\}$$

Novel approach to EM analysis of p/g grids

- Damage of a single link doesn't imply the grid failure: the redundant paths provide voltage supply to the circuits
- Redundancy allows the electric current to redistribute when the EM induced void causes a local resistance increase
- Grid fails when voltage variation, caused by EM induced increase of resistances, exceeds a designer specified threshold at any node
- The proposed EM assessment methodology is based on analysis of IR drop evolution in the interconnect



B. Li, et al., IRPS 2018

Stress build-up in interconnect trees

- Interconnect tree (IT): the connected metal segments within one layer, confined by the liners
- Korhonen's model is applicable for each branch of the tree:

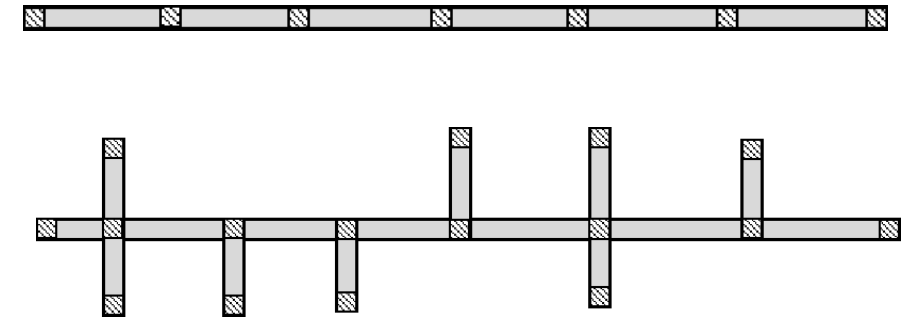
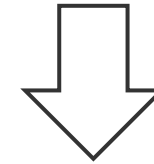
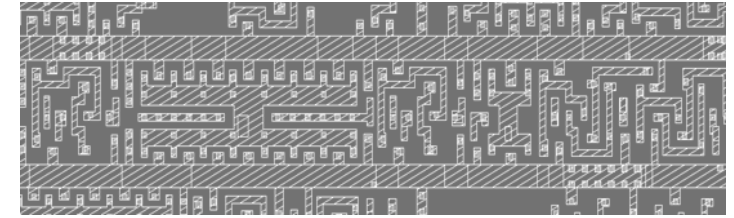
$$\frac{\partial \sigma}{\partial t} = \frac{B\Omega}{k_b T_m} \frac{\partial}{\partial x} \left\{ D_a \left(\frac{\partial \sigma}{\partial x} - \frac{q^* \rho}{\Omega} j \right) \right\} \quad D_a = D_0 \exp \left(-\frac{Q}{k_B T} \right)$$

- Atomic flux continuity in each junction links per-branch stress equations:

$$\sum_k w_{ik} K_{ik} \left(\frac{\partial \sigma_{ik}}{\partial x} \Big|_{x=x_i} - \frac{q^* \rho j_{ik}}{\Omega} \right) = 0$$

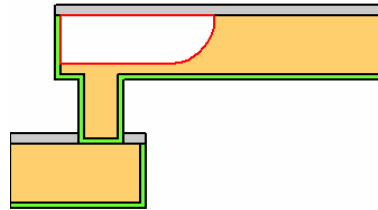
- Void nucleation ($s > s_{\text{crit}}$): flux discontinuity and stress gradients near the void surface

$$\frac{\partial \sigma(t)}{\partial x} \Big|_{x=x_s} = \frac{\sigma(t)}{\delta}$$



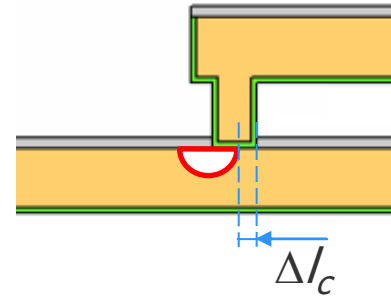
Simulation of EM-induced voltage evolution

- Voiding criteria: stress exceeds critical value



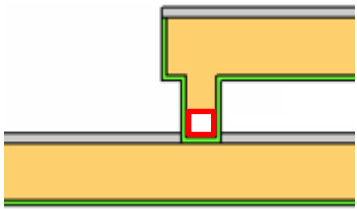
Voided branch:

$$\Delta R(t) = \left(\frac{\rho_{liner}}{S_{liner}} - \frac{\rho_{Cu}}{S_{Cu}} \right) l_v(t)$$



Void under downstream via:

$$G^{Via}(t) = G_0^{Via} |2r_{via} - \Delta l_c| / 2r_{via}$$

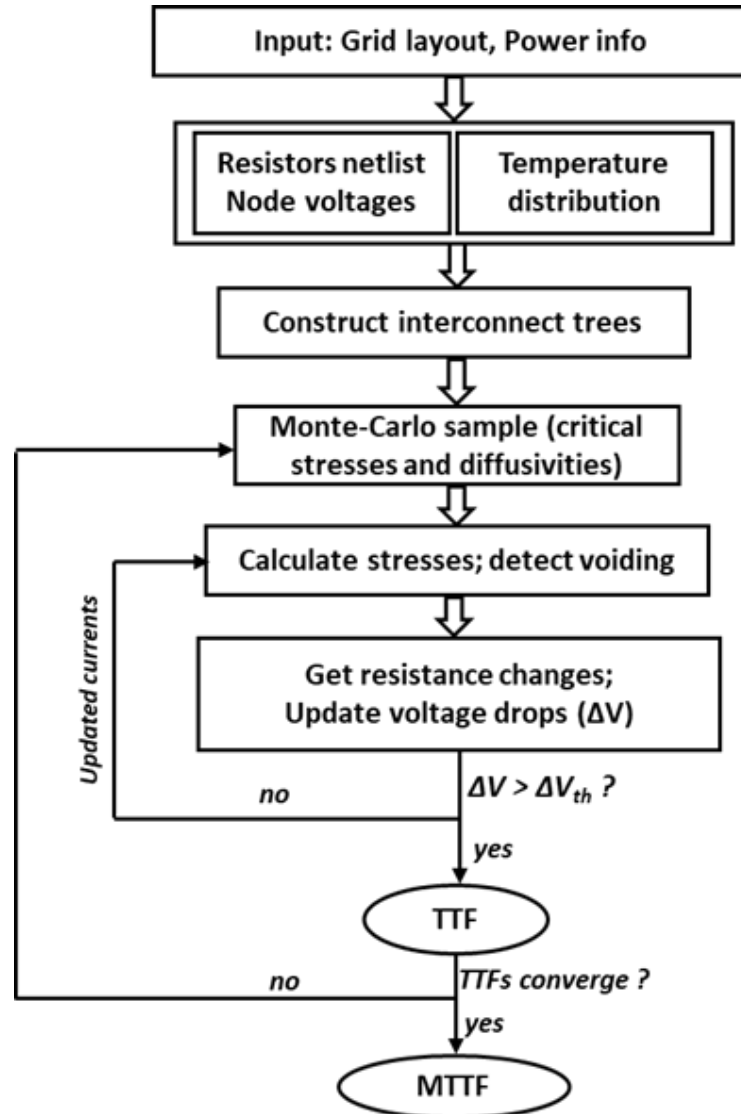


Void in upstream via:

$$\Delta R^{Via}(t) = \frac{\rho_{liner}}{2r_{via} h_{liner} - h_{liner}^2} l_v^{Via}$$

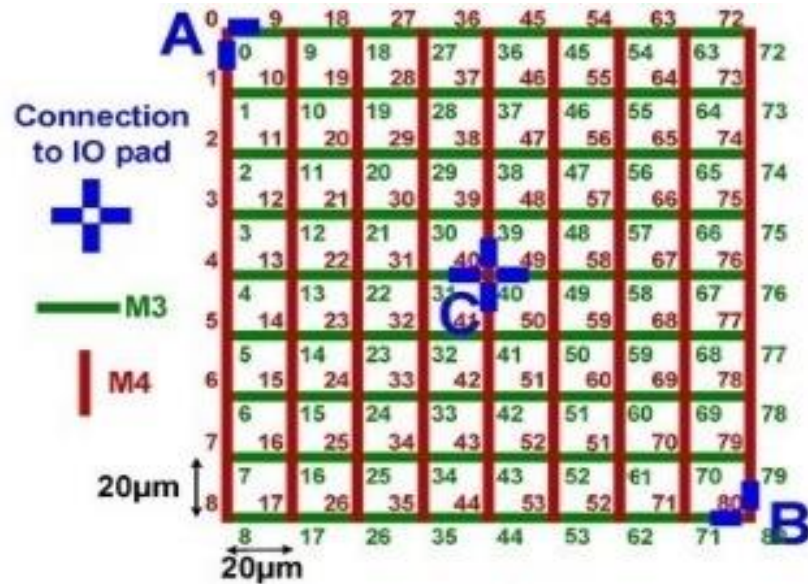
- Initial node voltages $\mathbf{U}$: solve the matrix equation $\mathbf{G} \times \mathbf{U} = \mathbf{I}_s$. $\mathbf{G}$ - conductance matrix, $\mathbf{I}_s$ - vector of current sources (constant)
- Modified voltages $\mathbf{U}_{mod}$: from the matrix equation $(\mathbf{G} - \Delta \mathbf{G}) \times \mathbf{U}_{mod} = \mathbf{I}_s$ (S.Chatterjee, M.Fawaz, and F.N.Najm, ICCAD, 2013)

Temperature-aware EM assessment flow



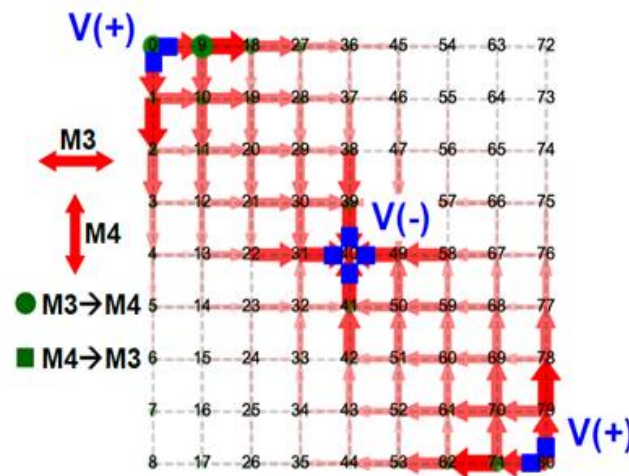
- Resistors netlist and calculated $T(x,y)$ - input for EM stress simulation
- Voltage increase above a threshold – defines time-to-failure (TTF)
- Monte-Carlo loop for statistical analysis (due to random variations of σ_{crit} and D_a)

Model calibration: grid-like test structure



C. Zhou, et al., VLSI Symposium
2018; TDMR 2019

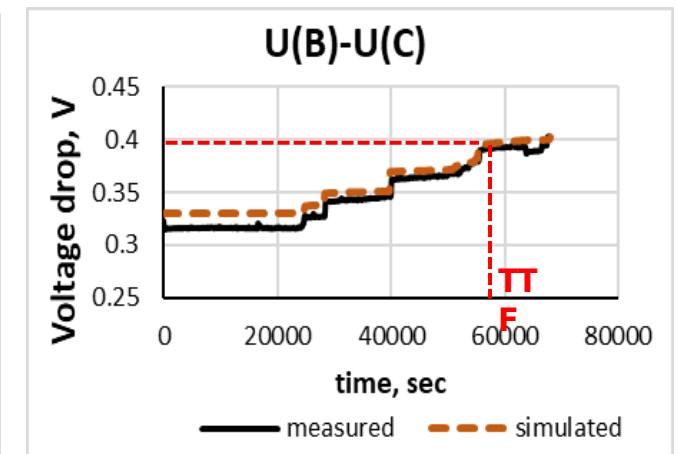
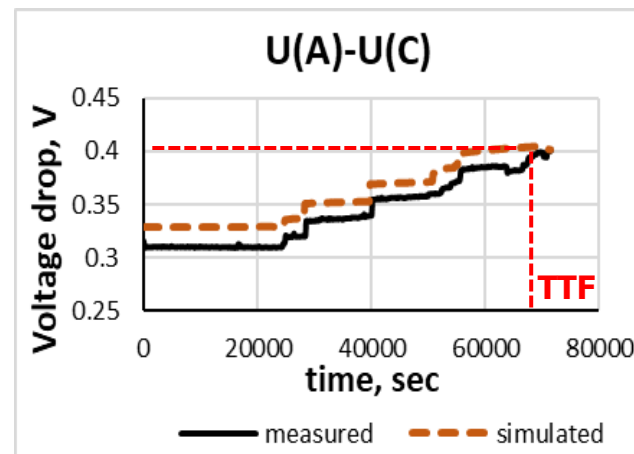
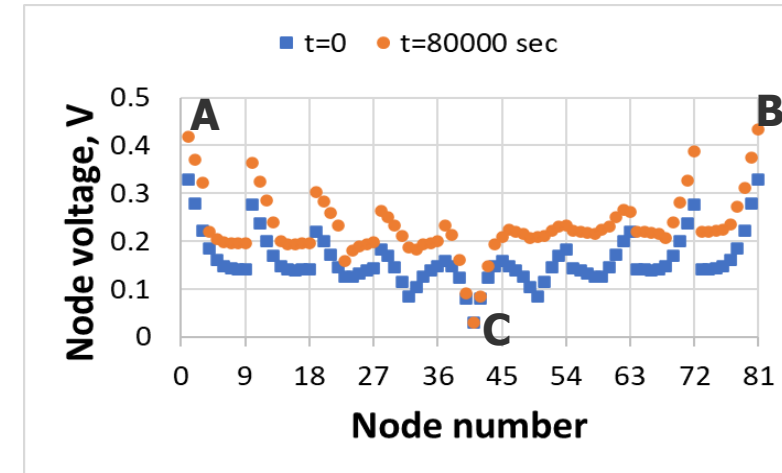
- Two metal layers (M3, M4)
- 3 terminal voltage supply; 10 mA source current
- Analysis with uniform and non-uniform temperature distribution



Many redundant paths exist for
anode-cathode current delivery

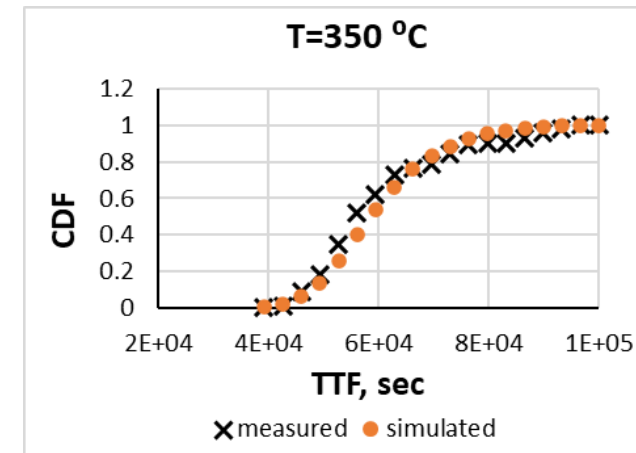
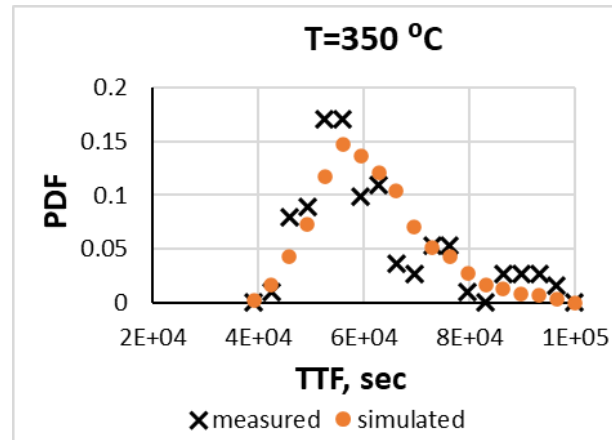
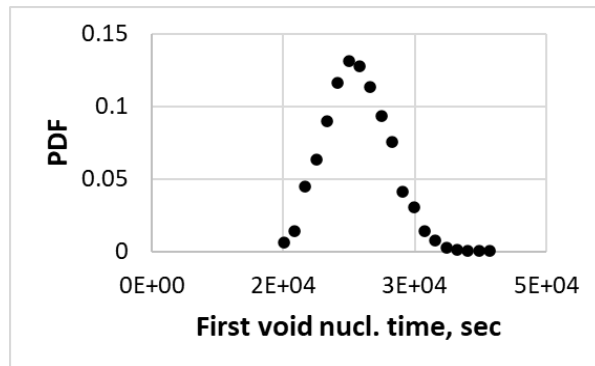
Increase of anode-cathode voltage drop as a grid failure criterion

- Voltage drop evolution between anodes and cathode, $\Delta U(A-C)$ and $\Delta U(B-C)$, characterizes the grid degradation
- The criterion of grid failure $\Delta U(\text{anode-cathode}) > 0.4 \text{ V}$ was accepted
- Good fit between simulated and measured kinetics of voltage drop between both anodes and cathode

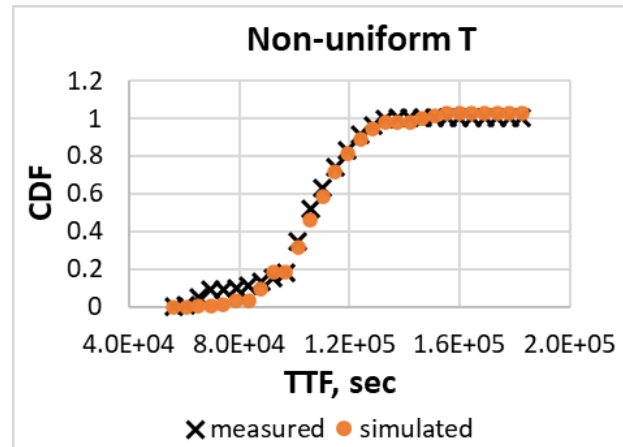
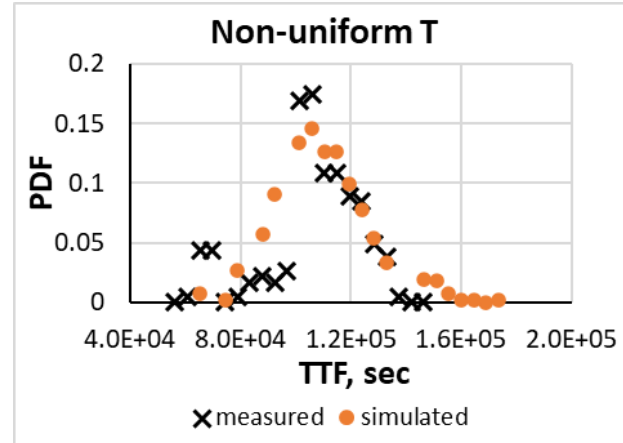
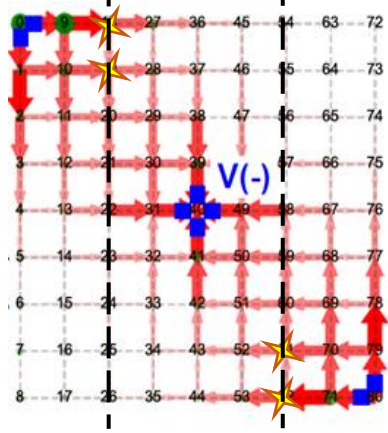
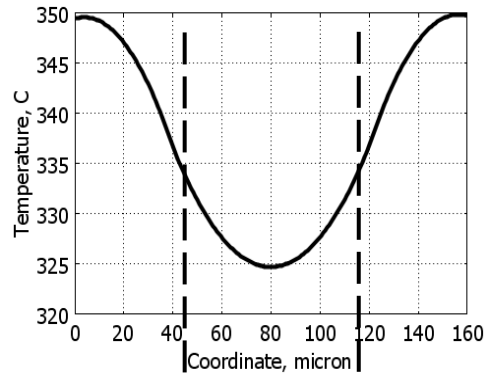


TTF statistics for the grid at uniform temperature (T=350°C)

- Lognormal distribution for σ_{crit} providing $\langle \sigma_{\text{crit}} \rangle = 300$ MPa and $\text{stdev} = 60$ MPa
- Normal distribution for diffusion activation energy: $\langle Q \rangle = 0.95$ eV, $\text{stdev} = 0.005$ eV
- MTTF with uniform T is $\sim 6 \cdot 10^4$ sec

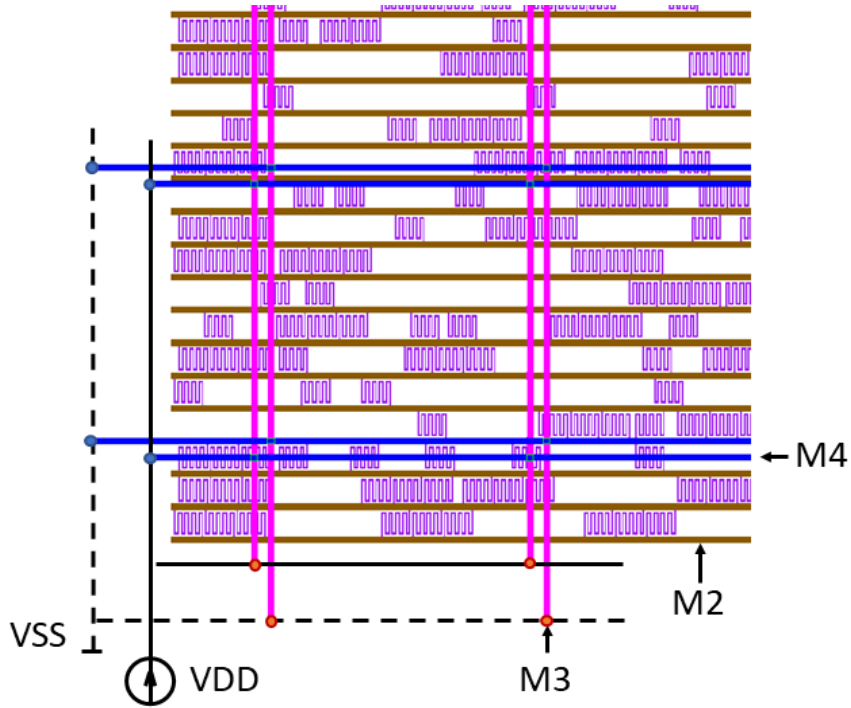


Effect of non-uniform temperature on TTF distribution

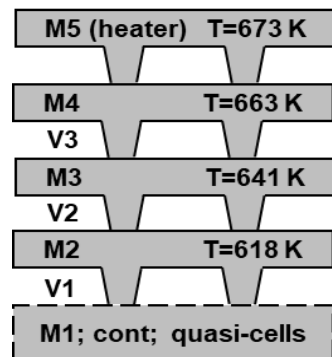


- Increased voiding probability in vicinity of anodes – due to atomic flux divergency caused by ∇T
- MTTF shift to 10^5 sec – caused by decreased temperature in the central section, and by the changed voiding locations

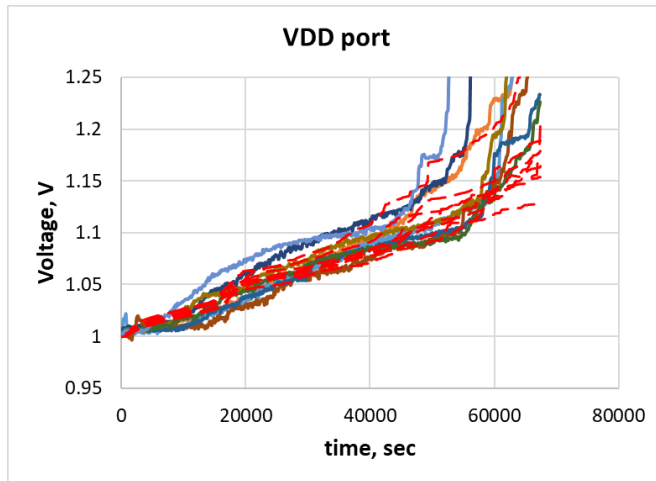
Model validation using on-chip power/ground test grid



- “Quasi-cells” with high-resistance poly-resistors replaced real circuits, for accelerated EM tests at $T \sim 350^\circ\text{C}$
- Contains layers M1-M4; layer M5 serves as heater
- Connectivity to VDD/VSS external ports through M3 and M4 rails
- High current densities up to $2 \cdot 10^{11} \text{ A/m}^2$ causes fast EM degradation of the rails



VDD port voltage evolution



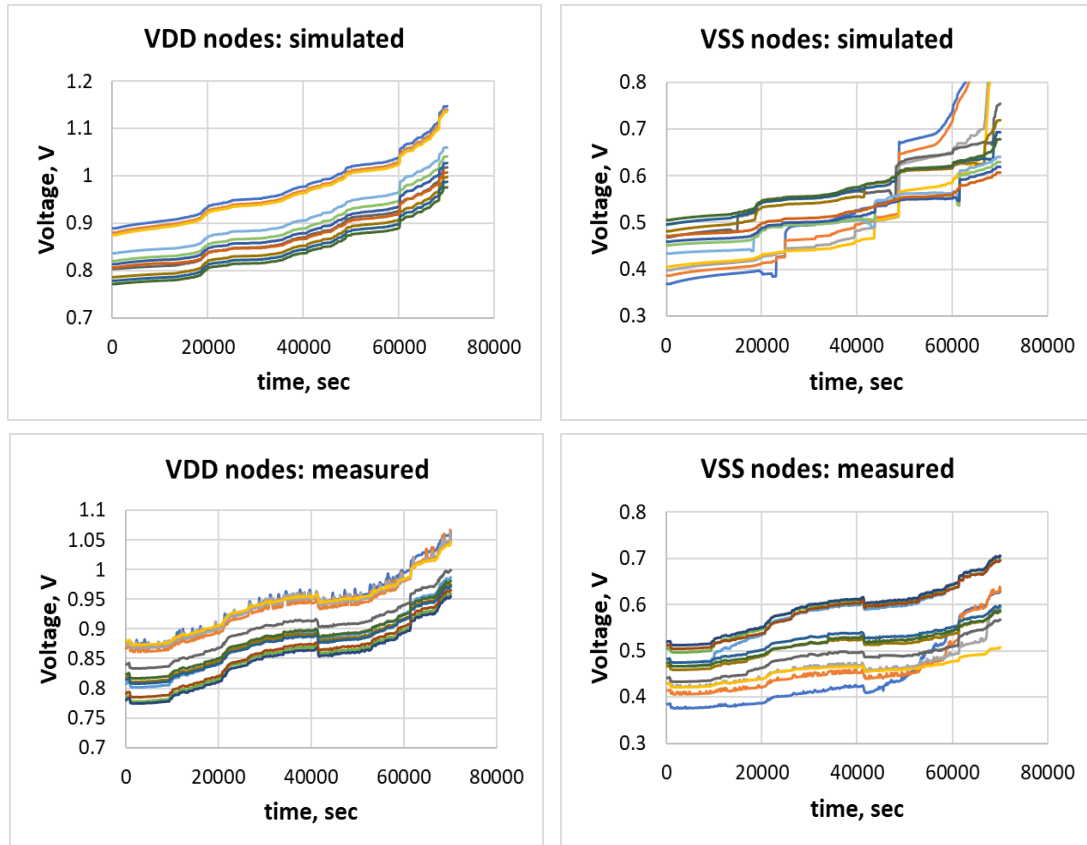
Simulated voltage evolution (dashed lines) vs measured data (bold lines) on VDD port

- VDD port voltage evolution characterizes overall grid resistance increase
- Calibrated critical stress:
 $\langle \sigma_{\text{crit}} \rangle = 160 \text{ MPa}$ and $\text{stdev} = 50 \text{ MPa}$
- Diffusion activation energy: $\langle Q \rangle = 0.93 \text{ eV}$, $\text{stdev} = 0.005 \text{ eV}$

Voiding statistics for one Monte-Carlo sample

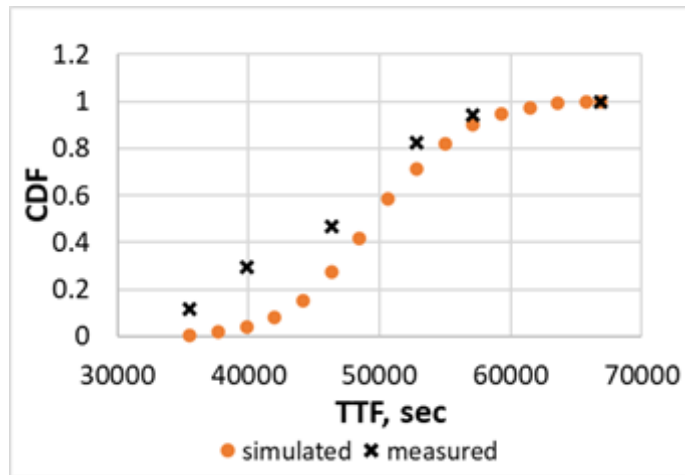
Via type	Number of voids
V3: M3-M4 upstream vias	86
V3: M4-M3 downstream vias	29
V2: M2-M3 upstream vias	67
V2: M3-M2 downstream vias	136

Analysis of the results: simulation vs measurement



- Gradual voltage increase in VDD nodes: degradation of the net due to voiding in upstream vias
- EM failure of VSS net is caused mainly by undercutting the downstream vias - resulted in abrupt voltage changes

TTF distribution and MTTF for the power/ground grid



	measured	simulated
MTTF	50418 sec	50368 sec
Stddev of TTF	9410 sec	5670 sec

- Good fit between simulated and measured MTTF and stddev of TTF
- Future work: get more experimental data and elaborate more accurate procedure for model parameters calibration

Conclusions

- EM assessment of the power grid includes numerical analysis of stress build-up in interconnect trees and compact models for void evolution
- Temperature gradients are able to change voiding locations due to creation of atomic flux divergency
- TTF of the grid is defined by EM-induced increase of voltage drop
- MTTF is determined by statistical distributions of critical stress and diffusivity
- Direct comparison of simulation results with measurements has demonstrated validity of the developed assessment methodology

Thank you !