Challenges for Interconnect Reliability: From Element to System Level

O. Varela Pedreira[1], H. Zahedmanesh[1], Y. Ding[1,2], I. Ciofi[1], K. Croes[1]

[1] imec, Leuven, Belgium

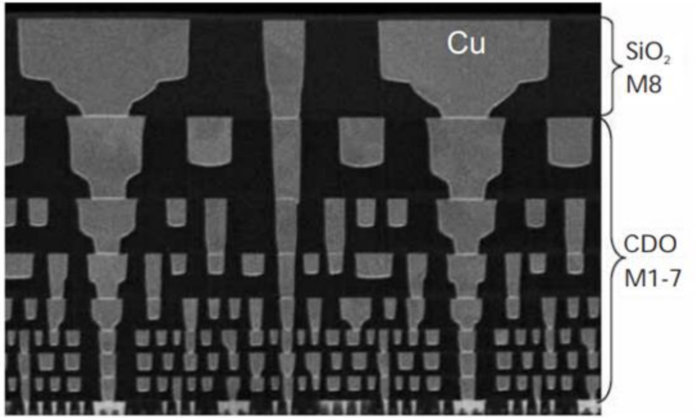
[2] Department of Materials Engineering, KU Leuven, Leuven, Belgium

Introduction

- Interconnects: structures that connect electrically elements from an integrated circuit

- Function: transmit and distribute signals and power across the circuit

- Back-end stack is formed by:
  - Conductive metal lines to transport charges
    - Al, Cu,...
  - Dielectric to isolate metal lines
    - SiO_2, low-k's, airgap (ultimate solution)

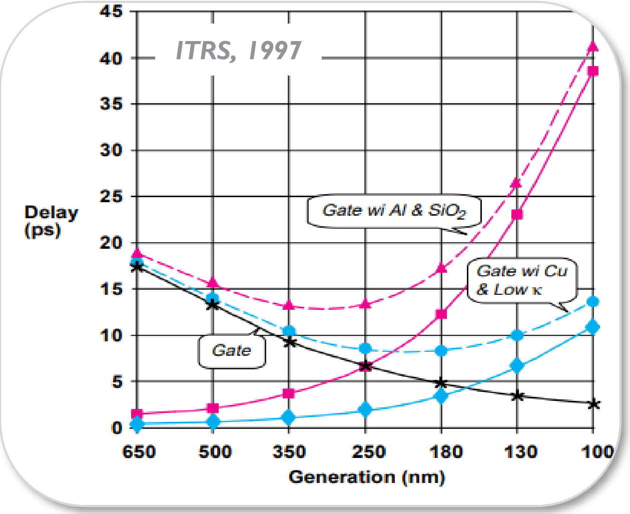


SEM image of INTEL 45nm Cu/low-k interconnect stack (Ingerly, D. et al., IEEE IITC 2008)

public

Introduction

- Interconnect scaling limits the circuit performance
  - Smaller Cu cross-sectional areas → ↑R_{line} & ↑R_{via}
  - Small spacing → ↑C
- Impact of scaling in reliability
  - ↑ current densities → ↑ Joule Heating
  - ↓ EM lifetimes
  - ↓ TDDB lifetime



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Interconnect scaling: Impact on reliability

- Einstein equation for mass transport:

$$J_{mass} = \frac{DC}{k_B T} \cdot \left[Z^* \mathrm{q}\, \rho\, \mathrm{j_e} - \Omega \cdot \nabla\sigma + \frac{Q^*}{T} \nabla T \right]$$

D is diffusion term = $D_o \exp\left[-\frac{E_D}{k_B T}\right]$

C is concentration of atoms

Electromigration

Stress voiding

Part of the Qualification process

Thermomigration

From single-link EM towards system level EM

Impact of thermal gradients on metal migration

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Outline

- Impact of thermal gradients on metal migration
  - Motivation
  - Test structure
  - Model approach
  - Experimental approach & failure analysis
- System level Physics-based EM modelling
  - Motivation
  - Model description
  - Case study: Power delivery network (PDN)
- Conclusion

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Outline

- **Impact of thermal gradients on metal migration**
  - **Motivation**
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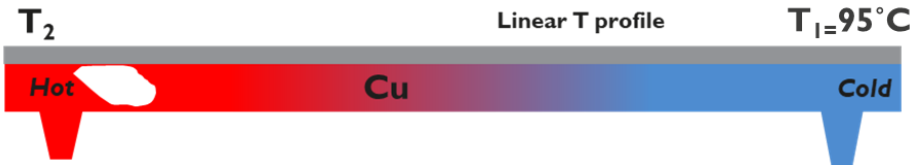
Motivation
Thermomigration

- Gradient in temperature acts as an external driving force for atom movement
  - Atoms preferentially move from hot regions to cold regions
    - Higher probability of dislocation for atoms in hot regions



- Result is net diffusion (mass transport) in the direction of the negative temperature gradients

$$F_{TEMP} = \frac{Q^*}{T} \nabla T$$

With Q^* the heat of transport (in kJ/mol)

Zahedmanesh H. et al., Micro Rel, 2020

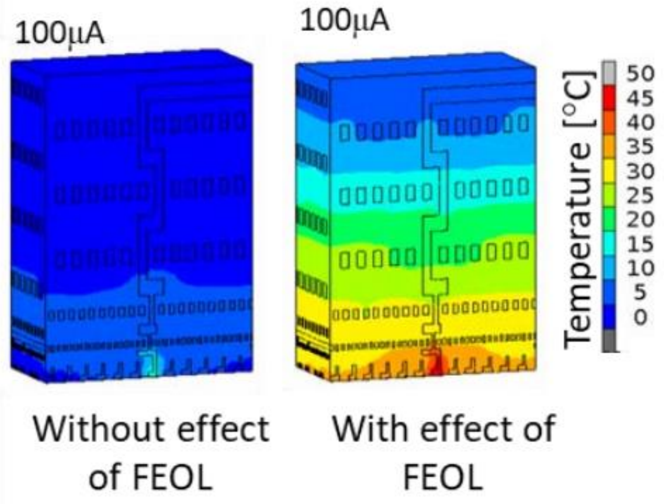
public

Motivation

Why are thermal gradients becoming relevant?

- Joule heating in scaled interconnects is enhanced by:
  - BEOL
    - Drastic increase of current density
    - Increase resistivity of used metals (Ru, Co, Cu)
    - Poor thermal conductivity for porous dielectrics (low-k)
  - FEOL:
    - Transistors are closer to BEOL
    - Higher clock frequencies generate hot spots

Temperature increase in the BEOL for overmolded package with natural convection (cooling):



Lofrano M. et al., iTherm, 2022

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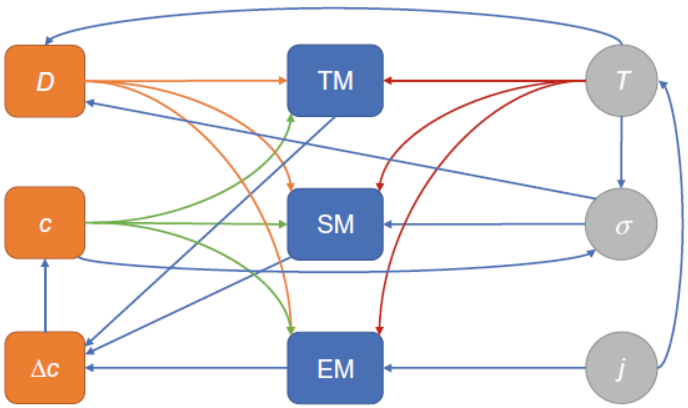
Motivation

Why are thermal gradients becoming relevant?

- Synergy between mechanisms



Lienig J., Thiele M., "Fundamentals of Electromigration-Aware Integrated Circuit Design", 2018

  - Interaction and coupling between TM, SM and EM which would be further enhanced by temperature gradients

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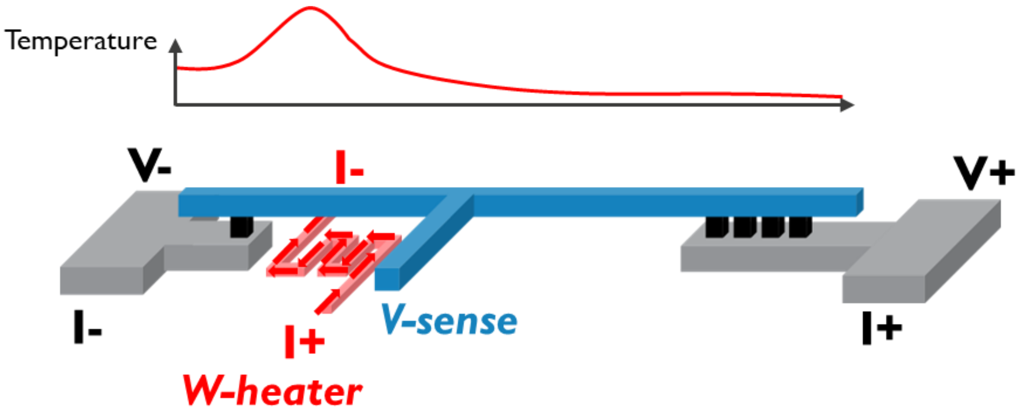
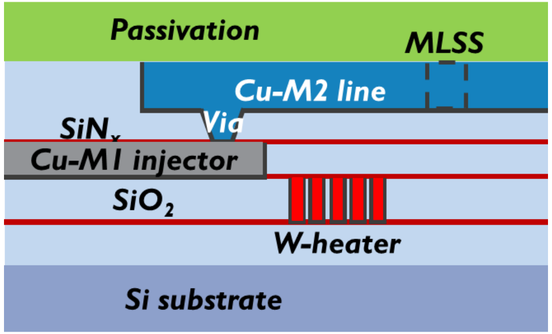
How to assess the impact of temperature gradients?

- Special test structure that allows void kinetics studies
  - W-heater allows to locally heat up a portion of the M2 level





Ding Y. et al., Microelectronics Reliability 2022

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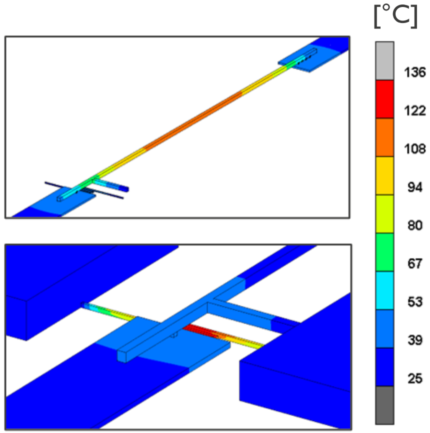
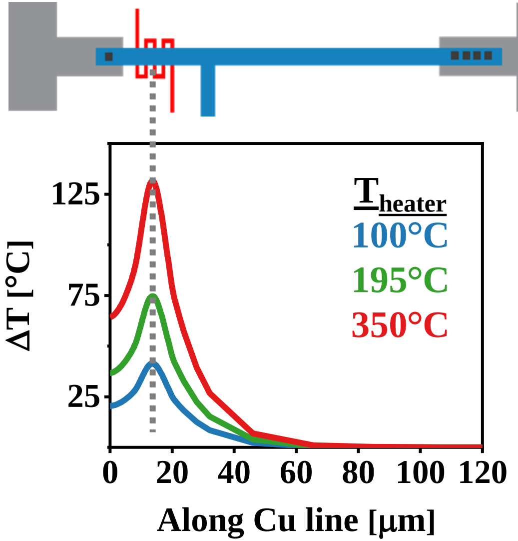
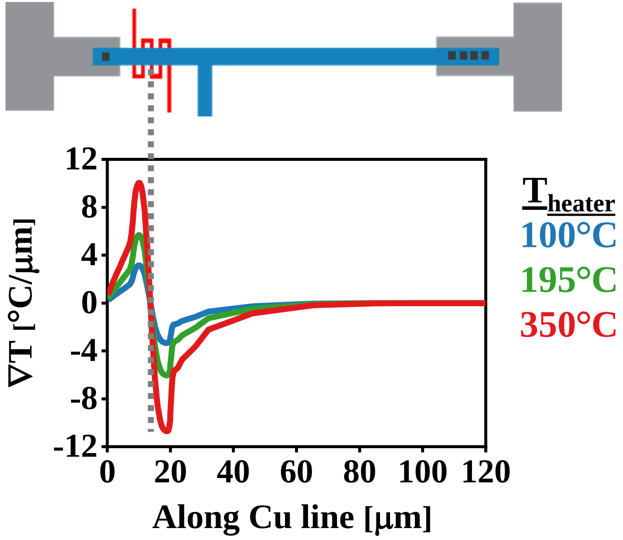
How to assess the impact of temperature gradients?

Combined modelling approach

1. Finite Element thermal model calibrated with Si data
   - Output
     - Joule heating: average temperature increase at the W-heater and Cu-line
     - Temperature gradient: calculation based on the temperature profile along the Cu-line







Ding Y. et al., Microelectronics Reliability 2022

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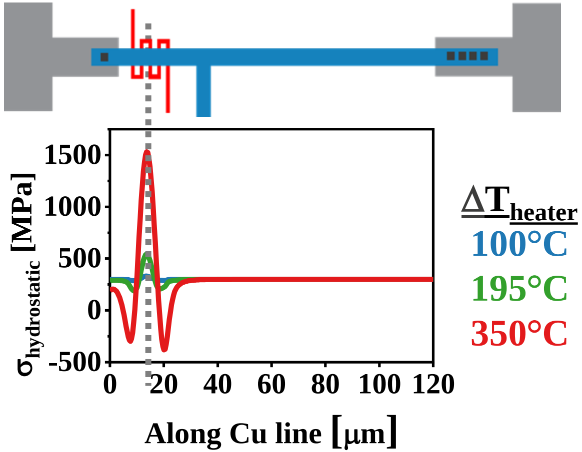
How to assess the impact of temperature gradients?

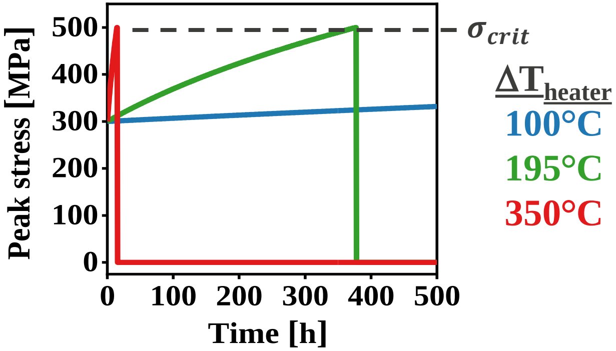
Combined modelling approach

2. 1D numerical TM model:
   - Stress change in the interconnect under TM+SM
   - Outputs:

$$\frac{d\sigma}{dt} = \frac{d}{dx}\left(\frac{DB\Omega}{k_B T}\left(\frac{d\sigma}{dx} - \frac{Q^*}{\Omega T}\frac{dT}{dx}\right)\right)$$



Model estimates the void location at the Cu line above the heater.



Faster void formation for ↑ΔT@ heater

Ding Y. et al., Microelectronics Reliability 2022

Zahedmanesh H. et al., Microelectron. Reliab., 2020

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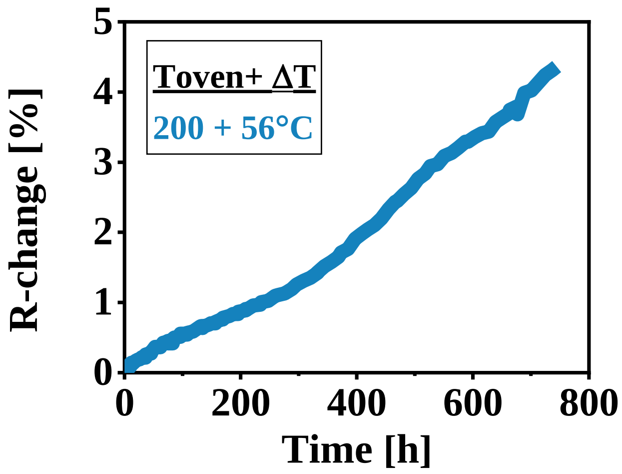
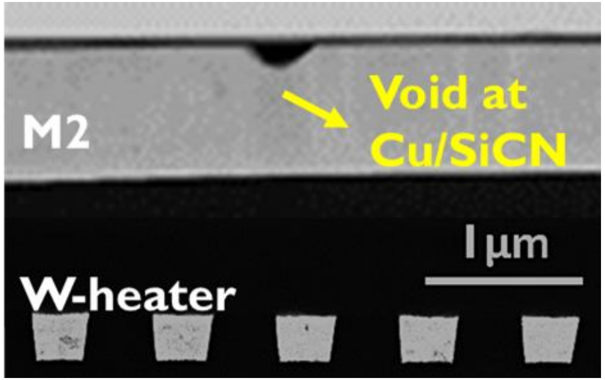
Experimental results

Ding Y. et al., IEEE IRPS 2023

- Package level with:
  - T_{oven} = 100, 150, 200 °C
  - ΔT@M2 = 37-76 °C
- Continuous R-change monitoring:



- FIB/SEM images show **voids at M2 on top of the heater** → confirms model predictions



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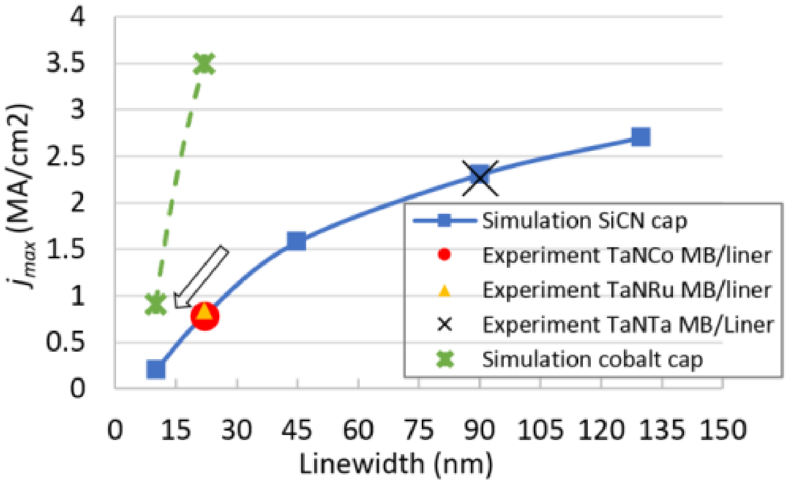
Metal reliability: impact of scaling

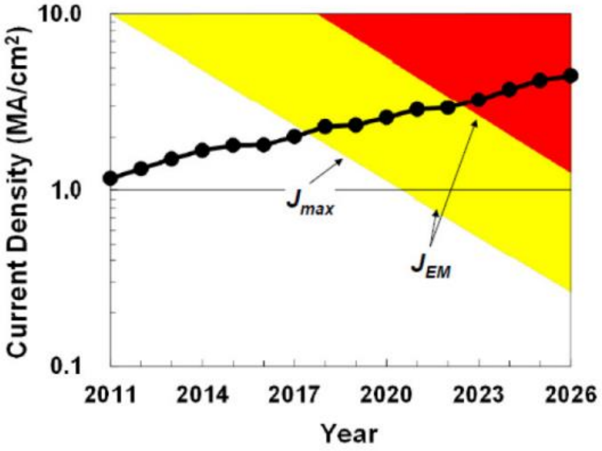
Electromigration

- Abrupt degradation of J_{MAX} with line width
  - $J_{MAX} < 1MA/cm^2$ at 22nm CD



Zahedmanesh H. et al., IEEE IITC 2019

- On future nodes J_{MAX} is expected to exceed J_{EM}



ITRS, 2015

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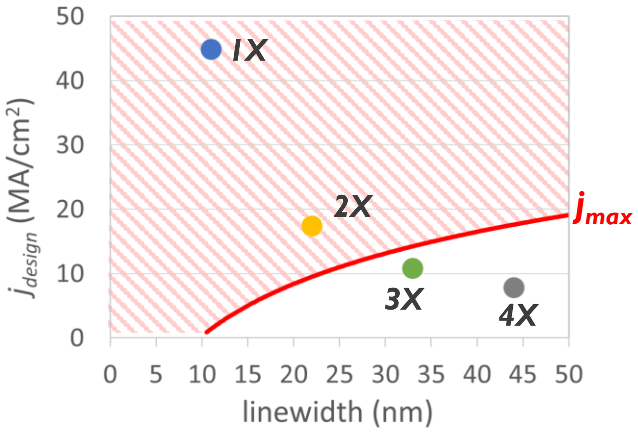
Metal reliability: impact of scaling

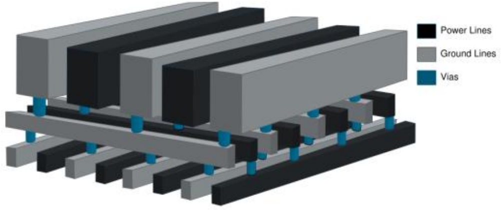
The inflection point of J_{MAX} and J_{design}

- The standard design approach for EM is based on $J_{single\text{-}wire} < J_{MAX}$ criterium
- Dilemma for EM predictions as single isolated interconnect EM tests may not be readily translated into metrics for interconnect network systems.

* j_{design} values for Ring Oscillator operation



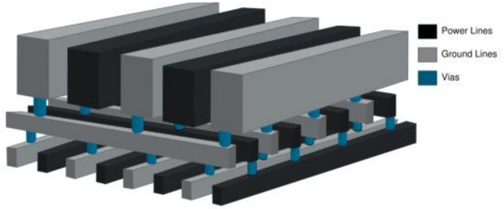
Zahedmanesh H. et al., 2023, in press

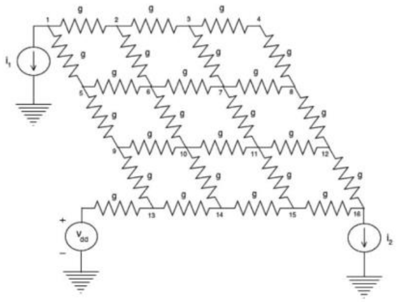


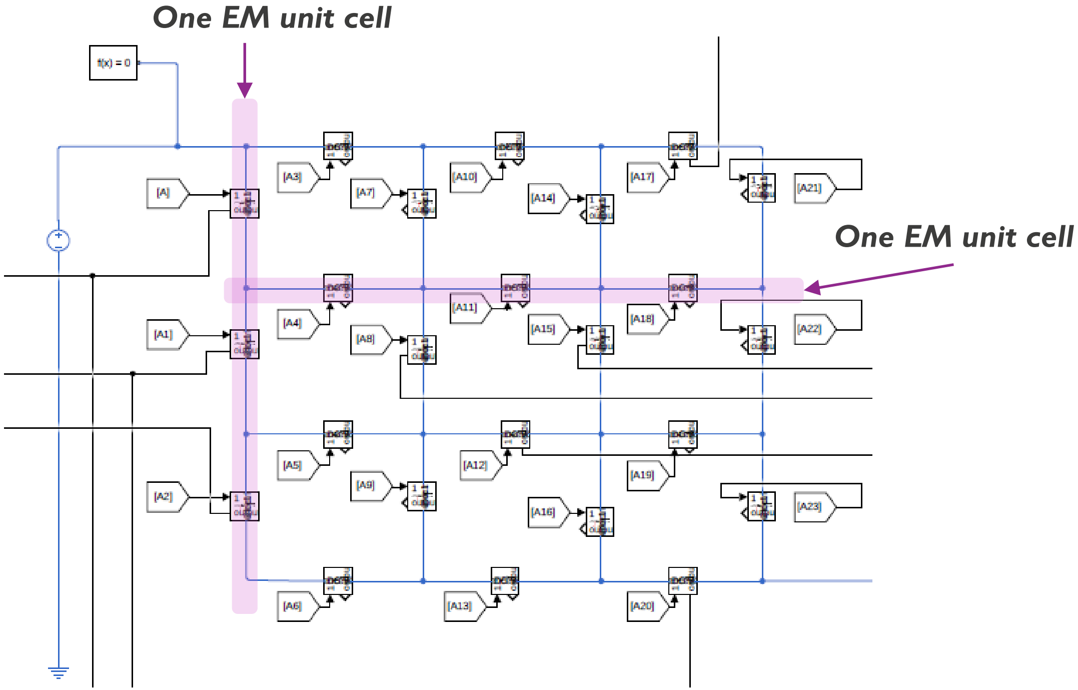
The linewidth of power delivery network needs to be at least 3-4x wider than the minimum linewidth to pass element level EM requirements with Cu metallization

➔ Examine circuit operation and layout to determine if additional EM margins exist

Circuit discretization based on "EM unit cells"







- EM unit cells: single long interconnects with multiple tapping points.
- EM induced mass-transport is restricted to within a single EM unit cell.

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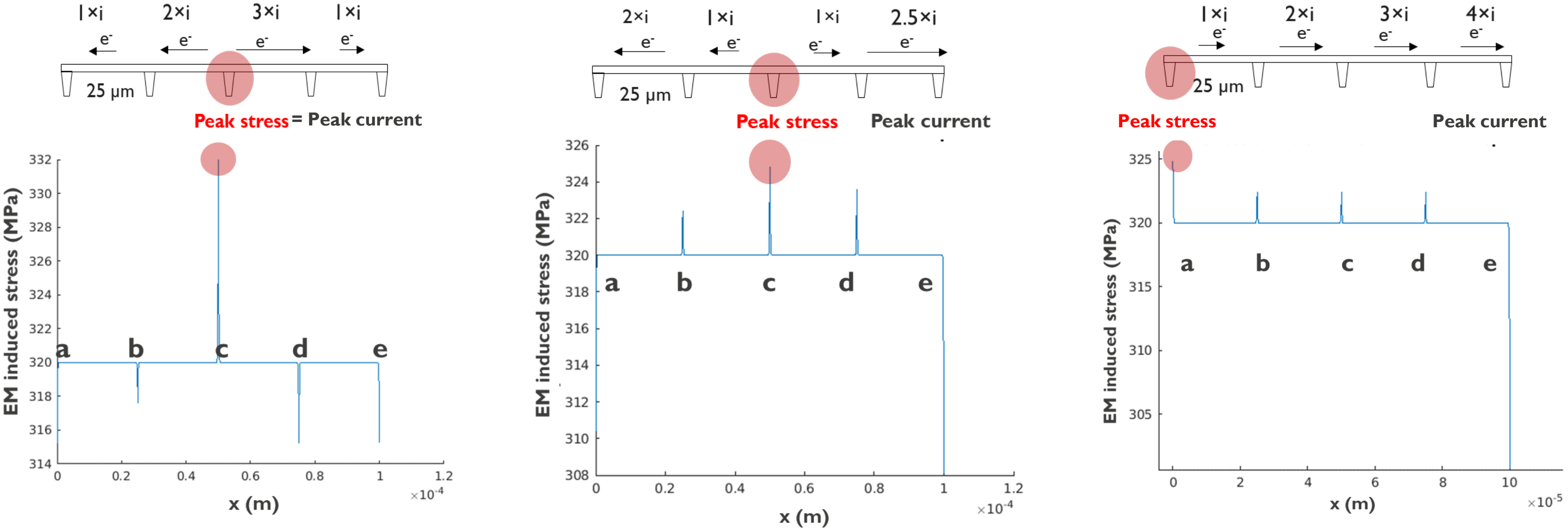
Stress-based or Current-based analysis?



Peak tensile stress and peak current occurred in the same segment

Peak tensile stresses occur in different locations than peak current

- Predicting failure locations based on peak tensile stresses is more accurate as stress is the driving force for void nucleation

Zahedmanesh H. et al., ACM/IEEE SLIP, 2021
Zahedmanesh H. et al., IEEE IRPS, 2022

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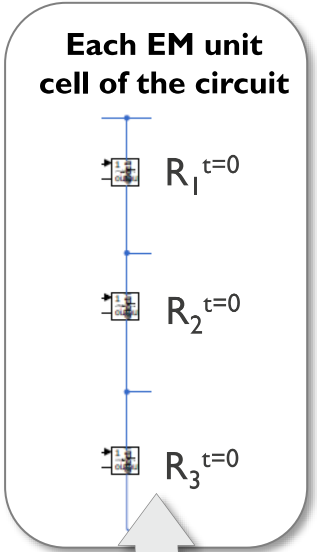
Algorithmic approach

Zahedmanesh H. et al., ACM/IEEE SLIP, 2021
Zahedmanesh H. et al., IEEE IRPS, 2022

Solve electrical circuit and derive currents in every segment

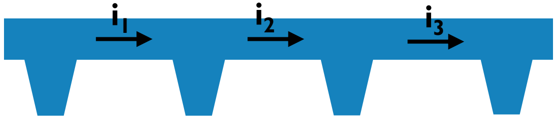


$i_1^{t=0}$
$i_2^{t=0}$
$i_3^{t=0}$

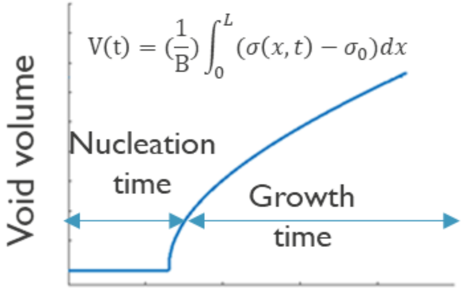
Initial condition: σ along the EM unit from the previous iteration

Run Physics based EM model on every EM unit and obtain change of resistance

Physics based EM simulator



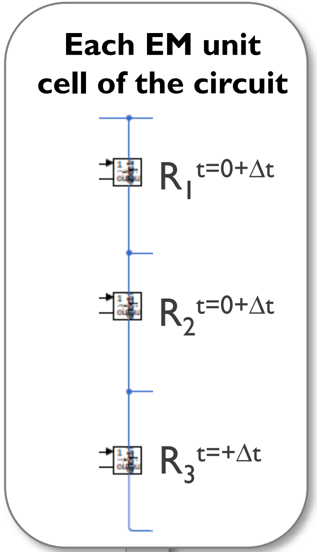
$$\frac{\partial \sigma}{\partial t} = \frac{d}{dx}\left[\kappa\left(\frac{d\sigma}{dx} + \psi\right)\right]$$



$R_1^{t=0+\Delta t}$
$R_2^{t=0+\Delta t}$
$R_3^{t=+\Delta t}$

Save stress along the EM unit

Solve electrical circuit and derive currents in every segment



$i_1^{t=0+\Delta t}$
$i_2^{t=0+\Delta t}$
$i_3^{t=0+\Delta t}$

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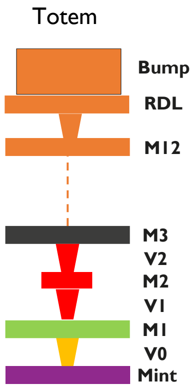
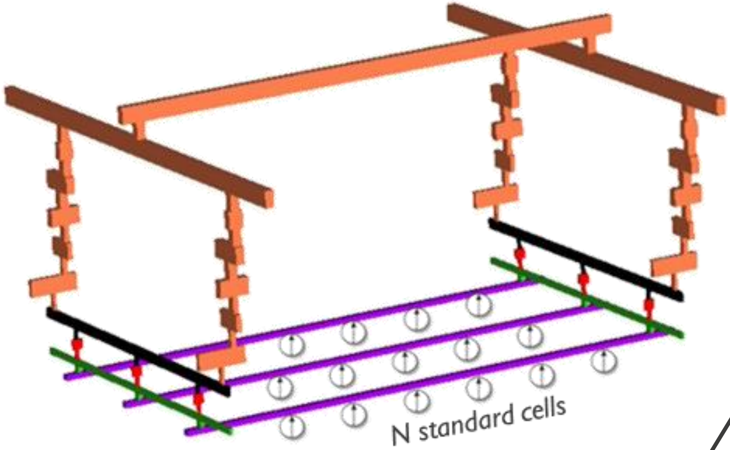
Case study: Simulation of PDN design

- PDN is constructed in a circuit analyzer

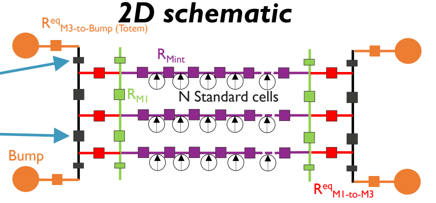
Cross-section of the BEOL layers



3D representation of PDN

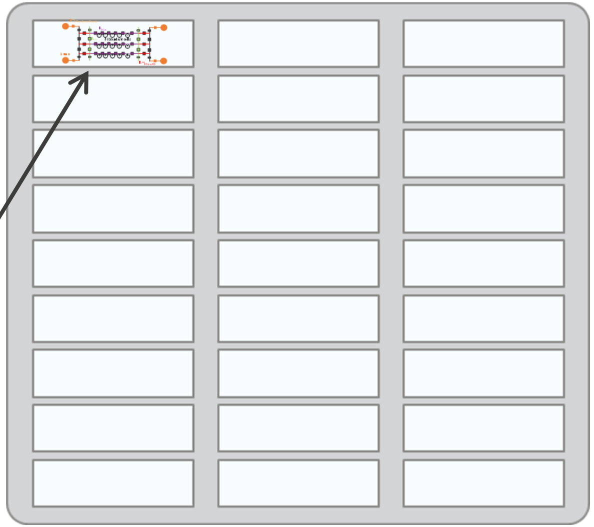


2D schematic



- *EM unit cell i.e. segments where voids can form (part of interconnect network in between FDPs)*

Simulation domain for PDN design 9×3 tiles



Zahedmanesh H. et al., IEEE IRPS, 2022

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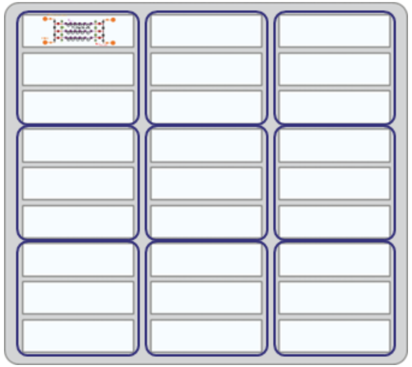
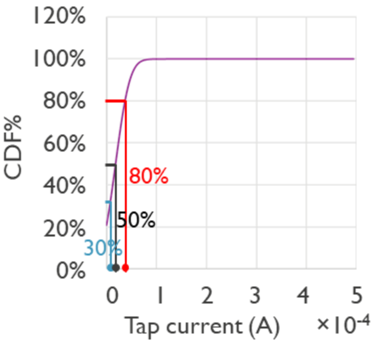
Impact of SC current heterogeneity across the core area

The simulated core area is divided into 9 subdomains



Distribution of tap currents at standard cell level obtained from EDA simulations



Higher heterogeneity of standard cell current across the simulated core area

Median current everywhere, homogeneous

50%	50%	50%
50%	50%	50%
50%	50%	50%

Low current almost everywhere

30%	30%	30%
30%	50%	30%
30%	30%	30%

Heterogeneous with one area of high current

50%	30%	30%
30%	30%	80%
50%	30%	30%

Highly heterogeneous Many areas of high current

80%	80%	30%
30%	50%	30%
50%	80%	80%

Zahedmanesh H. et al., IEEE IRPS, 2022

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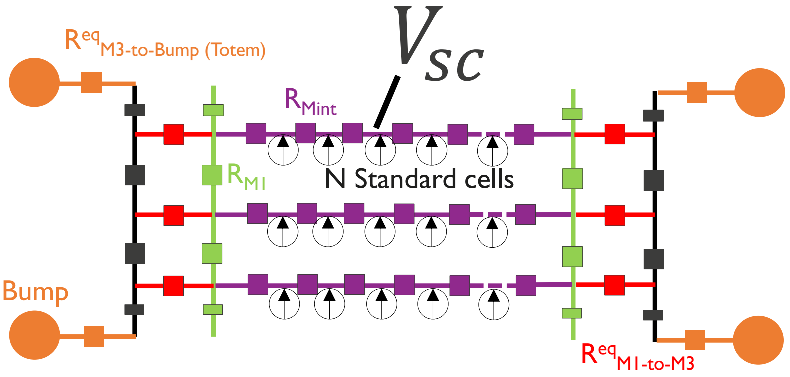
Metric for evaluation of EM impact on system operation

- The IR drops determined at the *standard cell* (SC) tapping points:

$$IR\ drop_{sc}(\%) = \left(\frac{2\Delta V_{sc}}{V_{dd-}V_t}\right) \times 100$$

  - V_{sc} : IR drop at the standard cell
  - V_{dd} = 0.7V
  - V_t = 0.2V (threshold voltage)



- $IR\ drop_{sc}(\%)$<10% to ensure optimal system operation and to prevent timing errors

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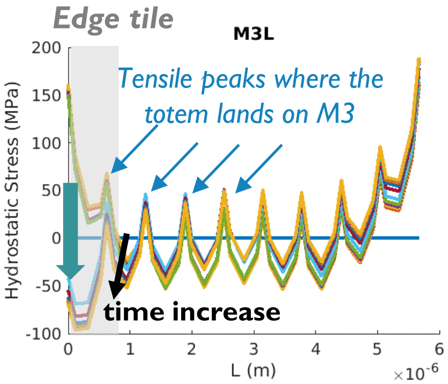
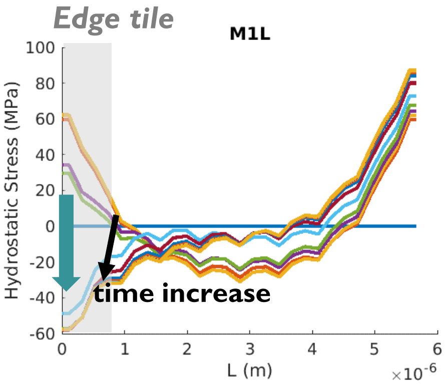
EM stress in copper M1 and M3

Stress change from tensile to compressive after void nucleation



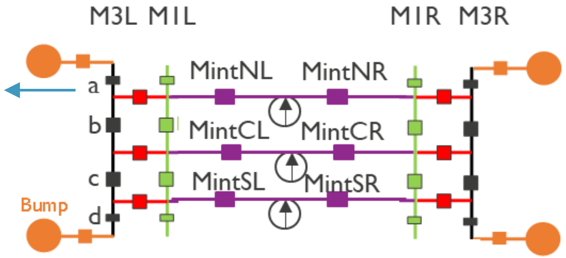
Change of current direction in M1L results in change of stress towards compressive



Median current everywhere, homogeneous

50%	50%	50%
50%	50%	50%
50%	50%	50%

j_{M3} ~20 MA/cm^2



Void location	Nucl. time (0.1yr)
M3La	2.04
M1Ld	0.27
M3Ra	0.01

- Peak EM induced stresses occur at the edge tiles explaining the localization of the failures
- Voids nucleate early in segments with low critical stress (tail of σ_{crit} distribution)

Zahedmanesh H. et al., IEEE IRPS, 2022

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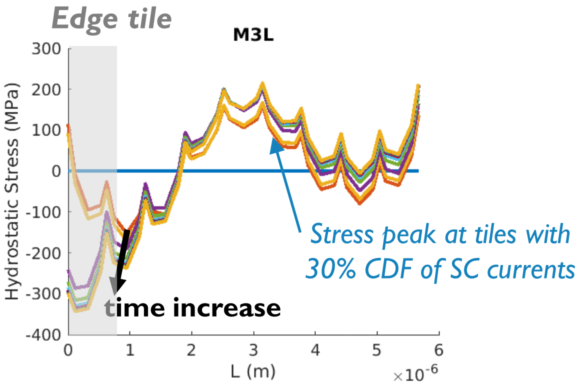
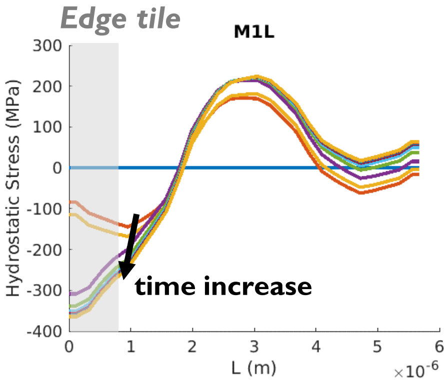
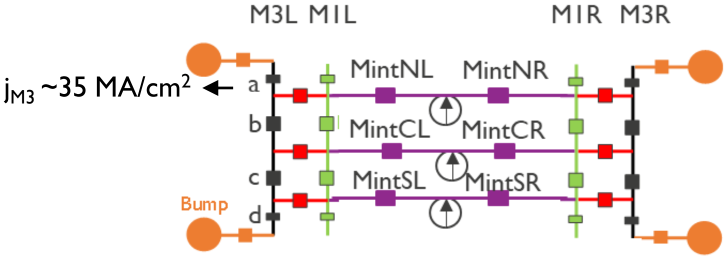
EM stress in copper M1 and M3





Highly heterogeneous
Many areas of high current

80%	80%	30%
30%	50%	30%
50%	80%	80%



Void location	Nucl. time (0.1yr)
M3La	0.06
M3Ra	0.004

- Depending on standard-cell current distribution, stresses can become higher at locations with relatively lower standard-cell current and M1 stresses become comparable to M3.

Zahedmanesh H. et al., IEEE IRPS, 2022

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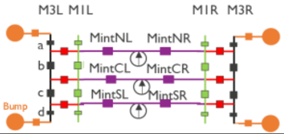
Impact of metallization & SC current distribution across the PDN

Metallization scheme	M1 to M12: Copper Mint: Ruthenium	M1 to M12: Copper Mint: Ruthenium	M1 to M12: Copper Mint: Ruthenium	M1 to M12: Copper Mint: Ruthenium	M1 to M12: Copper Mint: Copper
Standard-cell (SC) current across simulated core area (CDF %)	Median current everywhere, homogeneous 50% | 50% | 50% 50% | 50% | 50% 50% | 50% | 50%	Low current almost everywhere 30% | 30% | 30% 30% | 50% | 30% 30% | 30% | 30%	Heterogeneous with one area of high SC current 50% | 30% | 30% 30% | 30% | 80% 50% | 30% | 30%	Highly heterogeneous with many areas of high SC current 80% | 80% | 30% 30% | 50% | 30% 50% | 80% | 80%	Median current everywhere, homogeneous 50% | 50% | 50% 50% | 50% | 50% 50% | 50% | 50%
Voided segments and time to nucleation  	*Seg — TTN (0.1 yr)* *M3La — 2.04* *M1Ld — 0.27* *M3Ra — 0.01*	*Seg — TTN (0.1 yr)* *M3Ra — 0.6* *M1Ld — 0.3*	*Seg — TTN (0.1 yr)* *M3Ra — 0.11*	*Seg — TTN (0.1 yr)* *M3La — 0.06* *M3Ra — 0.004*	*Seg — TTN (0.1 yr)* *M3La — 14.37* *M3Ra — 0.01* *M1Ld — 0.29* *MintNL — 0.07*
Max EM induced **IR-drop (%) @ 10yr**	**1.9%**	**0.26%**	**0.54%**	**3.0%**	**3.3%**

- Direct correlation between SC current distribution and the EM induced IR-drop
- In all cases, multiple voided segments BUT no catastrophic failures and minimal EM impact on IR-drop at standard cell
- ~1.7x higher impact of PDN EM on IR-drop on PDNs with Cu Mint cf. Ru Mints rails

Zahedmanesh H. et al., IEEE IRPS, 2022

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- **Conclusion**

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Conclusion

- ***Impact of thermal gradients on metal migration:***
  - Voiding due to temperature gradients may become dominant on advanced interconnects.
  - Test structure that allows local heating to investigate the impact of TM (and potentially EM+TM)
  - Combined modelling approach predicts:
    - Temperature gradient along the locally heated segment of the Cu interconnect
    - Increase tensile stress along the locally heated segment → Indication of void formation
  - First experimental data confirms predictions of the model

- ***Circuit level Electromigration analysis:***
  - A physics-based coupled Electrical-EM modelling framework is developed
  - Metric for system performance based on IR drop → indicates impact of EM on system deterioration
  - Case study: PDN
    - Impact of current distribution: Heterogeneous current distribution can change location of EM hot spots
    - Impact of metallization: Ru rails reduced the impact of EM in PDN on IR-drop cf. Cu rails

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Thank you for your attention

Contact email:* *Olalla.VarelaPedreira@imec.be

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