Analog Layout Automation on Advanced Process Technologies

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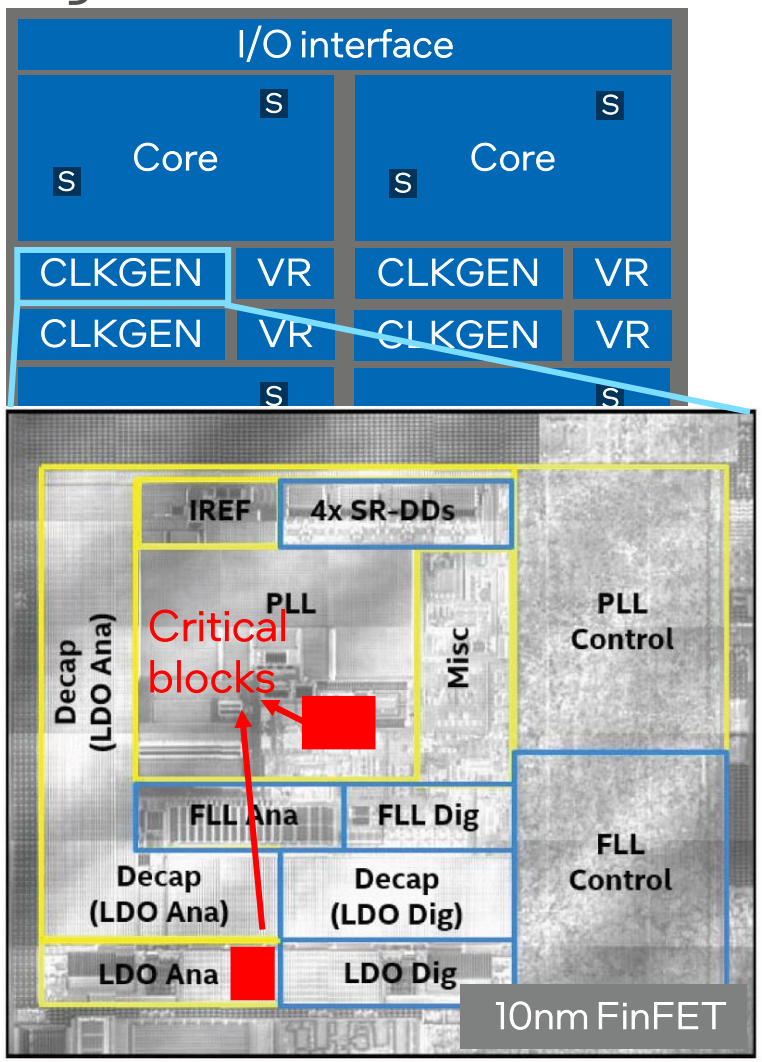
Analog Mixed Signal (Physical) Design

High-Performance SoC



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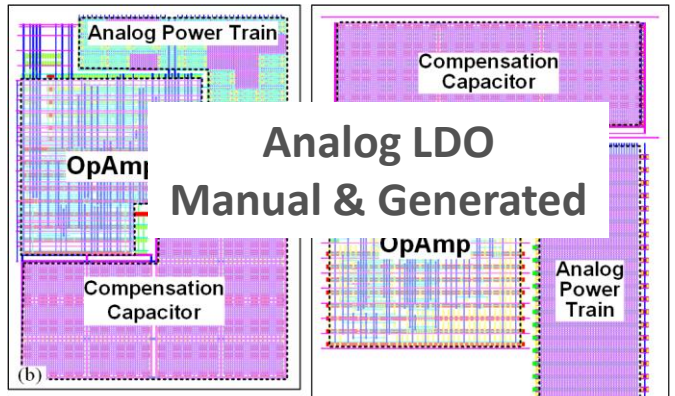
Schematic-Layout Co-Design

How Can Automation Help?

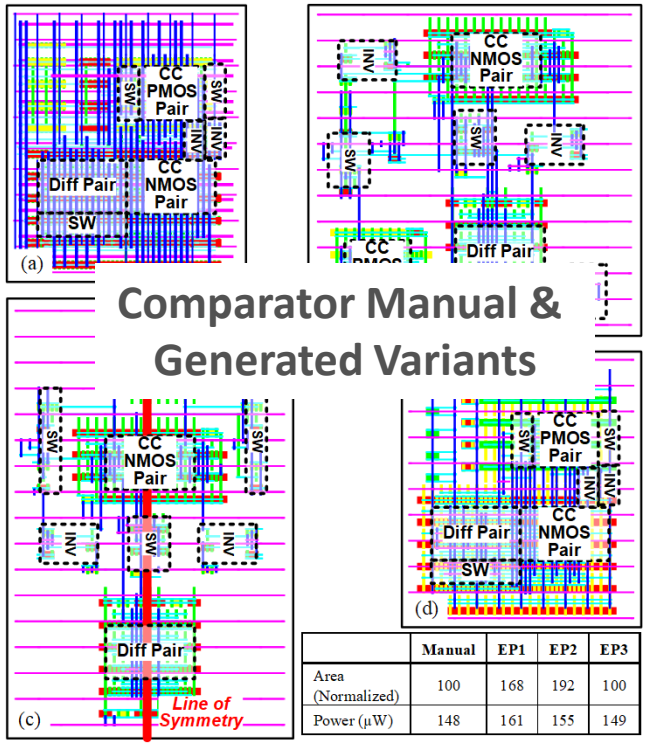
- Accelerate time to first layout (and iterations)
- Embrace analog and custom digital
- <100% completion is okay
  - Correct by construction
  - Easy to revise

ALiGN for Power Delivery Circuits on Intel 16 Technology

- Multiple entry points
- Low dropout voltage regulators
- 10-60x faster TAT

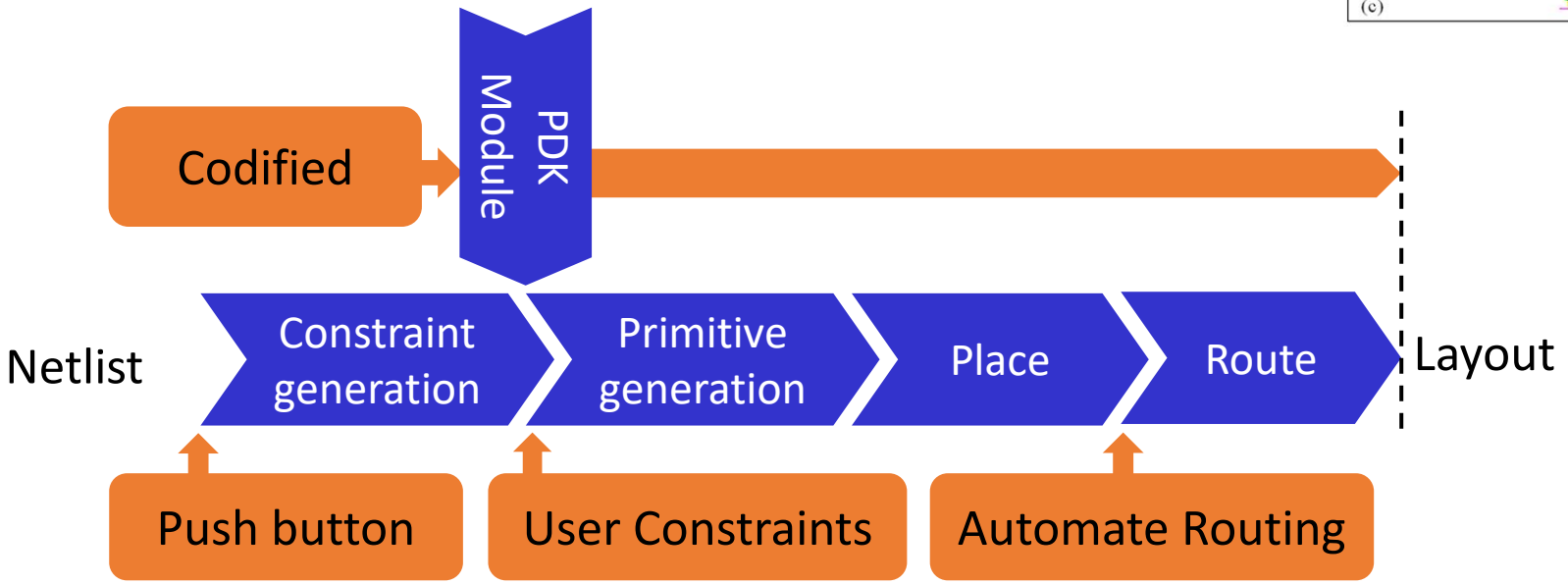


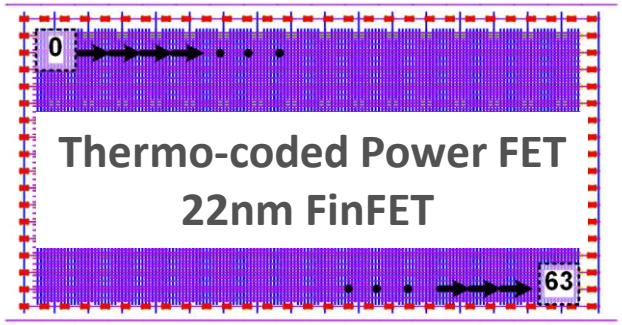
Analog LDO Manual & Generated



Comparator Manual & Generated Variants

	Manual	EP1	EP2	EP3
Area (Normalized)	100	168	192	100
Power (µW)	148	161	155	149





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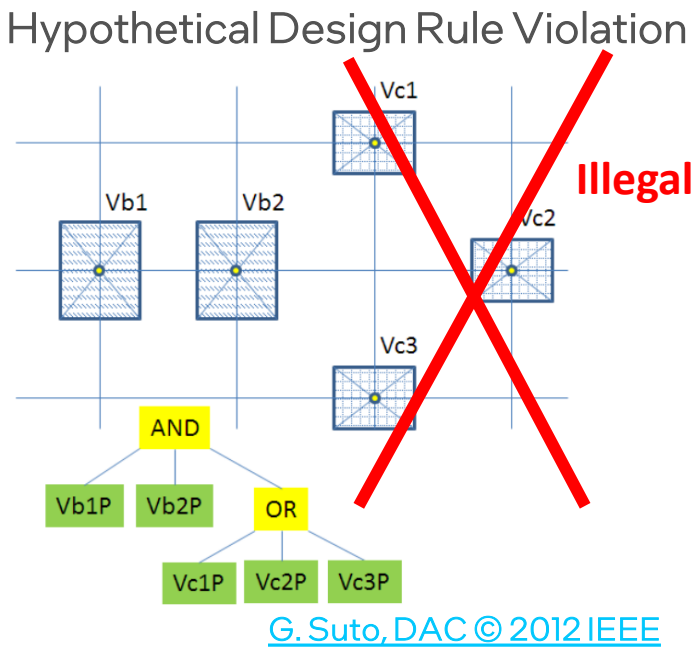
Extensions To ALiGN

- Boolean satisfiability based analog router
- Constraint-driven layout generation
  - Verified by satisfiability modulo theory
- Parameterized cells and standard cells



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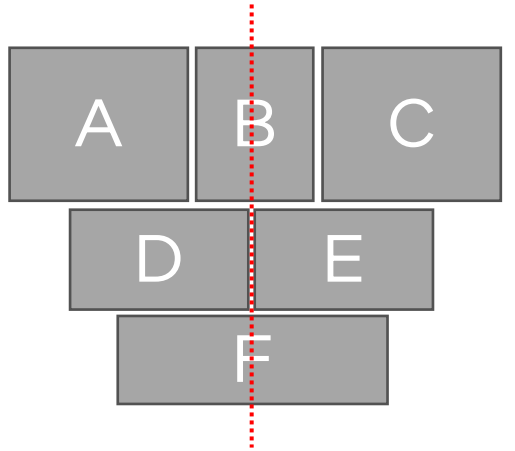
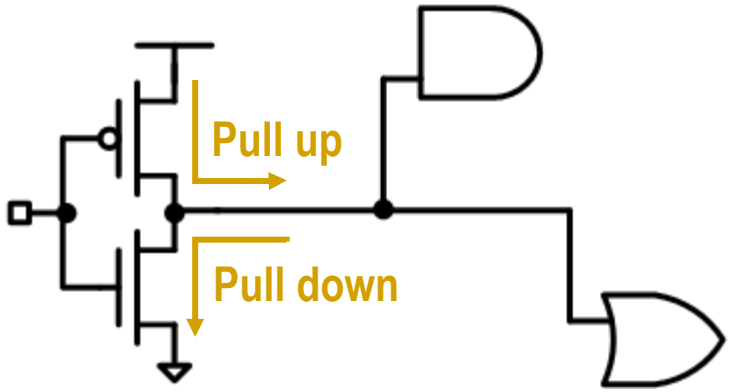
```
{
    "constraint": "Floorplan",
    "order": true,
    "symmetrize": true,
    "regions": [
        ["A", "B", "C"],
        ["D", "E"],
        ["F"]
    ]
}
```

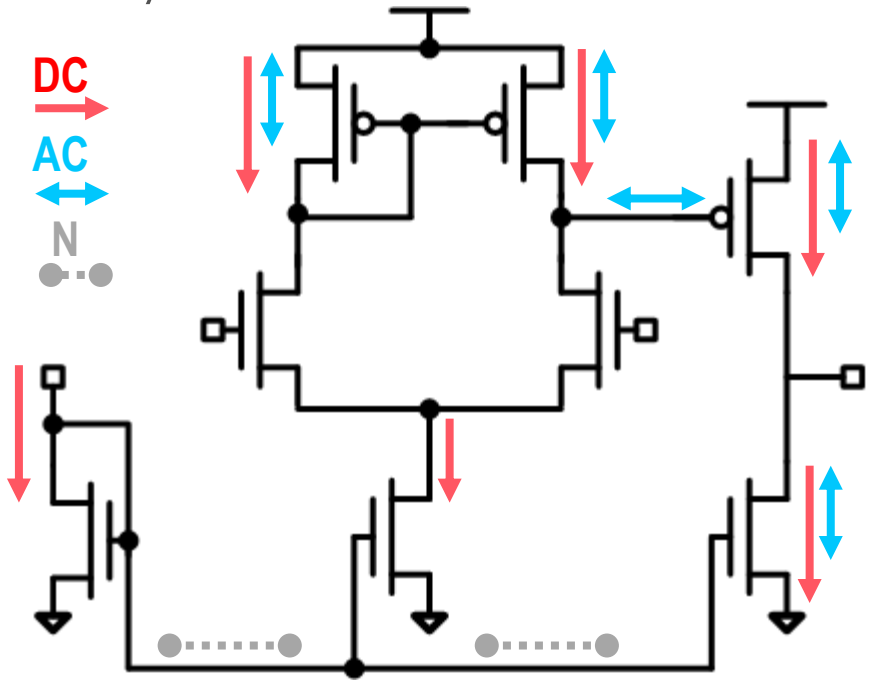
```
# Order horizontal
yield A.urx <= B.llx
yield B.urx <= C.llx
# order vertical
yield F.ury <= D.lly
yield D.ury <= A.lly
# Vertical line of symmetry
yield v_line == (A.cx + C.cx)/2
yield v_line == B.cx == F.cx
yield v_line == (D.cx + E.cx)/2
```



Research Opportunities

- Analog-centric routing algorithms
  - Channel-to-gate => Channel-to-gate, channel-to-channel
  - Fewer pins => Many pins due to transistor arrays
  - RC => R, RC, CC, Reliability





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- Scalability to complex, hierarchical blocks
  - Floorplanning with multiple power islands and routing grids
- Robust constraint generation
  - Avoid constraint engineering or programming burden