The ALIGN Automated Analog Layout Engine: Progress, Learnings, and Open Issues

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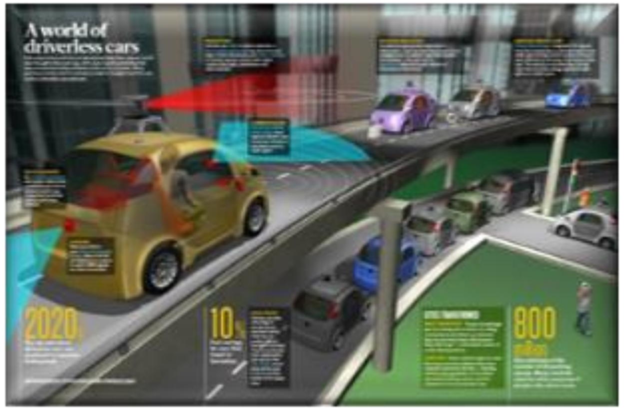
Why analog design automation?

Demand

- The real world is analog, but processing is (largely) digital
- At the very least, need A2D conversion
  - Maybe a lot more – in-sensor computing, RF, …



[Waldrop, Nature]

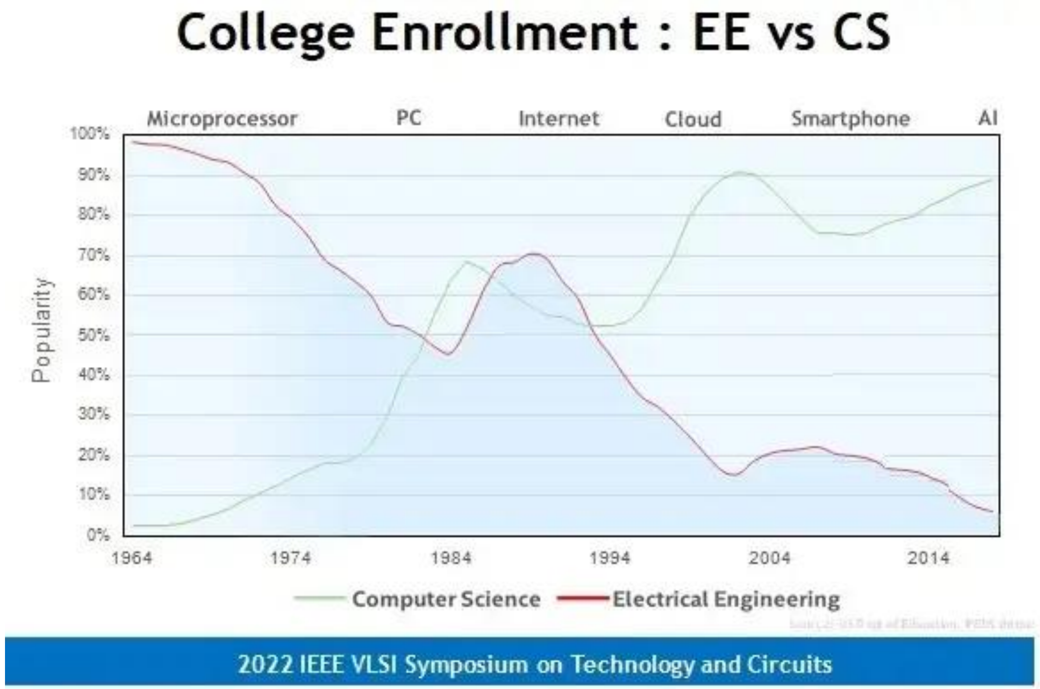
[http://adtellintegration.com]

EDA360 Insider

70% of re-spin issues are AMS in nature: How mixed-signal design can mess up a perfectly good SoC

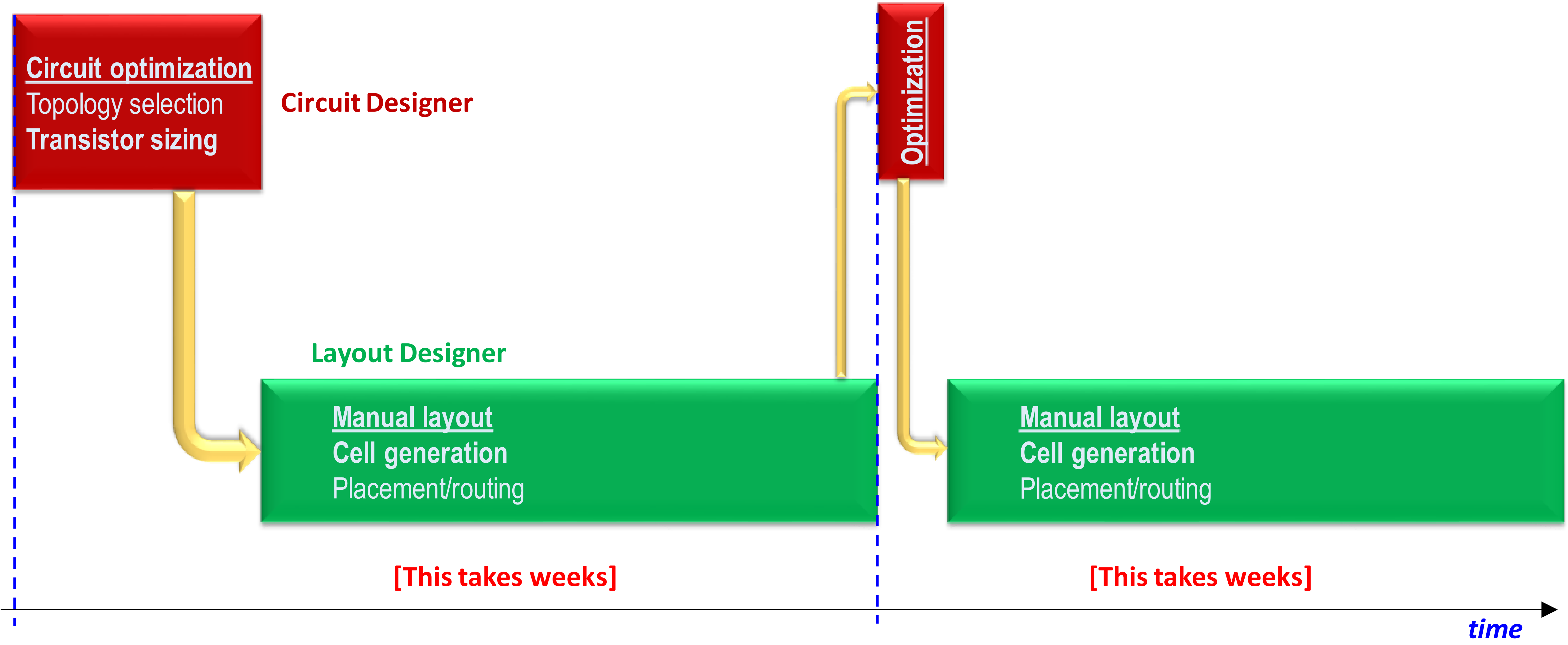
Supply

- Finding designers is hard
- Finding analog designers is harder



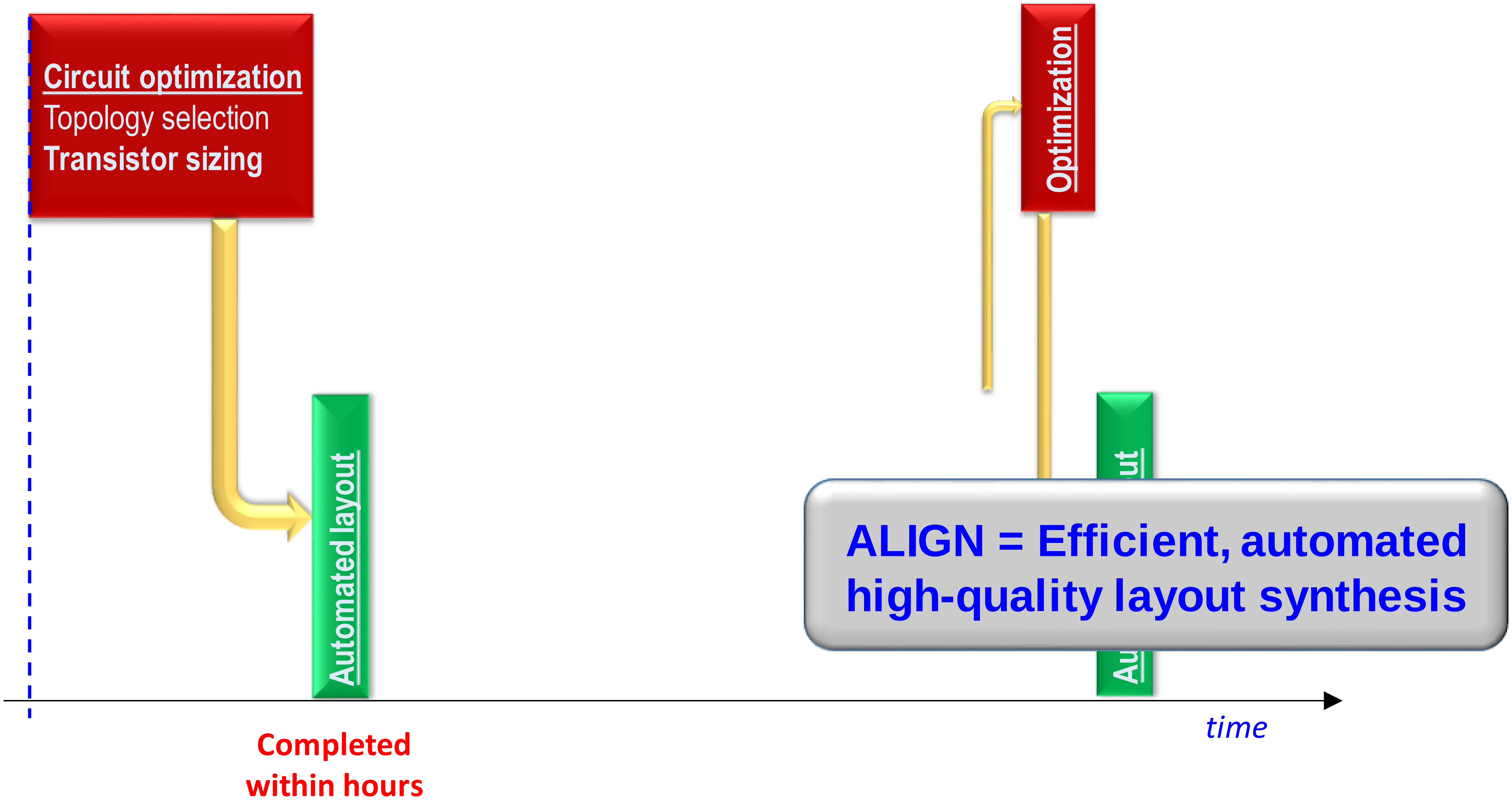
ALIGN motivation: The optimization/layout/optimization cycle

- Layout has significant impact on performance



ALIGN motivation: The optimization/layout/optimization cycle

- Automatic layout helps the circuit designer



EDA for analog layout: from 2018 to today

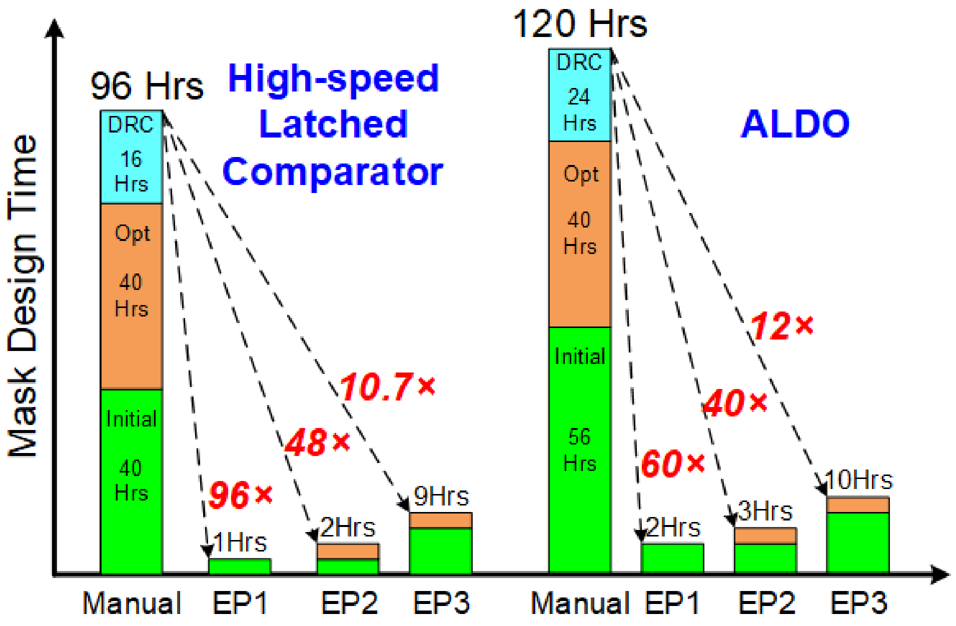
Snapshot in 2018

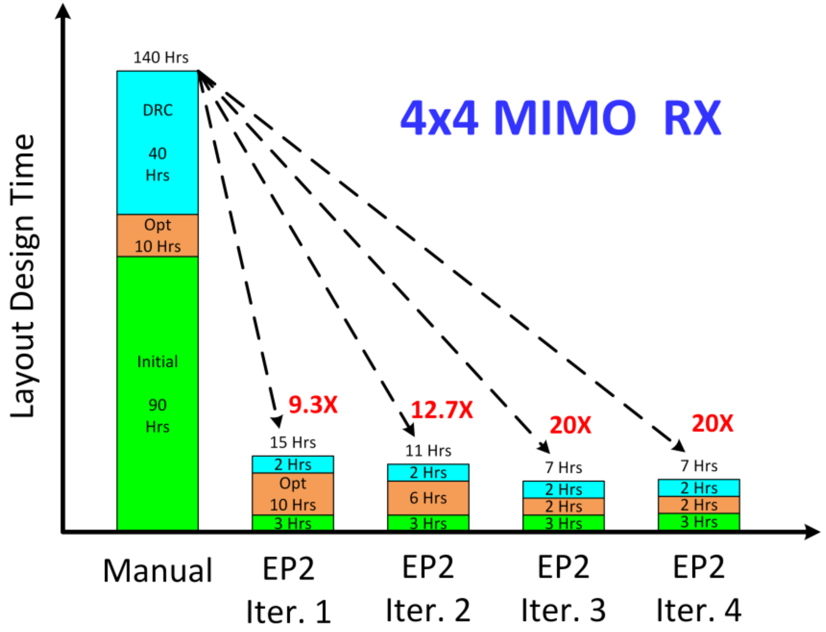
- Several circuit-specific approaches
  - Operational transconductance amplifiers (OTAs)
  - Voltage-controlled oscillators (VCOs)
  - …
- No use of machine learning
- Very little open-source software
- Strong long-term efforts in Europe (e.g., TUM, KU-Leuven), relatively little in the US (exception: CMU, UCB)

Snapshot today

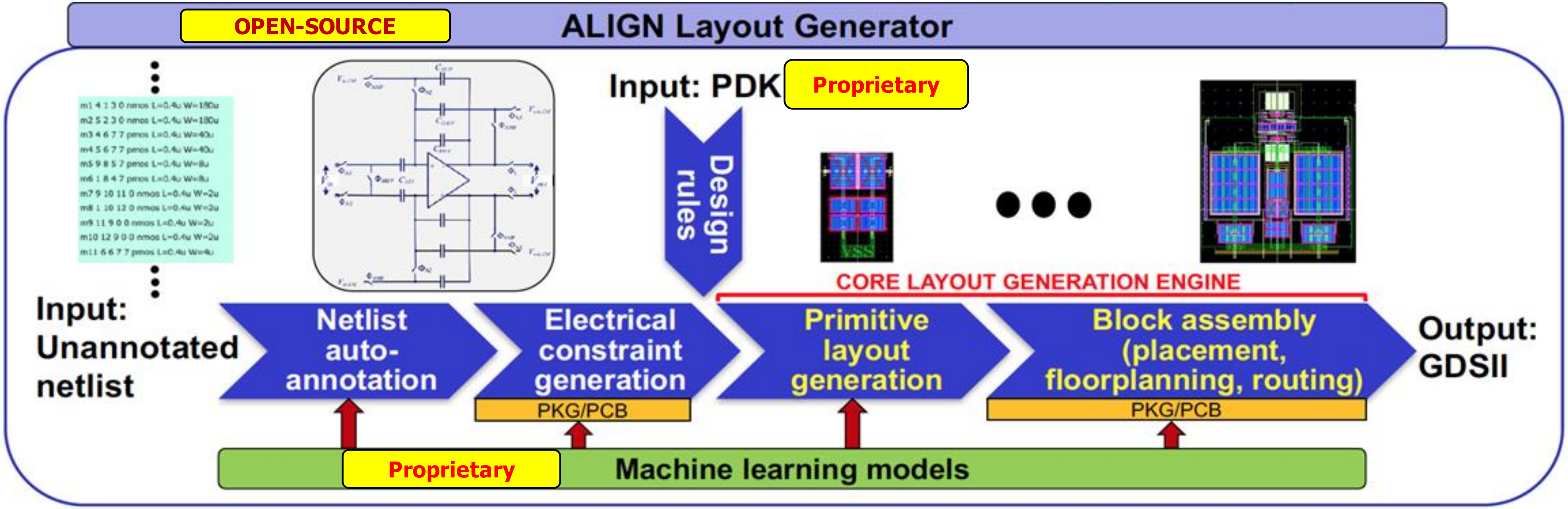
- Public-domain software
  - ALIGN, MAGICAL, BAG2
- More generalized approaches, classifying circuits into categories
  - Low-frequency analog
  - Wireline/high-speed links
  - Wireless/RF
  - Power delivery
- Larger global footprint
  - Several strong efforts in the US, Taiwan, …
  - More global efforts in the area
  - Internal efforts at several companies

Designer productivity enhancements from ALIGN

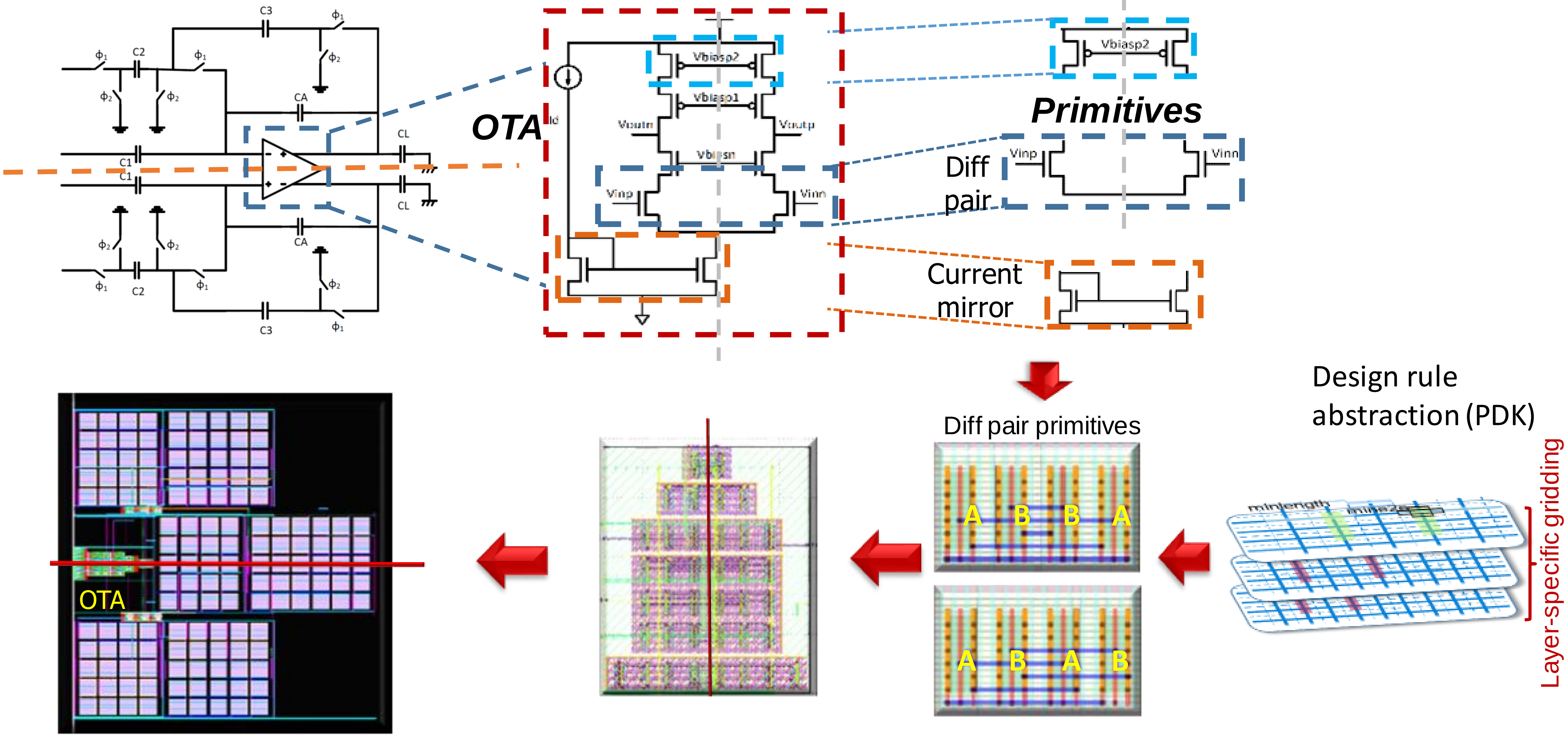




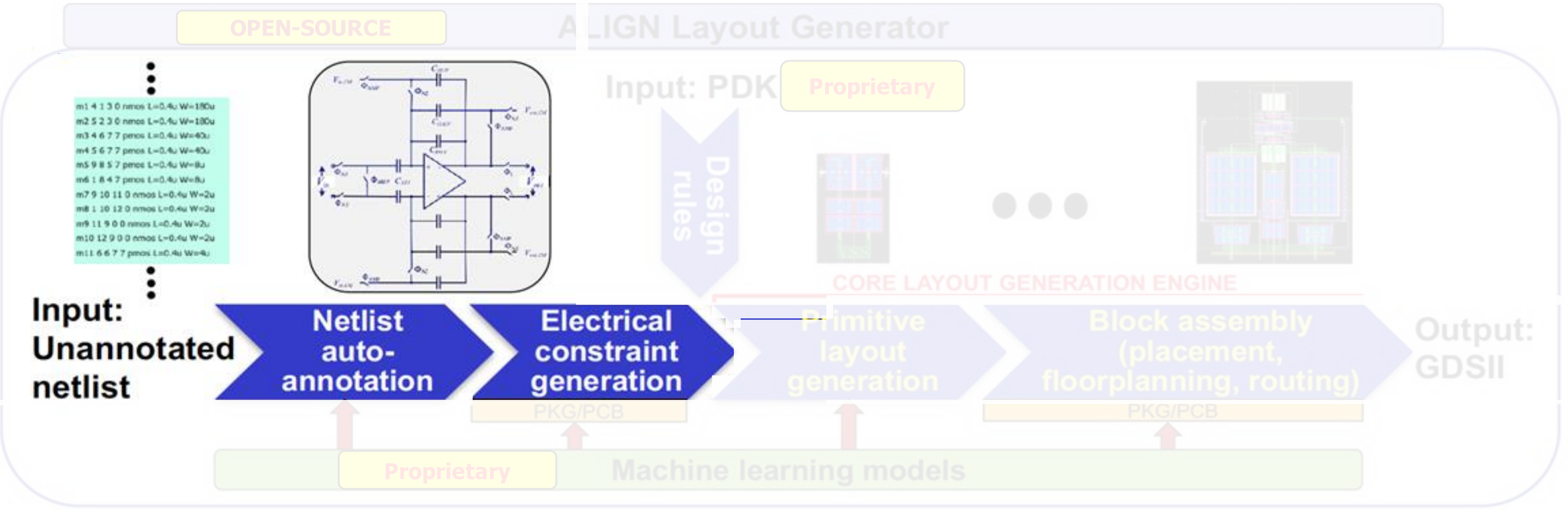
ALIGN: Layout generation from netlist → GDSII



Identifying structure and function in a switched capacitor filter

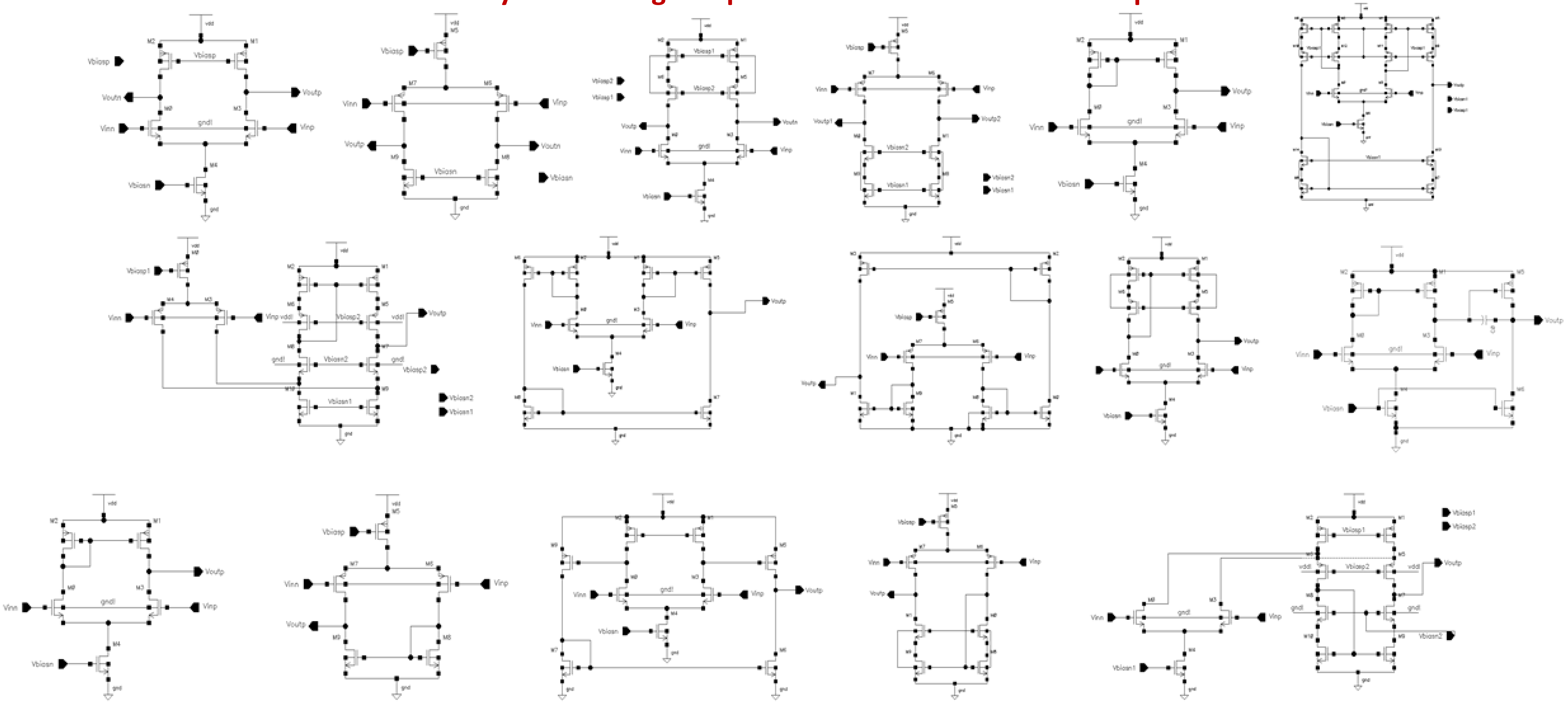


Auto-annotation



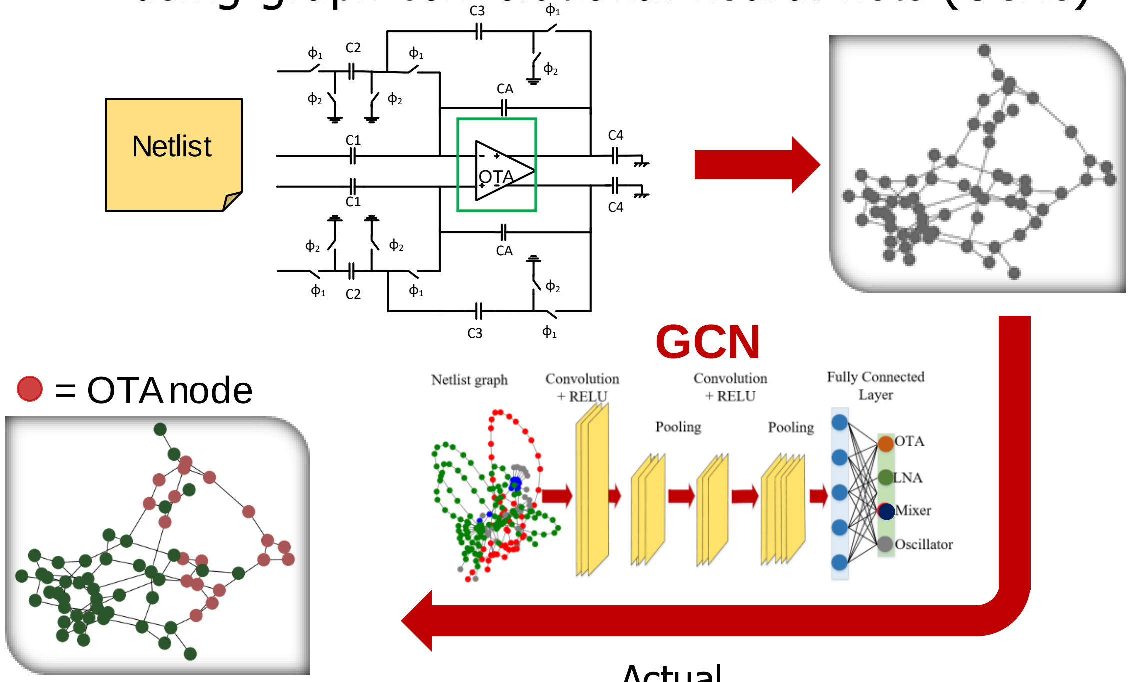
Example 1: Recognizing analog components

Different ways of building an operational transconductance amplifier



Netlist auto-annotation

- Approach A: Use machine learning to identify commonly-encountered topologies
- Philosophy: Variations of core structures found using graph convolutional neural nets (GCNs)

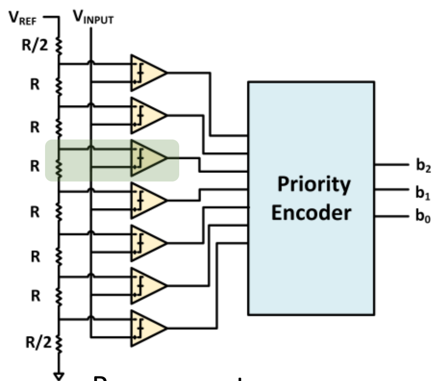


Phased array circuit

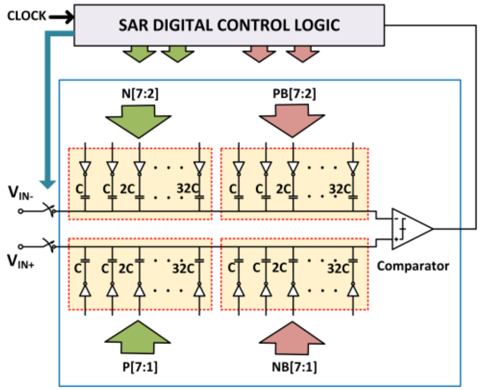
Predicted \ Actual	LNA	MIXER	OSC	BPF	BUF	INV
LNA	78	0	0	0	0	0
MIXER	0	120	0	0	0	0
OSC	0	0	132	0	0	0
BPF	0	0	0	136	0	0
BUF	0	0	0	0	32	0
INV	0	0	0	0	0	24

[Kunal, DATE20]

- Approach B: Identify array structures in a layout
- Philosophy: array structures often together with symmetry/matching/CC; design once + replicate

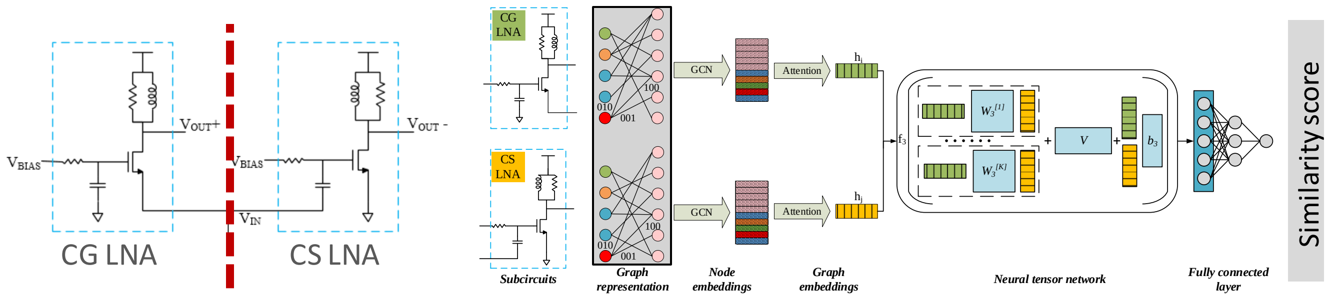


R, comparator array



Univ. of Washington SAR ADC

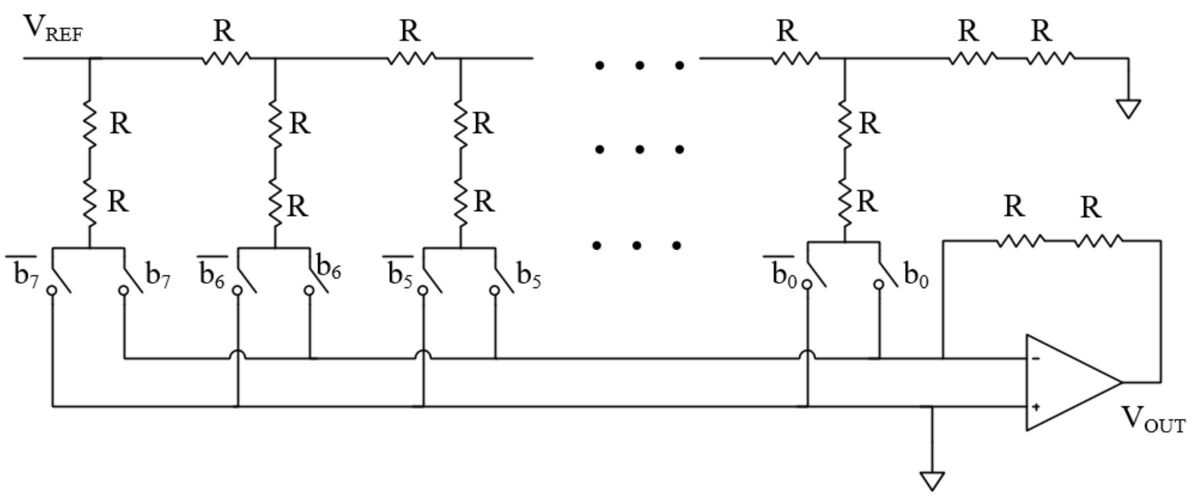
- Approximate matching
  - Find "graph edit distance" using neural tensor network

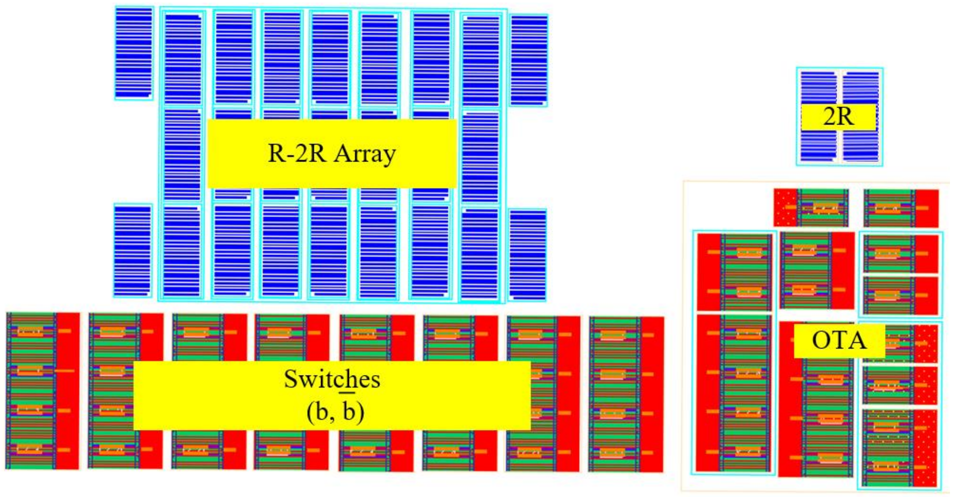


[Kunal, ICCAD20]

From auto-annotation to layout

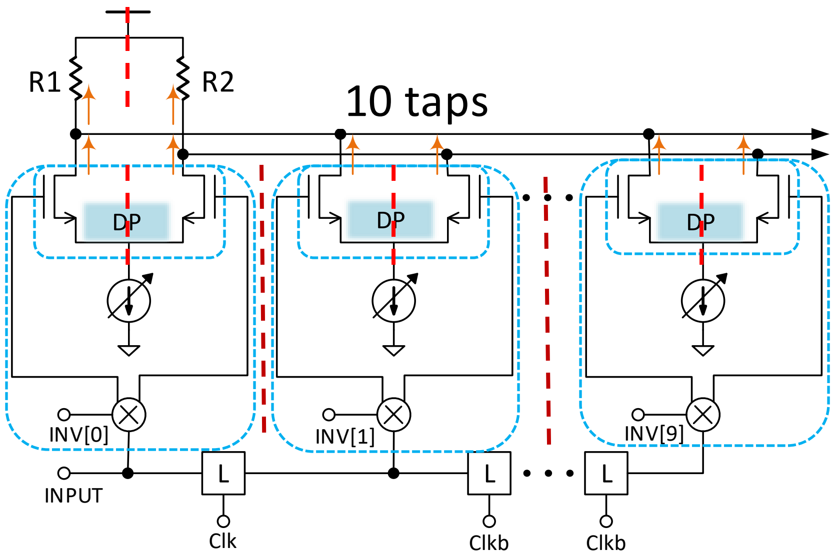
R-2R DAC

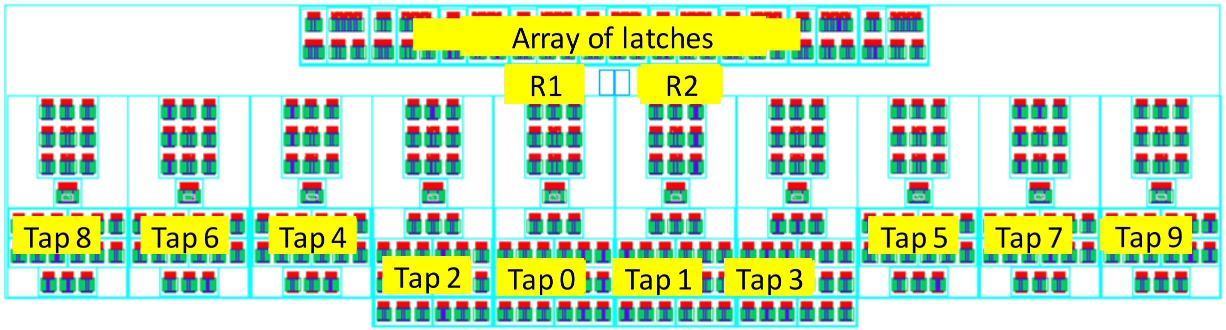




10-tap FIR Equalizer

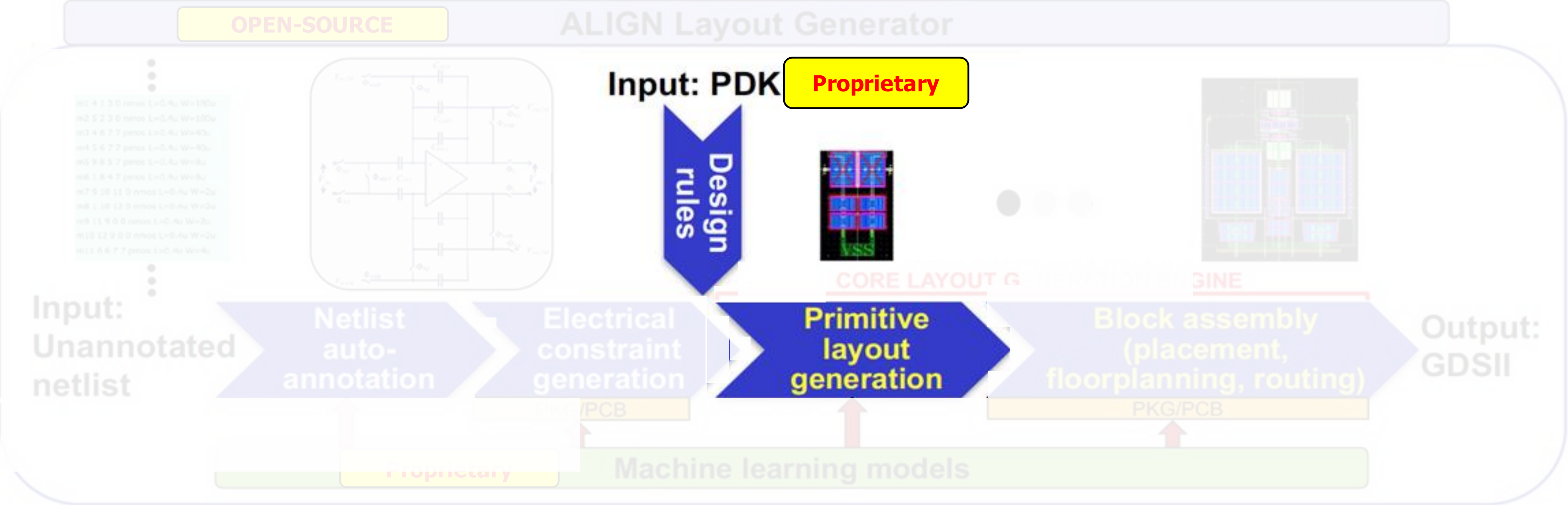
- Taps symmetric wrt each other; wrt R1 and R2
- Approximate matching: 5-bit/7-bit current sources





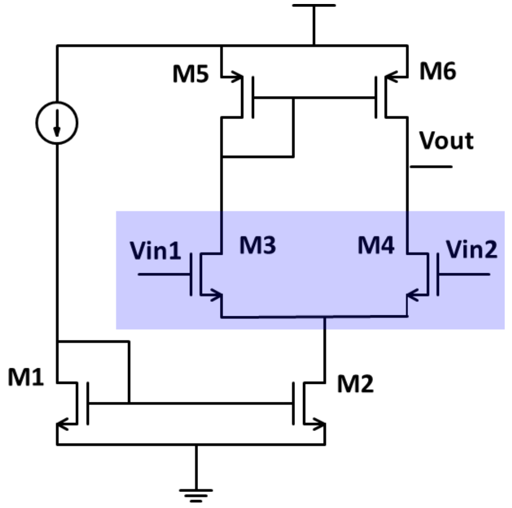
[Kunal, ICCAD20]

PDK abstraction and cell generation

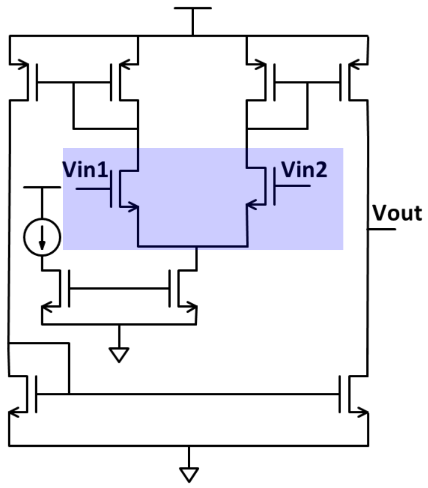


Primitive cells

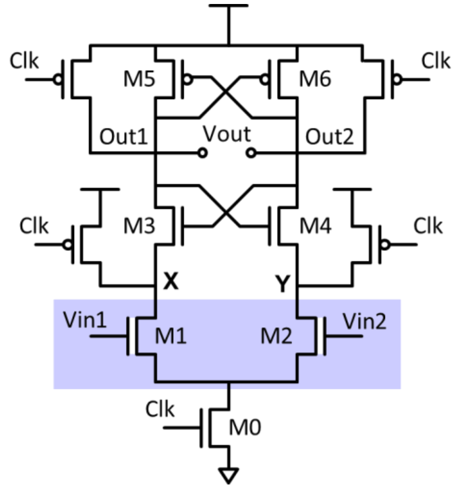
- Examples: current mirrors, differential pairs, Rs, Cs, …
- Lowest level of hierarchy, assembled together through block assembly



5T-OTA



Current mirror OTA

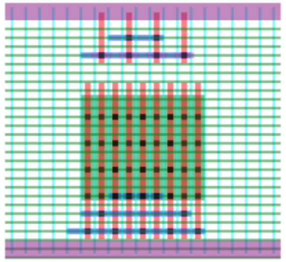


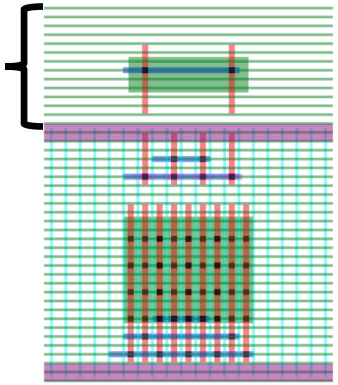
StrongARM comparator

Primitive cell generation: Parameterization

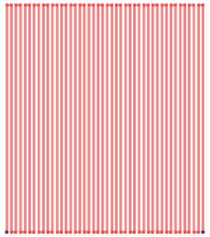
Body flag

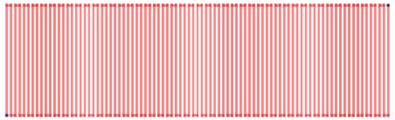
Body contact

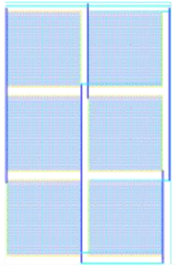

Body flag: OFF

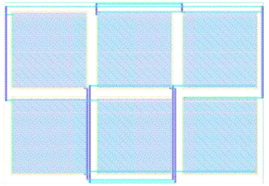

Body flag: ON

By aspect ratio

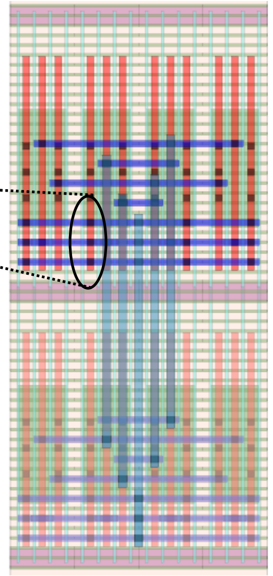

10K resistor
Aspect Ratio:1x2


10K resistor
Aspect Ratio: 2x1

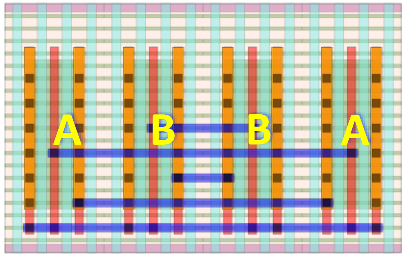

50fF Capacitor Array
Aspect Ratio: 2x3


50fF Capacitor Array
Aspect Ratio: 3x2

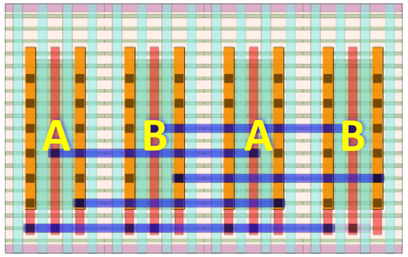
3 parallel wires to reduce R



By layout pattern

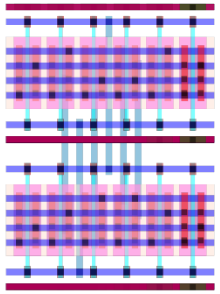


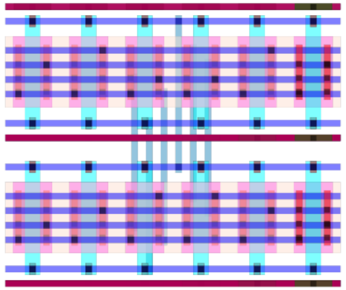
DP – Common centroid



DP – Interdigitated

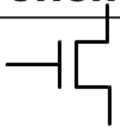
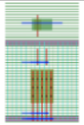
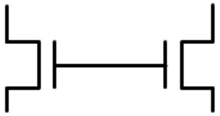
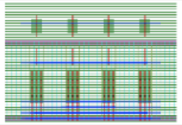
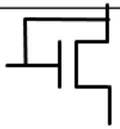
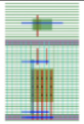
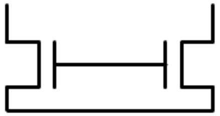
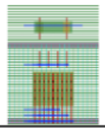
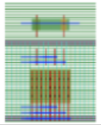
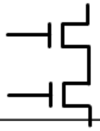
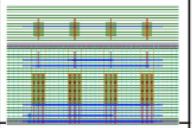
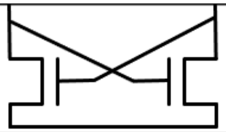
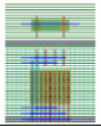
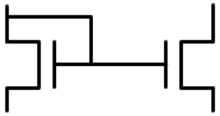
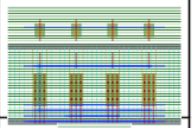
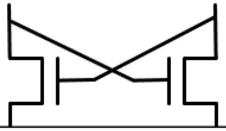
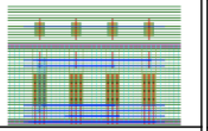
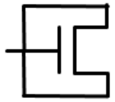
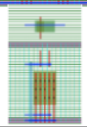
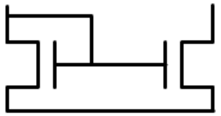
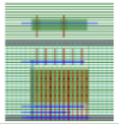
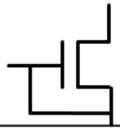
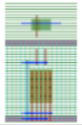
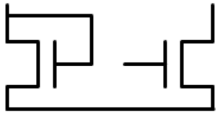
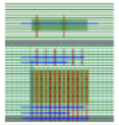
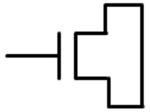
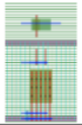
By # fins/fingers
Active width
Gate length, …


Lg: Lmin


Lg: 4xLmin

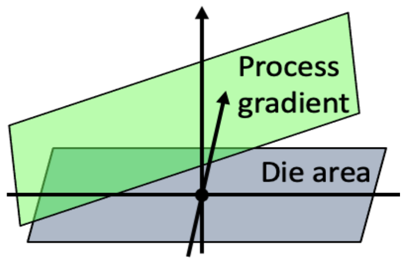
Also: by # stacked transistors, by wire width within primitive, …

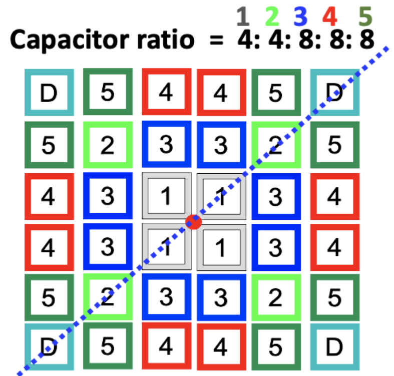
List of primitives

Primitive	Schematic	Layout	Primitive	Schematic	Layout
Switch			Differential load (CMC)		
Diode-connected load (DCL)			Current mirror load (CMC_S)		
Differential pair (DP)			Cascode pair (CP)		
Cross-coupled pair (CCP_S)			Level shifter (LS)		
Cross-coupled pair1 (CCP)			Dummy		
Current mirror (CM)			Dummy1		
Current mirror1 (CMFB)			Decoupling cap (decap)		

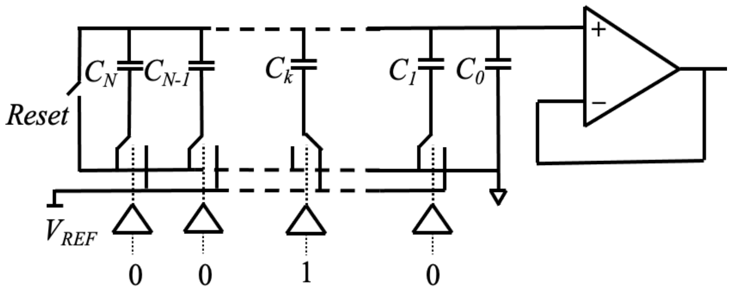
These cell layouts can be parameterized

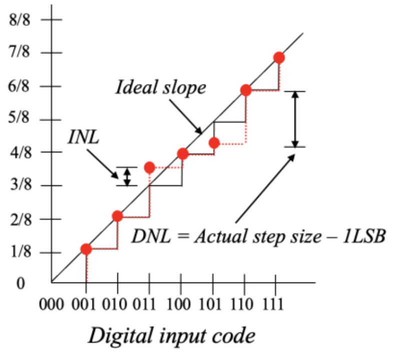
Common-centroid array layouts





Common centroid layout
D = Dummy



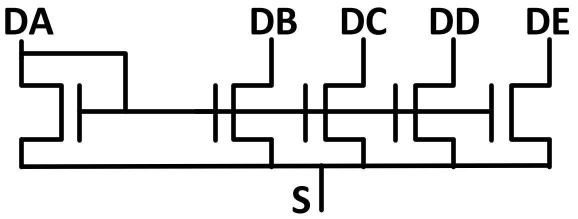


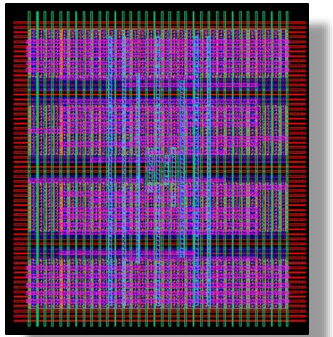
3dB frequency

$$f_{3dB} = \frac{1}{2(N+2)\ln(2)\tau} \qquad \tau = RC$$

Transistor arrays

\# unit cells: [4, 4, 4, 10, 10]

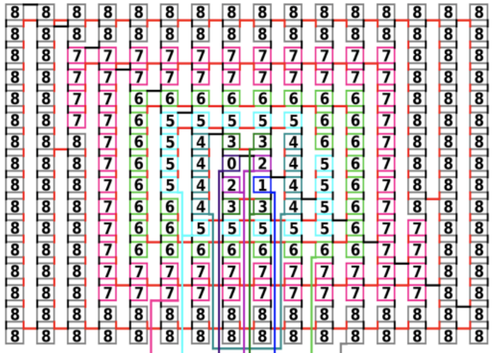




D	D	E	E	D	D	E	E
E	B	B	A	A	C	C	D
D	C	C	A	A	B	B	E
E	E	D	D	E	E	D	D

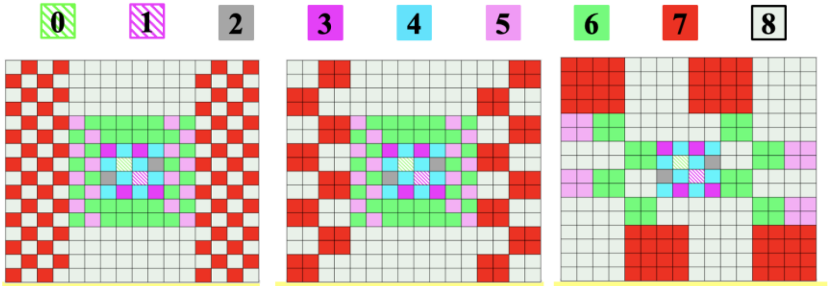
Max IR-drop: 5.7mV
Max dev in current: 0.8%

Capacitor arrays



\# Vias = 15 ,f_{3dB} = 993 MHz

Spiral



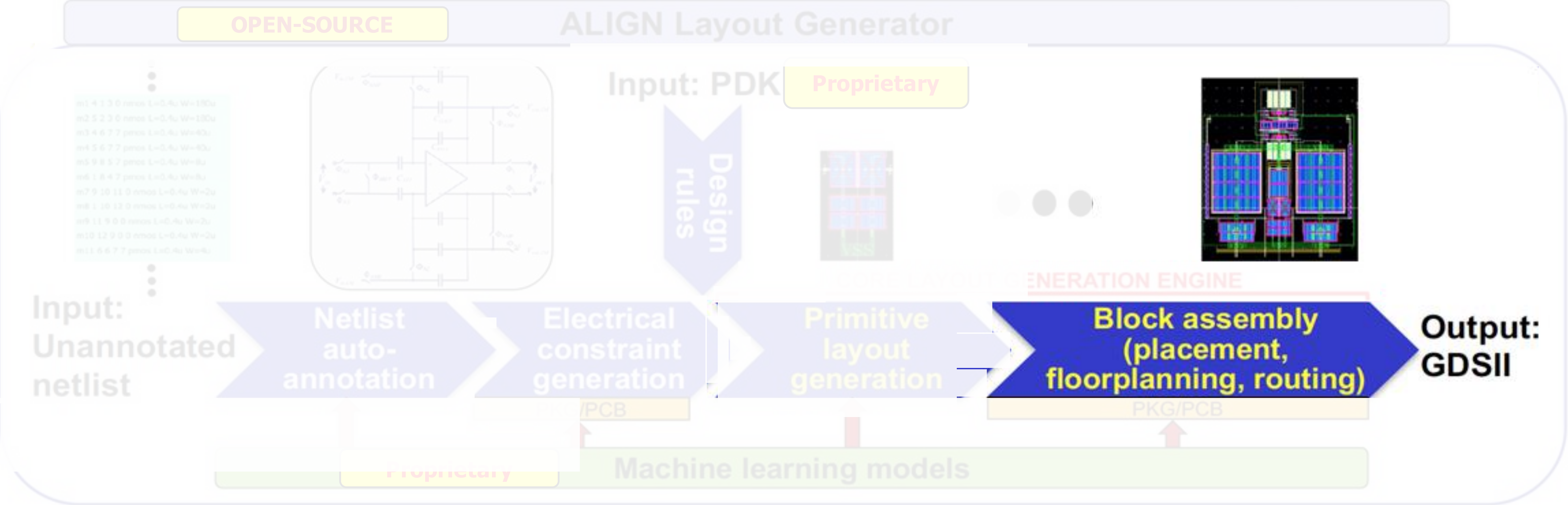
{DNL,INL}={0.038,0.031} f_{3dB} = 42MHz

{DNL,INL} = {0.039,0.032} f_{3dB} = 102MHz

{DNL, INL} = {0.023,0.028} f_{3dB} = 429MHz

Block chessboard

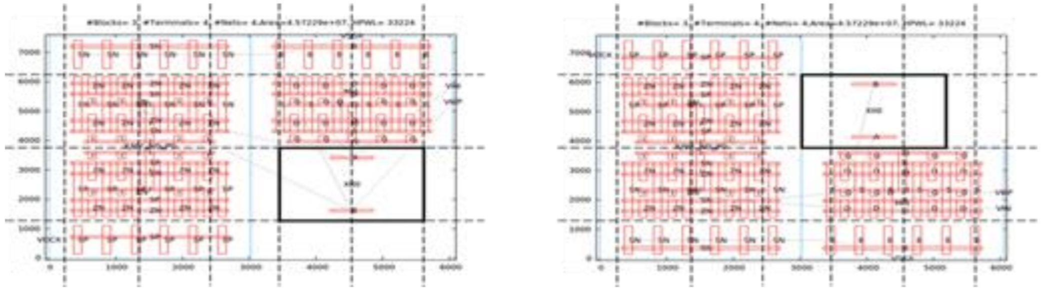
Placement and routing



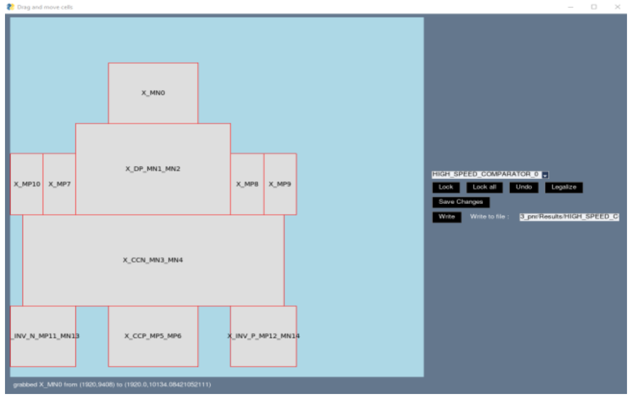
Placers

- Placer for every hierarchy chosen based on #cells
- Enumerative placer
  - Exhaustively searches all possible floorplans using sequence pairs.
- Integer linear programming (ILP) placer
  - If floorplan space cannot be enumerated in reasonable time
  - Quickly placement for overconstrained floorplans
  - Interactive GUI to edit placements and legalize them using ILP
- Simulated Annealing (SA) placer
  - For large problems
  - On-grid placement
  - Supports user-defined placement
  - Enhancement of sequence pair to handle corner cases of ordering/alignment/abutment/symmetry constraints
- Analytical placer
  - Global placement: reformulated EA placer.
  - Detail placement: ILP.

On grid placement (left on grid, right off grid)

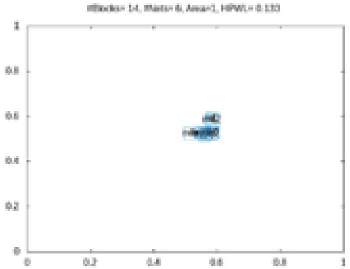


Interactive GUI to edit placement

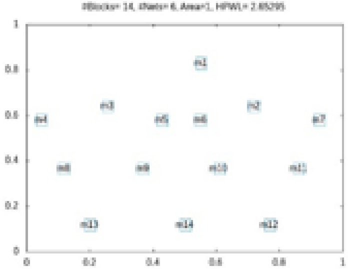


Analytic placer

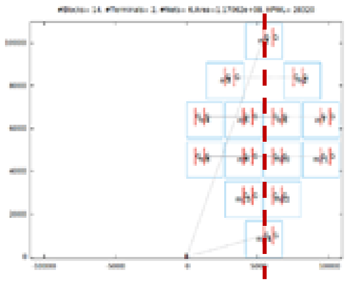
Initial placement



Global placement



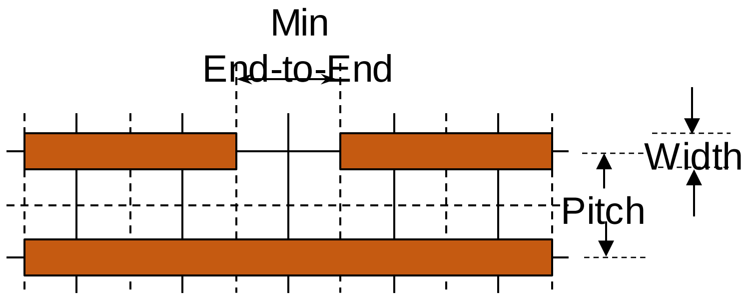
ILP-based compaction



Routers

FinFET router

- Gridded routing



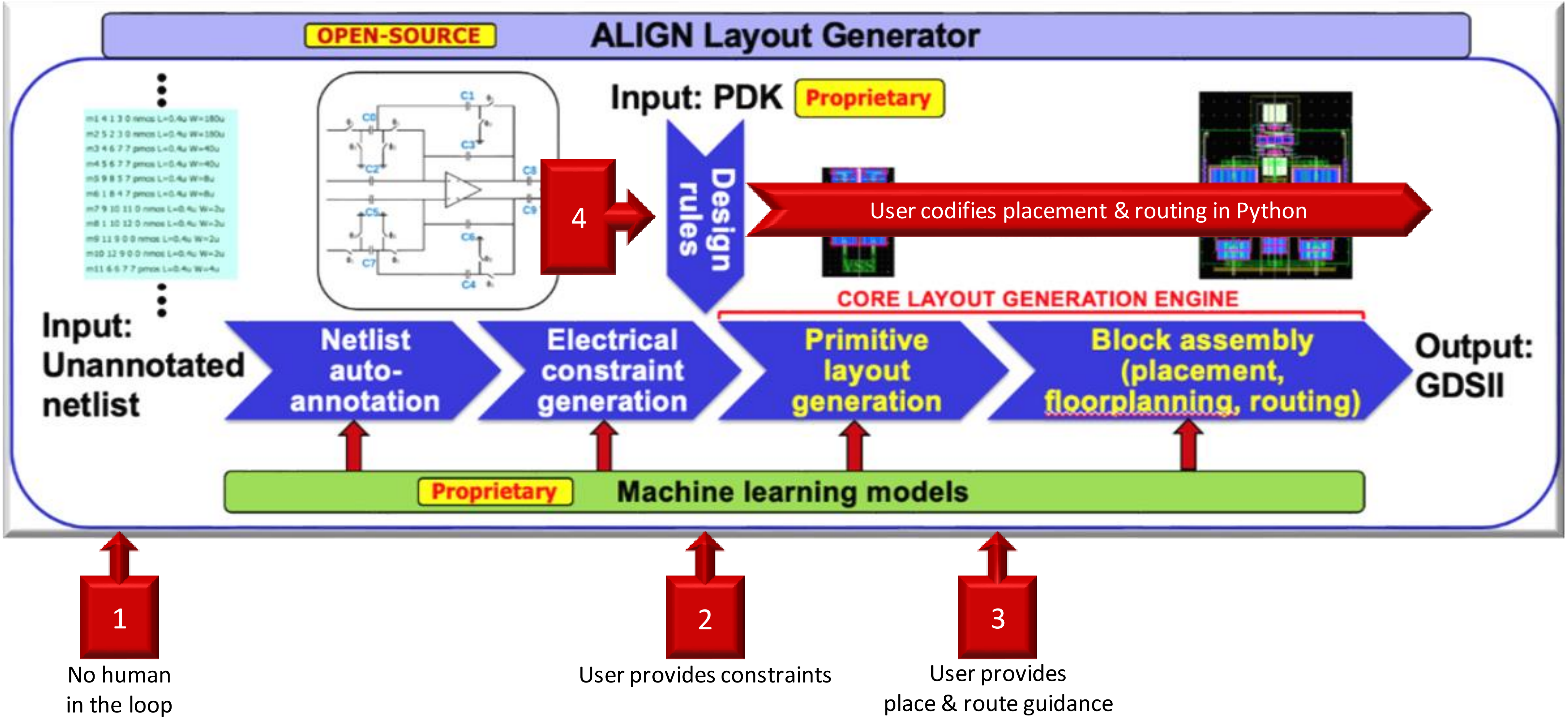
- Applied to
  - Commercial PDKs (FinFET: 12nm, Bulk: 65nm), ASAP7, FinFET Mock PDK*
  - Internally within Intel to 22, 14, 10, and advanced FinFET process technologies
- Global + detailed route on the grid
  - Shielding, symmetry, matching, max-length
  - “Multi-connections” for wire sizing
- Also: SAT-based router

Bulk router

- A* routing on Hanan-grid
  - Layers costed using their respective sheet resistance
- Bi-directional routing on layers that allow it
- Non-default design rule (NDR) handling:
  - Custom width and spacing for each net
  - Via stack with cut-arrays
- Preferred routing layers
  - Restrict routing to user specified layers
  - Pins on other layers are first via’ed to preferred layers before routing
- Fine grained routing control
  - Use of user specified virtual pins to control net topology
  - Block and net specific routing blockages
  - Change routing direction of layers for any net
  - Specify order in which the nets have to be routed

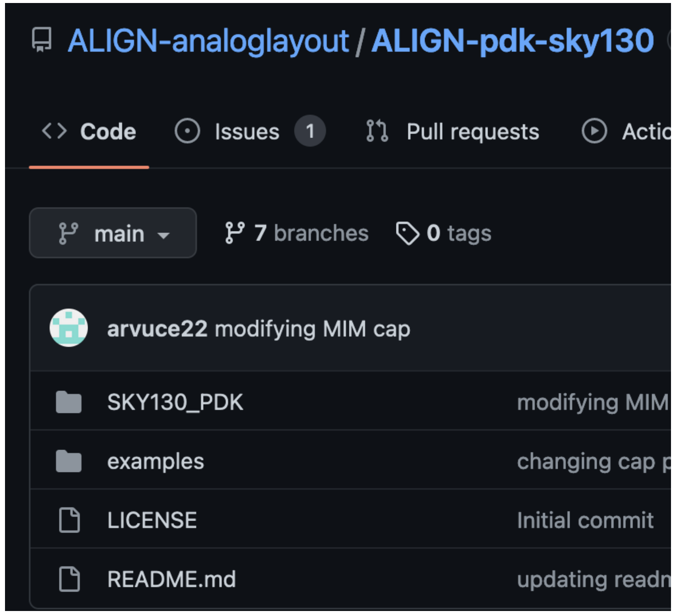
Multiple entry points into ALIGN

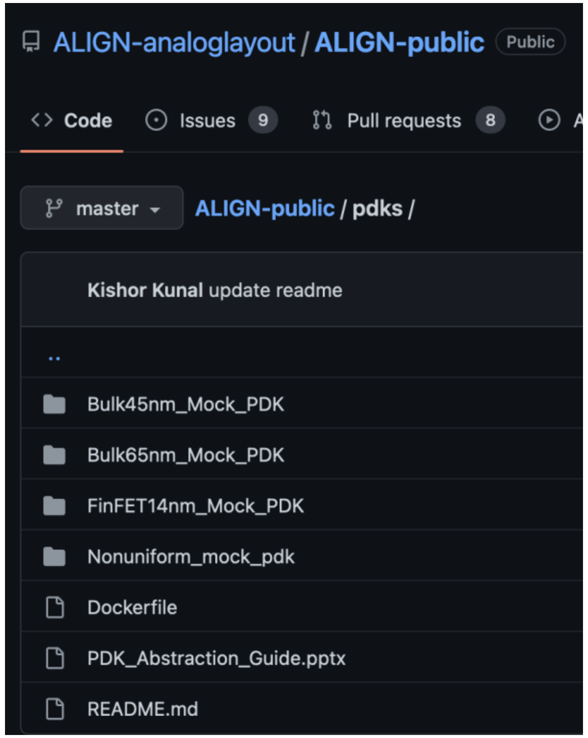
- Helpful for designers, easy to facilitate due to our modular software



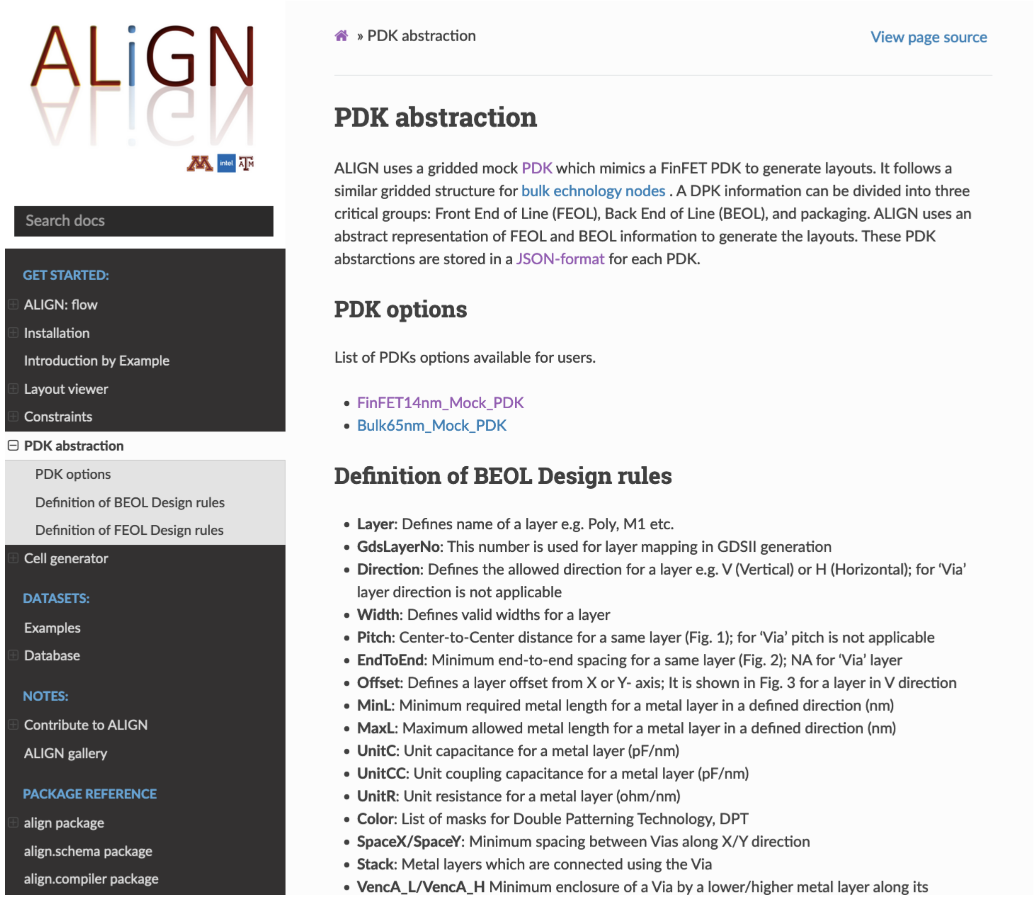
Enabling multiple PDKs

- NDA limitations!
- Working with a foundry to ship ALIGN layers.json with PDK
- Available public-domain or Mock PDKs





- Documentation on setting up a new PDK



» PDK abstraction

View page source

PDK abstraction

ALIGN uses a gridded mock PDK which mimics a FinFET PDK to generate layouts. It follows a similar gridded structure for bulk echnology nodes . A DPK information can be divided into three critical groups: Front End of Line (FEOL), Back End of Line (BEOL), and packaging. ALIGN uses an abstract representation of FEOL and BEOL information to generate the layouts. These PDK abstarctions are stored in a JSON-format for each PDK.

PDK options

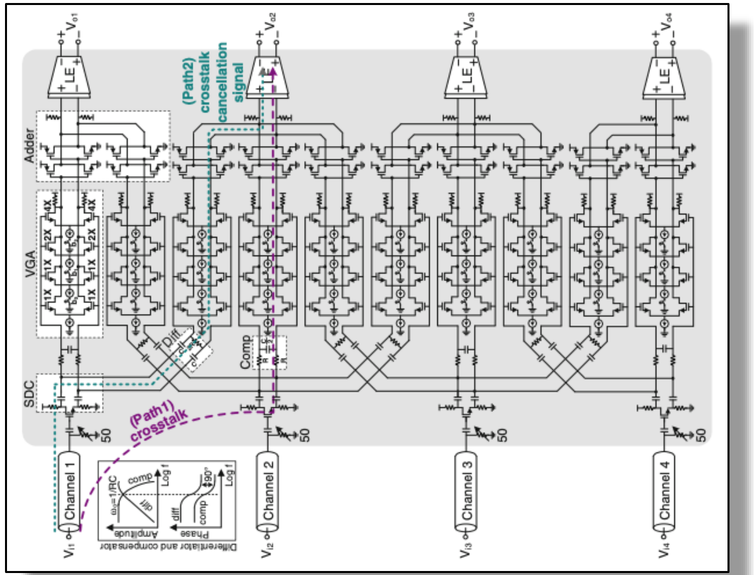
List of PDKs options available for users.

- FinFET14nm_Mock_PDK
- Bulk65nm_Mock_PDK

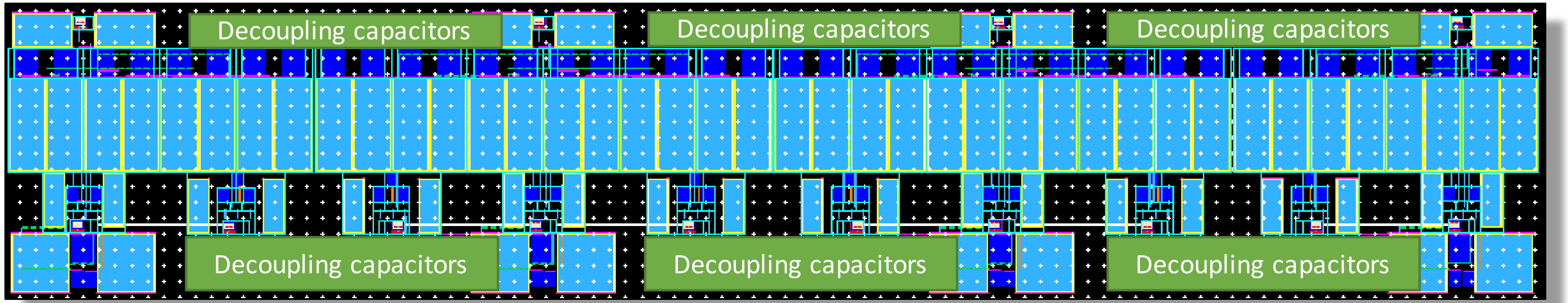
Definition of BEOL Design rules

- **Layer**: Defines name of a layer e.g. Poly, M1 etc.
- **GdsLayerNo**: This number is used for layer mapping in GDSII generation
- **Direction**: Defines the allowed direction for a layer e.g. V (Vertical) or H (Horizontal); for 'Via' layer direction is not applicable
- **Width**: Defines valid widths for a layer
- **Pitch**: Center-to-Center distance for a same layer (Fig. 1); for 'Via' pitch is not applicable
- **EndToEnd**: Minimum end-to-end spacing for a same layer (Fig. 2); NA for 'Via' layer
- **Offset**: Defines a layer offset from X or Y- axis; It is shown in Fig. 3 for a layer in V direction
- **MinL**: Minimum required metal length for a metal layer in a defined direction (nm)
- **MaxL**: Maximum allowed metal length for a metal layer in a defined direction (nm)
- **UnitC**: Unit capacitance for a metal layer (pF/nm)
- **UnitCC**: Unit coupling capacitance for a metal layer (pF/nm)
- **UnitR**: Unit resistance for a metal layer (ohm/nm)
- **Color**: List of masks for Double Patterning Technology, DPT
- **SpaceX/SpaceY**: Minimum spacing between Vias along X/Y direction
- **Stack**: Metal layers which are connected using the Via
- **VencA_L/VencA_H** Minimum enclosure of a Via by a lower/higher metal layer along its

On-chip crosstalk cancellation and reutilization (XTCR) circuit

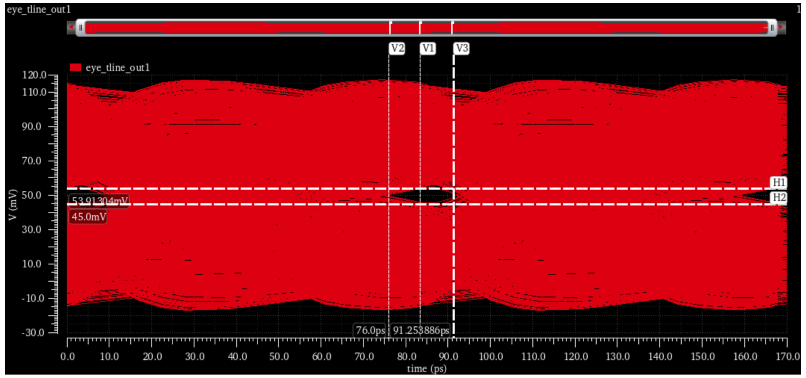


Schematic

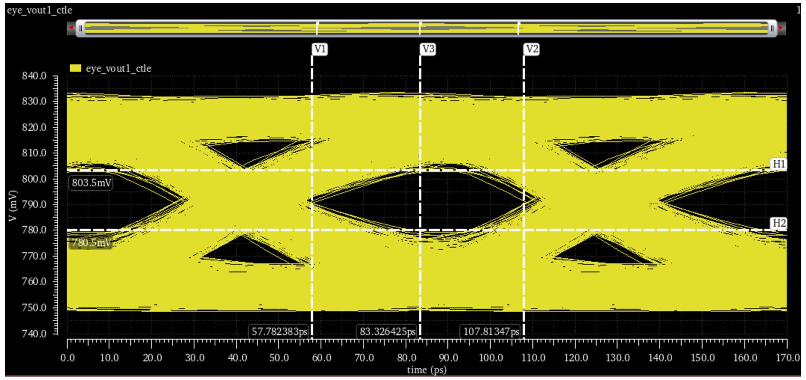


Layout ($479.70\ \mu m \times 95.13\ \mu m$)

194 Transistors
(20 PMOS, 174 NMOS: 174)
174 Passives
(102 Resistors, 72 Capacitors)



Input from the channel



Output

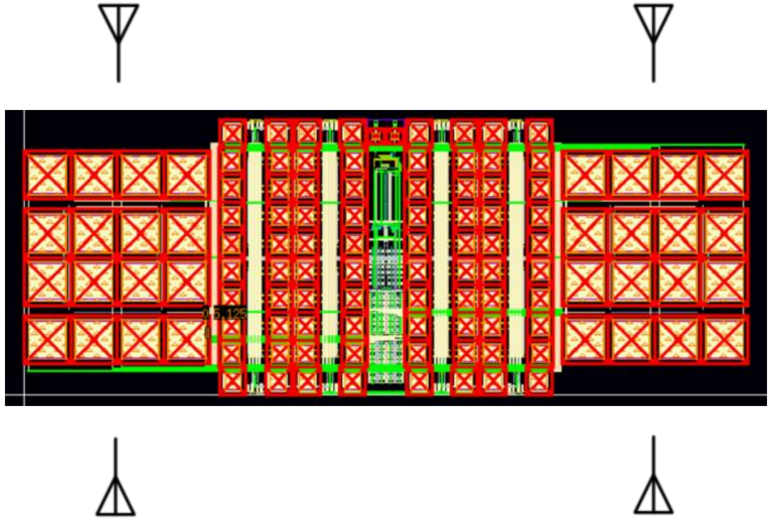
Frequency: 12 GHz (Period = 83 ps)

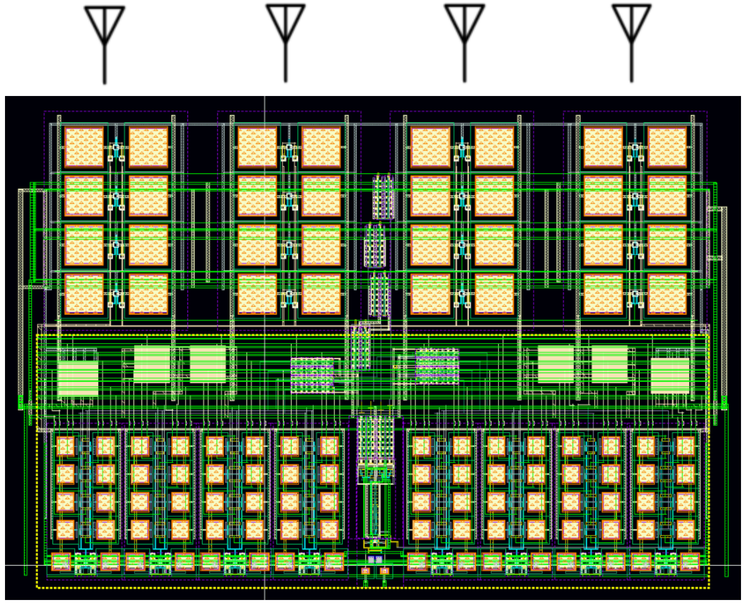
Metrics	Eye @ input	Eye @output	Improvement
Horizontal eye	15.25 ps (18% of period)	50.03 ps (60% of period)	330%
Vertical eye	8.19 mV	23.50 mV	280%

MIMO receiver

ALIGN Layout | **Manual Layout**

Antennas





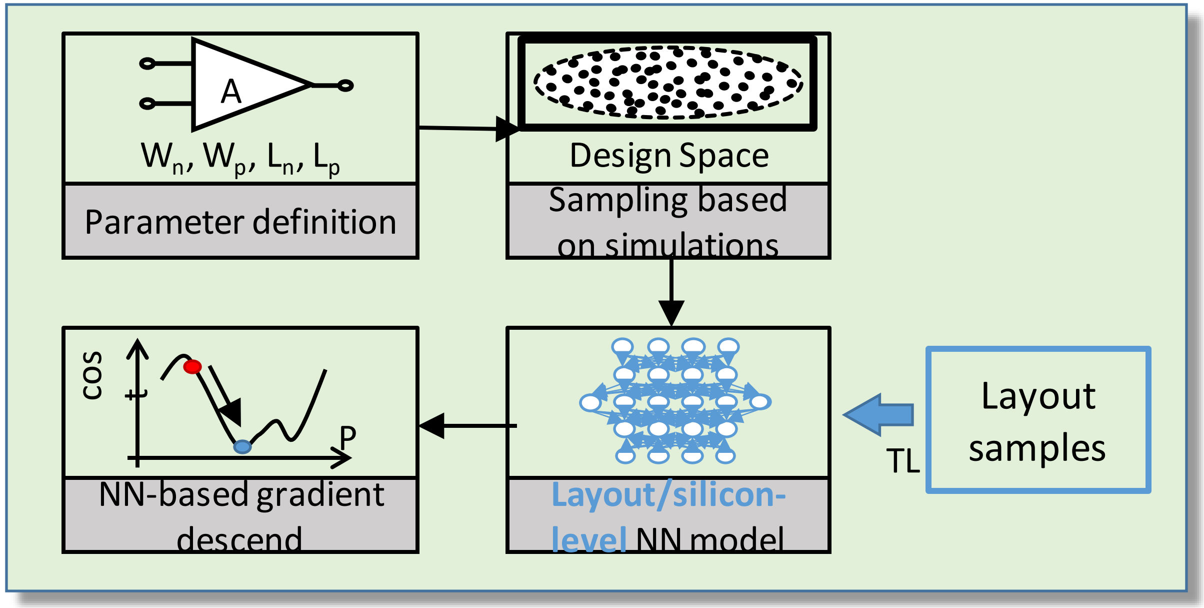
ALIGN layout 39% smaller than manual layout

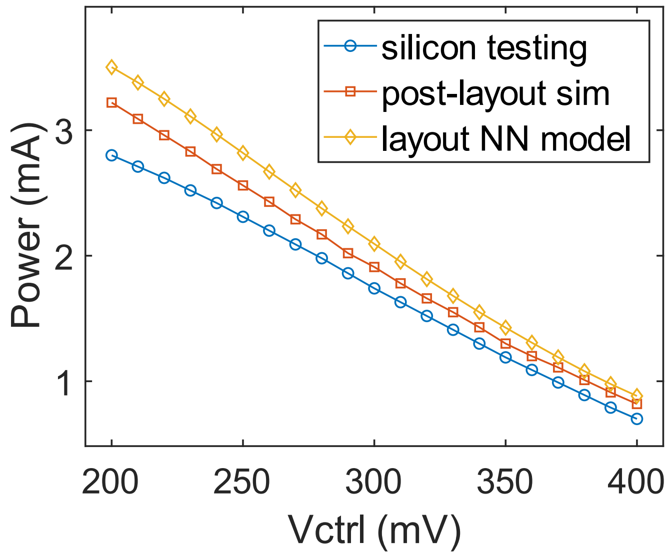
Taped out (TSMC65)

1.489mm × 0.568mm = 0.845mm² | **1.443mm × 0.963mm = 1.389mm²**

Parameters	ALIGN Layout	Manual Layout
Gain	22.39 dB	22.84 dB
Noise Figure (NF)	9.48 dB	9.82 dB
In-Beam B1dB	-21.1 dBm	-19.05 dBm
Out-of-Beam B1dB	0.7 dBm	0.4 dBm

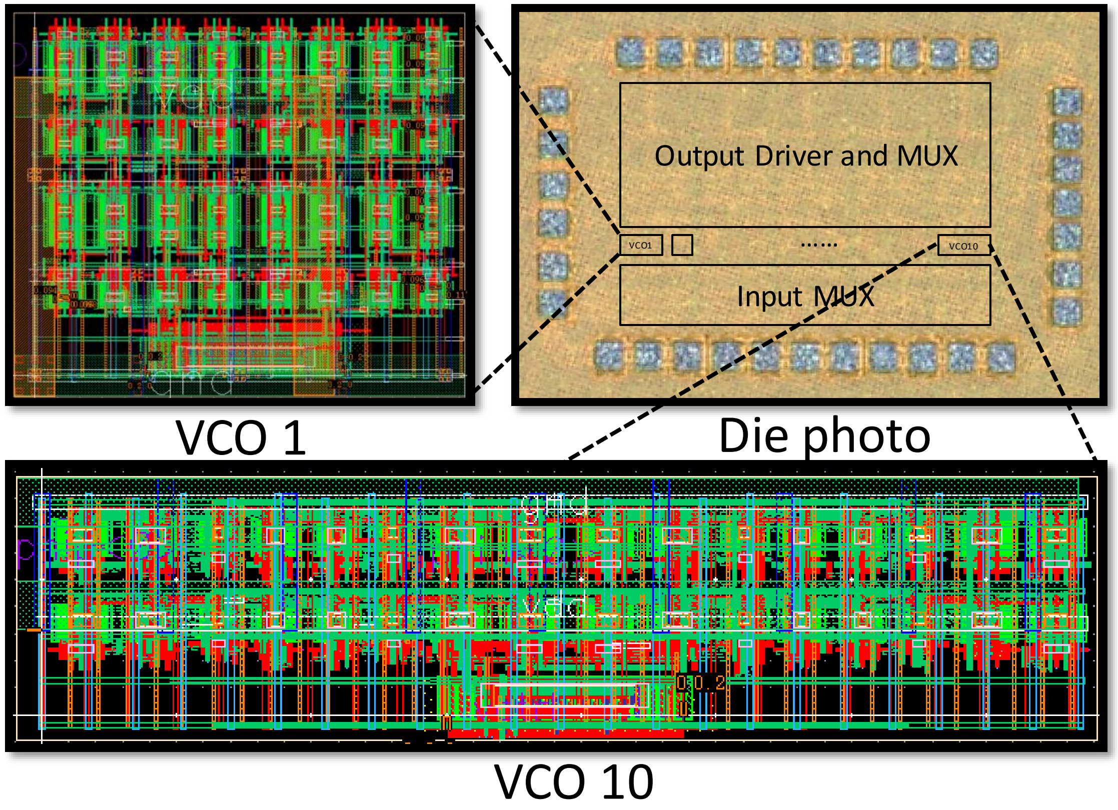
VCO Layout + sizing (collaboration with USC)





Die photo

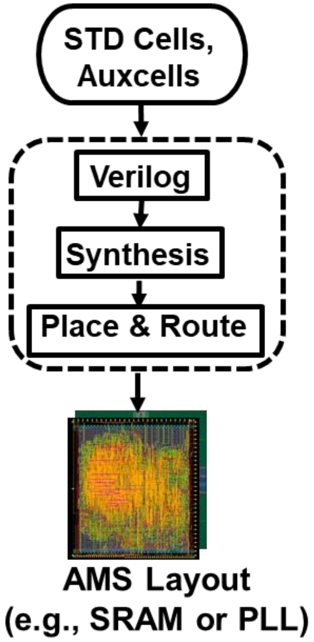
(showing layouts of 2 out of 10 VCOs)

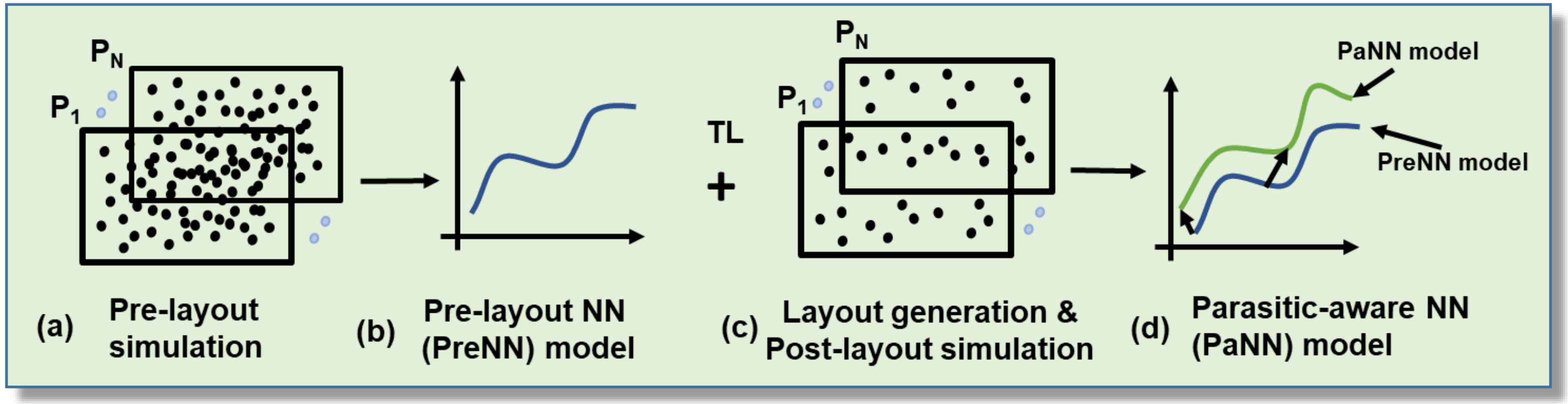


[Liu *et al.*, ICCAD21]

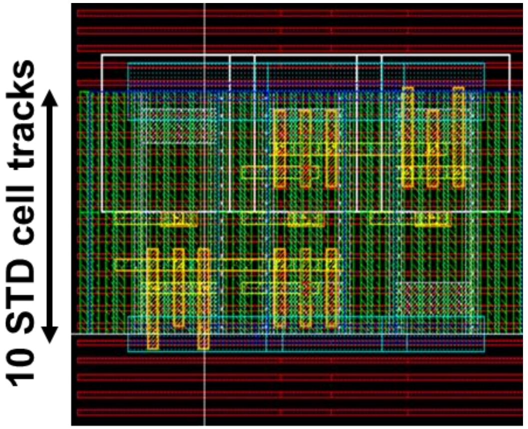
Memory cells (FASoC + ALIGN ("digital analog"): collaboration with UVA

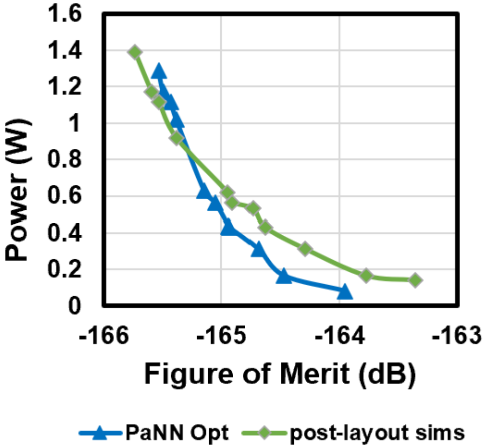
AMS synthesis flow



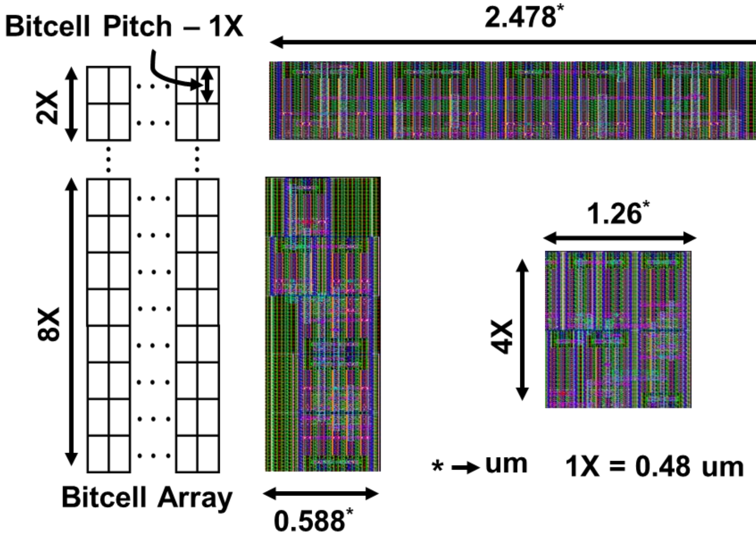


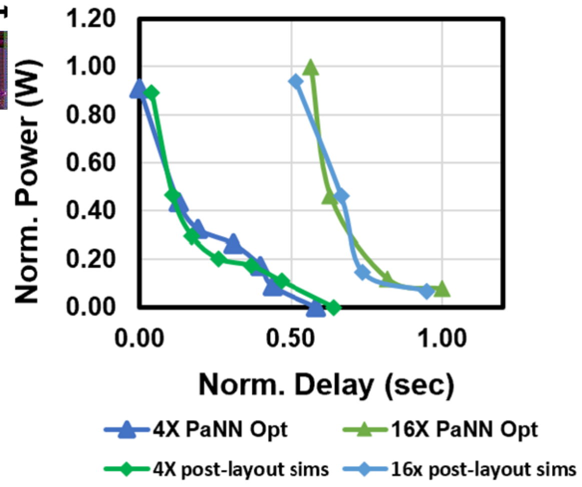
Tristate buffer





Sense amp



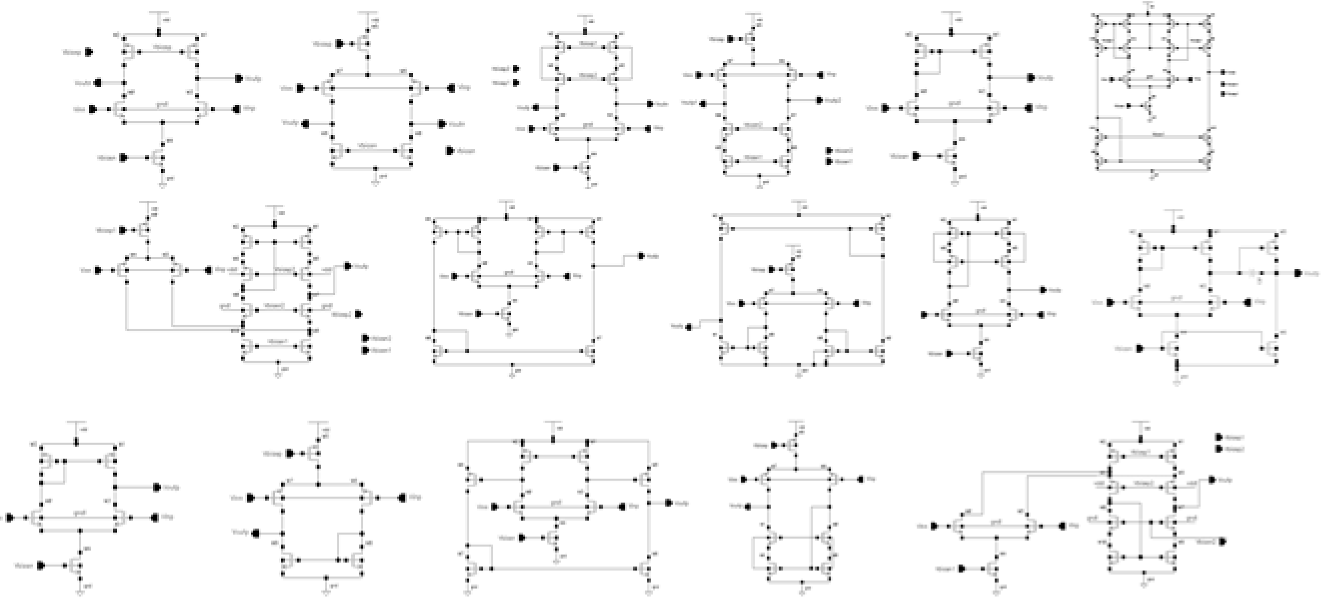


[Kamineni *et al.*, DATE 23]

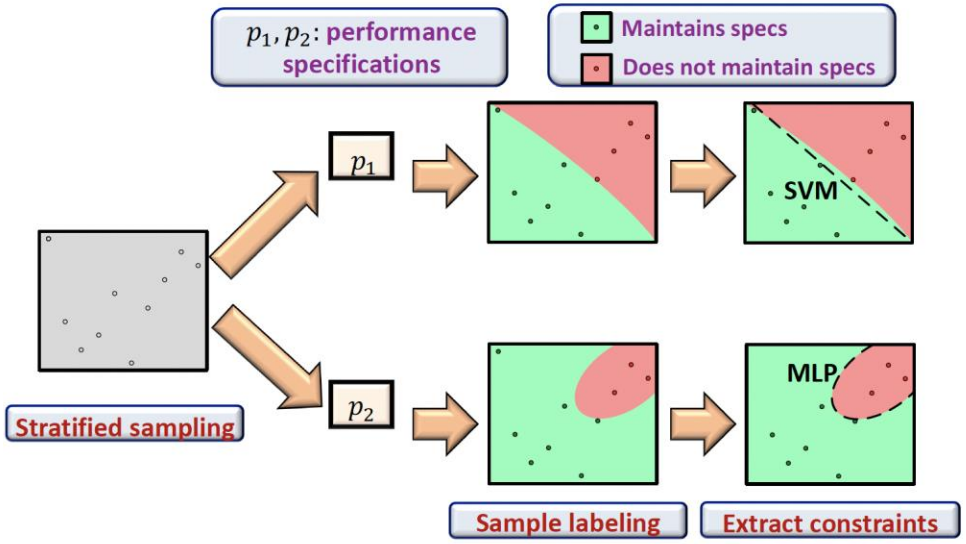
Handling performance constraints still an open issue

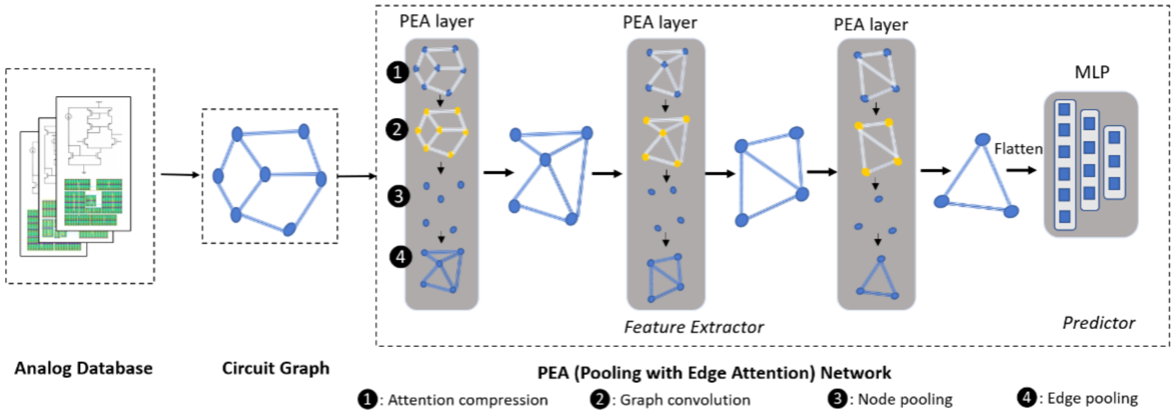
- Types of circuits
  - Operational transconductance amplifiers
  - Comparators
  - Filters
  - Analog-to-digital/digital-to-analog converters
  - Equalizers
  - Clock-data recovery circuits
  - Phase-locked loops/delay-locked loops
  - Low-noise amplifiers
  - Mixers
  - Voltage-controlled oscillators
  - Variable-gain amplifiers
  - Low-dropout regulators
  - Capacitive voltage regulators
  - Inductive DC-DC converters
  - …
- Unit structures are not arbitrarily composable

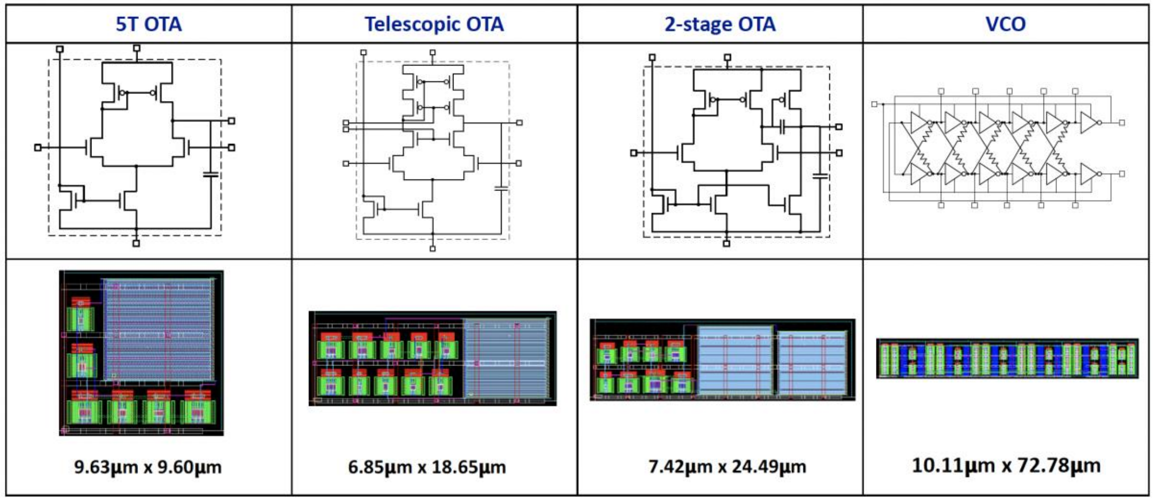
- Each has different performance metrics:
  - OTA: gain, unity gain frequency, bandwidth, CMRR, PSRR, phase margin, slew rate, …
  - DAC: integral nonlinearity, differential nonlinearity, gain, offset, ENOB, sampling rate, …
  - Voltage regulator: ripple, efficiency, standby current, load regulation, PSRR, …
- Multiple allowable topologies – e.g., for OTA:



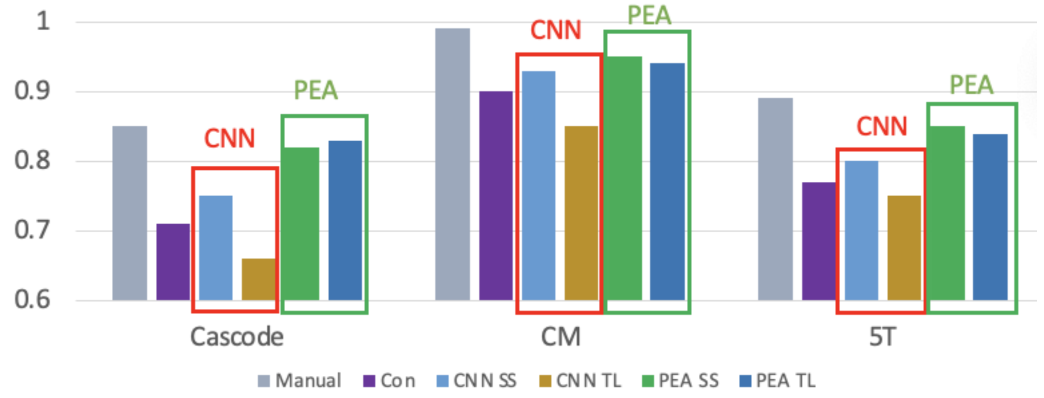
Performance optimization: ML-based







Layout score: close to 1 means close to spec



ALiGN

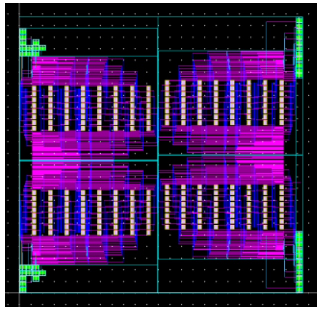
Summary

- We have come a long way since 2018
  - Acknowledgments: we have built upon and benefited from past work
  - But 4.5 years is not enough to build a complete solution

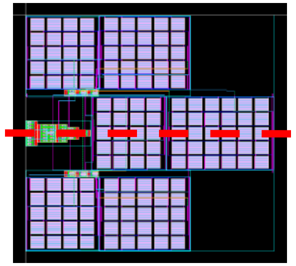
- Open issues
  - Automated performance constraints
  - Learning from designer constraints
  - Routing (Soner Yaldiz's presentation)
  - Supporting multiple PDKs (one-time), working with industry flows
    - Can support PCELLs, PDK kit parts
  - More mature row-based placement for upcoming technologies

ALIGN gallery

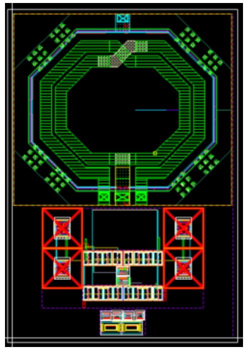
Analog: UW SAR ADC



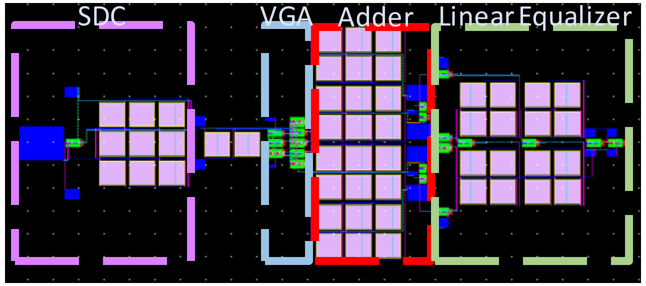
Analog: SC Filter



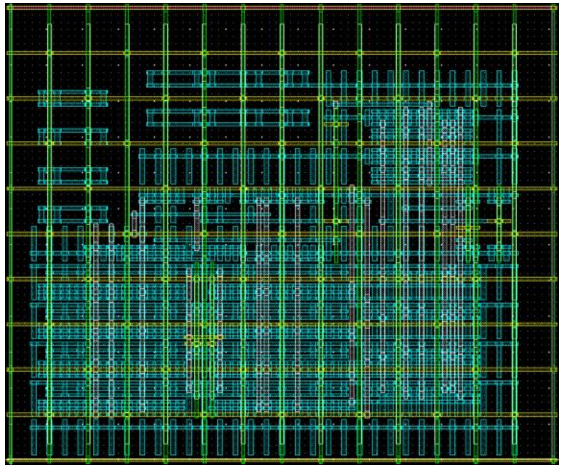
Wireless: BPF



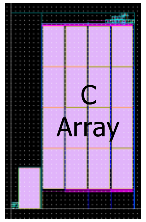
Wireline: Equalizer



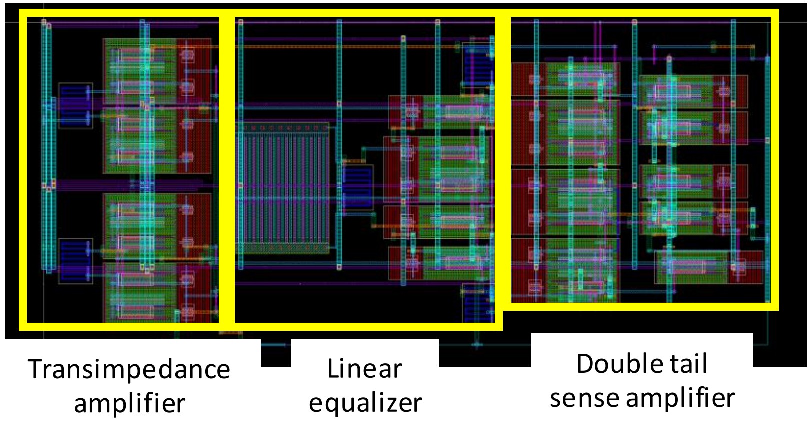
Wireline: Comparator



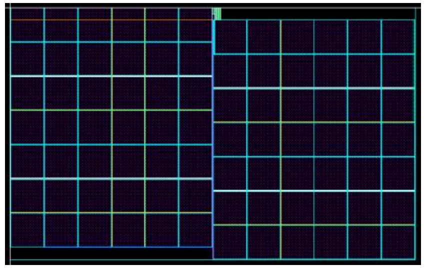
Analog: Capacitive DAC



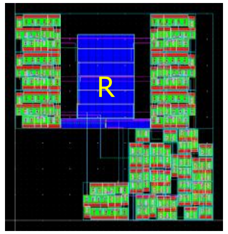
Wireline: Optical Receiver



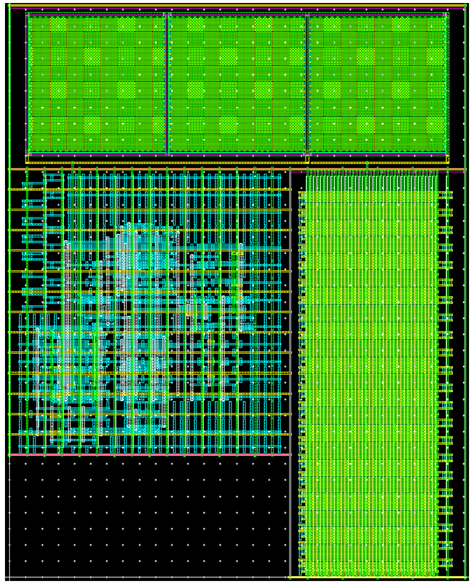
Power delivery: SC DC-DC



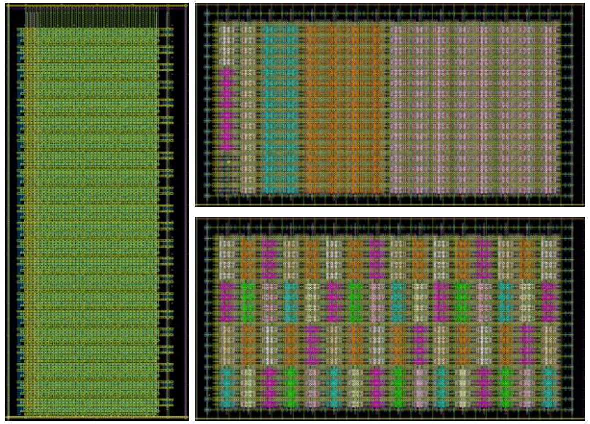
Analog: Flash ADC



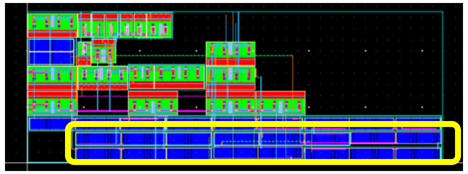
Power delivery: LDO



Power delivery: Powertrains

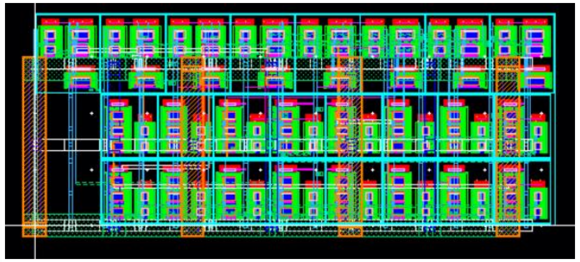


Analog: R2R DAC



Technologies
GF12, ASAP7,
Intel (Various),
TSMC65

Wireline: VCO



ALiGN

Special thanks to the entire ALIGN team

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TEXAS A&M UNIVERSITY.