Learning from the Implicit Functional Hierarchy in an Analog Netlist

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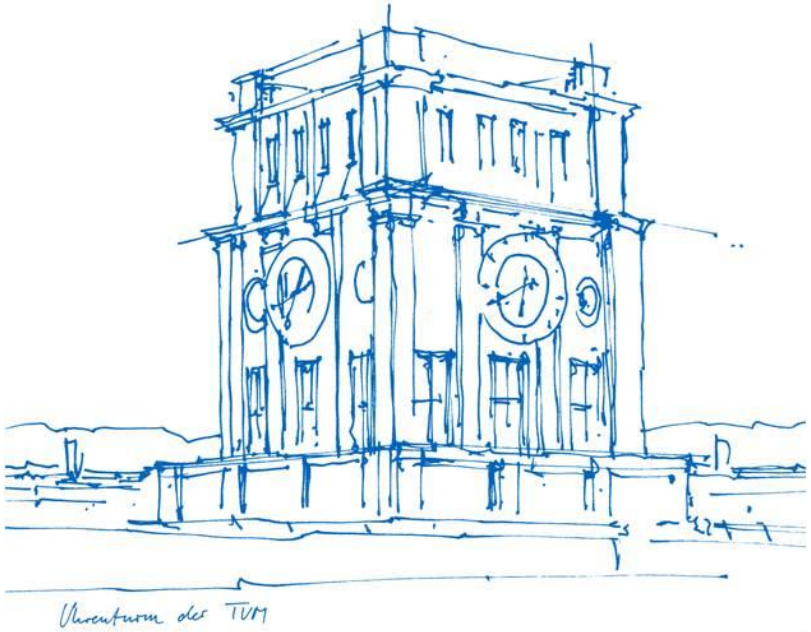

Content

- Constraints/rules from hierarchical structure (sizing)
- Constraints/rules from netlist and signal flow (placement) [slide 14, video minute 18:45]
- Constraints/rules/functions from hierarchical function (modeling) [slide 22, video minute 27:40]

Content

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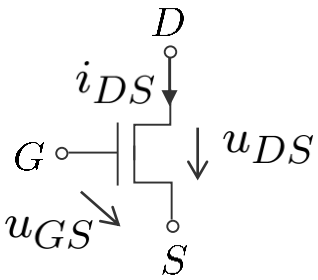
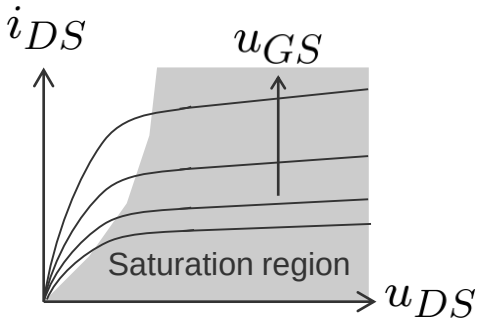
- Constraints/rules from netlist and signal flow (placement)
- Constraints/rules/functions from hierarchical function (modeling)

Sizing Constraints – Transistor (1)



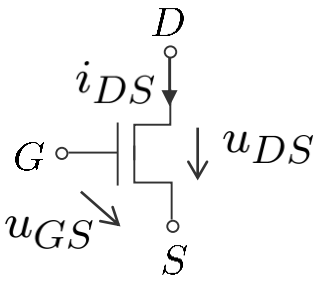


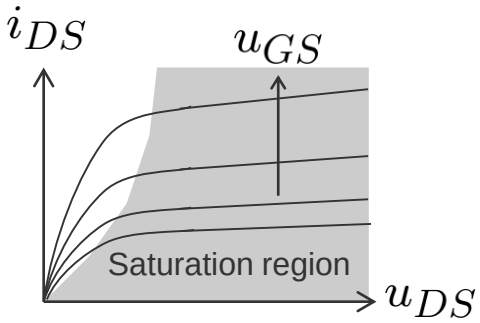
Voltage-controlled current source:

$$i_{DS} = K \cdot \frac{W}{L} \cdot (u_{GS} - U_{th})^2 \cdot (1 + \lambda \cdot u_{DS})$$

- Keep transistor in saturation: $u_{DS} - (u_{GS} - U_{th}) \geq U_{satmin}\,,\quad u_{GS} - U_{th} \geq 0\,,\quad u_{DS} \geq 0$

Sizing Constraints – Transistor (2)





Voltage-controlled current source:

$$i_{DS} = K \cdot \frac{W}{L} \cdot (u_{GS} - U_{th})^2 \cdot (1 + \lambda \cdot u_{DS})$$

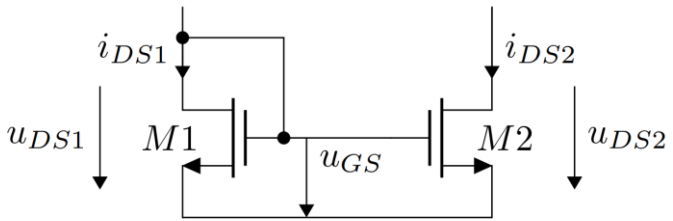
- Minimize variance of drain-source current due to manufacture variation:

$$\sigma^2_{iDS} = \sum_{X=K,W,L,U_{th}} \left(\frac{\partial i_{DS}}{\partial X}\right)^2 \cdot \sigma^2_X \longrightarrow \frac{\sigma^2_{iDS}}{i^2_{DS}} = \frac{A_K}{W \cdot L} + \frac{\sigma^2_W}{W^2} + \frac{\sigma^2_L}{L^2} + \frac{4}{(u_{GS} - U_{th})^2} \cdot \frac{A_{Uth}}{W \cdot L}$$

$$\left(\frac{\sigma_K}{K}\right)^2 = \frac{A_K}{W \cdot L} \qquad \sigma^2_{Vth} = \frac{A_{Vth}}{W \cdot L}$$

$$W \cdot L \geq A_{minA}\,, \quad W \geq W_{minA}\,, \quad L \geq L_{minA}$$

Sizing Constraints – Current Mirror



$$r = \frac{i_{DS2}}{i_{DS1}} = \frac{\frac{W_2}{L_2} \cdot (u_{GS} - U_{th2})^2 \cdot (1 + \lambda \cdot u_{DS2})}{\frac{W_1}{L_1} \cdot (u_{GS} - U_{th1})^2 \cdot (1 + \lambda \cdot u_{DS1})}$$

- Prepare regular layout (fingers, interdigitated/common centroid):
- Reduce impact of local manufacturing variation:
- Reduce impact of channel length modulation in circuit:

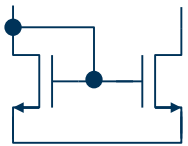
$$L_1 = L_2\,, \quad W_2 = r \cdot W_1$$

$$\|u_{GS} - U_{th1,2}\| \geq U_{GSmin}$$

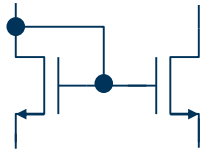
$$\|u_{DS2} - U_{DS1}\| \leq \Delta U_{DSmax}$$

Structural Blocks – Transistor Pairs

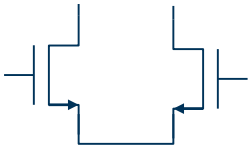
- 203 variants (Bell number)
- Few transistor pairs with design-relevant function, e.g.,



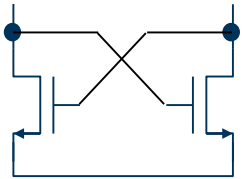
2-transistor current mirror



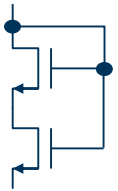
Level shifter



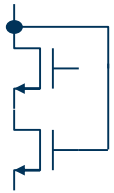
Differential pair



Flipflop

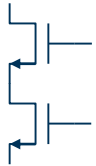


Voltage reference 1



Voltage reference 2

Current mirror load

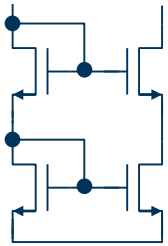


Cascode pair

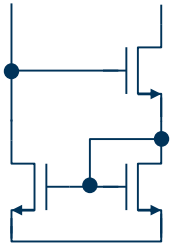
Mixed pair

Structural Blocks – Transistor Groups

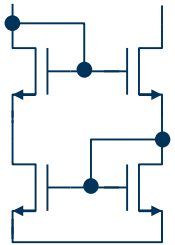
- E.g., current mirrors with 3 or 4 transistors, differential stage,



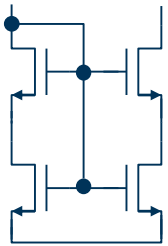
Cascode current mirror (cm)



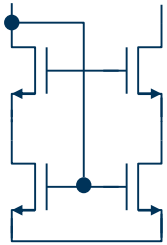
Wilson cm



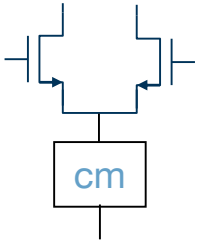
Wilson 2 cm



4-transistor cm



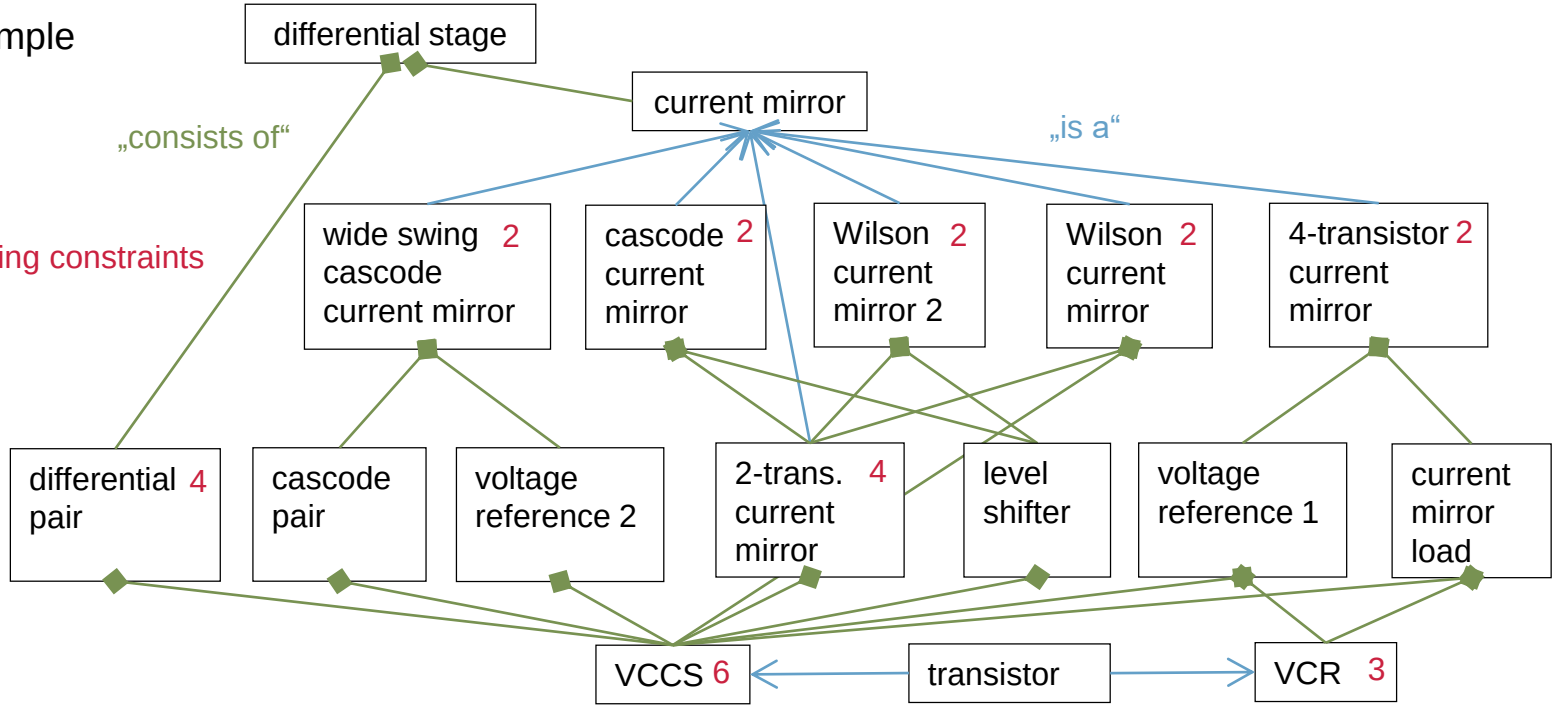
Wide-swing cascode cm



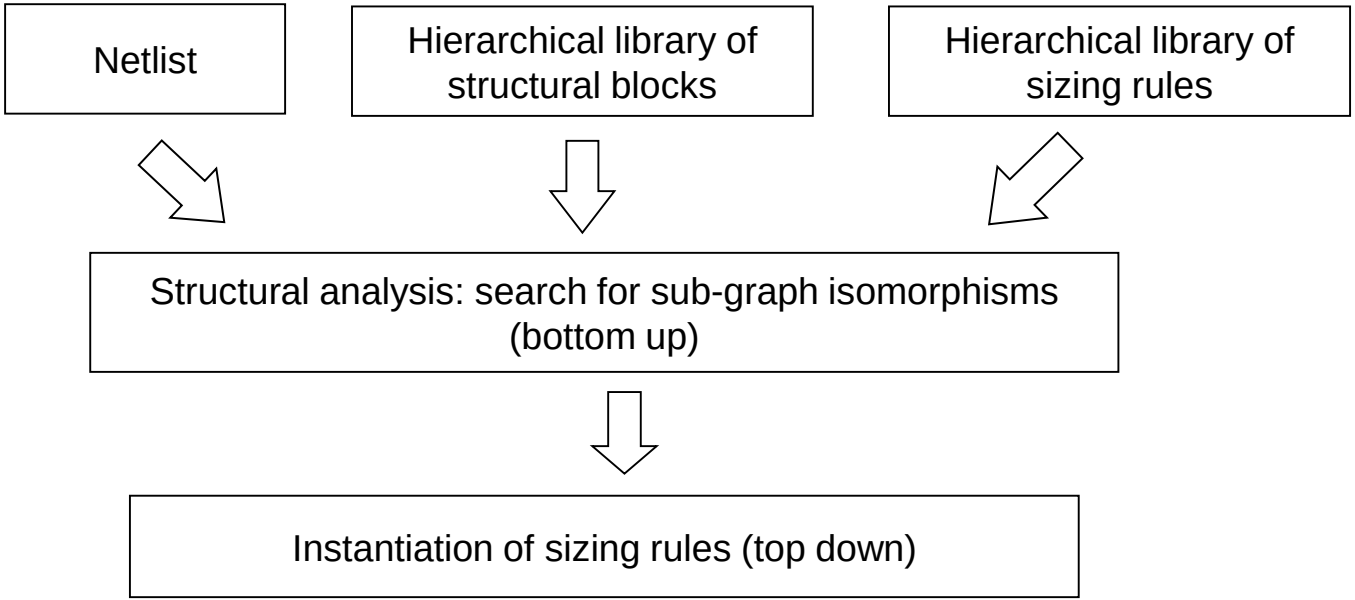
Differential stage

Hierarchical Library of Structural Blocks

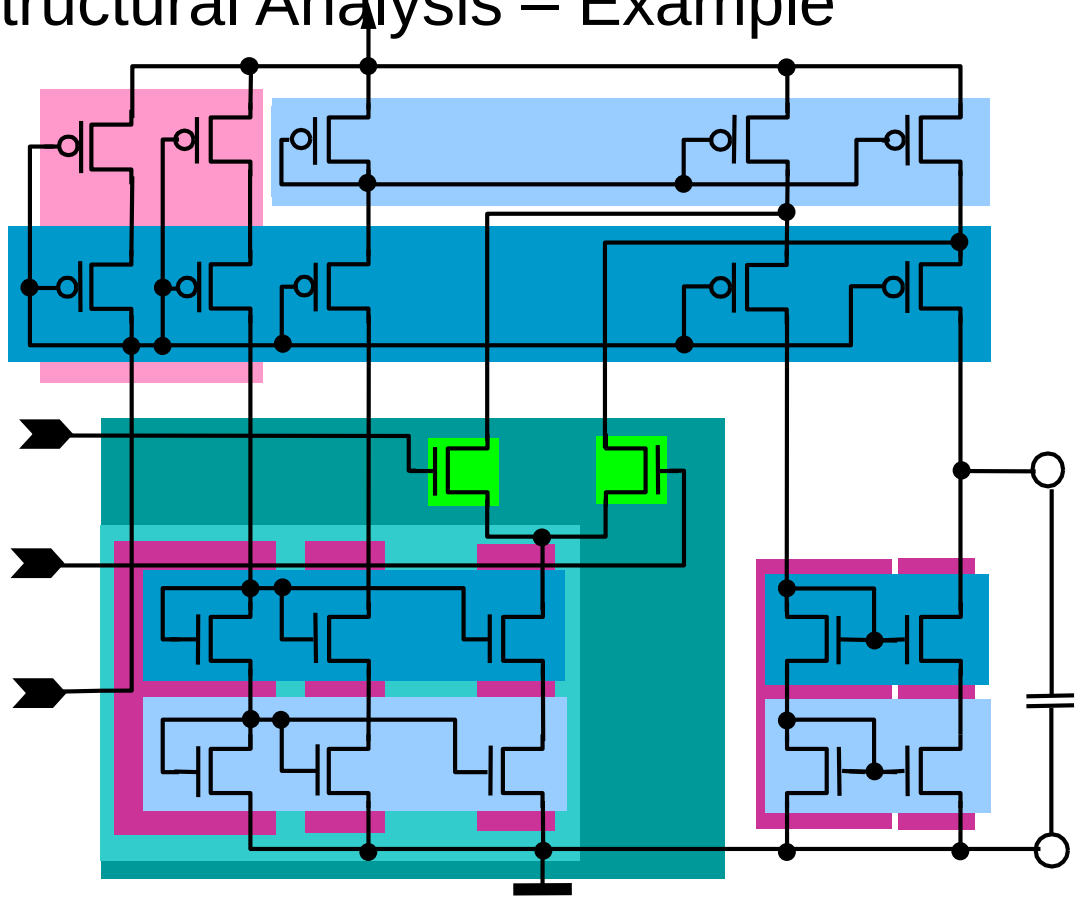
- Example



Structural Analysis of a Netlist



Structural Analysis – Example



voltage reference 1

current mirror load

2-trans. current mirror

level shifter

differential pair

4-transistor current mirror

current mirror (bank)

level shifter (bank)

cascode current mirror

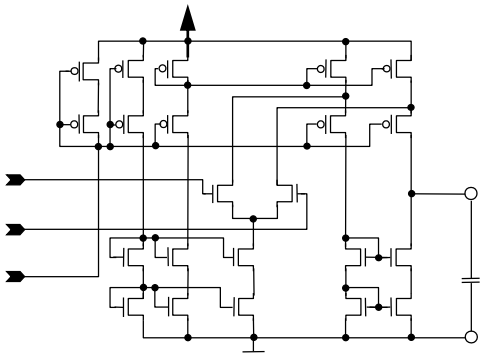
casc. curr. mirror bank

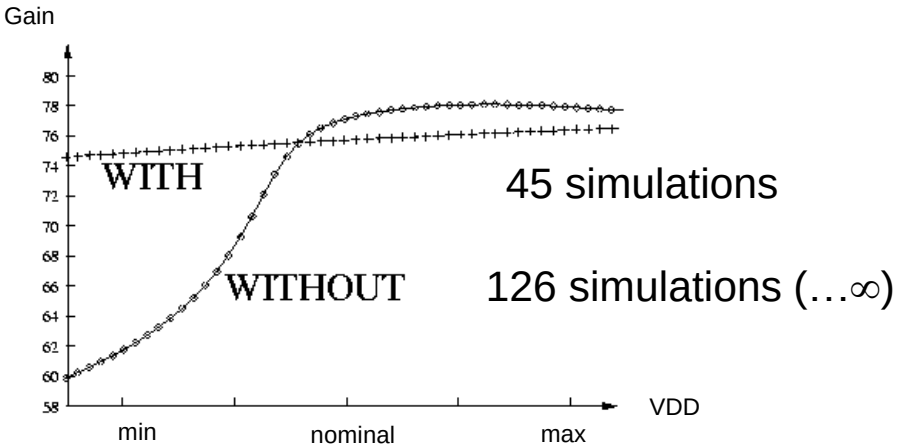
differential stage

30 equations + 160 inequalities → 190 sizing rules

Influence of Sizing Constraints on Sizing Process

- Typical example

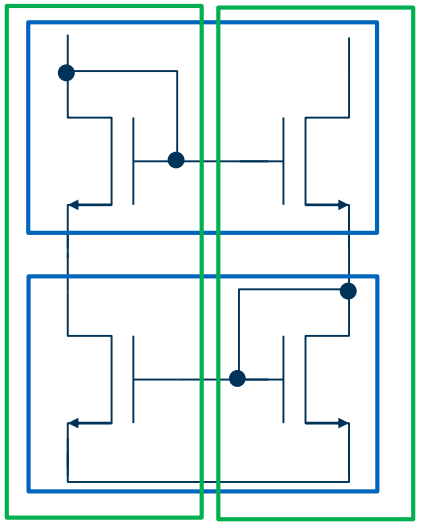




- Better efficiency and convergence of sizing process
- Higher circuit robustness

It Is Not That Easy

- Arbitration of transistor groups: “If a transistor is part of group A, it is not part of group B.”
- Several ways of composition, e.g., Wilson 2 current mirror:



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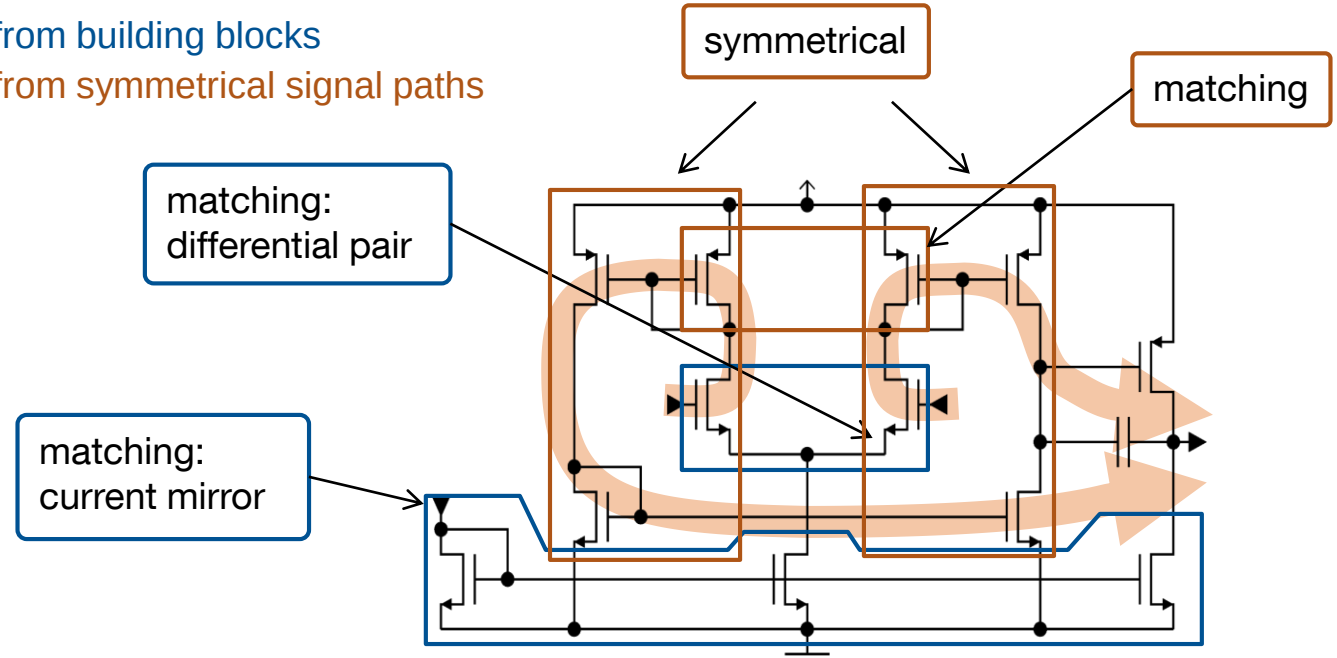
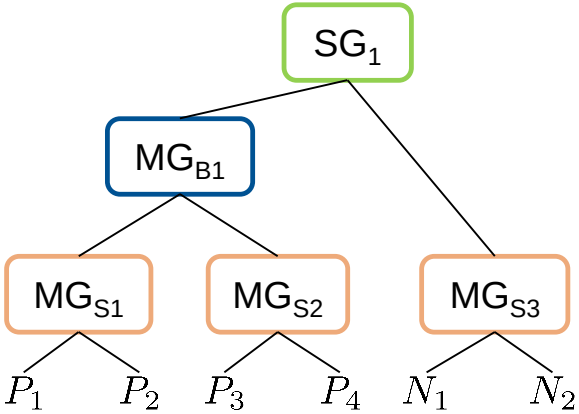
Constraints Across Building Blocks

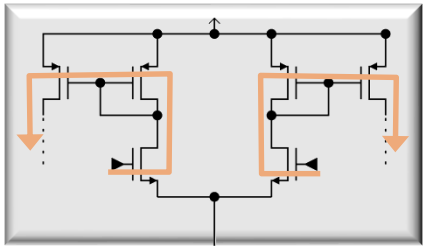
- Constraints from building blocks
- Constraints from symmetrical signal paths

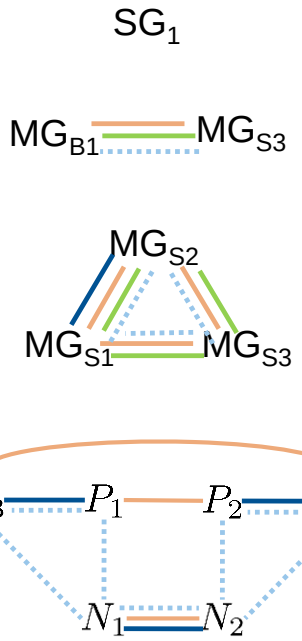


Placement Plan Construction from Constraint Hierarchy

- Priority:
  1. Matching constraints (symmetry path)
  2. Matching constraints (building blocks)
  3. Proximity constraints (building blocks)
  4. Symmetry constraints
  5. Proximity constraints (netlist)
- $MG_{S/B}$: Matching group (symmetry/building blocks)
- SG: Symmetry group
- PG_N: Proximity group (netlist)

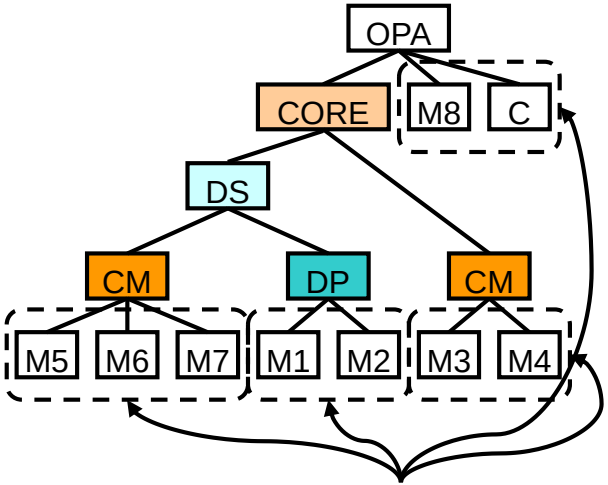




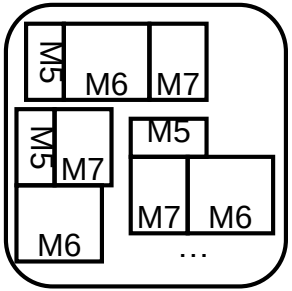


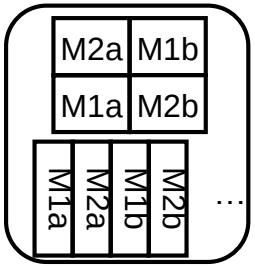
3.: NA
4.: fully meshed

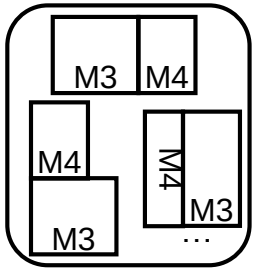
Placement: Enumerate Basic Building Blocks

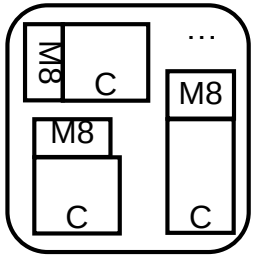


Basic building blocks



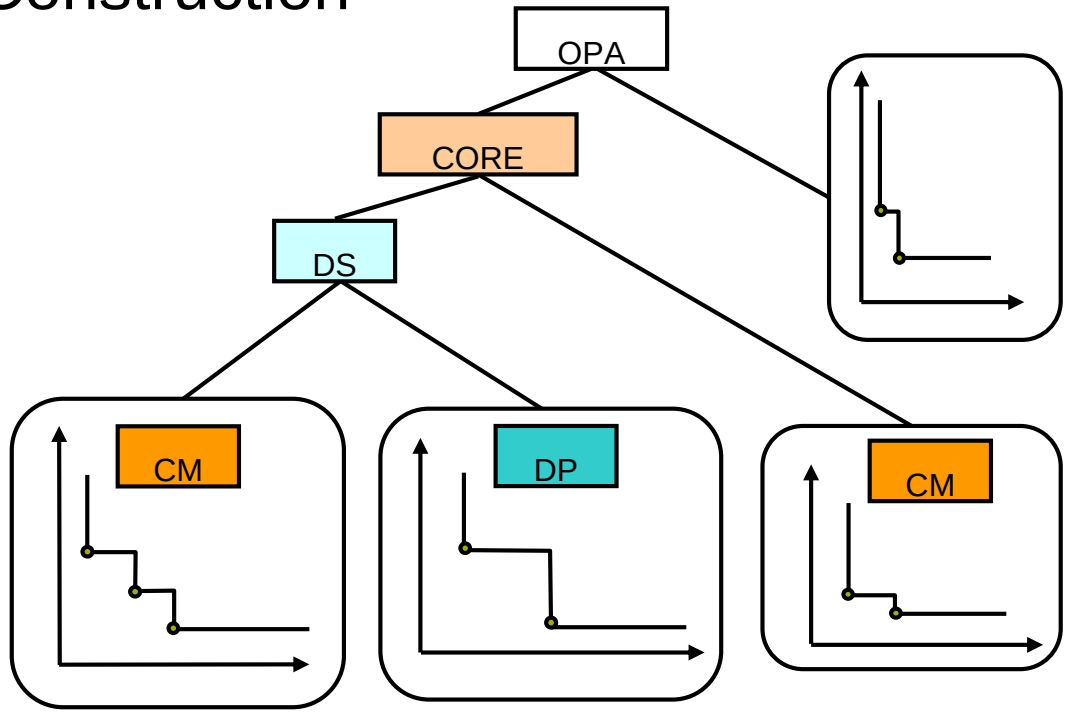






Bottom-up Placement Construction

- Code placements as B* trees in enhanced shape functions
- Enhanced shape functions are added horizontally/vertically
- Bottom up along placement plan
- White space is utilized
- Constraints are provably kept



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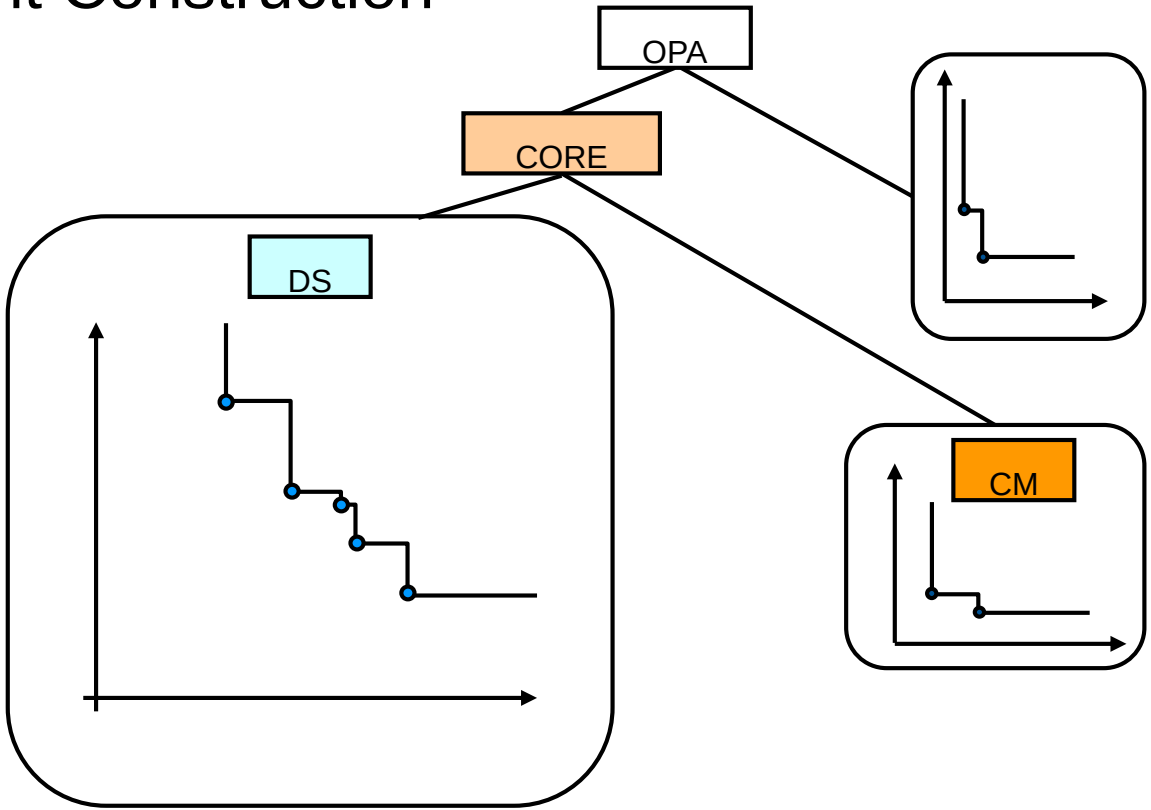

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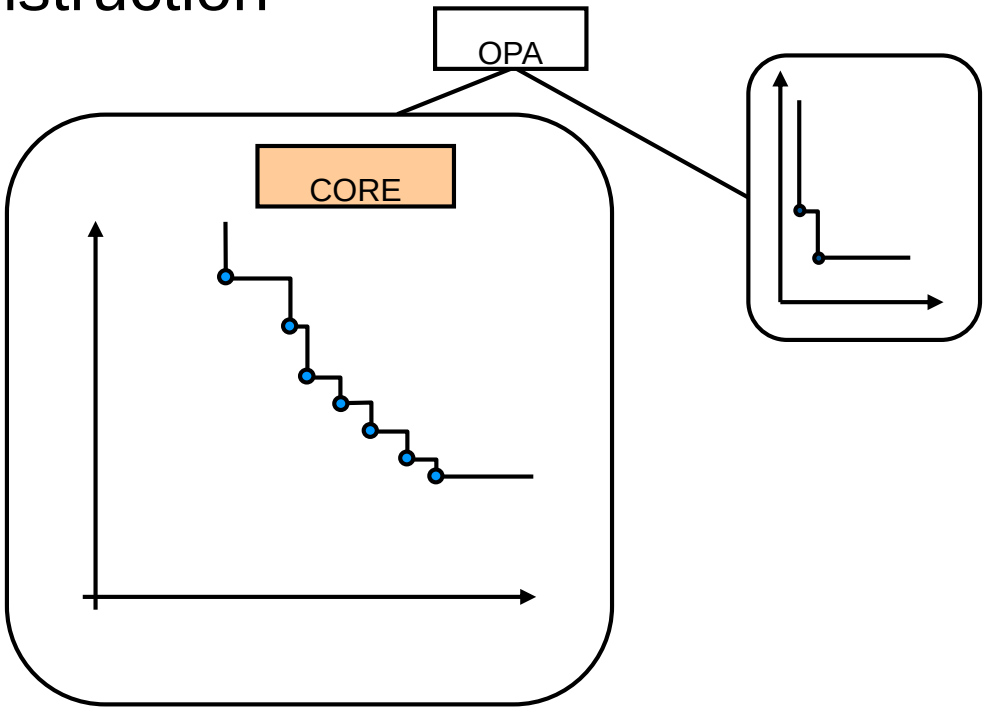

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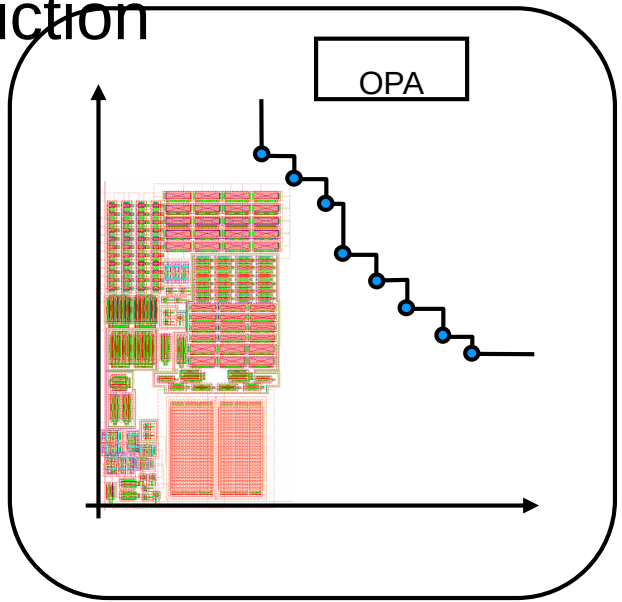

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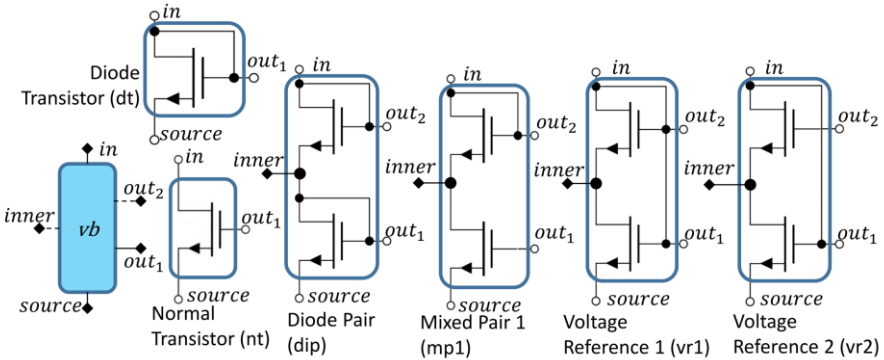
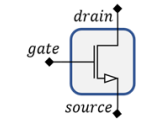
Beyond Structural Blocks: Functional Blocks



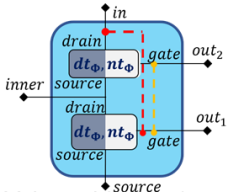
- Example voltage bias (vb)
- Converts current into node in into voltage at node $out1$ or at nodes $out1$ and $out2$
- E.g., part of current mirror

- Blocks representing a certain analog function within analog circuit
- Number of pins may vary depending on structural implementation by transistor netlist
- One functional block refers to several structural implementations
- One structural implementation refers to several functional blocks

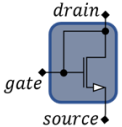
Functional Block Library



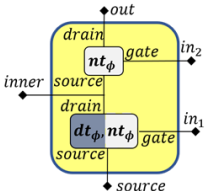
Normal transistor (nt)



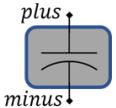
Voltage bias (vb)



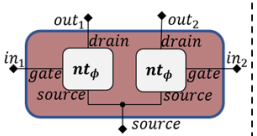
Diode transistor (dt)



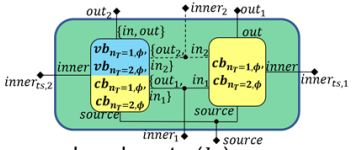
Current bias (cb)



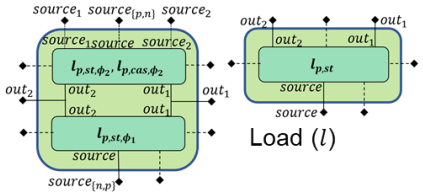
Capacitor (cap)



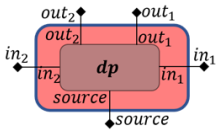
Differential pair (dp)



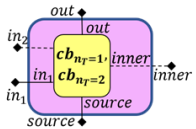
Load parts (l_p)



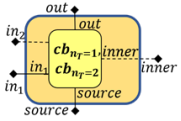
Load (l)



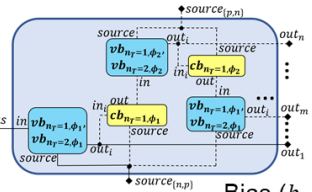
Transconduc-tor first stage (tc_s)



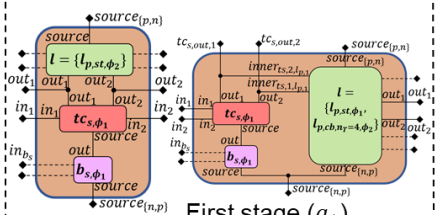
Stage bias (b_s)



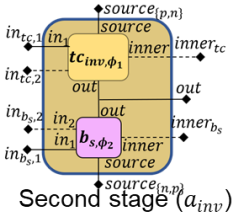
Transconduc-tor second stage (tc_{inv})



Bias (b_O)

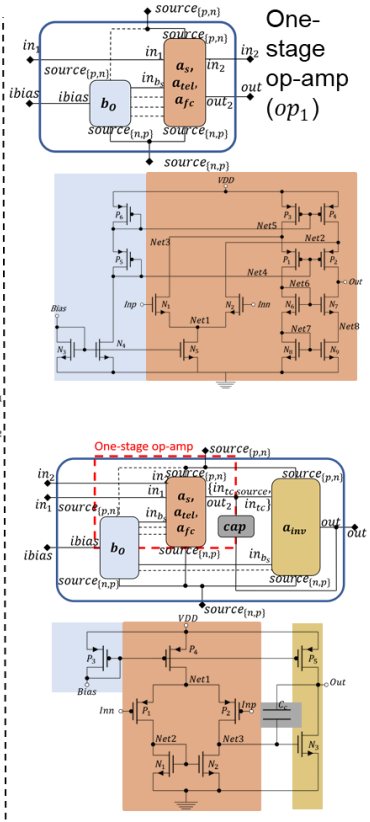


First stage (a_1)



Second stage (a_{inv})

One-stage op-amp (op_1)



Hierarchical Performance and Constraint Library

	Symmetry constraints	Behavioral constraints	Intermediate performance equations	Op-amp performance equations
Devices			Saturation vds **Net capacitance**	Area Quiescent power
Structures	Current mirror constraints	Current mirror behavior		
Amplification stage subblocks	Load Non-inverting transconductor	Complementary transconductor	**Transconductance** *Output conductance*	
Amplification stages	Inverting stages	Output voltage offset	*Stage output resistance* Stage open-loop gain Stage non-dominant poles Stage zeroes	Common-mode input voltage Output voltage Common-mode rejection ratio **Unity-gain bandwidth**
Op-amp			Dominant pole Positive zero	Open-loop gain Slew rate Phase margin

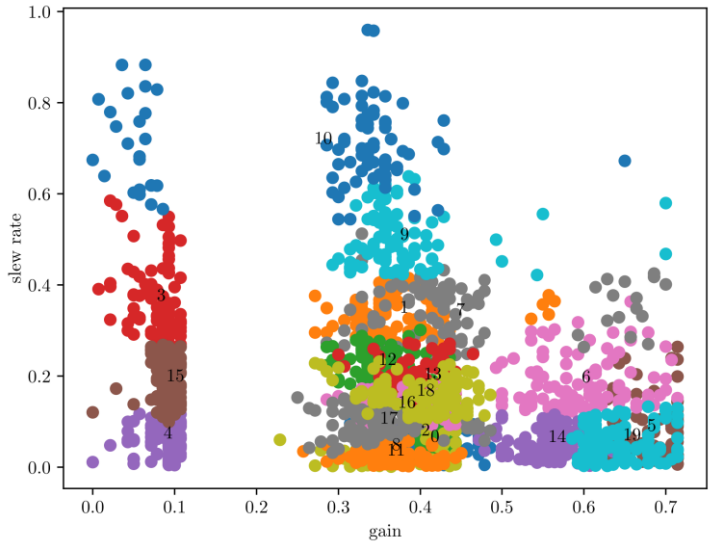
Design – Clustering and Modeling with Neural Networks

Performance	Minimum	Maximum
gain	$40\,dB$	$140\,dB$
slew rate	$2\,\frac{V}{\mu s}$	$217\,\frac{V}{\mu s}$
phase margin	55°	90°
transit frequency	$3\,MHz$	$173\,MHz$

- >500 opamp structures
- ~20 different structural building blocks : transistor pairs, current mirror types, analog inverters
- Functional block characterization: load, transconductance, bias, opamp stage
- >150 sizings for various specs for each opamp structure
- Overall ~100,000 designs with these details: structure, hierarchy of building blocks, functional blocks, sizing, performance

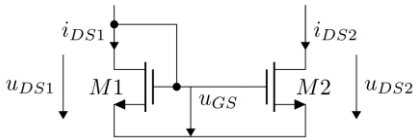
Neural-network Driven Topology Selection

- Build neural network, e.g., for ~20 clusters of performance subranges, mapping performance on topology
- Speed up topology selection by applying this neural network (reduced set of potential topologies compared to enumeration)
- Precision > 70%, recall > 70%

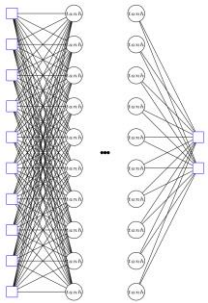


Neural-network Driven Circuit Sizing

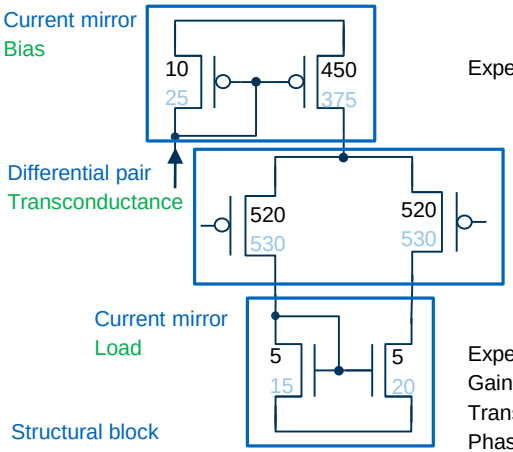
- Determine a neural network for each functional block that maps circuit specification on sizing of block
- Independent sizing of functional blocks of a circuit, e.g.,



Input:
- Functional blocks M1, M2 belong to
- Circuit performance and sizing of reference block
- Circuit specification



Output:
Sizing of M1, M2



Conclusion

- Hierarchical libraries of building blocks
- Associated generic sets of constraints, rules and functions
- Set-up of constraints, rules and functions crucial for synthesis, sizing and layout

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- Maximilian Neuner*
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- Michael Eick
- Martin Strasser
- Tobias Massier
- Robert Schwencker
- Stephan Zizala
- Josef Eckmüller

(ordering according to (*expected) PhD graduation starting from most recent)

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