Joint Optimization of Sizing and Layout for AMS Designs: Challenges and Opportunities

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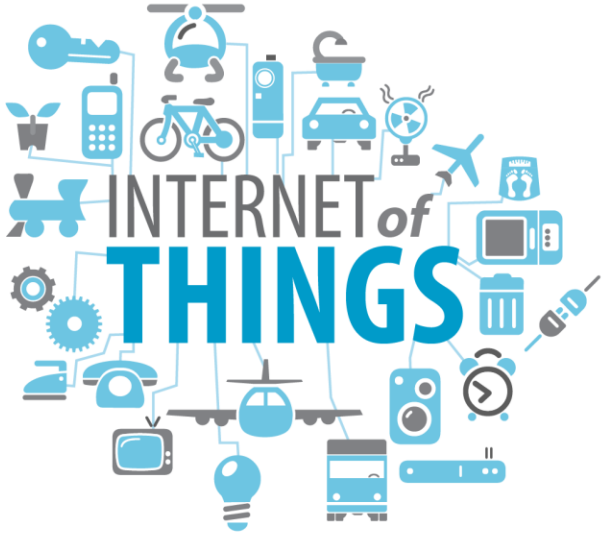
Analog ICs: Introduction

- Sensor related applications and real-world interfaces require analog circuits
- Increasing market demand: Internet of Things (IoT), autonomous and electric vehicles, communication and 5G networks…



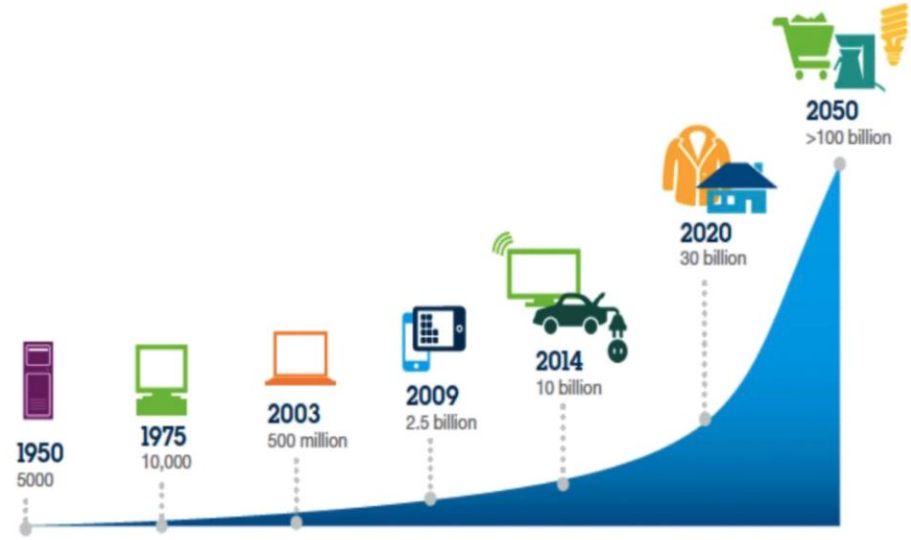
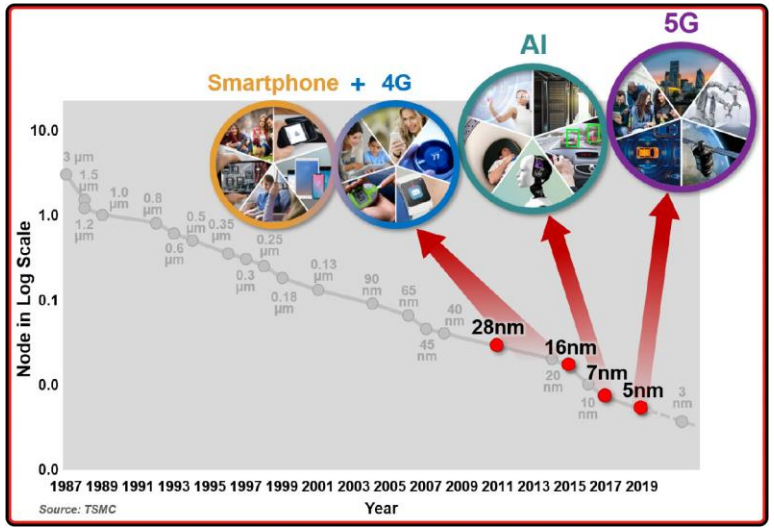
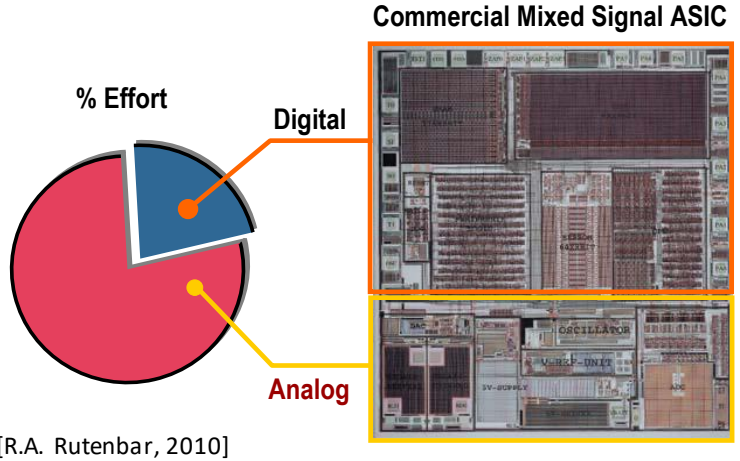


Image Sources: IBM, Ansys, public technology

Motivations for Analog Automation

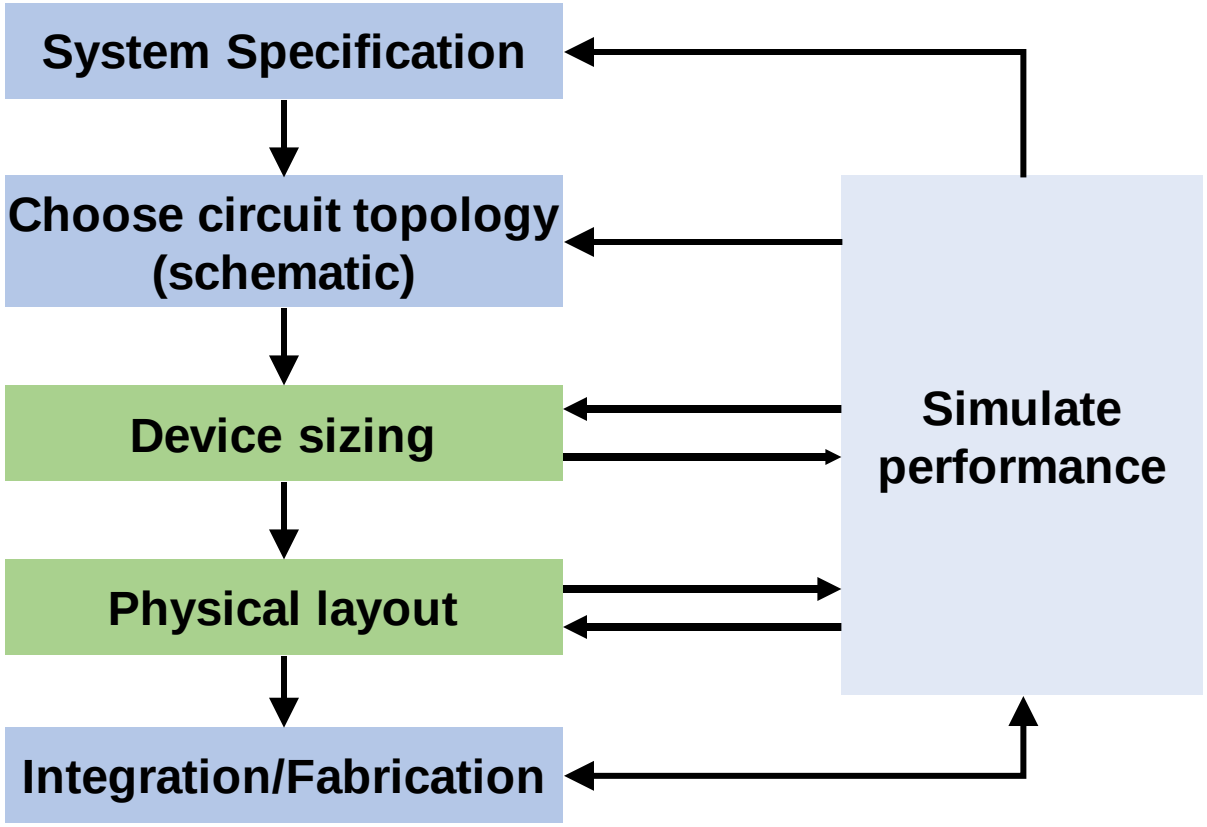




[R.A. Rutenbar, 2010]

- There exist repeating tasks:
  - Design is carried from one process fap to another
  - Same design needs to be altered for a new set of performance specifications
- Analog is here to stay:
  - Not all analog blocks can be converted to digital
  - Converting everything to digital and exploiting the existed automation is not a viable option
- Better community & computers

Analog Design Challenge



- Heavily manual and iterative process
- Simulations involved in every step, but they can be very costly
- Sizing/resizing and updated layout is required

Analog Sizing Task

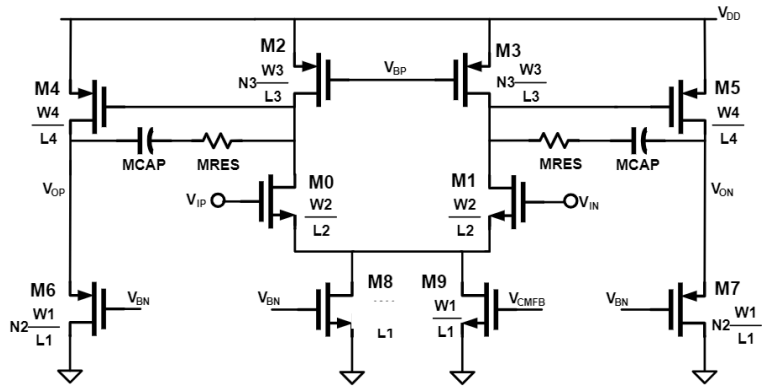
Specifications

minimize $Power$
s.t. DC Gain > 60 dB
CMRR > 80 dB
PSRR > 80 dB
Output Swing > 2.4 V
Output Noise $< 3 \times 10^{-4}$ V_{rms}
Phase Margin > 60 deg
Unity Gain Frequency > 40 MHz
Settling Time $< 3 \times 10^{-8}$ s
Static error < 0.1
Saturation Margin > 50 mV

Design parameters & ranges

Parameters	LB	UB
L1 (μm)	0.18	2
L2 (μm)	0.18	2
⋮	⋮	⋮
W1 (μm)	0.22	150
W2(μm)	0.22	150
⋮	⋮	⋮
N3(integer)	1	20
N4(integer)	1	20

Topology

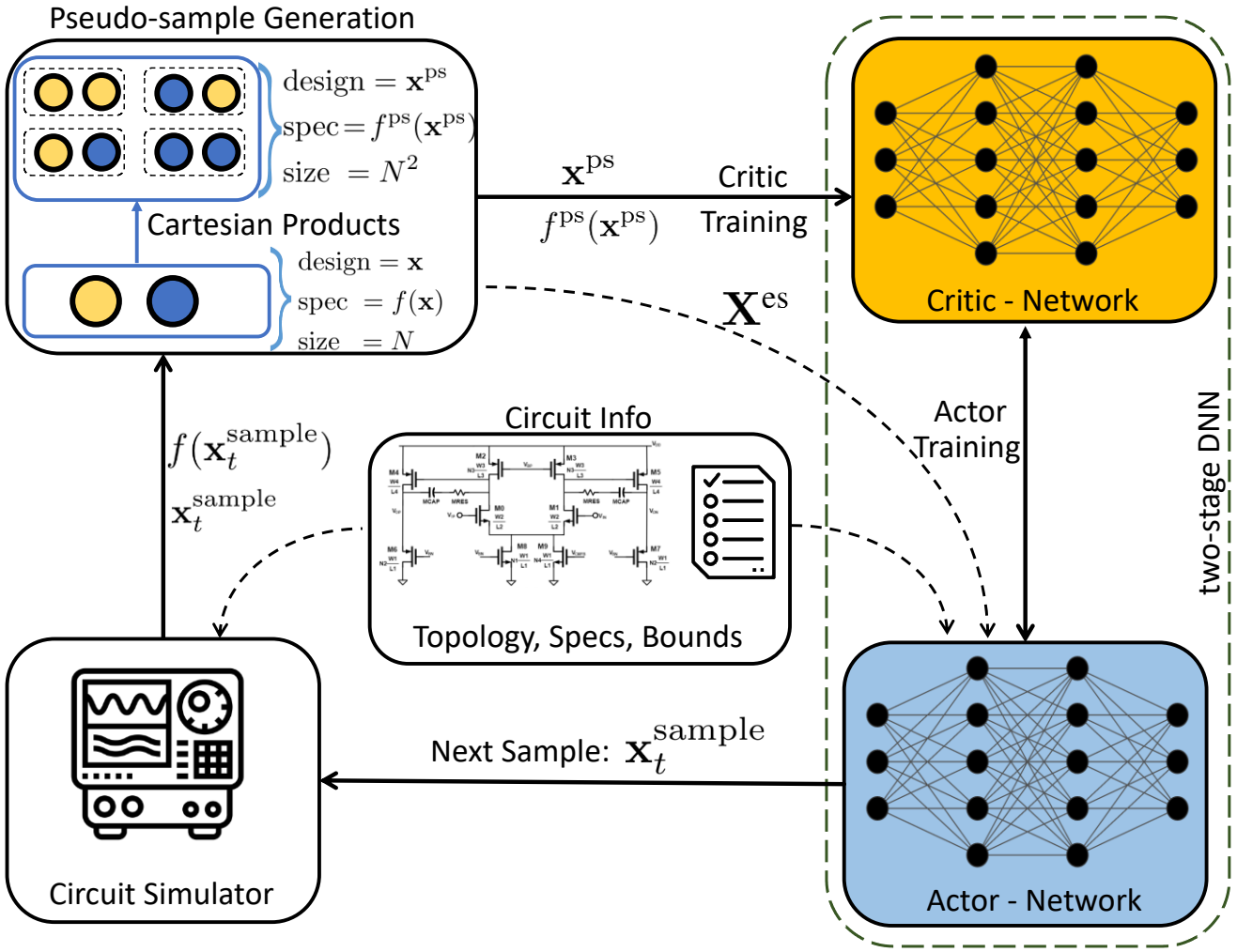


Miller OTA

What is the optimal sizing?

DNN-Opt: An RL Inspired Analog Optimizer

[Budak+, DAC'21]

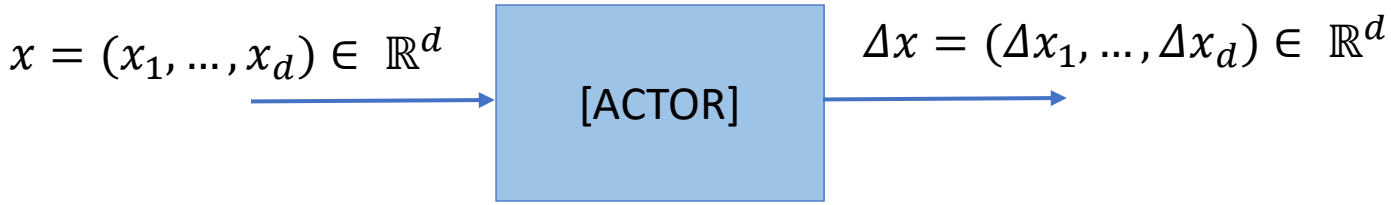


- Pseudo-sample Generator: Increases the sampling data based on original sample's cartesian products
- Critic: Neural Network proxy for real circuit simulator
- Actor: Neural Network based design space exploration engine
- Circuit simulator: Real performance evaluator. Generates data for training and validates results

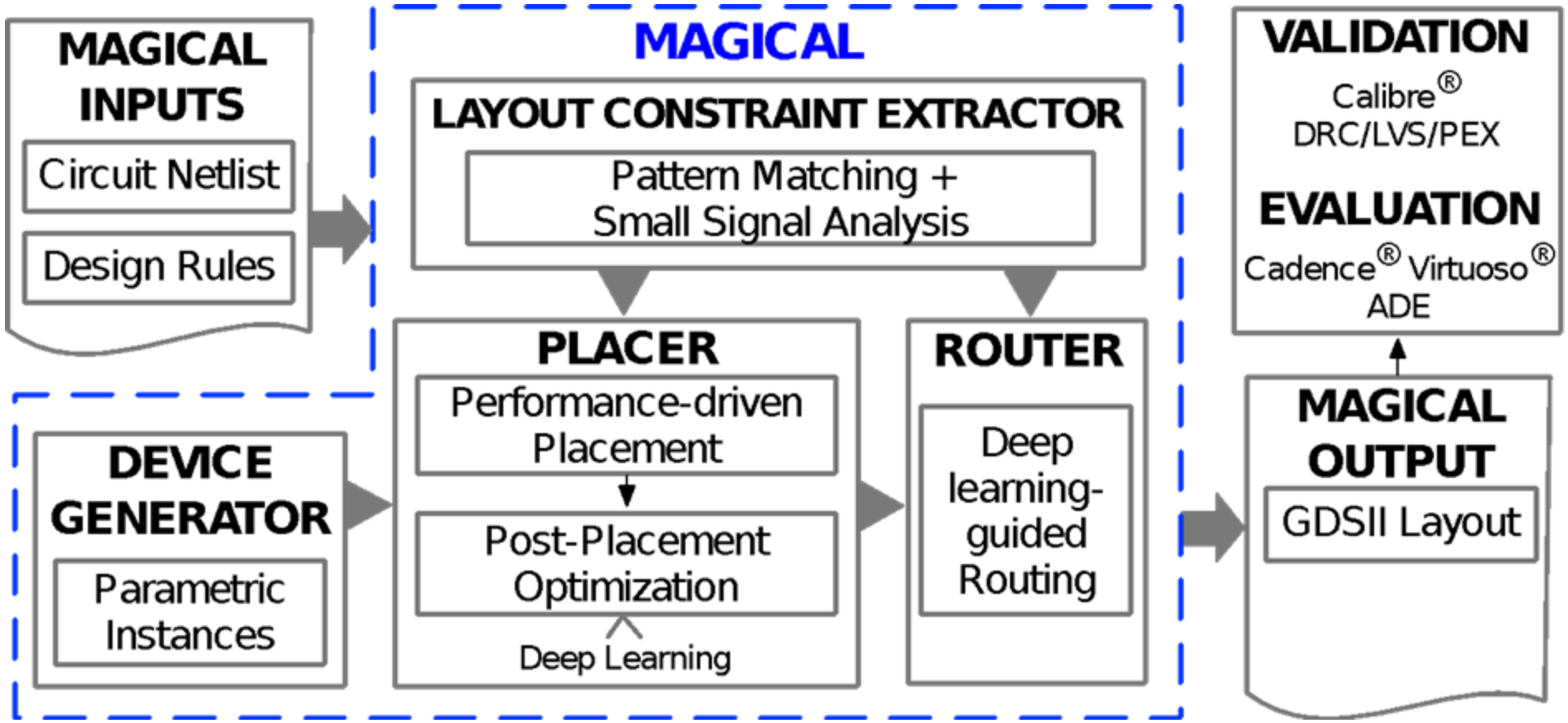
DNN-Opt: Networks

- Assume existence of a set of designs $\{x \in \mathbb{R}^d\}$ and their evaluations $\{f(x) \in \mathbb{R}^k\}$
- Train two networks: Actor & Critic Networks
  - One network to judge the performance of $(x, \Delta x)$ pairs.

  - One network to suggest an action given state x



MAGICAL: MAchine Generated IC Analog Layout

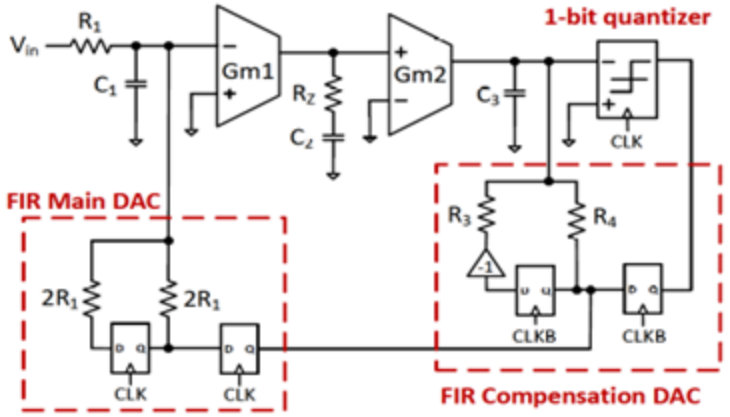


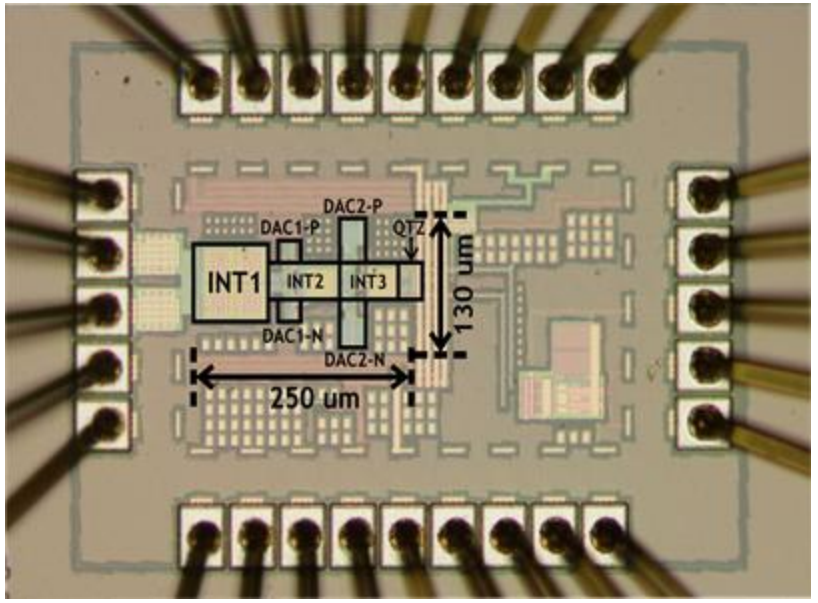
Open source MAGICAL (v1.0) release https://github.com/magical-eda/MAGICAL [Chen+, IEEE D&T'21]

MAGICAL Tapeout Proven

[Chen+, IEEE CICC'21

- 1GS/s 3rd-order high-performance continuous time ΔΣ modulator
- Include various sub-block types
  - Three integrators: one passive, two active
  - Two FIR-based feedback DACs
  - One comparator
  - + Digital logics
- TSMC 40nm
- SOTA performance cf. the original manual design [IEEE SSC-L'20]





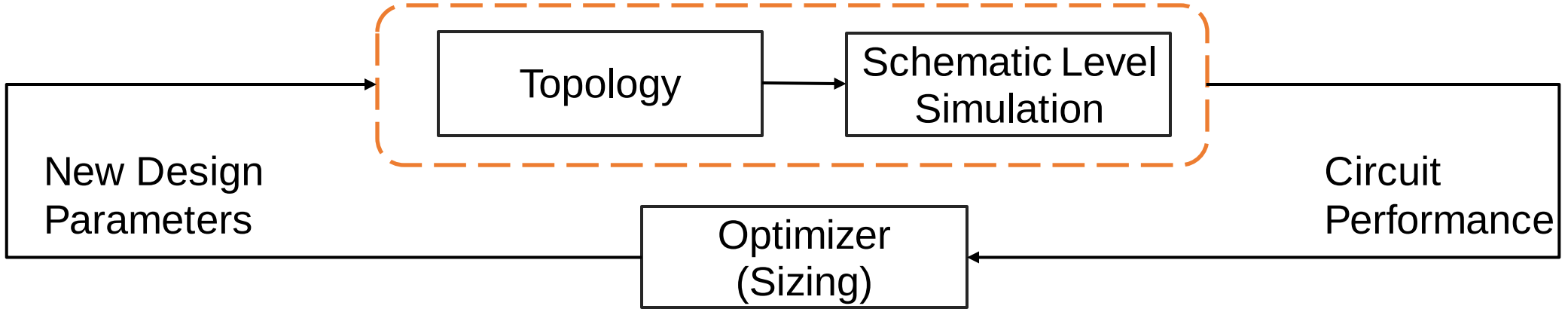
Joint Sizing & Layout: Motivations

Why layout and sizing should be considered together?

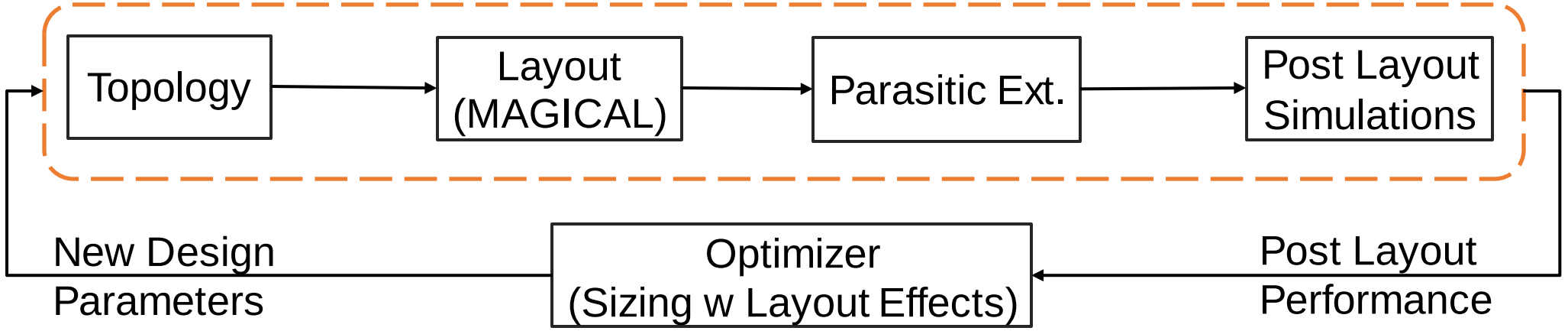
- Parasitics has large effect on the final performance
- Parasitics are only available after layout
- Performance after layout may largely deviate from schematic simulation results
- Considering layout effects during sizing is crucial

Joint Sizing & Layout: An Integrated Approach

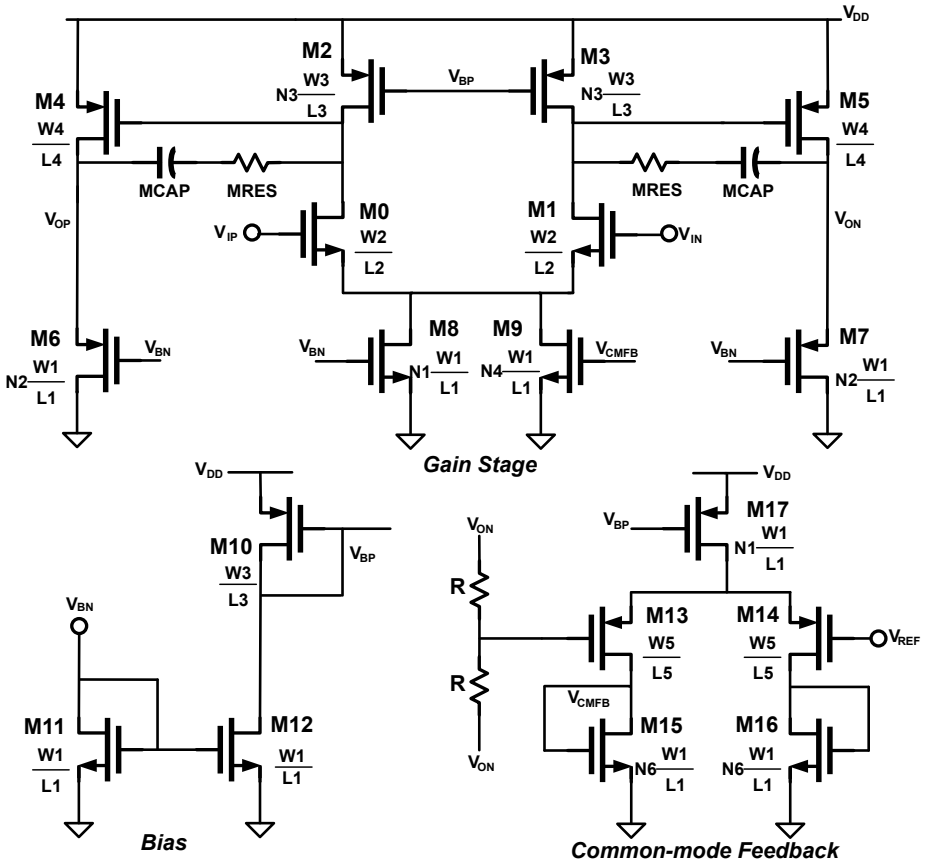
Conventional Schematic Sizing Framework



Layout in the Loop Sizing Framework



A Case Study: Miller OTA in TSMC 40nm



- Design: Two-Stage OTA in TSMC 40nm
- 17 design variables to be tuned
- Optimization Problem: 1 objective, 10 constraints

minimize Power

s.t. DC Gain > 45 dB — Settling Time < 100 ns

CMRR > 55 dB — Saturation Margins > 50 mV

PSRR > 55 dB — Unity Gain BW. > 40 MHz

Out. Swing > 1 V — RMS Noise < 400 uV_{rms}

Static error< %2 — Phase Margin > 60 deg.

A Case Study: Miller OTA in TSMC 40nm

Quantitative analysis of performance degradation due to layout effects

We first run a layout agnostic optimization, i.e., sizing based on pre-layout performance

Schematic Optimized	Intent	DNN-Opt	Designer
Power (mW)	minimize	**0.51**	0.53
Output Swing (V)	≥ 1	**0.99***	0.92
Gain (dB)	≥ 46	**48.1**	46.7
CMRR (dB)	≥ 55	**66.1**	56.2
PSRR (dB)	≥ 55	**63.7**	55.8
Phase Margin (deg)	≥ 57	**62.1**	57.2
RMS Noise (uV)	≤ 400	**380**	390
Rise Time (ns)	≤ 50	**21.3**	22.2
Static Error (%)	≤ 1.2	**1.08**	1.19
UGB (MHz)	≥ 85	**85.9**	85.0

Generate Layout via MAGICAL

Obtain post-layout performance

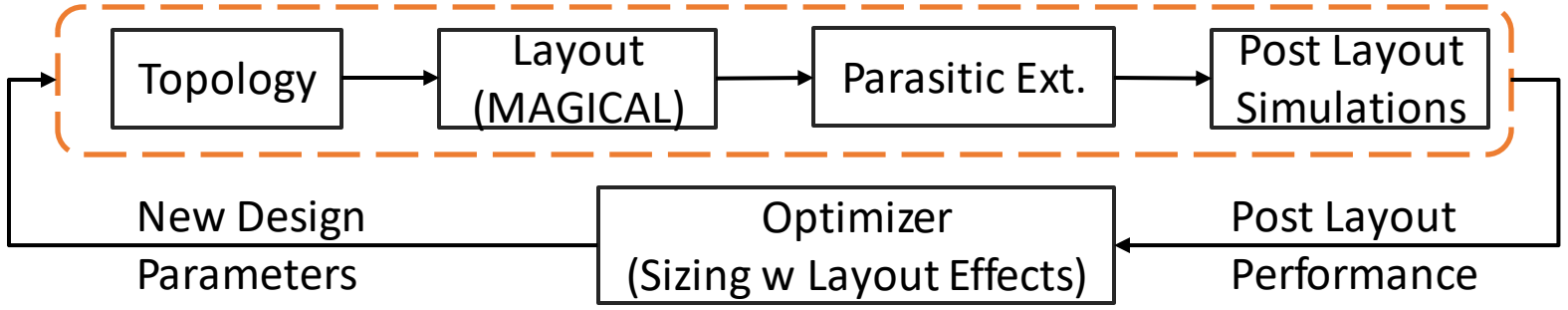
Then we create the layout of optimized design and measure post-layout performance

Schematic Opt + Layout	Intent	DNN-Opt	Designer
Power (mW)	minimize	0.53	0.53
Output Swing (V)	≥ 1	0.96*	**0.97***
Gain (dB)	≥ 45	17.9*	**47.8**
CMRR (dB)	≥ 55	25.6*	**53.7***
PSRR (dB)	≥ 55	25.7*	**55.6**
Phase Margin (deg)	≥ 60	**75.1**	69.9
RMS Noise (uV)	≤ 400	370	370
Rise Time (ns)	≤ 100	**23.0**	110*
Static Error	≤ 2	**1.07**	2.52*
UGB (MHz)	≥ 40	41.6	**42.0**

- Gain, CMRR, and PSRR are severely reduced for DNN-Opt generated design after layout effects
- Output swing, Gain, CMRR, PSRR do not satisfy the design intent after layout
- Designer's design shows better resilience against the layout effects

A Case Study: Miller OTA in TSMC 40nm

Use Proposed Optimization Flow to Include Layout Effects

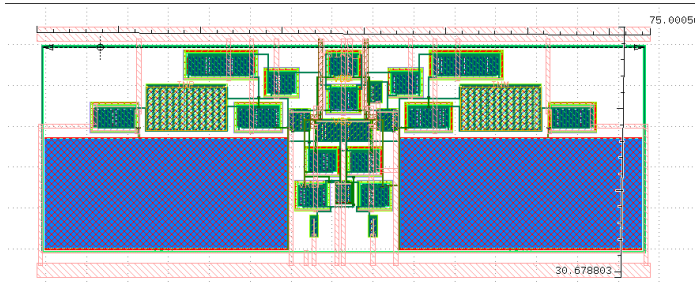


Post-Layout Optimized	Intent	DNN-Opt	Designer
Power (mW)	minimize	**0.39**	0.53
Output Swing (V)	≥ 1	**1.11**	0.97*
Gain (dB)	≥ 45	46.1	**47.8**
CMRR (dB)	≥ 55	**56.7**	53.7*
PSRR (dB)	≥ 55	**58.9**	55.6
Phase Margin (deg)	≥ 60	**70.7**	69.9
RMS Noise (uV)	≤ 400	370	370
Rise Time (ns)	≤ 100	**26.9**	110*
Static Error	≤ 2	**1.2**	2.52*
UGB (MHz)	≥ 40	31.3*	**42.0**

- Output swing, Gain, CMRR, PSRR are all restored and now satisfies design intent
- DNN-Opt solution only fails to meet one constraint (UGB) where designer's designs fails in four (output swing, CMRR, rise time, static error)
- Layout-in-the-loop sized solution overperforms the designer's solution in seven metrics and falls behind only in two metrics

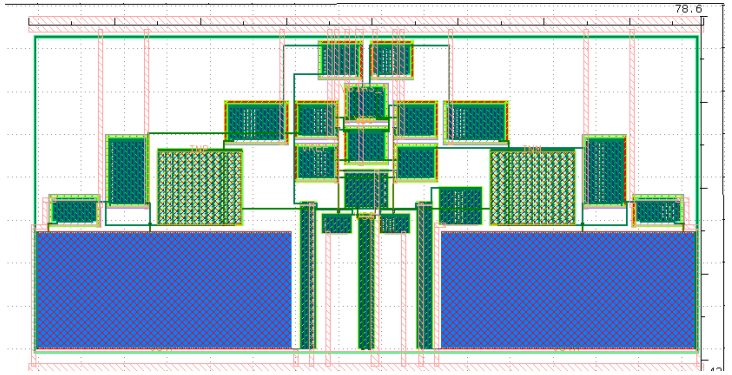
A Case Study: Miller OTA in TSMC 40nm

MAGICAL Layout from Designer Schematic



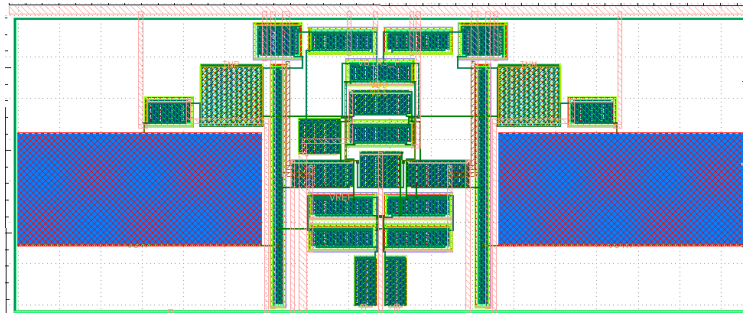
- More compact
- Designer experience seems helpful to later-stage layout
- The total area is around $75\mu m \times 30\mu m$

MAGICAL Layout from DNN-Opt Schematic



- 47% larger than MAGICAL layout from designer schematic
- Key devices with abnormal sizes cause deviation in transconductance and output resistance when layout is include
  ➔ significant degradation in metrics such as gain, CMRR and PSRR
- The abnormal-sized devices may also increase parasitic capacitance and resistance, further degrading the UGB

Layout aware DNN-Opt with MAGICAL



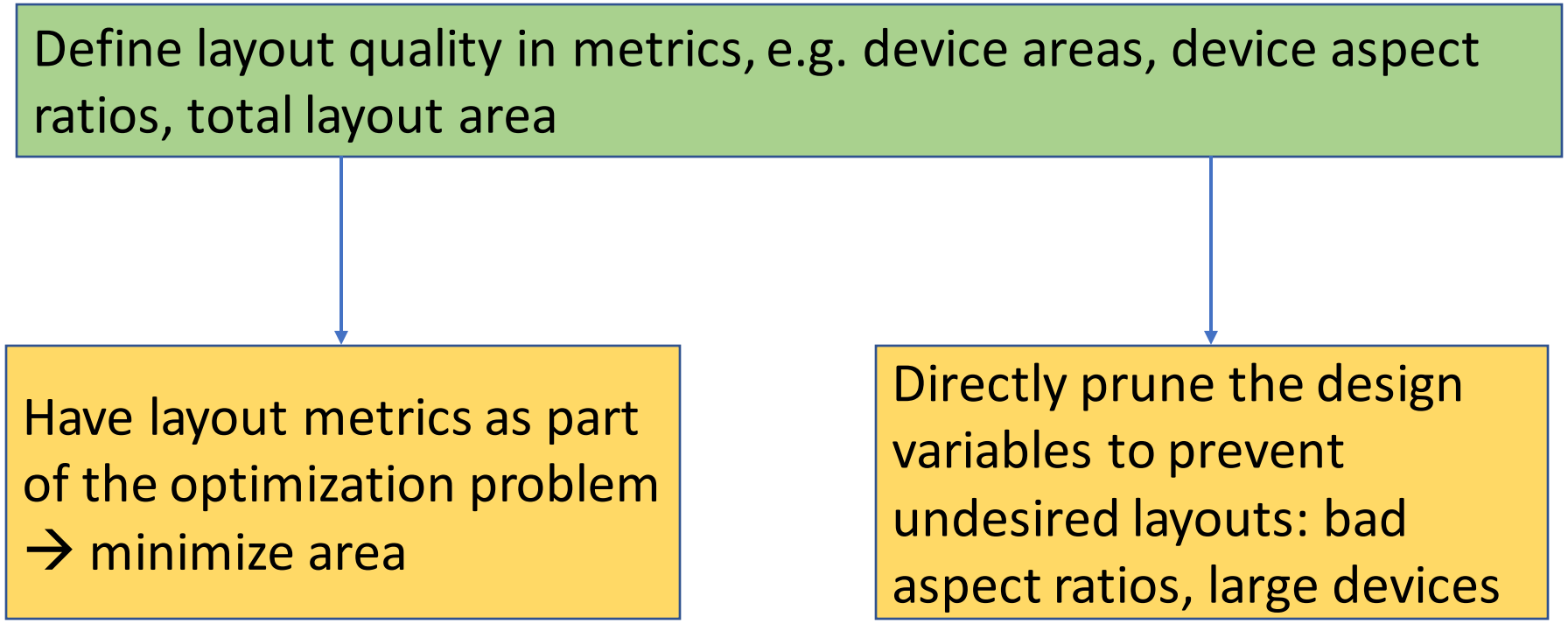
- Best performance
- However, 60% larger area than that from designer schematic
  - There still exist abnormal-sized devices

A Case Study: Take-Aways

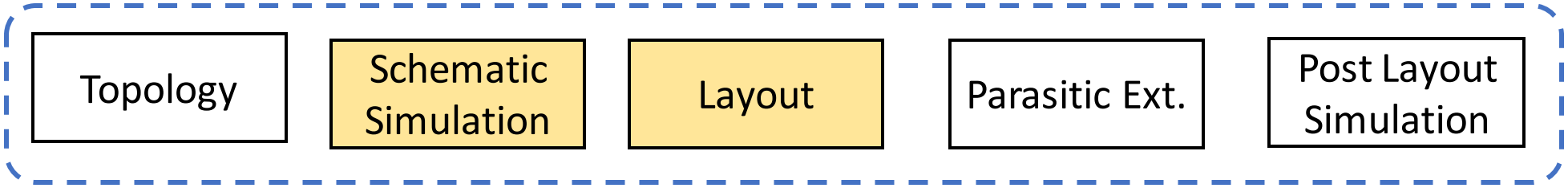
- Parasitics have large impacts on the analog IC performance
- Schematic-based sizing lacks in performance after layout effects are included
- If the optimizer is tuned to include layout effects, the post-layout performance can be improved significantly
- However, some large area penalty observed – more research to be done, e.g., to add area as a constraint or objective in the formulation

Opportunities and Future Directions

- Obtain Compact Layouts

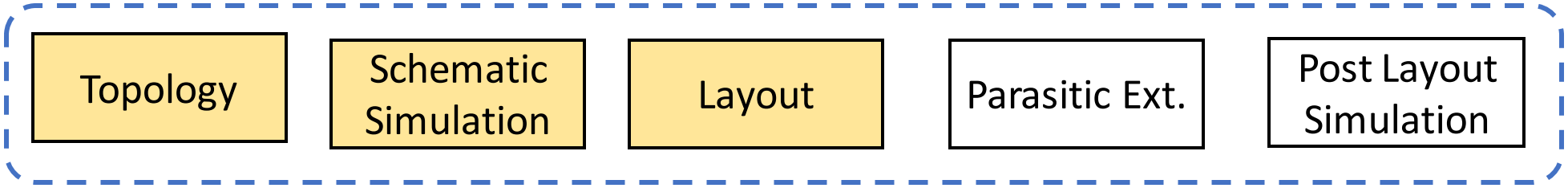


Opportunities and Future Directions



- Towards Efficient Layout-Aware Analog Sizing:
  - *Issue:* Repeating the whole flow in an optimization loop is costly
  - *Efficient:* Use multi-fidelity models to by-pass costly simulations:
    - Run layout, parasitic ext., and post layout sim only seldomly for verification and guidance
    - Parasitic prediction from placement: no routing, and PEX

Opportunities and Future Directions



- Towards Joint Analog Synthesis:
  - A longer-term goal
  - End-to-end analog “S&PR” (like RTL to GDSII for digital)
  - Analog circuit topology generation using ML

THANK YOU!