

International Symposium on Physical Design



March 26-29, 2023
Online with virtual participation



SYNOPSYS®

Gate-All-Around Technology is Coming What's Next After GAA?

Invited talk at ISPD'23

Victor Moroz and Alexei Svizhenko

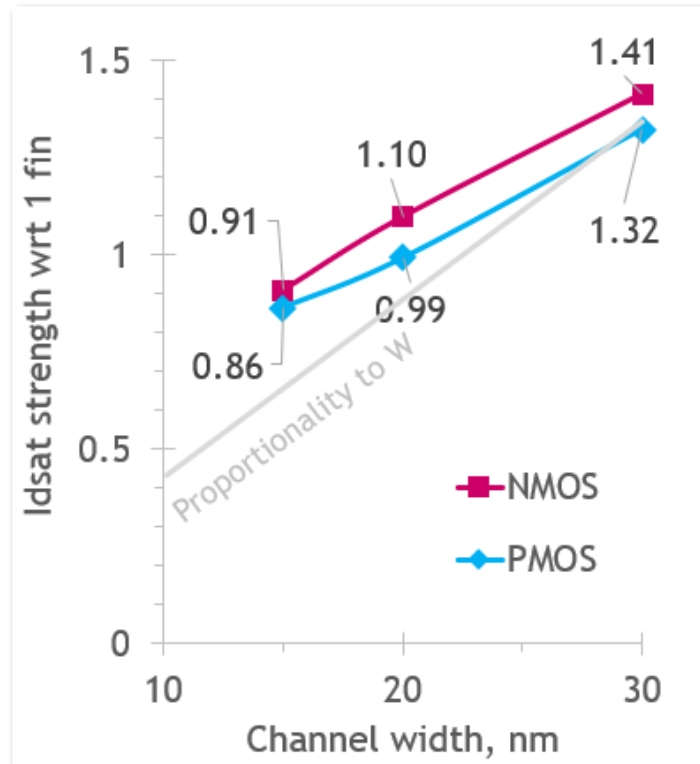
March 27, 2023

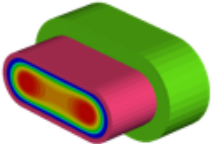
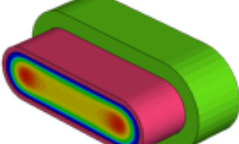
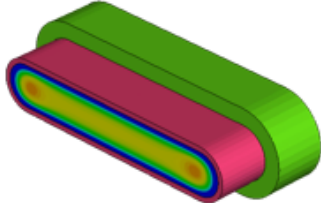
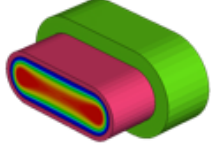
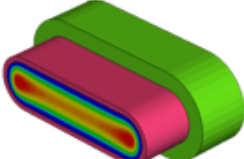
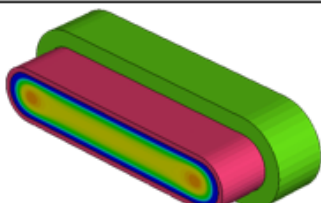
Outline

- 10Å GAA and CFET technologies
- DTCO tool flow: from virtual PDK to logic block PPA
- Benchmarking GAA and CFET PPA for low power logic
- The impact of M1 and M2 design rules and metal choices
- Summary

GAA Transistor Strength Engineering

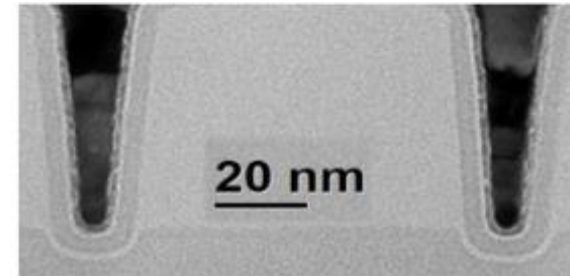
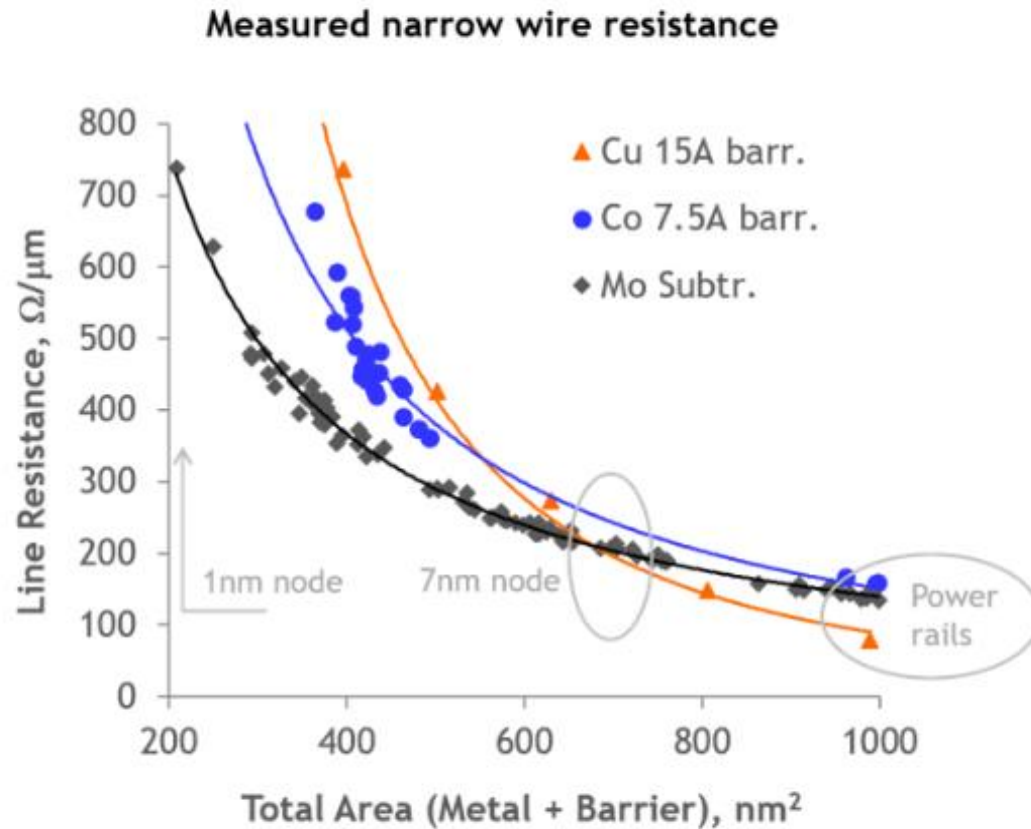
Driving strength of 3 stacked GAA channels vs 1 fin



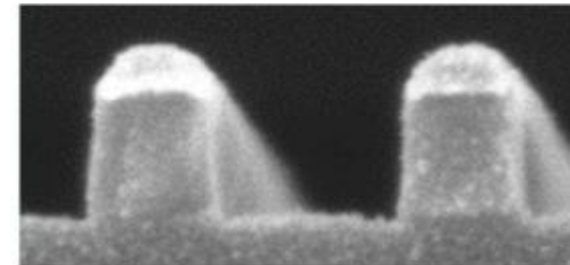
GAA	W = 15 nm	W = 20 nm	W = 30 nm
NMOS			
PMOS			

- Driving strength of 1 fin can be matched by:
 - 3 stacked GAA channels that are 18nm wide, or
 - 4 stacked GAA channels that are 12nm wide
- Narrow GAA channels perform disproportionately well due to the beneficial quantum confinement. For details, see Smith Lee et al., SISPAD 2015.

Interconnect Scaling: Narrow Wire Resistance

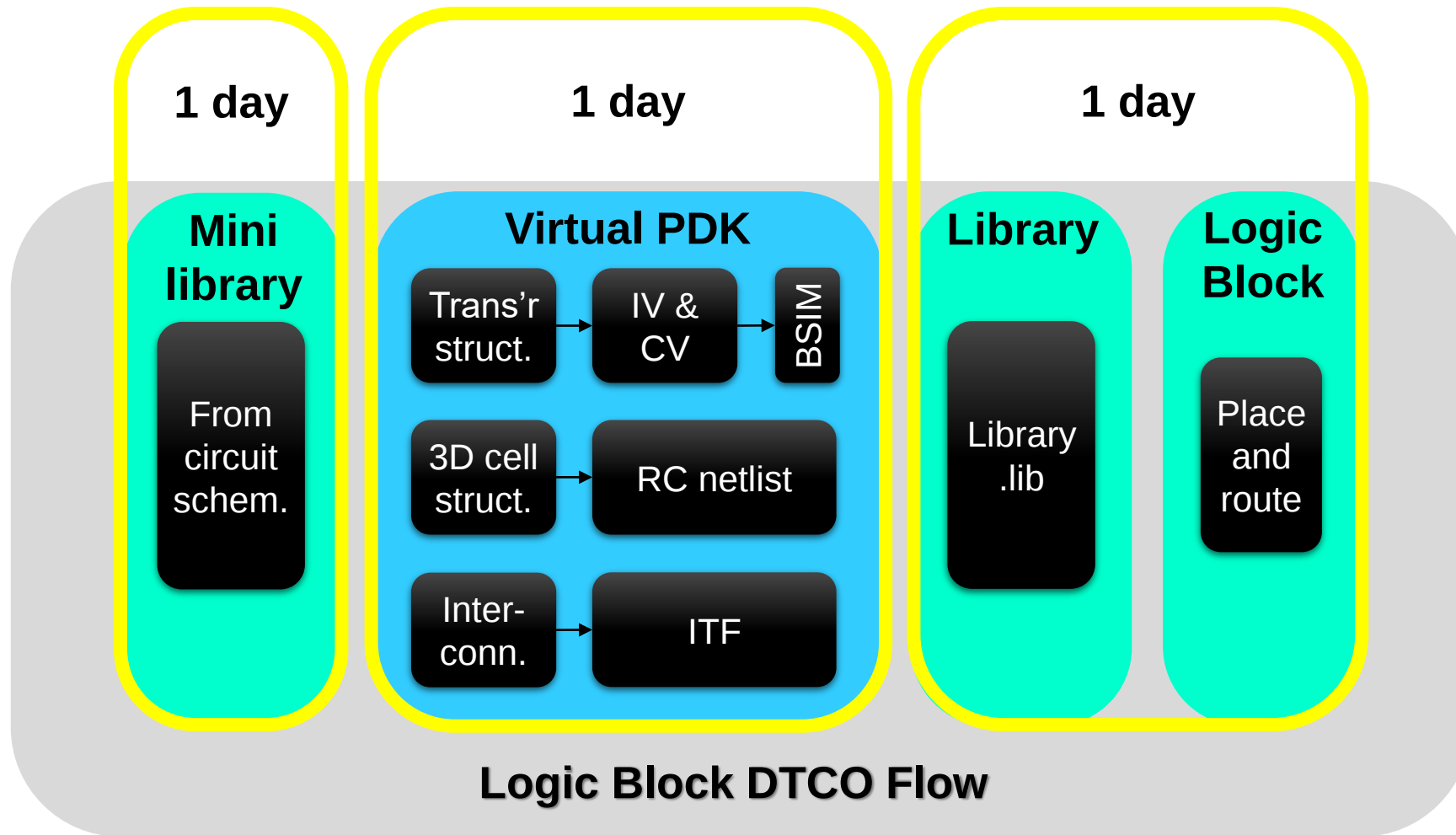


Ru buried power rail



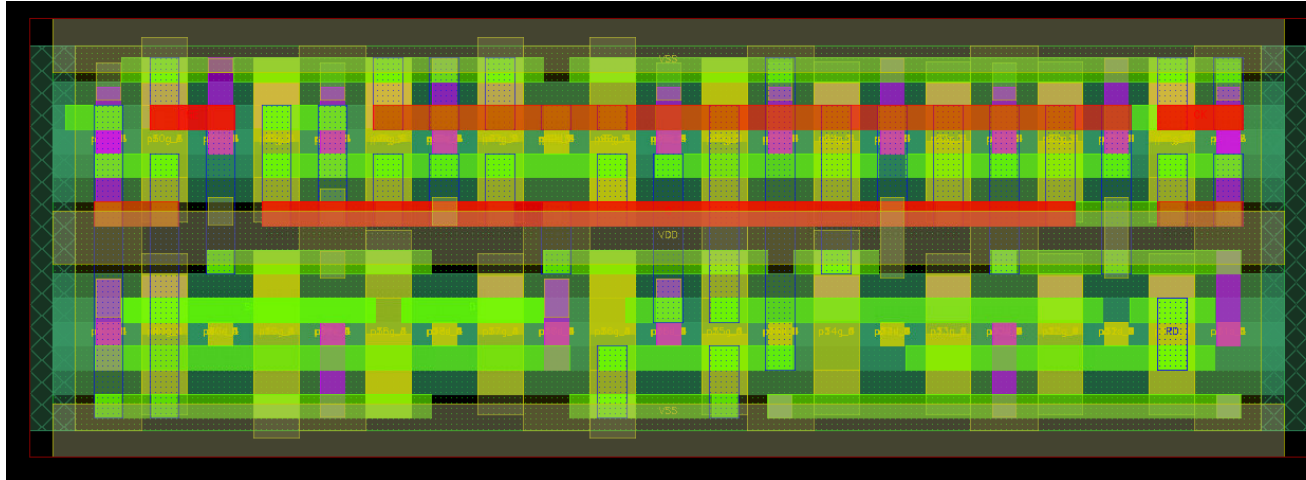
Mo subtractive patterning

Logic Block PPA Analysis Tool Flow with TAT of 3 Days

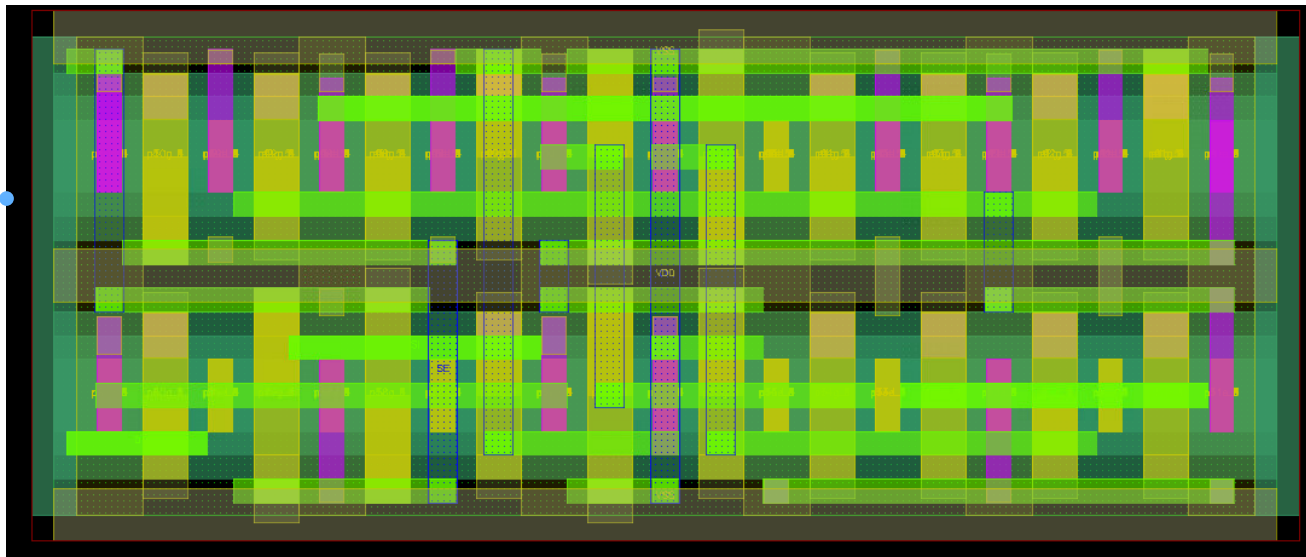


CFET Asynchronous flop FSDPRBQ_HTY2M2_4 double height

Layout



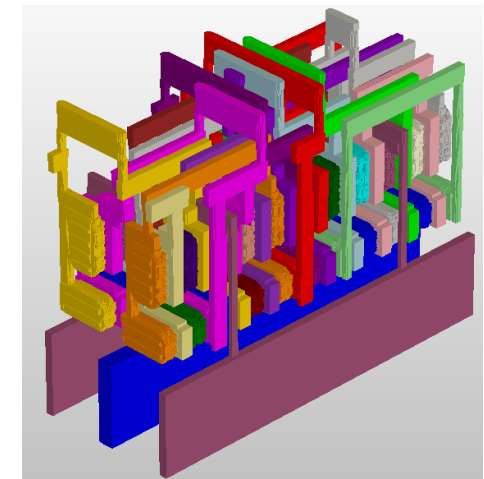
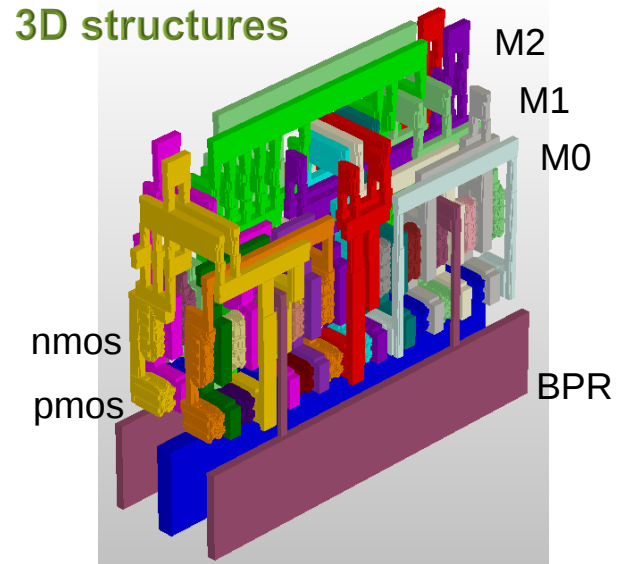
4 tracks
tall library



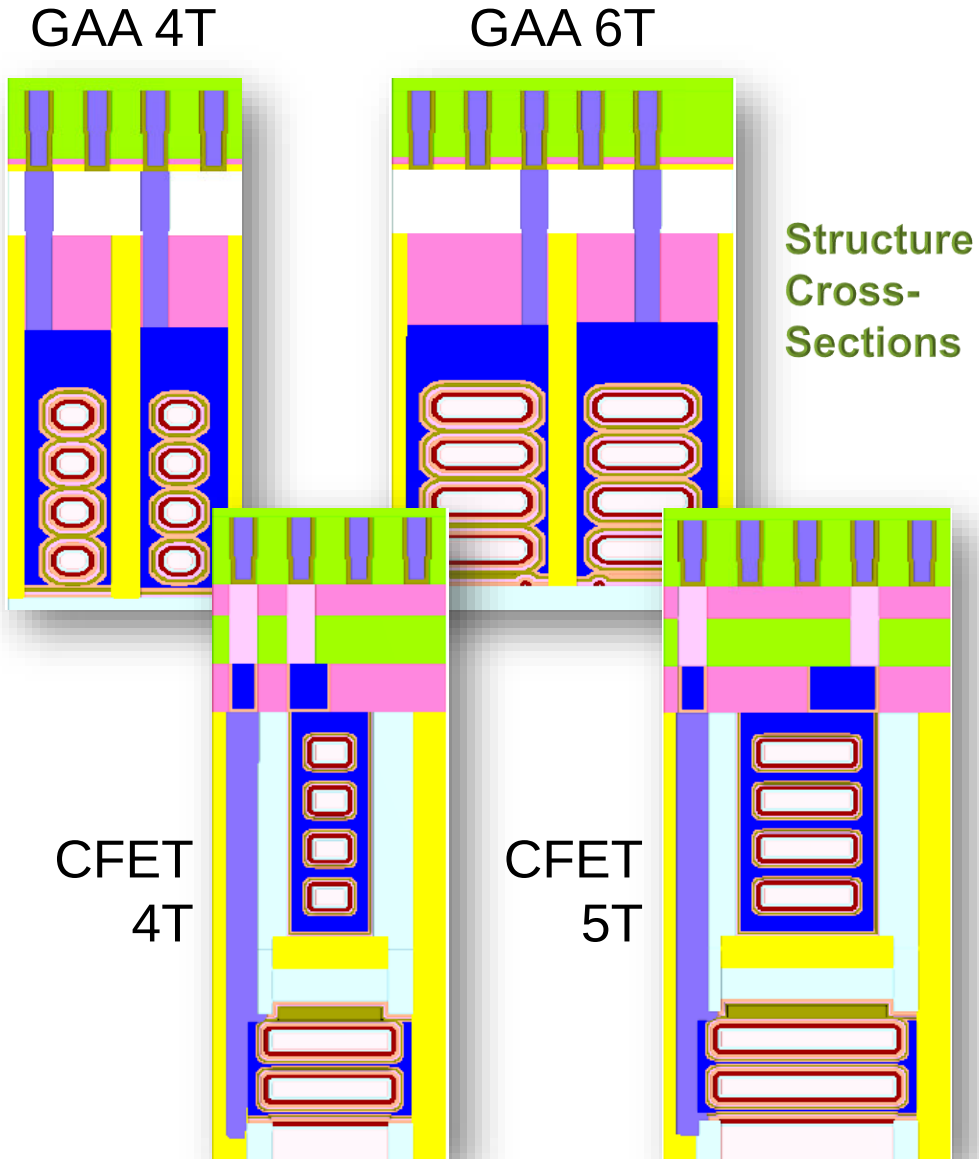
5 tracks
tall library

25%
larger
area

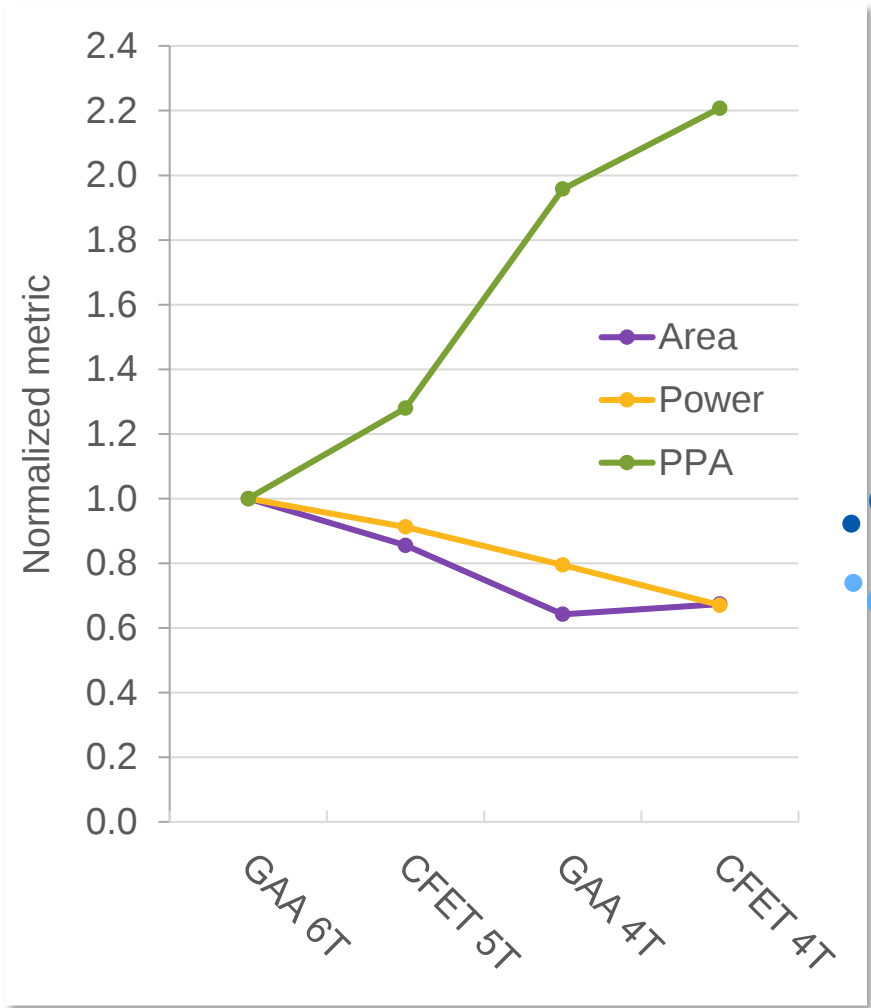
3D structures



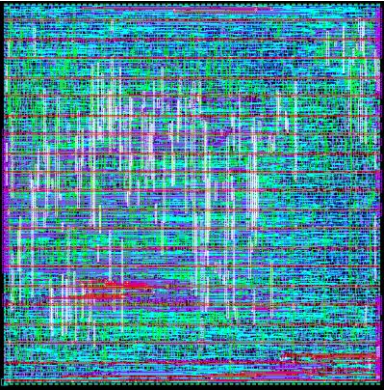
Benchmarking GAA vs CFET Using DTCO Flow



Mobile CPU PPA at iso-performance



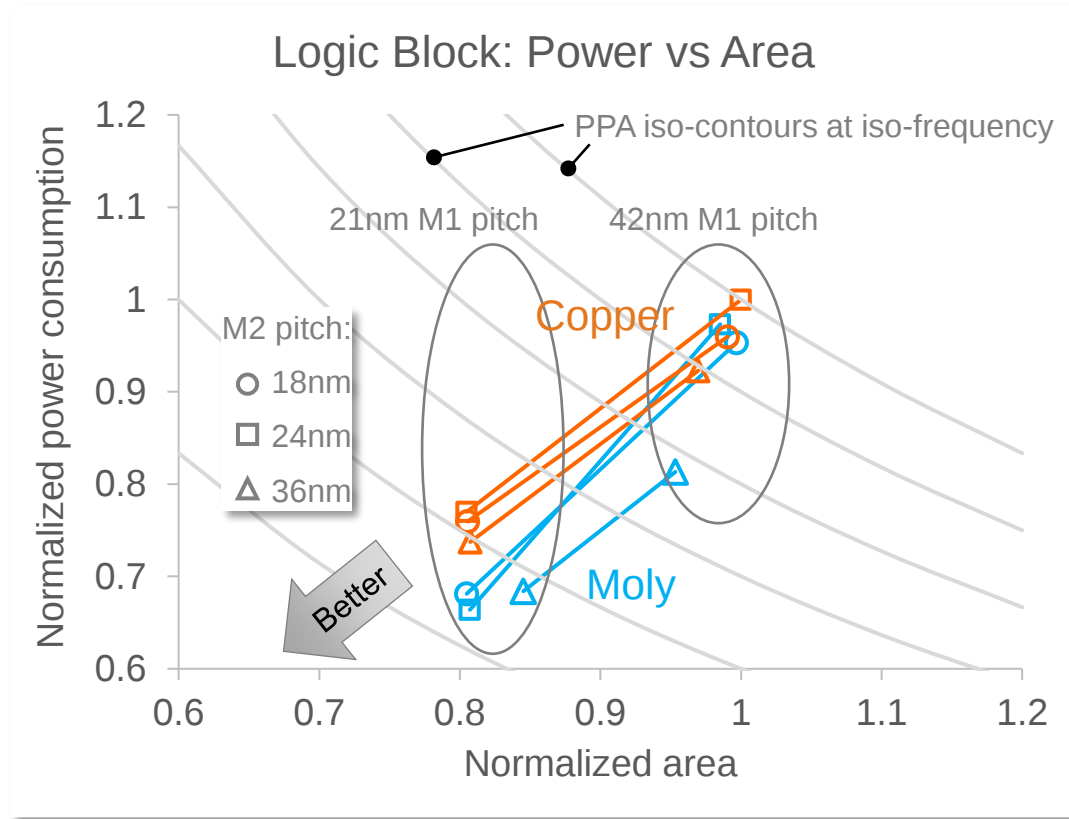
Logic block



Getting to 4 tracks is more important for logic than getting to CFET

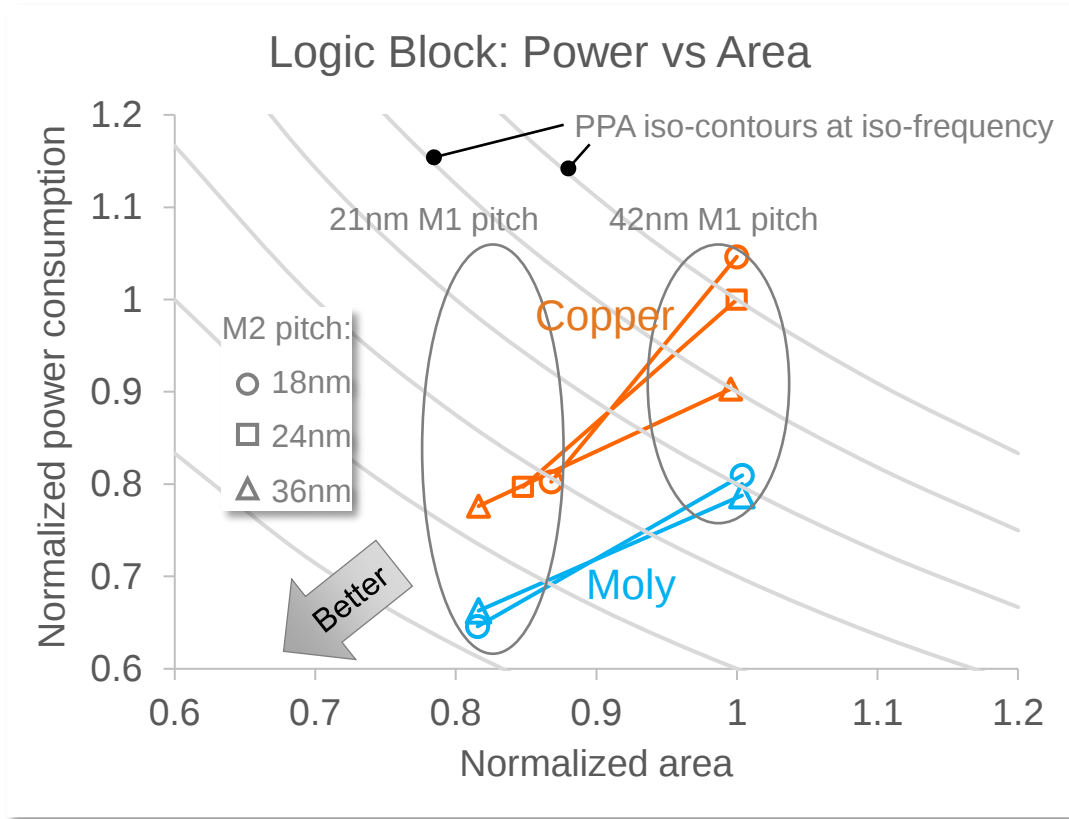
CFET is just a 25% PPA boost for logic, but it shrinks SRAM by 2x

Low Power CFET Logic PPA: Copper vs Moly M1 & M2



- Huge PPA range (~50%) for different M1 and M2 technology options!
- Huge (~40%) PPA gain for moving from 42nm M1 pitch (1 CPP) to 21nm (1/2 CPP) due to the better pin access
- Mild PPA gain for moving to larger M2 pitch due to the better wire R and C
- Some PPA gain (~10%) for moving from copper to molybdenum

High Performance CFET Logic PPA: Copper vs Moly M1 & M2



- Huge PPA range (~50%) for different M1 and M2 technology options!
- Huge (~30%) PPA gain for moving from 42nm M1 pitch (1 CPP) to 21nm (1/2 CPP) due to the better pin access
- M2 pitch only matters when M1 pitch is large
- Bigger PPA gain (~15%) for moving from copper to molybdenum

Summary

- CFET logic has a similar area to GAA, but 25% lower power
- However, CFET SRAM has 2x area scaling over GAA
- M1 & M2 pitches and metal choices for CFET technology have a huge ~50% impact of PPA
- The choices are different for HPC vs LP
- DTCO tool flow enables fast evaluation and tuning of different technologies and design rules