Reshaping System Design in 3D Integration: Perspectives and Challenges

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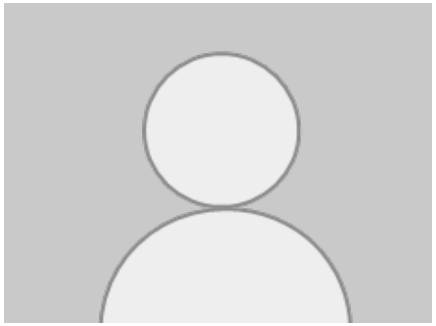

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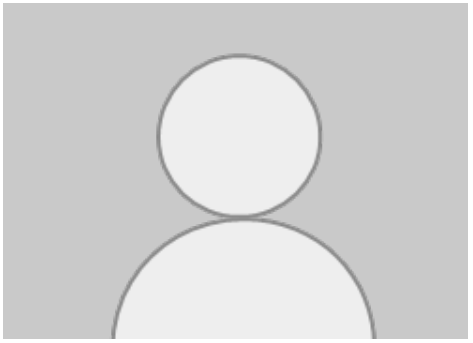
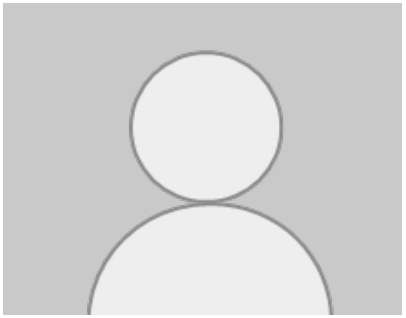
Outline

- Introduction to current system trend
- Three observations to paving the way to easier 3D system prototyping and implementation
- Conclusions and future perspectives



Introduction

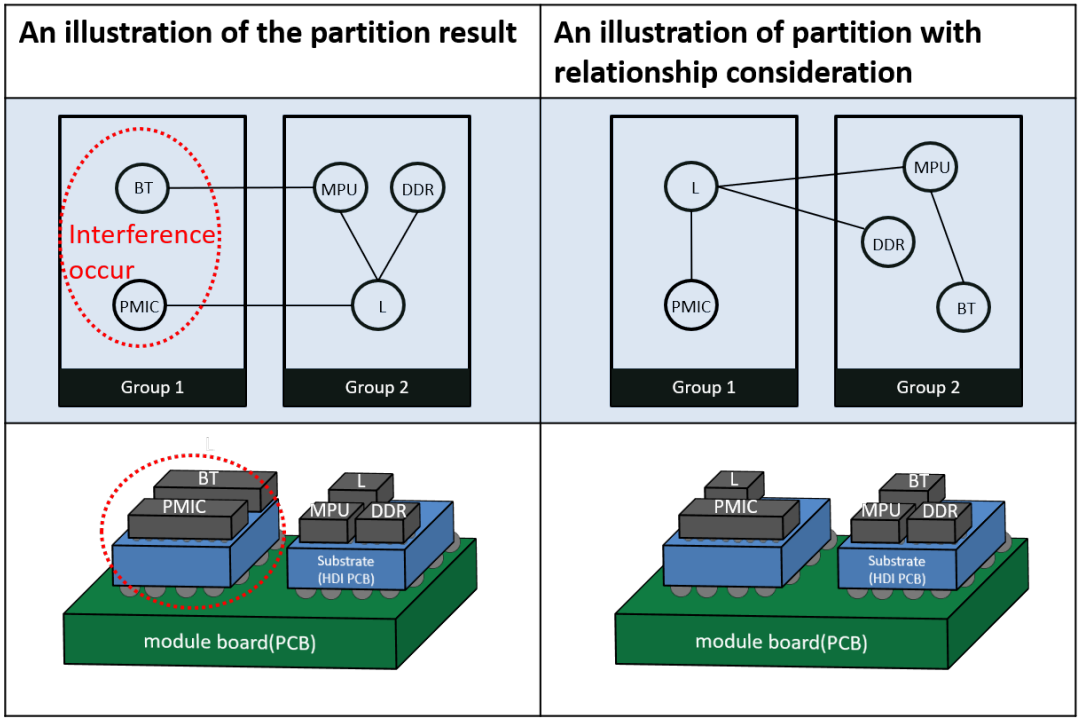
- Currently electronics system designs are facing fast turnaround cycles due to fast-changing cost structures
- How should we react to this trend?



- Fast system prototyping in lower-cost 3D integration
- More efficient and effective 3D interconnection in modern AI devices
- Embracing physical issues in advanced packaging

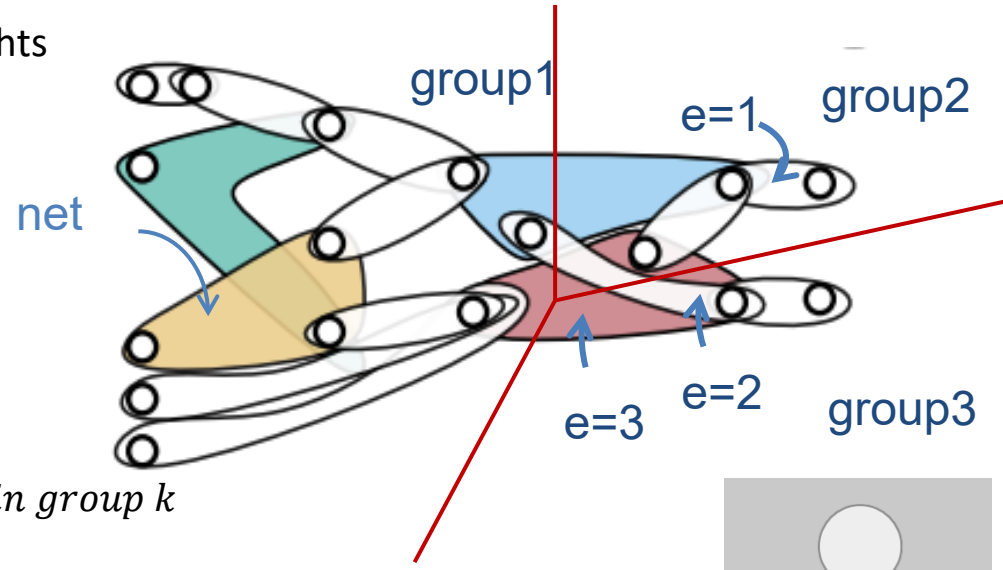
Motivation on Customized Prototyping

- IP becomes a critical issue when chipletizing the system: reuse or disaggregation/decomposition
  - Monolithic die can be decomposed into functional blocks or reorganized with other dies
- In the high-speed or frequency system, devices packed in a package or placed closely may cause degraded performance or dysfunction. Cut-only partition is not enough.

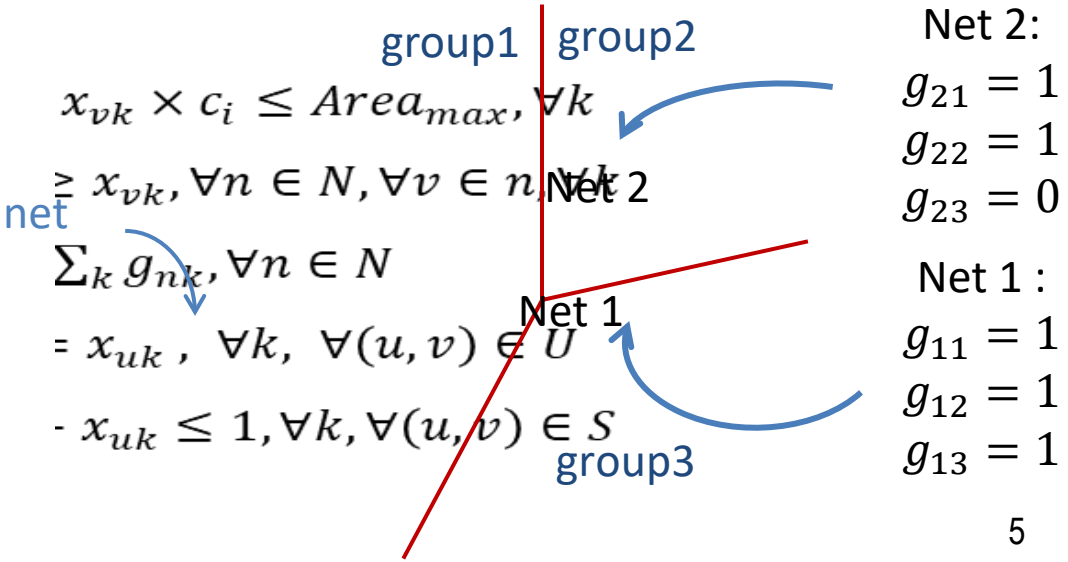


Design-aware Partition: A Sample

- Input: Hypergraph with node and net's weights
  - w_i : *weight of net i*
  - c_i : *area of node i*
  - k : *# of groups*
  - U : *union constraints set*
  - S : separation *constraints set*
- Output: Distribution of each node
- ILP Variable:
  - e_i : *# of groups net i connect*
  - x_{ik} *(node distribution)*: $\begin{cases} 1, if\ node\ i\ is\ in\ group\ k \\ 0, otherwise \end{cases}$
  - g_{ik} *(net connectivity)*: $\begin{cases} 1, if\ net\ i\ connects\ to\ group\ k \\ 0, \quad otherwise \end{cases}$



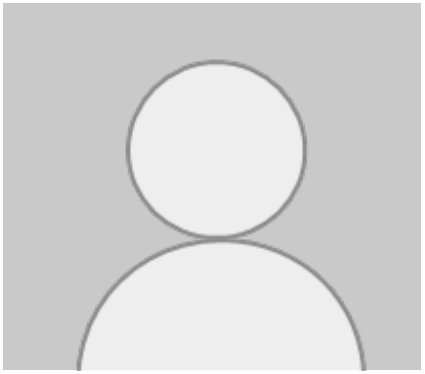
- **Objective**
  - $min\ \sum_i (e_i - 1) \times w_i$
- Constraints
  - $\sum_k x_{vk} = 1, \forall\ v \in V$
  - $\sum_{v \in V} x_{vk} \times c_i \leq Area_{max}, \forall k$
  - $g_{nk} \geq x_{vk}, \forall n \in N, \forall v \in n, \forall k$
  - $e_i = \sum_k g_{nk}, \forall n \in N$
  - $x_{vk} = x_{uk}\ ,\ \forall k,\ \forall (u,v) \in U$
  - $x_{vk} + x_{uk} \leq 1, \forall k, \forall (u,v) \in S$

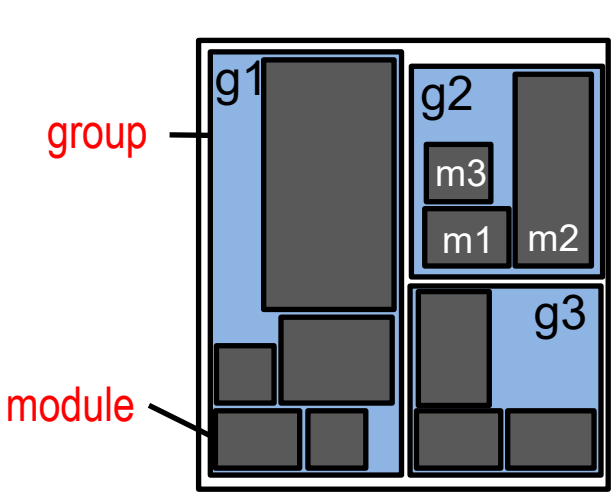


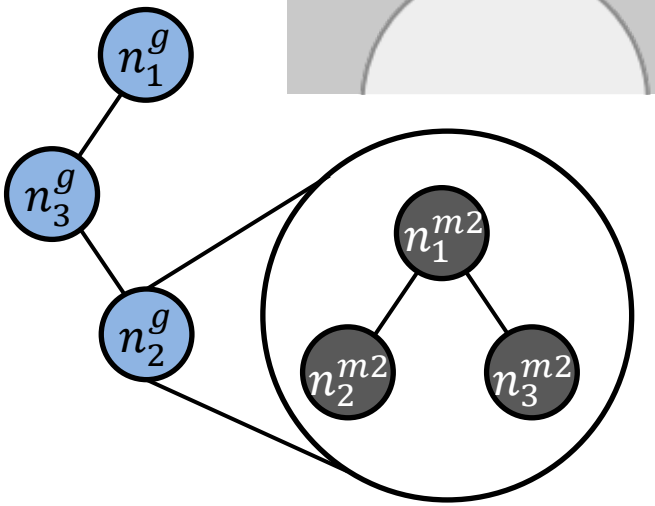
Prototyping 3D System: Floorplan

- HB* tree construction

- Our floorplan is based on HB* tree representation[9].
- For simplification of the problem, we remove passive devices from the design.
- Build HB* tree according the partition result.
- Two types of macro
  - Group
  - Module in the group



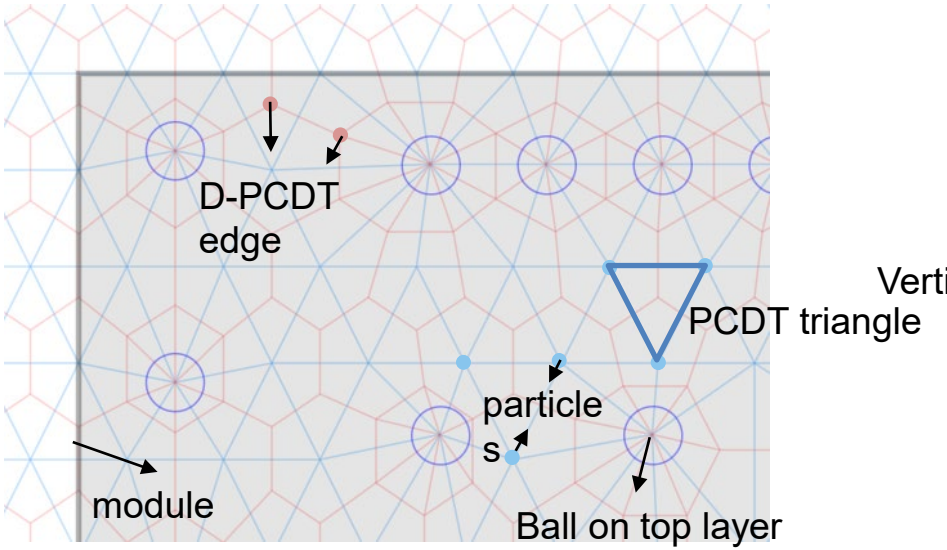


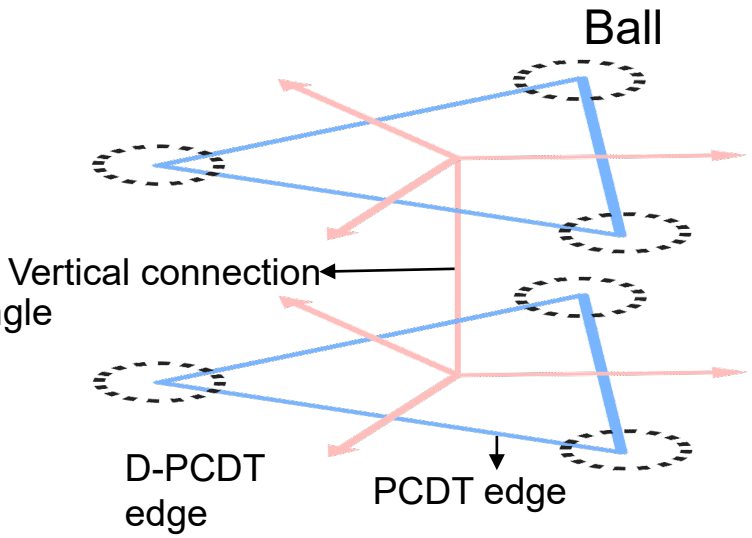


[9]Y.-K. Ho and Y. Chang, "Multiple chip planning for chip-interposer codesign," 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC), pp. 1–6, 2013.

Prototyping 3D System: Routing

- Routing graph construction
  - Apply constrained Delaunay triangulation (CDT) with adding uniformly spreading point to build a particle-insertion-based CDT (PCDT).
  - Our PCDT is generated by ball points and particles.
  - Then generate a dual graph of PCDT (D-PCDT) for routing grid.
  - In addition, we generate edges between different layers.





Our Experiments

- Setup

- The implementation was done in C++. All experiments were performed on a 2.5 GHz 64-bit Linux machine with 162 GB memory. To evaluate our work, we applied our method to five cases. All of the cases contain several modules with balls placed in irregular positions, passive devices, netlist, and design constraints.

Testcase	# ICs	# passive devices	# nets	# design constraints
Case1	6	220	198	25
Case2	7	109	151	40
Case3	9	80	181	22
Case4	11	131	203	39
Case5	14	120	342	32

Table : Information of testcases

Our Experiments

- Design-aware partition

Testcase	hMetis[1]				Ours			
	K	UBF	IO reduction	Violation	K	UBF	IO reduction	Violation
case1	2	0.4	26.4%	3	2	0.4	27.3%	0
	3	0.4	15.2%	3	3	0.4	21.8%	0
Case2	2	0.4	29.1%	1	2	0.4	31.4%	0
	3	0.4	13.7%	2	3	0.4	28.3%	0
Case3	2	0.4	26.1%	1	2	0.4	28.7%	0
	3	0.4	13%	1	3	0.4	23.55%	0
Case4	2	0.4	16.9%	5	2	0.4	22.9%	0
	3	0.4	13.2%	4	3	0.4	15.3%	0
Case5	2	0.4	40.7%	4	2	0.4	41%	0
	3	0.4	37%	3	3	0.4	38%	0
			1.00				1.31	

Table : Comparison of partition results

Our Experiments

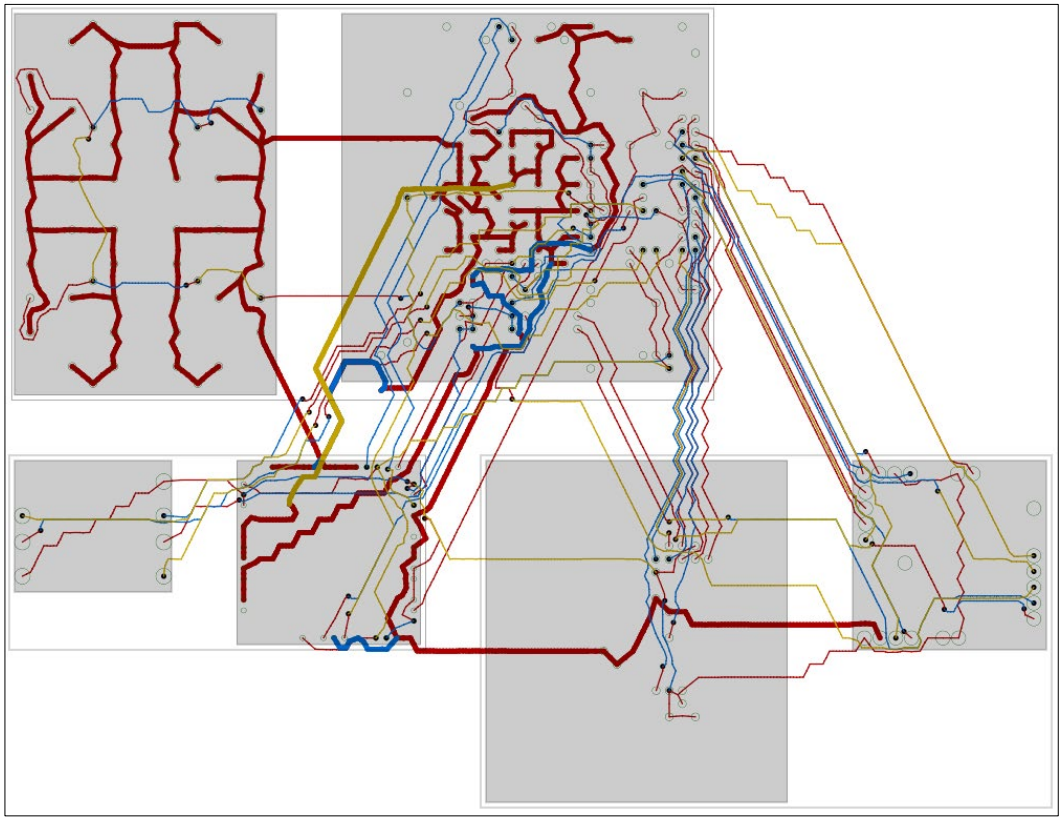
- System relayout

Testcases	K	UBF	# SIG	# PWR	[18]			Ours		
					Sig Wire length	Max IR-drop	# Vias	Sig Wire length	Max IR-drop	# Vias
Case1	3	0.4	31	12	701860	18%	144	665049	9%	143
Case2	3	0.4	27	10	571515	9%	48	574057	10%	44
Case3	3	0.4	31	11	1027168	9%	72	990718	9%	75
Case4	3	0.4	64	12	1654947	20%	148	1614387	10%	142
Case5	3	0.4	59	14	2168143	21%	166	2142549	10%	150
					1.00	1.00	1.00	0.97	0.71	0.96

Table : Comparison of routing results

[18] T. -C. Lin, D. Merrill, Y. -Y. Wu, C. Holtz and C. -K. Cheng, "A Unified Printed Circuit Board Routing Algorithm With Complicated Constraints and Differential Pairs," *2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2021, pp. 170-175.

Our Experiments



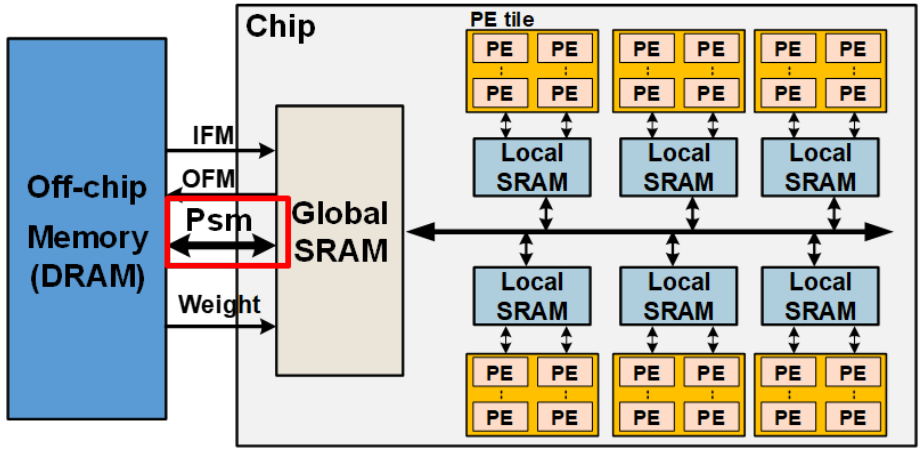
Challenges on 3D System Prototyping

- This is still one rough prototyping, we need a fair estimate of all resources for more accurate system cost evaluation
- Real-world implementation cost can be somehow integrated in such prototyping
- 3D implemented system needs a verification (physical) tool so that the prototypes/products can be evaluated for the feasibility

Near-Memory Computing using 3D-Memory

- The Von-Neumann bottleneck is caused by massive off-chip data movement, which results in high energy dissipation.
  - For the DNN accelerator, the partial sum (Psm) will be accessed with external memory massively and frequently.

➡ **Need larger on-chip buffer to increase on-chip data reuse and decrease data movement with DRAM.**

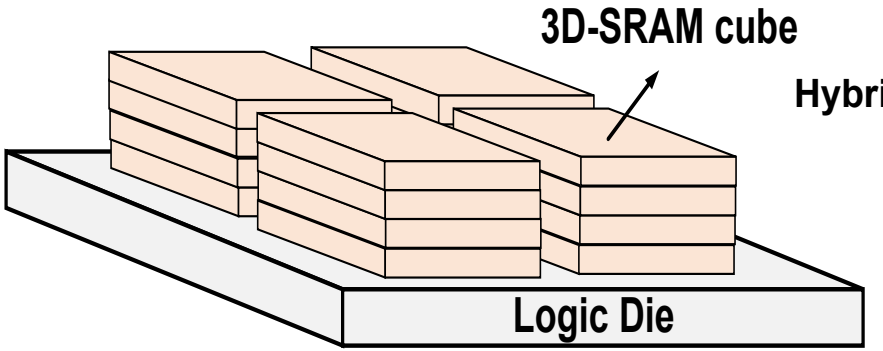


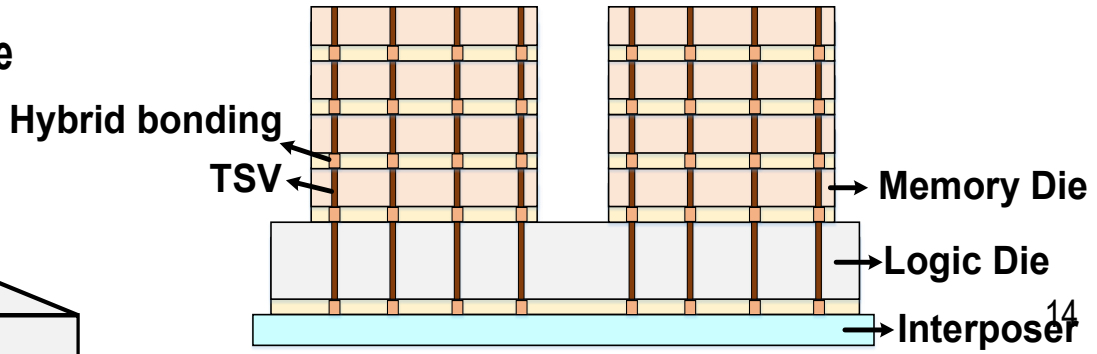
DNN accelerator

Challenges of TSV 3D integration

- We can stack the 3D-SRAM cubes on logic die by TSV technologies to increase the on-chip buffer size.
  - Decrease the data movement between on-chip and off-chip memory.
- The complexity and overhead of interconnection architecture will increase due to 3D integration, which result in higher energy cost of on-chip data movement.

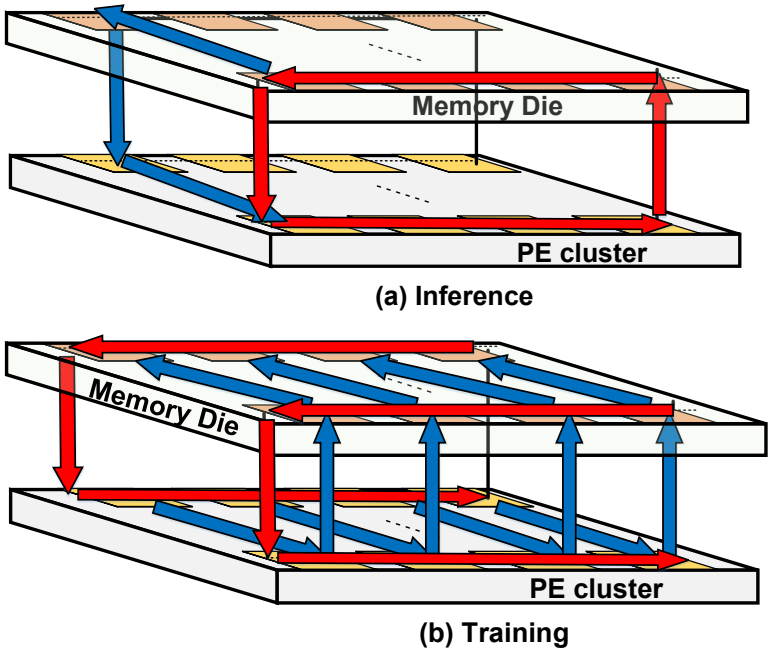
Require a flexible and uncomplicated 3D interconnection architecture to solve the overhead caused by 3D integration.

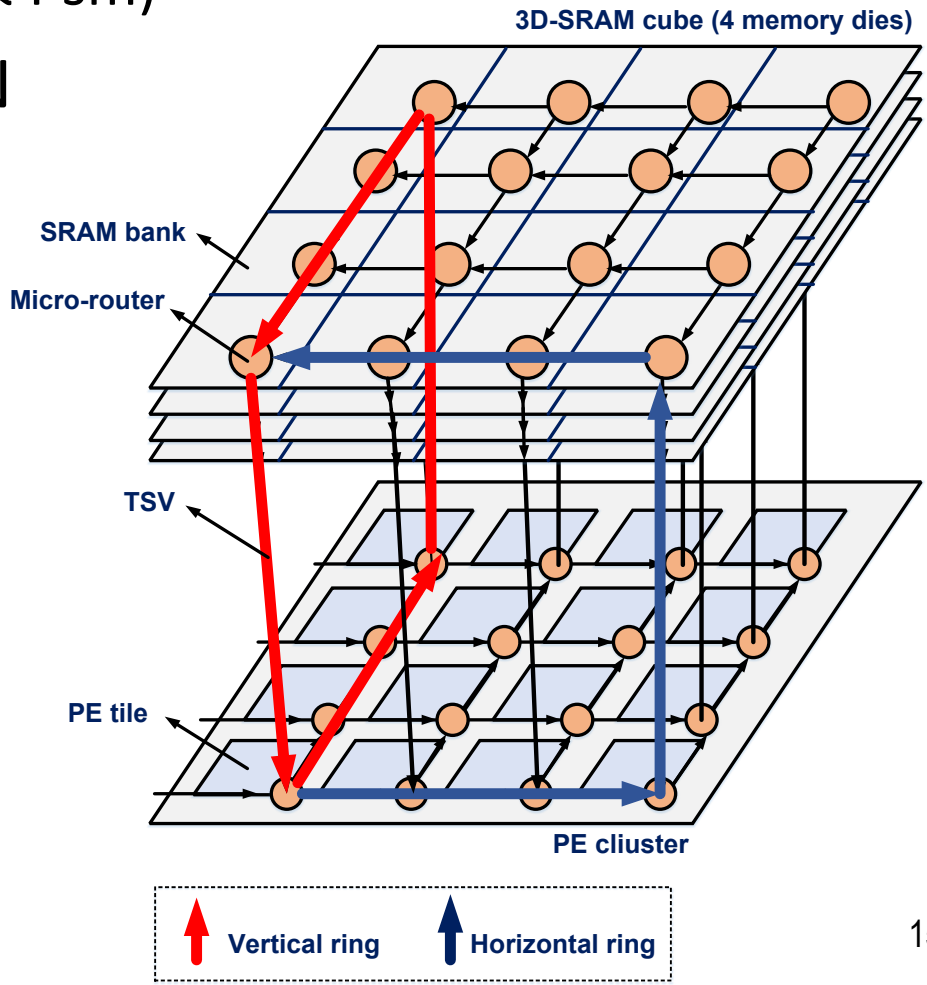




Flexible 3D Interconnection Architecture

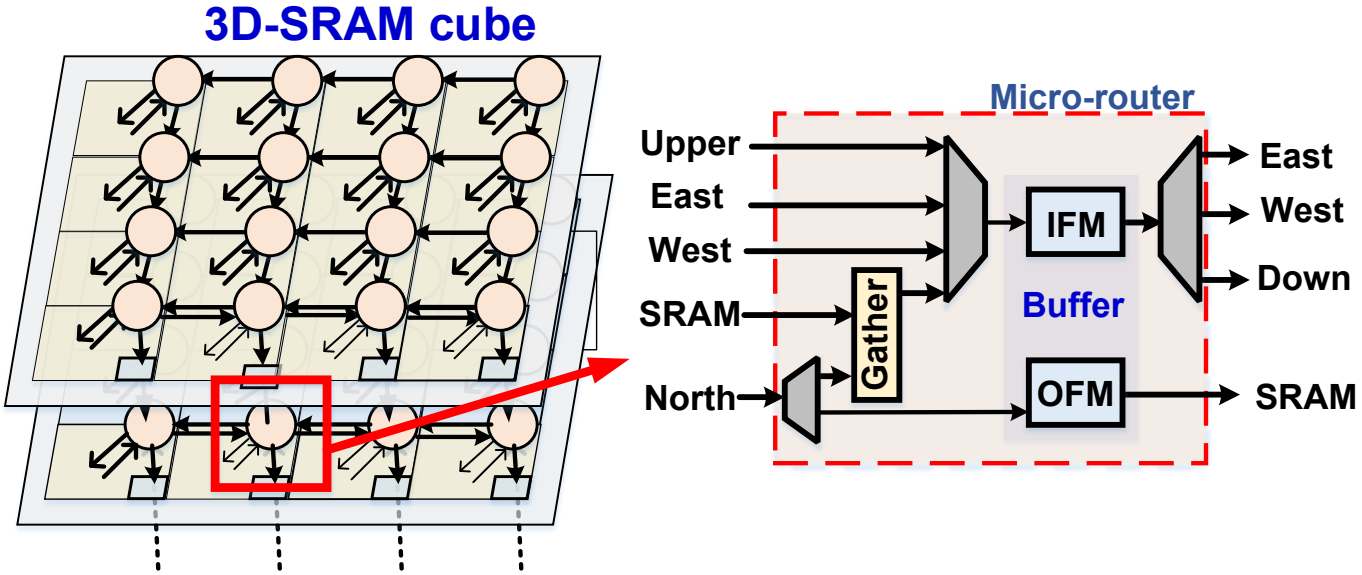
- 3D cross-ring interconnection architecture
  - Vertical rings (for IFM & Psm)
  - Horizontal rings (for weight & Psm)
- Efficient Dataflow for DNN
  - Inference
  - Training





Micro-Architecture of Micro-Routers

- The switch circuits and specified buffers are adopted for replacing the complicated crossbar and arbiter.
- The micro-routers transfer the input data to the certain output ports based on the data type.
  - The input the data will be sent to the specific buffers according to data type(IFM, weight, etc.), which can be determined by the bit region of input data and direction of input then be sent to certain output port.



Comparisons of 3D Interconnection Architectures

- The 3D mesh-based NoC can support complicated dataflow, and the 3D Ring-based NoC can achieve lower energy cost of data movement.
- The 3D cross-ring with efficient dataflow and micro-routers can achieve both the advantages of 3D-mesh and 3D ring-based NoC. Moreover, the 3D cross-ring can save the number of required TSV.

Interconnection architectures	Flexibility	Energy cost of data movement	Required TSV (Bandwidth between dies)
3D Mesh-based NoC	Support complicated dataflow	High, require complicated routers	Maximum
3D Ring-based NoC	Support only regular dataflow	Low, just need simplified routers	Medium
3D Cross-ring	Support various dataflow	Medium, cooperate with micro-routers	Minimal

Implementation Challenges in Advanced Packaging

- Fan-out wafer level packaging (FOWLP)
  - Higher density integration
  - Providing the area surrounding the chip for connecting more I/Os with redistribution layer (RDL)
  - Example: InFO (wafer level integrated fan-out) from TSMC
- Die-to-die (D2D) interfaces for successful SiP/2.5D/3D implementations still need continuous efforts

Via Types

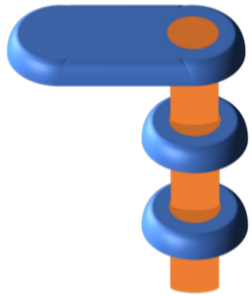
- Stagger vias (also called offset vias)
  - The vias in which any two adjacent layers will not overlap

(a) The offset vias that occupy the same region in each layer.

(b) The offset vias that will not route back to the same region in prior layers.

Figure 6: Offset vias (stagger vias) are the vias in which any two adjacent layers will not overlap.

- Stacking via
  - Have better signal/power integrity (SI/PI)
  - When the via stacking is higher than 4-tiers, it will suffer 45% higher line strain than the typical stagger



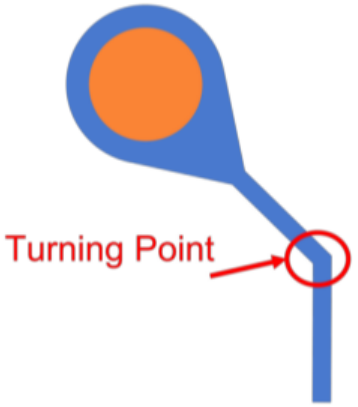
(a) Stack via. All the vias occupy the same space. Stack via may suffer from line strain problem.

- Stacking via is not always applicable, using offset via may solve this problem

Teardrop

- Teardrop has different angles and wirelength from via to the turning point

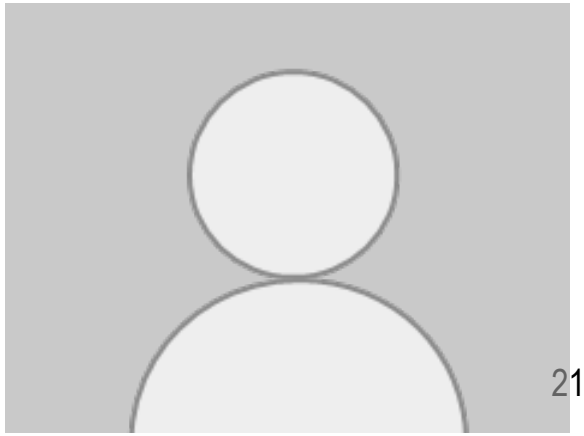
- In a prior work, they concluded that increasing wirelength from the via to the turning point will reduce the stress and the cracks to occur



(b) Teardrop structure. A metal is shrunk from via to the wire. The turning point may suffer from stress problem.

Vias and Teardrop Affect Routing

- Different arrangements of vias and teardrops
  - Cause different SI/PI and stress on such structure
- In D2D connection, the routing should be very dense
  - Vias and teardrops arrangements may cause the next RDL layer routing resource insufficient
- we should consider the SI/PI and the stress problem while performing RDL routing



SI/PI problem in Advanced Packaging

- SI/PI analysis
  - Applied after the layout phase
  - Enables high-precision analysis of actual system behavior
  - When the SI/PI analysis results are not good, the process may suffer from multiple rerouting and SI/PI reanalysis
- Co-simulation based D2D routing
  - Conventional approaches only worked on the routability of wires
  - SI/PI concerns usually are taken care of by simplified length matching

Conclusions and Future Perspectives

- Reshaping/Transforming system design in 3D for better/lower cost is a must, and we should have prototypes very efficiently to deal with the requirements from system house.
- How to deal with CIM 3D interconnection architecture, even future memory efficiency, is still an ongoing topic
- With heterogeneous chiplets combined in a package, chiplet PDK, ecosystems, and hybrid bonding constraints are emerging issues we need to take care of.