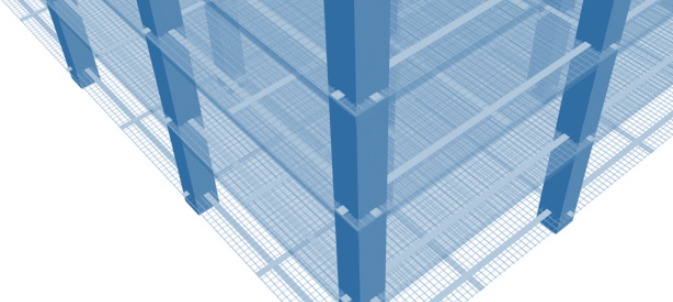
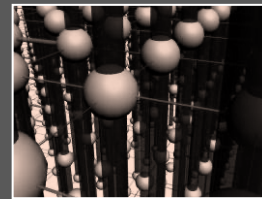
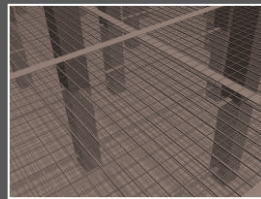
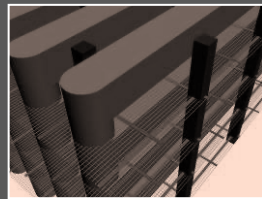
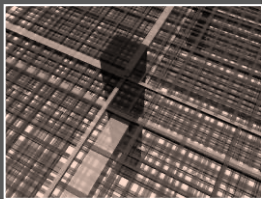




# On Legalization of Die Bonding Bumps and Pads for 3D ICs



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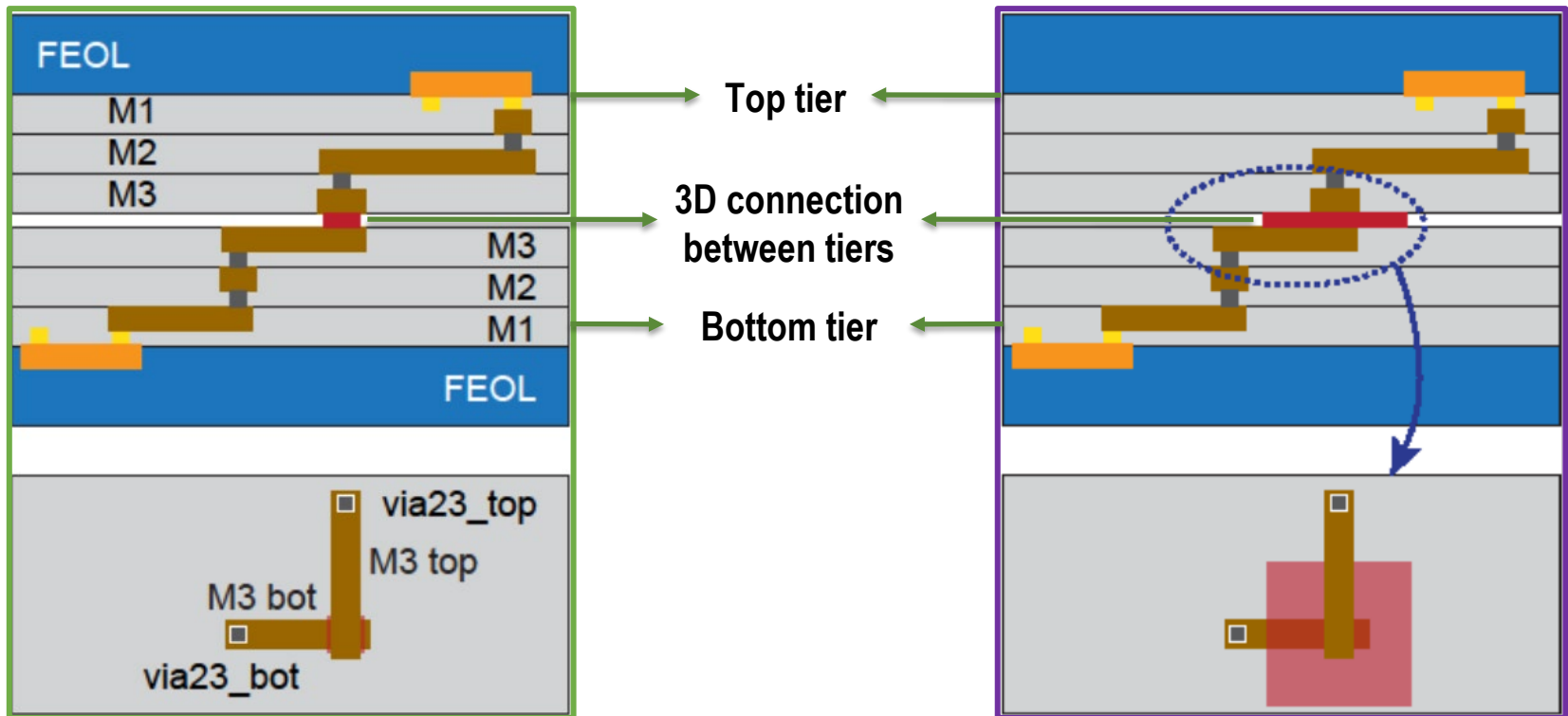
- **Problem Introduction**
- **Problem Analysis**
- **Proposed Solution(s)**
- **Types of Overlap Removal**
- **Results**

# Problem Introduction

## Routing in 3D ICs

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- The pitch of 3D via is hugely important in determining the type of 3D connection



A fine pitch 3D via with similar pitch as the other vias in the technology

A large 3D connecting via - Resembling a typical hybrid bonded via

- **Routing in 3D ICs is done similar to a 2D routing**
  - **Entire metal stack is considered at once**
  - **3D connection usually treated as a simple 2D via**
  - **Improves the routing efficiency when there are no DRCs due to 3D pitch**
- **Adopted in flows such as Macro-3D, Pin-3D for 3D IC designing**

- Routing is always done in 2 stages to reduce complexity and run-time
- Global Routing
  - Splits floorplan into grids
  - Virtually maps nets to grids considering congestion and routability
- Detail Routing
  - Physical routing within the routing grids
  - Adds vias for jumping between layers
- Problem for hybrid bonded 3D ICs
  - Large via size adds significant routing changes during detail routing

# 3D Via overlaps - 3D Flow/design type

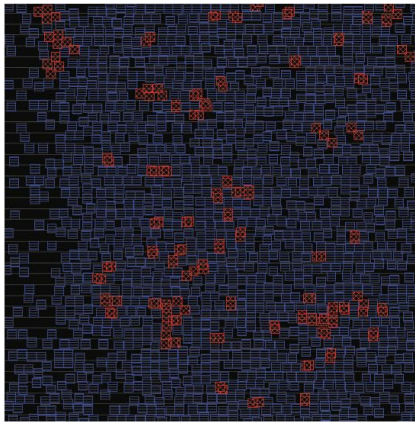
| Macro-3D Flow<br>Memory-on-Logic |            |             |
|----------------------------------|------------|-------------|
| 3D Pitch (um)                    | # Overlaps | % Occupancy |
| 1                                | 0          | 0.3         |
| 2                                | 2          | 1.1         |
| 5                                | 1410       | 7.2         |
| 10                               | 11080      | 28.2        |

| Pin-3D Flow<br>Logic-on-Logic |            |             |
|-------------------------------|------------|-------------|
| 3D Pitch (um)                 | # Overlaps | % Occupancy |
| 0.1                           | 0          | 0.3         |
| 0.2                           | 0          | 1.3         |
| 0.5                           | 0          | 8.9         |
| 1.0                           | 5315       | 32.2        |

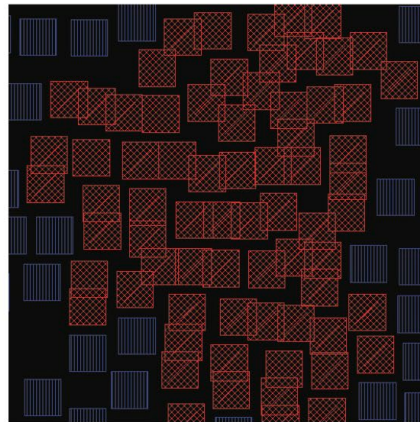
- As via size increases, overlaps occur with both 3D flows
- Note that these flows are not interchangeable
  - Macro-3D: Suited for memory-on-logic designs
  - Pin-3D: Suited for logic-on-logic designs

## 3D Via overlaps - Via pitch

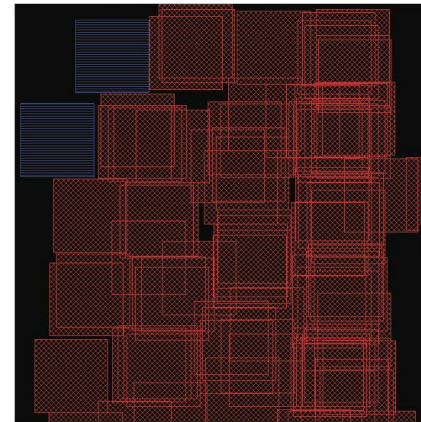
1um F2F bond pad pitch



5um F2F pitch



10um F2F pitch



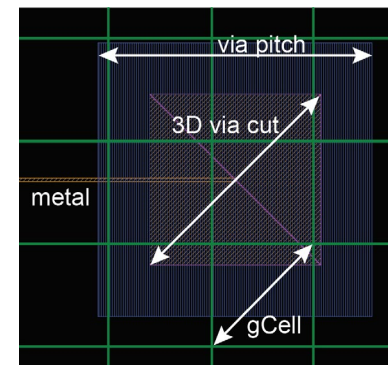
52um

### BEOL Dimensions

| Tech node       | 28nm |
|-----------------|------|
| M6 pitch        | 0.10 |
| Via pitch to M6 | 0.10 |

- Vias scaled to show spacing violations
  - In **red**: vias with spacing and/or short violations
  - In **blue**: Legal Vias
- Increased pitch size => worse via overlaps

Pictorial comparison of the BEOL dimensions and 3D via

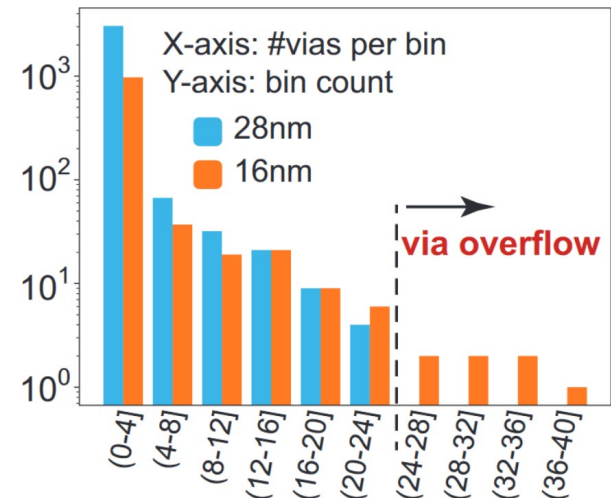


A 5um 3D pitch is larger than the gCell (global routing grid) used by the tool

# 3D Via overlaps - Technology node

- As technology node advances
  - BEOL dimensions shrink
  - 3D via pitch independent of 2D node scaling
  - Overlap issue worsens

| BEOL Dimensions and 3D Via |      |      |
|----------------------------|------|------|
| Tech Node                  | 28nm | 16nm |
| Mx pitch                   | 0.10 | 0.08 |
| Via pitch to Mx            | 0.10 | 0.08 |
| 3D Via pitch               | 5.00 | 5.00 |
| gCell width                | 1.48 | 1.08 |

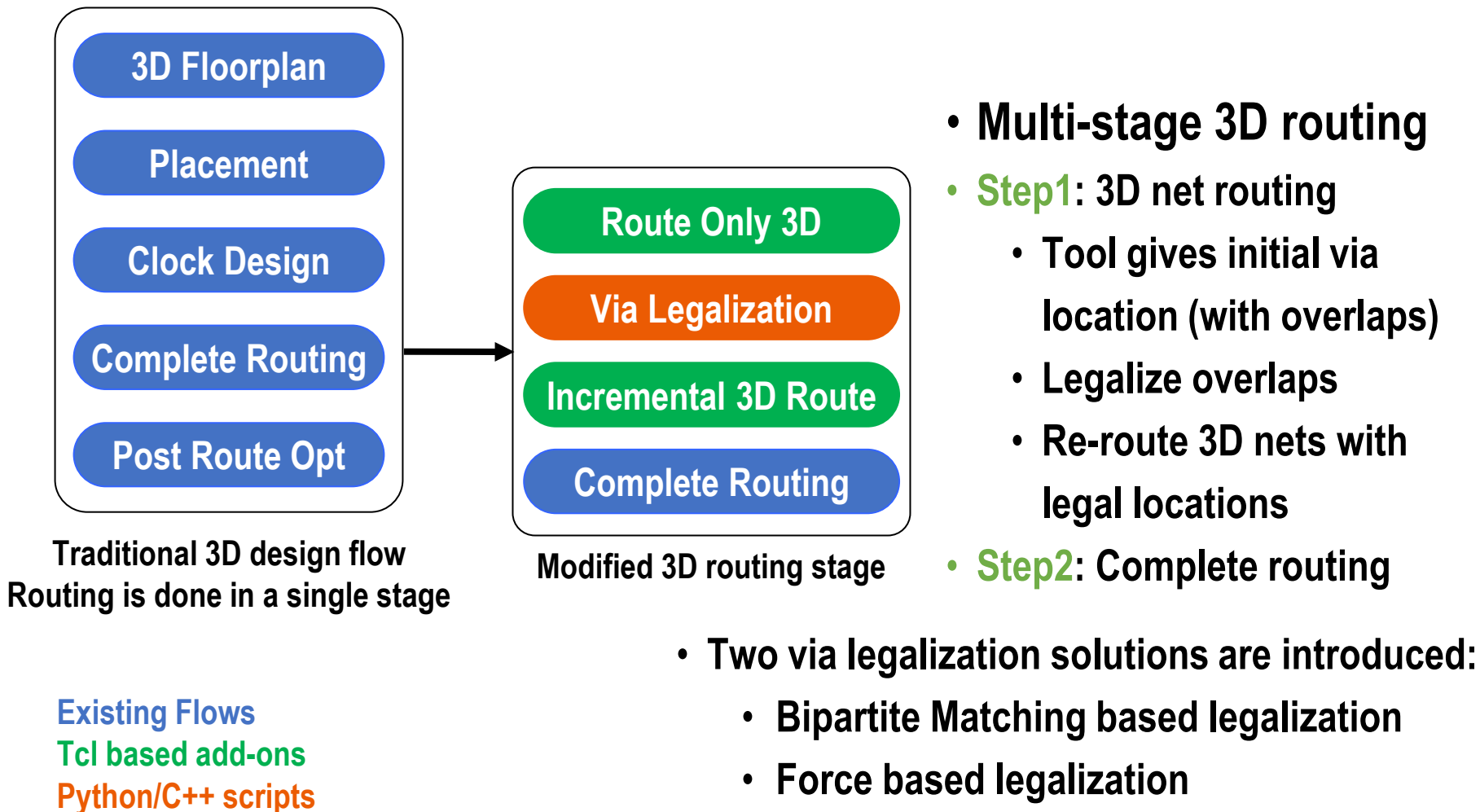


Histogram of 5um F2F bumps in 28nm and 16nm technologies

# Proposed Solution

## 3D Routing Flow

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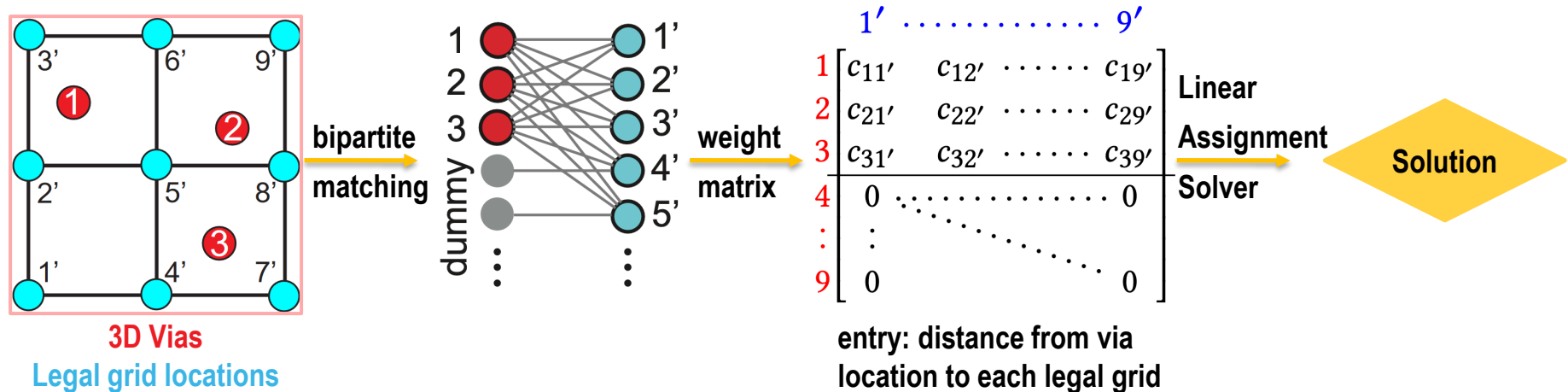


## Proposed Solution

# Bi-partite matching based legalization

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### Formulating a Bi-partite Matching problem from via assignment



#Legal grid locations can be too large

Optimal assignment is solved using Shortest Augmenting Path Algorithm

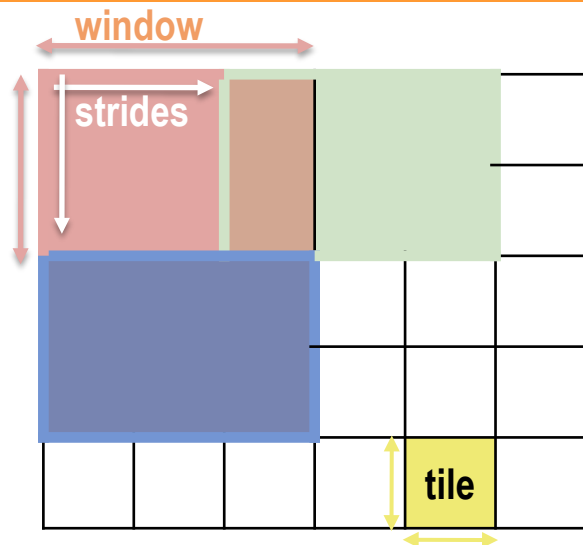
Complexity:

Time:  $O(\max(\#Vias, \#Grid\ Points)^3)$

Space:  $(\#Vias) \times (\#Grid\ Points) \times 8$  (8bytes needed to store float64)

Space requirement can easily exceed RAM capability for modern machines

## Reducing design complexity: Tiling floorplan



Window-based 2D floorplan grids.

Floorplan split into multiple tiles. Each tile is considered a single unit (1x1)

Multiple grid points (legal via locations) within a tile

Tiles are grouped into a window (2x3, here)

Via assignment problem is solved optimally within each window

The overlap between windows helps for any vias to move between windows

| Windowing parameters | Range            | Defaults |
|----------------------|------------------|----------|
| Tile width           | $[5p_x, 100p_x]$ | $30p_x$  |
| Tile height          | $[5p_y, 100p_y]$ | $30p_y$  |
| Window size (x)      | $[3t_w, 10t_w]$  | $3t_w$   |
| Window size (y)      | $[3t_h, 10t_h]$  | $3t_h$   |
| Horizontal stride    | $[1t_w, 3t_w]$   | $2t_w$   |
| Vertical stride      | $[1t_h, 3t_h]$   | $2t_h$   |

$p_x$  is the 3D via pitch along x

$p_y$  is the 3D via pitch along y

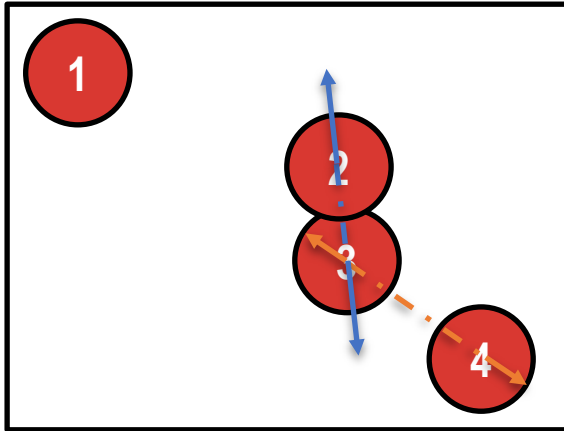
By default, each tile has a 30x30 grid for legal via locations

Parameters are tuned within the range using Bayesian Optimization

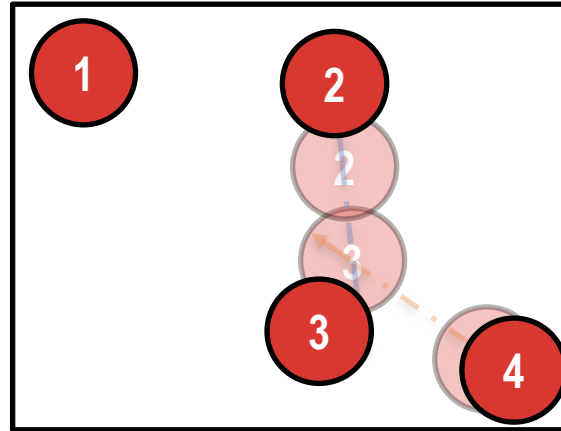
## Proposed Solution

# Force based legalization

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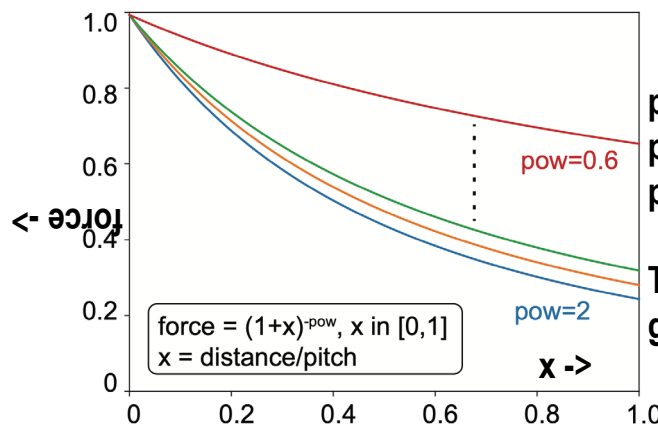


Repulsive forces added on each pair of overlapping vias – removes overlaps  
vias 2, 3 have overlap violations  
vias 3, 4 have spacing violations



Vias moved in discrete steps  $\propto$  Applied force

Additional force added towards initial via centers – reclaims unnecessary displacement



pow=2: Forces are more affected by closely placed vias

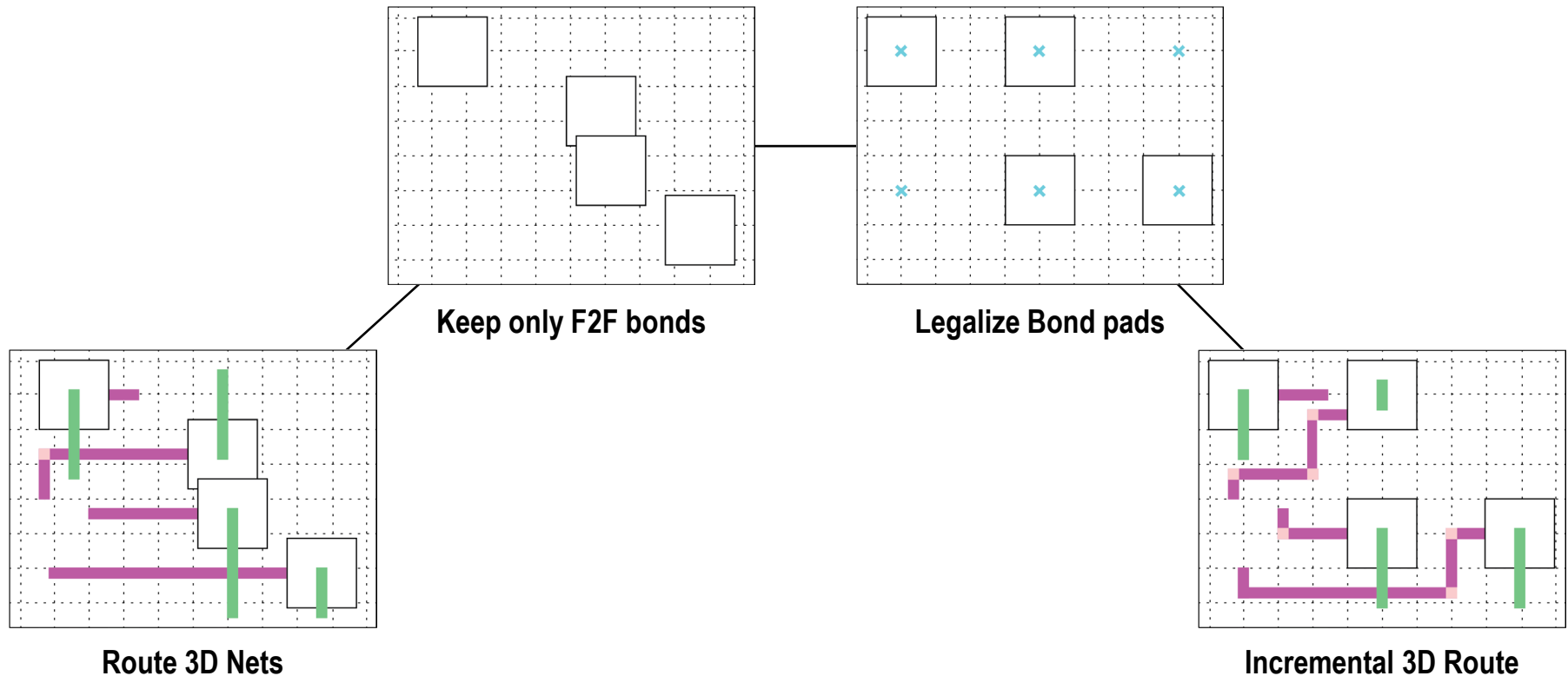
pow=0.6: Farther vias have a larger impact

The pow parameter is changed from 2  $\rightarrow$  0.6 gradually to make the forces more global.

## Proposed Solution

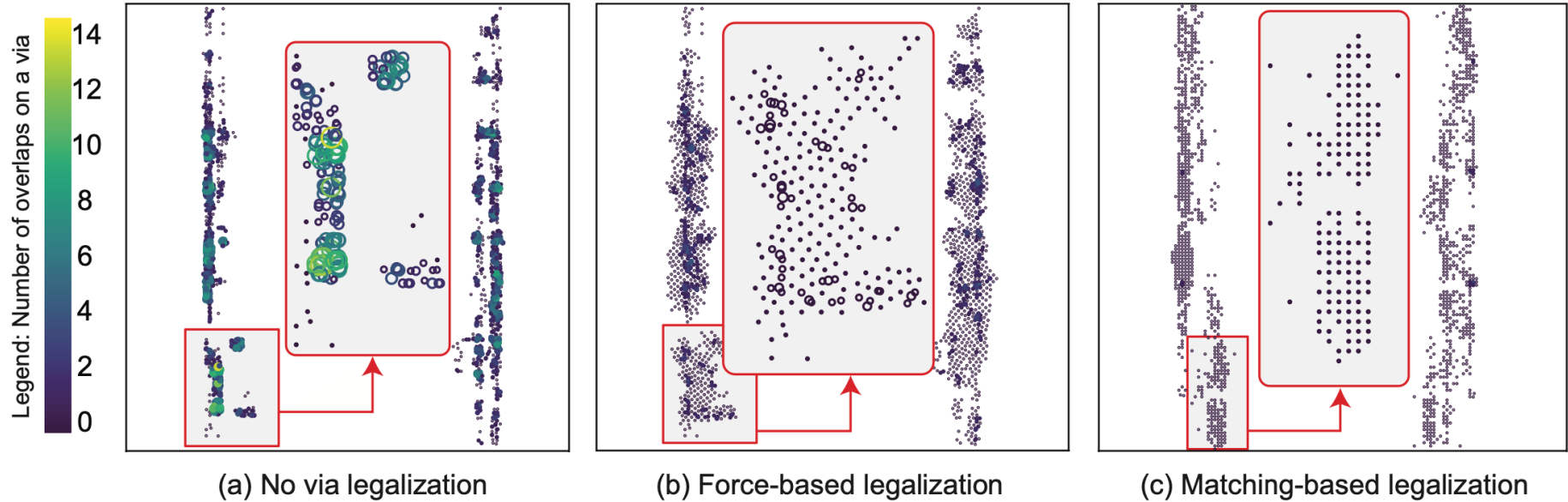
# Modified routing flow for 3D nets

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# Comparing Via Placement Results

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# Results: Hybrid Bonded 3D (5um pitch)

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| Application Processor 1 | Default | Force  | Bipartite |
|-------------------------|---------|--------|-----------|
| Frequency (GHz)         | 1.25    | 1.25   | 1.25      |
| WL (m)                  | 11.62   | 11.76  | 11.75     |
| WNS (ns)                | -0.119  | -0.091 | -0.094    |
| TNS (ns)                | -202.1  | -113.7 | -120.4    |
| Power (mW)              | 677.0   | 678.7  | 678.5     |
| #Vias                   | 5014    | 3246   | 3246      |
| #Violations             | 3538    | 0      | 0         |
| max displ. (um)         | -       | 29.9   | 31.6      |
| avg displ. (um)         | -       | 5.3    | 3.0       |

The default router creates a large number of violations

The modified routing flow limits vias on non-3D nets

Both methods work well for hybrid bonded 3D

Parameter tuned bipartite matching works better than force based in terms of displacement of vias

# Results: Micro-bump 3D (20um pitch)

16

| Application Processor 4 | Greedy | Bipartite |
|-------------------------|--------|-----------|
| Frequency (GHz)         | 1.25   | 1.25      |
| WL (m)                  | 11.56  | 11.41     |
| WNS (ns)                | -0.118 | -0.014    |
| TNS (ns)                | -25.15 | -5.04     |
| Power (mW)              | 796.6  | 794.4     |
| #Vias                   | 2957   | 2957      |
| #Violations             | 0      | 0         |
| max displ. (um)         | 601.0  | 385.1     |
| avg displ. (um)         | 127.5  | 68.1      |

**Micro-bump 3D has pre-placed bumps that are legal by construction**

**No violations in the default method: Greedy-based via assignment**

**Bipartite matching improves the overall design quality for micro-bumping**

# Results: Monolithic 3D (1um pitch)

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| Application Processor 1 | Default | Force  | Bipartite |
|-------------------------|---------|--------|-----------|
| Frequency (GHz)         | 1.50    | 1.50   | 1.50      |
| WL (m)                  | 3.64    | 3.71   | 3.70      |
| WNS (ns)                | -0.019  | -0.014 | -0.023    |
| TNS (ns)                | -0.450  | -1.057 | -2.220    |
| Power (mW)              | 350.5   | 351.5  | 350.7     |
| #Vias                   | 58039   | 53416  | 53347     |
| #Violations             | 5315    | 554    | 582       |
| max displ. (um)         | -       | 5.9    | 4.5       |
| avg displ. (um)         | -       | 0.6    | 0.5       |

The dense placement of vias in monolithic 3D and large interconnectivity not suitable for via legalization

A more advanced 3D router is required to handle such dense 3D connectivity

- **Automatic 3D via / bond-pad placement using EDA tools creates routing violations**
- **Proposed 2 solutions for removing overlaps with bi-partite matching based solution, and a force legalizer method**
- **Both the solutions are applicable for a wide range of 3D pitch values: 5um, 20um pitch tested**
- **Fixing violations early improves routing and timing in hybrid bonded 3D ICs**
- **Monolithic 3D IC requires changes to the routing algorithm**