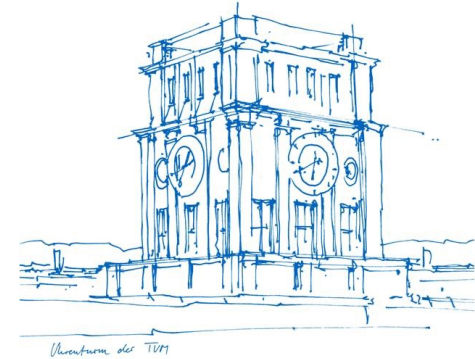


FXT-Route: Efficient High-Performance PCB Routing with Crosstalk Reduction Using Spiral Delay Lines

[Meng Lian](#), Yushen Zhang, Mengchu Li,
Tsun-Ming Tseng, and Ulf Schlichtmann
Technical University of Munich, Munich, Germany

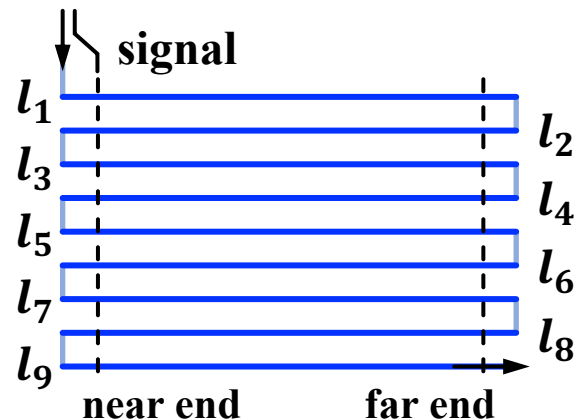


Outline

- [Delay matching](#)
- [Crosstalk noise](#)
 - Serpentine delay line
 - Spiral delay line
- Our method
 - [The along-the-edge routing](#)
 - [Spiral pattern synthesis](#)
- Experimental results
 - [Routing area reduction](#)
 - [Crosstalk reduction](#)

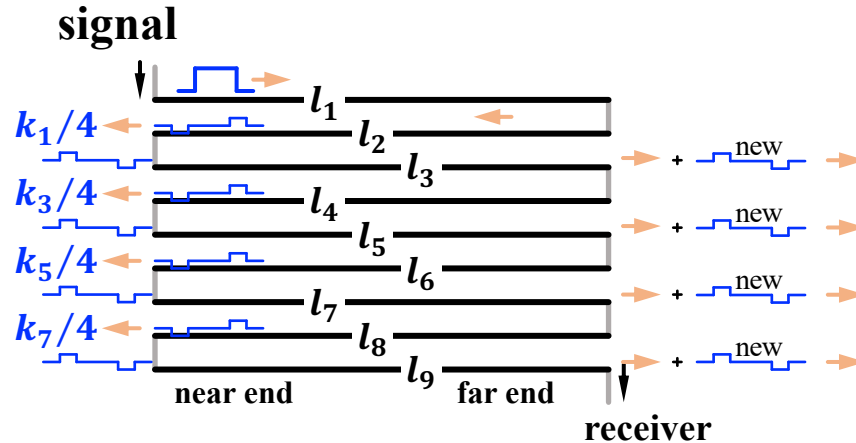
Delay matching

- Balance the delay of time-critical signals
- *Serpentine delay lines*
 - Speed-up effect
- Crosstalk alleviate
 - enlarge the wire segment separation



Crosstalk noise – Serpentine delay line

- Crosstalk magnitude: $k_{|m-n|}/4$ [1,2]
- t_d indicates the time for a signal to travel along one wire segment



source:

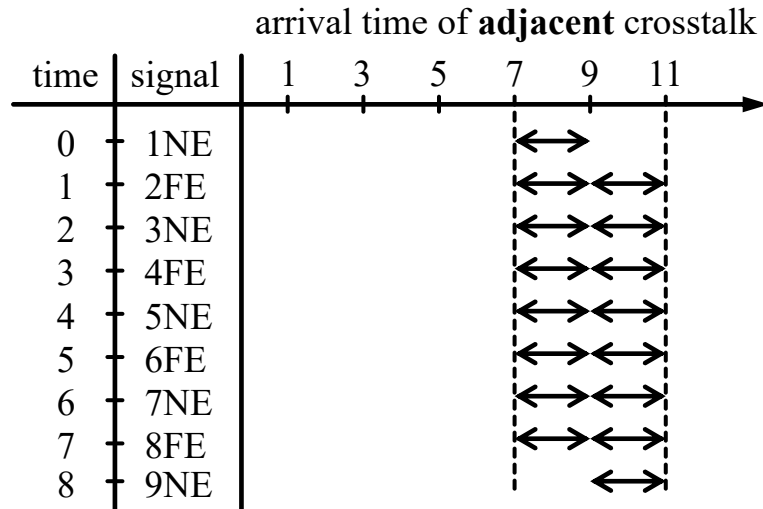
[1] Omar Ramahi. *Analysis of Conventional and Novel Delay Lines: A Numerical Study*. ACES, 2003.

[2] R-B Wu and F-L Chao. *Laddering wave in serpentine delay line*. IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B 1995.

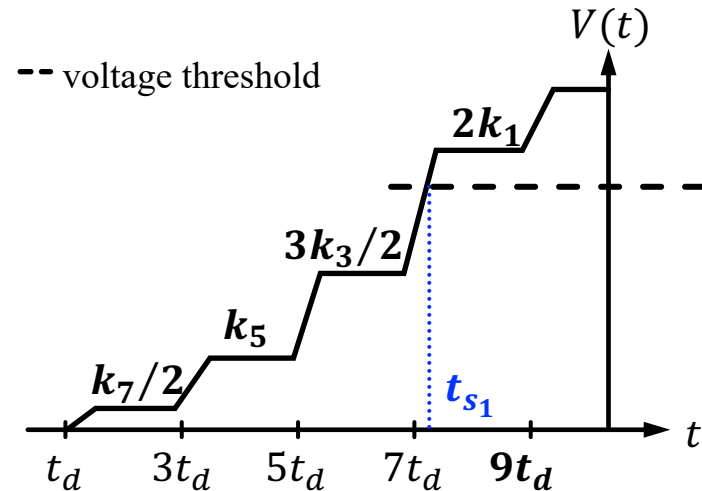
Crosstalk noise – Serpentine delay line

Time diagram

- Crosstalk $\propto 1/\text{wire separation}$

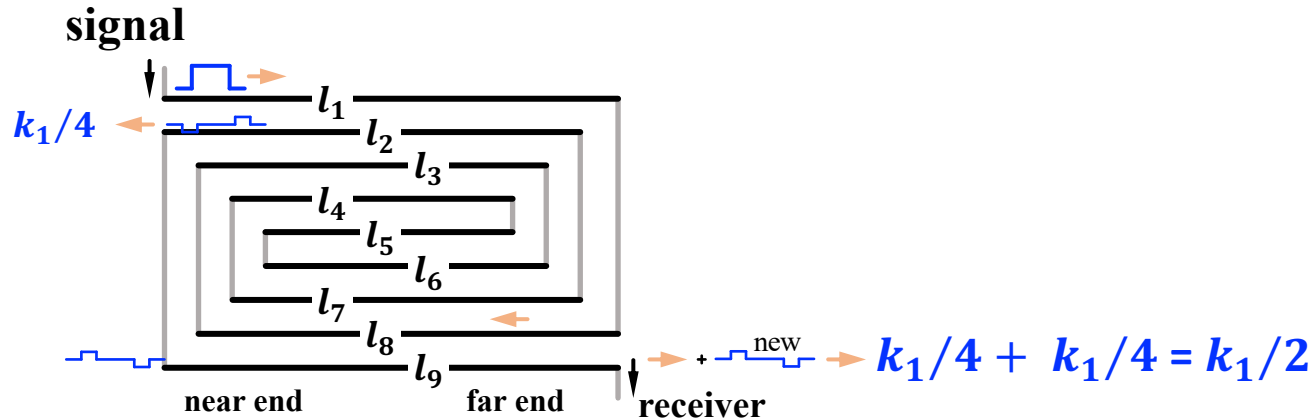


Receiving waveform



Crosstalk noise – Spiral delay line

- Crosstalk magnitude: $k_{|m-n|}/4$ [1,2]
- t_d indicates the time for a signal to travel along one wire segment



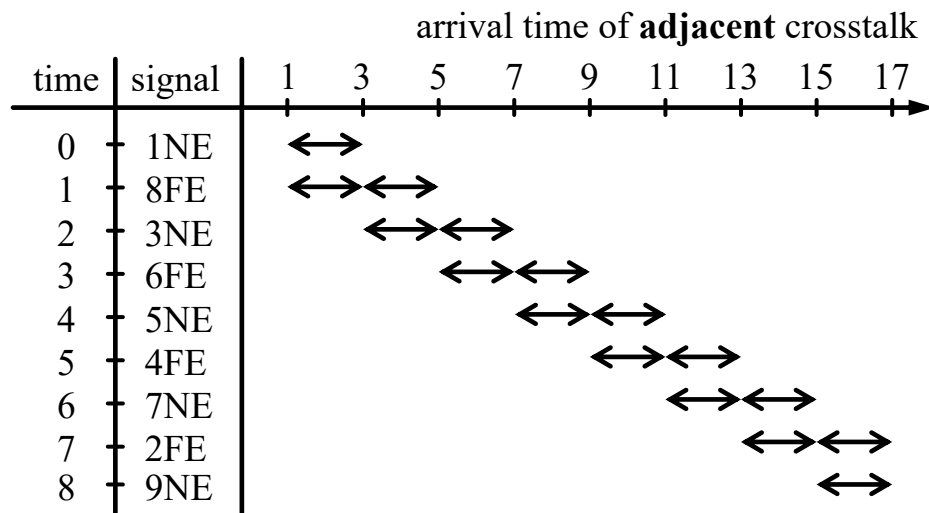
source:

[1] Omar Ramahi. *Analysis of Conventional and Novel Delay Lines: A Numerical Study*. ACES, 2003.

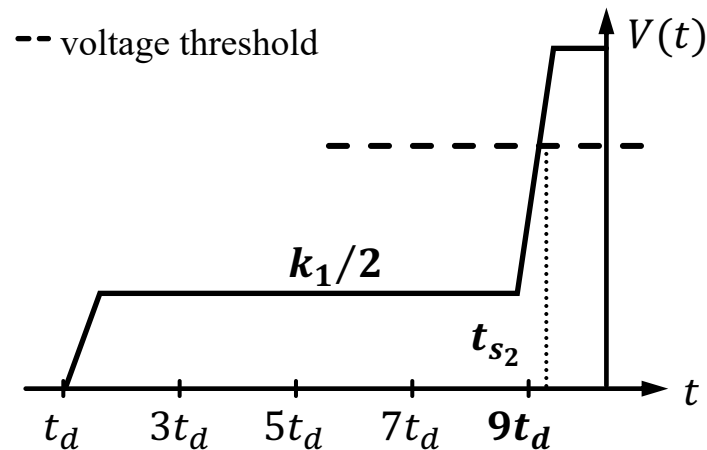
[2] R-B Wu and F-L Chao. *Laddering wave in serpentine delay line*. IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B 1995.

Crosstalk noise – Spiral delay line

Time diagram



Receiving waveform

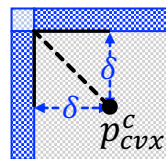


Our method

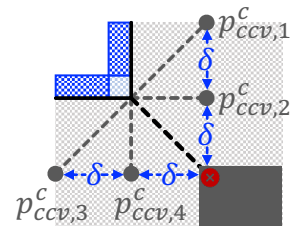
- Generate one wire at a time
- The along-the-edge routing
- Spiral pattern synthesis

Our method – The along-the-edge routing

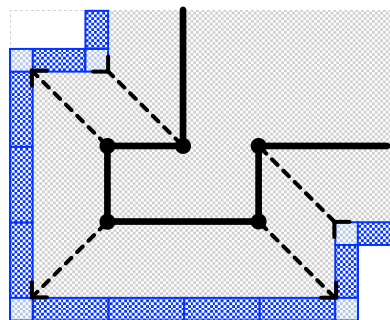
- Starting from the *edge*
 - maximally reserving the *center*
- Mixed-integer linear programming (MILP)
- Determine wire's main path
 - alongside the free space boundary
- Minimally acceptable unit length δ
- *Bending point candidate*



convex corner



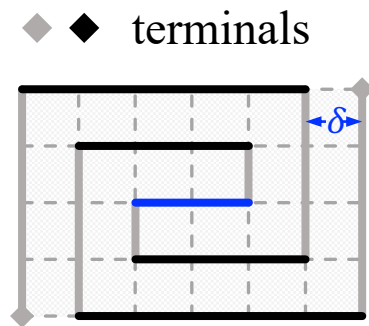
concave corner



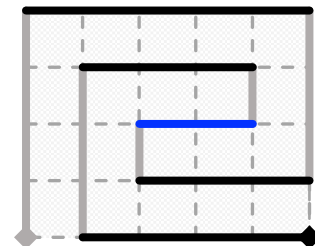
- boundary
- free routing area
- candidate
- wire segment

Our method – Spiral pattern synthesis

- Compensate for the required wire length
- Spiral pattern
 - *convex* and *concave* spirals



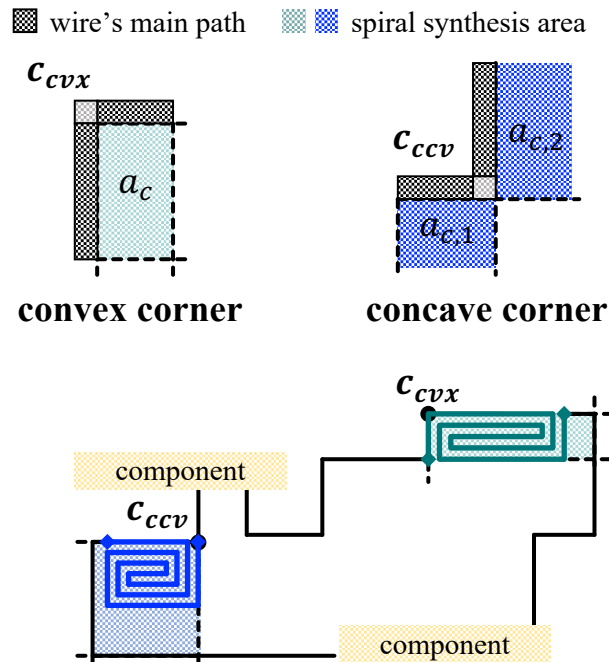
convex spirals



concave spirals

Our method – Spiral pattern synthesis

- Compensate for the required wire length
- Spiral pattern
 - *convex* and *concave* spirals
- Synthesizing spirals with prioritization
 - *convex* and *concave* corners
 - weight coefficient $\in [0,1]$
- Quadratic programming (QP)



Experimental results – Routing area reduction

case	n_w^1	l_{tot}^2	time ³ (s)	$a_\Delta^4(\%)$	$\hat{a}_\Delta^5(\%)$	$R_a^6(\%)$
1	12	448	5	71.82	14.99	66.86
2	16	2856	8	43.52	17.10	31.88
3	16	3046	10	42.20	14.12	32.92
4	16	5332	32	36.57	12.90	27.17
5	20	3802	26	32.50	16.77	18.91
6	36	19393	950	22.83	13.30	10.99

1.the number of wires, 2. the total required wire length, 3. the runtime, 4. and 5. the free space ratio of the original and minimized routing area, respectively, 6. the percentage routing area reduction

- $\delta = 1$
- Free space ratios: $a_\Delta = 1 - \frac{l_{tot}}{\text{original area}}$; $\hat{a}_\Delta = 1 - \frac{l_{tot}}{\text{minimized area}}$
- $R_a = \frac{\text{original area} - \text{minimized area}}{\text{original area}}$

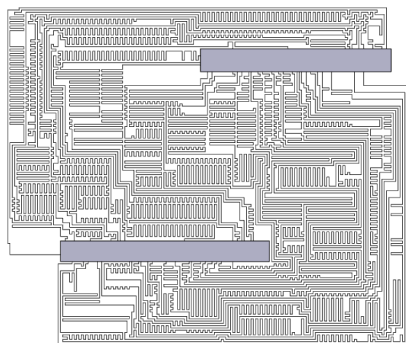
Experimental results – case 6

Original result

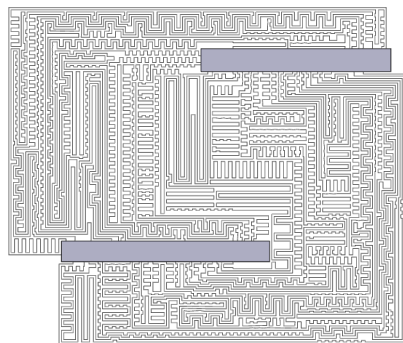
The state-of-the-art

Routing in the
original area

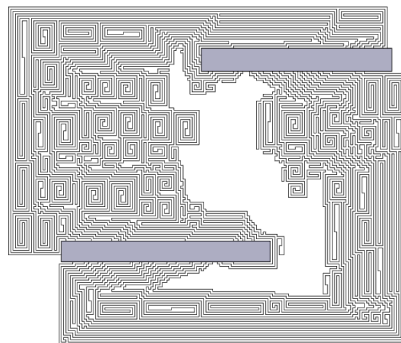
Routing in the
minimized area



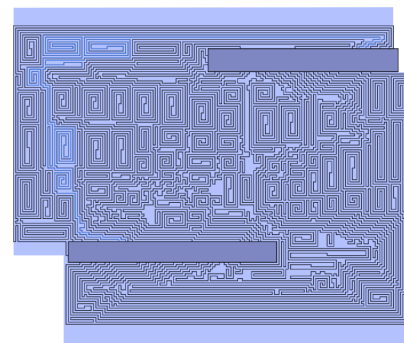
(a)^[1]



(b)^[2]



(c)



(d)

$1.6\times$

$R_a = 10.99\%$

source:

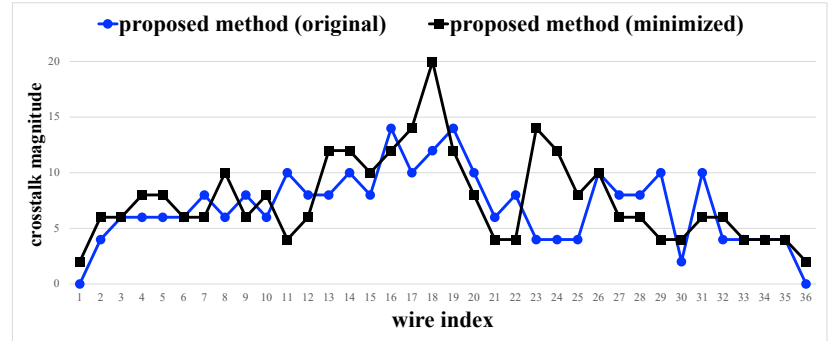
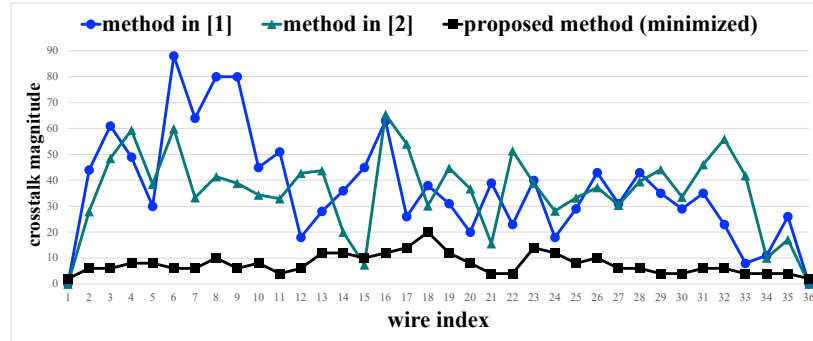
[1] Tan Yan and Martin D. F. Wong, *BSG-Route: A Length-Constrained Routing Scheme for General Planar Topology*, IEEE TCAD, 2009.

[2] Tsun-Ming Tseng et al. *ILP-Based Alleviation of Dense Meander Segments With Prioritized Shifting and Progressive Fixing in PCB Routing*, IEEE TCAD, 2015.

Experimental results – Crosstalk reduction

- k_d : the coupling coefficient for the near-end crosstalk induced within two parallel wire segments separated by d .
- $V_{\text{serpentine}} = (n - 1) \cdot \frac{k_d}{4}$
- $V_{\text{spiral}} = \frac{k_d}{2}$

		V_{max}	V_{avg}
method in	[1]	88.00	36.94
	[2]	65.43	35.66
proposed method in	original area	14.00	6.94
	minimized area	20.00	7.61



source:

[1] Tan Yan and Martin D. F. Wong. *BSG-Route: A Length-Constrained Routing Scheme for General Planar Topology*. IEEE TCAD, 2009.

[2] Tsun-Ming Tseng et al. *ILP-Based Alleviation of Dense Meander Segments With Prioritized Shifting and Progressive Fixing in PCB Routing*. IEEE TCAD, 2015.