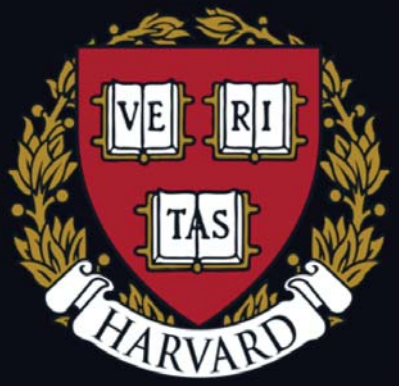
Advances in Carbon Nanotube Technologies: from Transistors to a RISC-V Microprocessor

Gage Hills, Christian Lau, Tathagata Srimani, Mindy D. Bishop, Pritpal Kanhaiya, Rebecca Ho, Aya Amer, Max M. Shulaker



Can Computing Systems Continue to Improve ?

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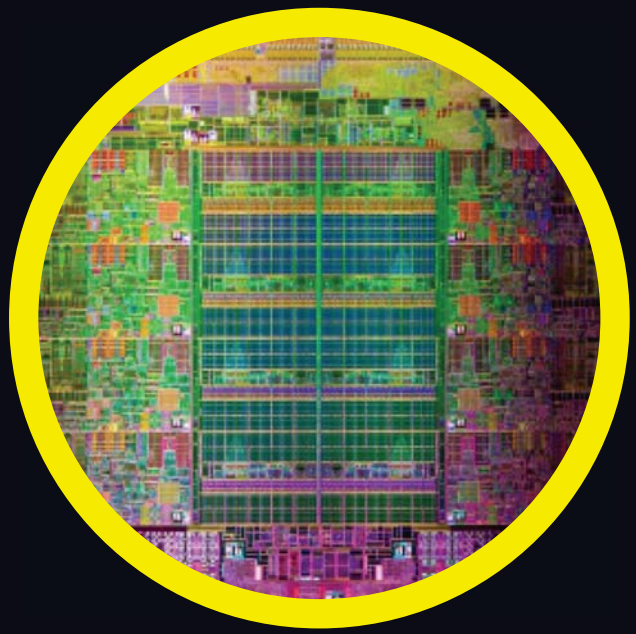
Dell's 1st computer: Turbo PC

Vodafone (11 lbs, 12,000 sold)

Can Computing Systems Continue to Improve ?

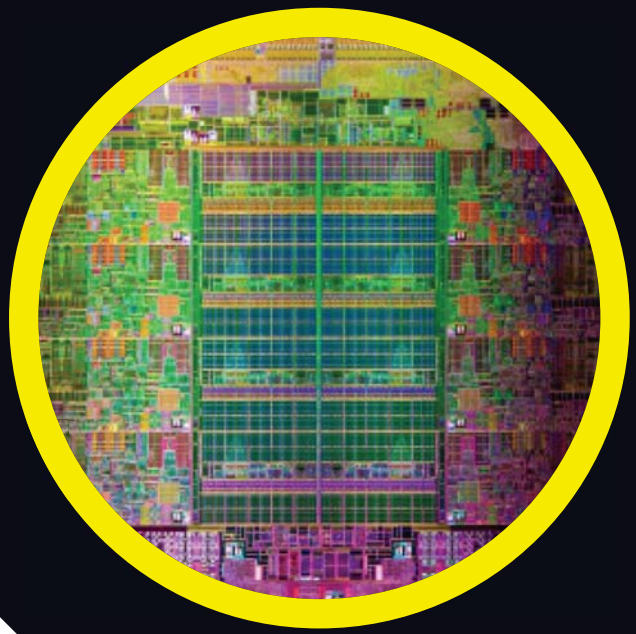
~30 years



>2,000,000X energy-efficiency

Can Computing Systems Continue to Improve ?

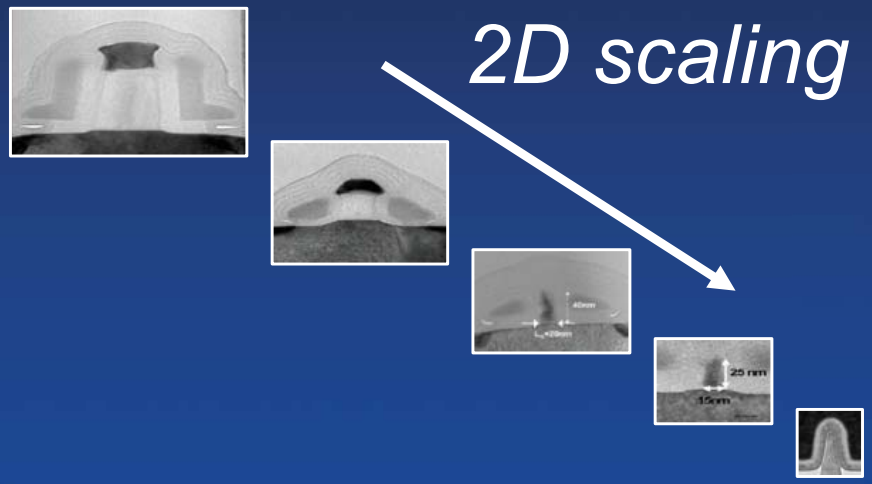
~30 years



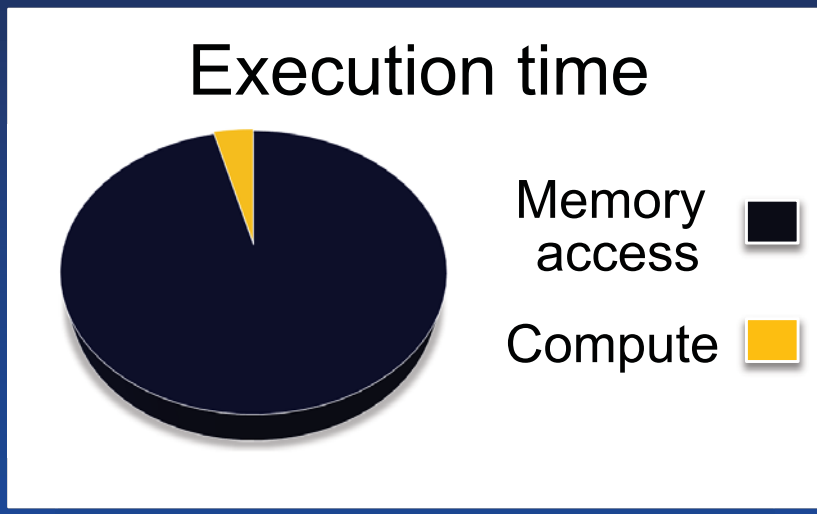
conventional approaches: *insufficient*

Many Obstacles *Simultaneously*

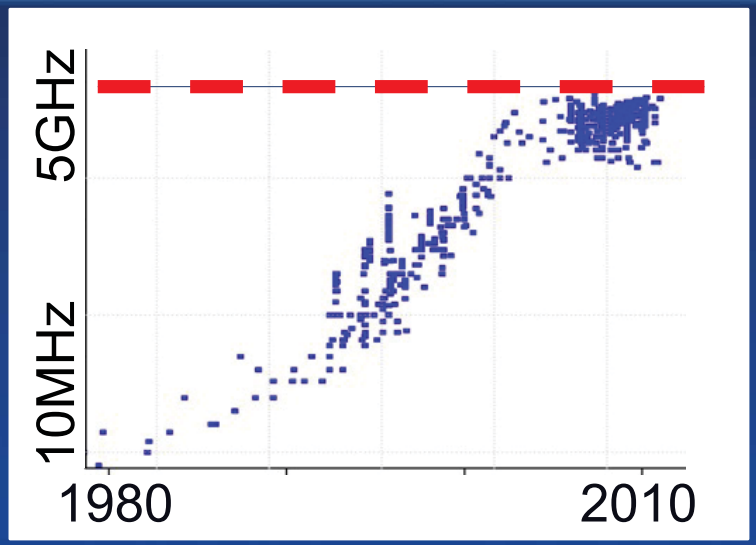
2D Miniaturization Wall



Memory Wall



Power Wall

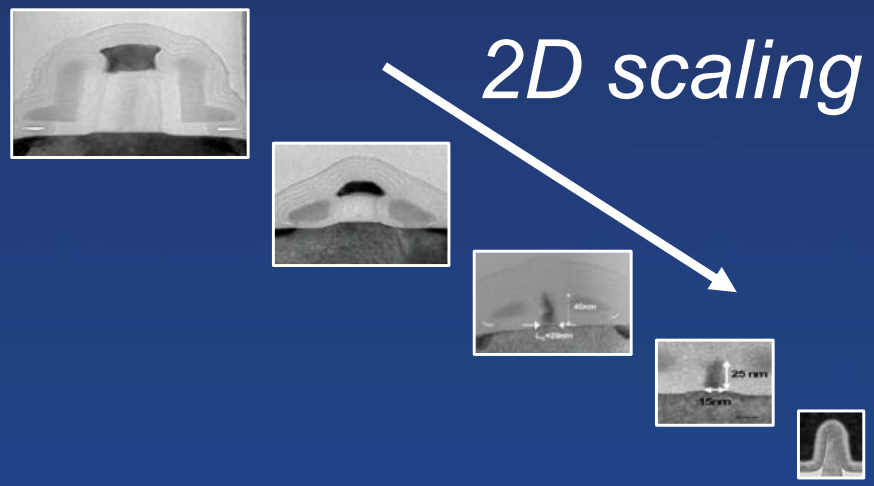


Also:
communication wall,
interconnect wall,
complexity wall,
resilience wall…

How to Improve Computing?

Conventional Approaches

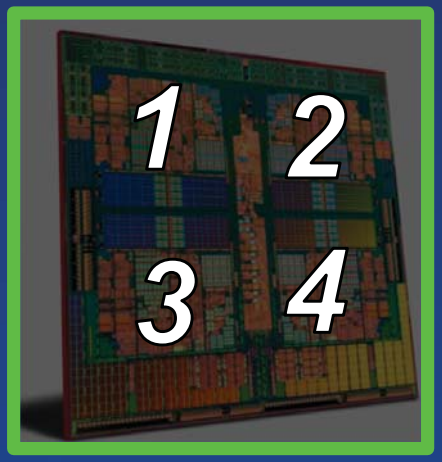
Conventional Silicon

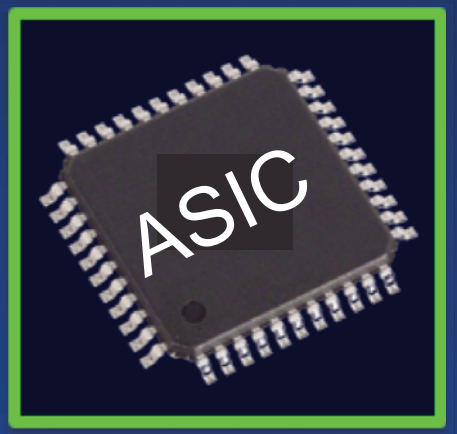


- Important, BUT:
  - Fundamental limits
  - Diminishing returns

Conventional Design

multi-cores



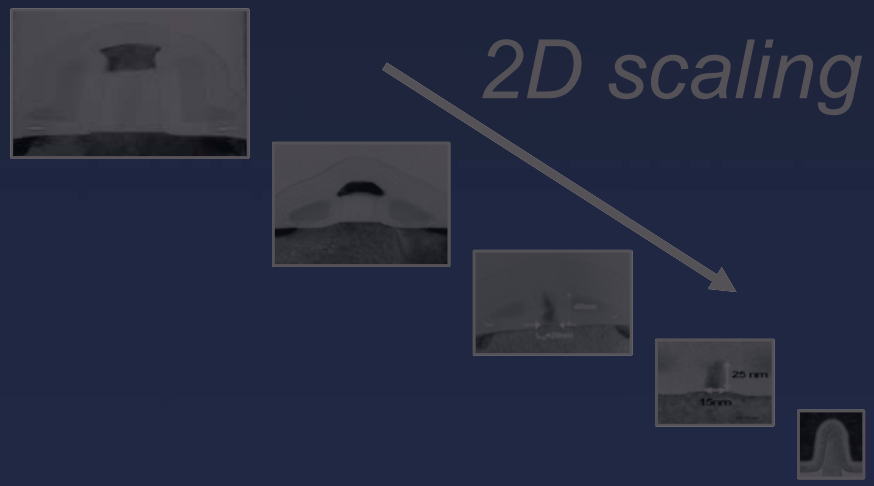


- Important, BUT:
  - Limited “Tricks”
  - Complexity

Conventional Approaches

Path for next-generation computing ?

Conventional Silicon



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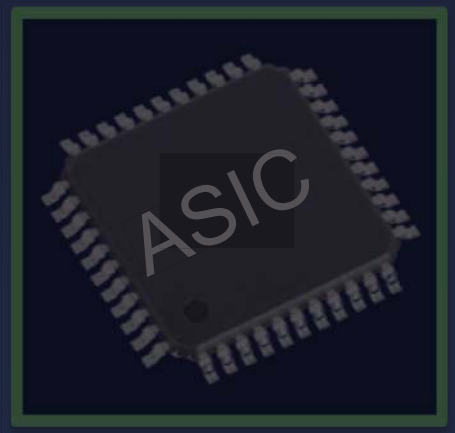


- Important, BUT:
  - Limited “Tricks”
  - Complexity

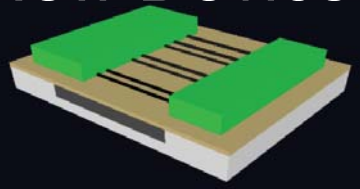
Solution: Nanosystems

Transform new nanotech

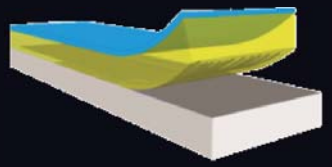
into new systems

enabling new applications

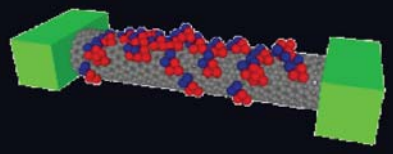
New Devices



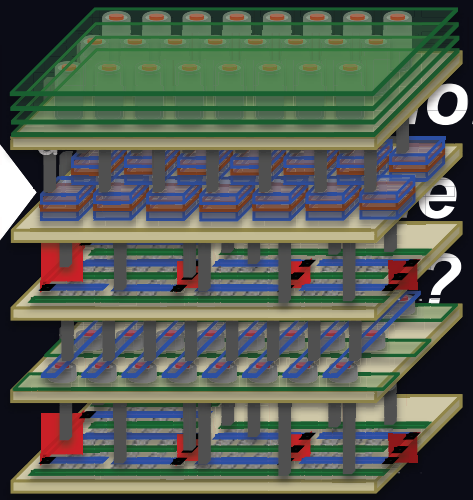
New Fabrication



New Sensors



Revolutionary Architectures



ons?

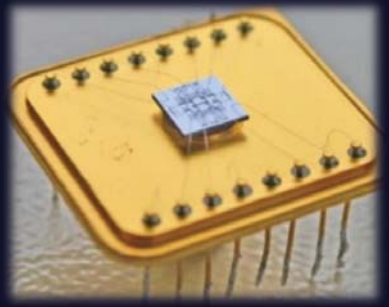
e fab

?

Abundant-Data Applications

Computer Chips Today

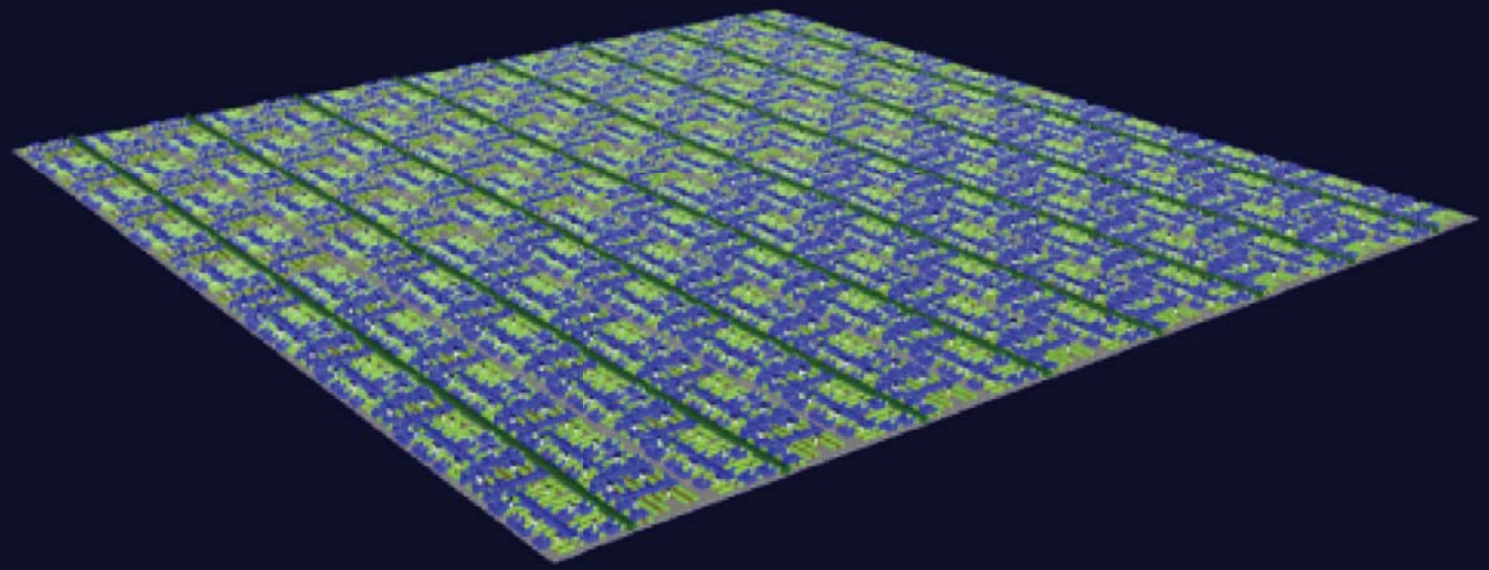
Limited to 2-Dimensional Circuits



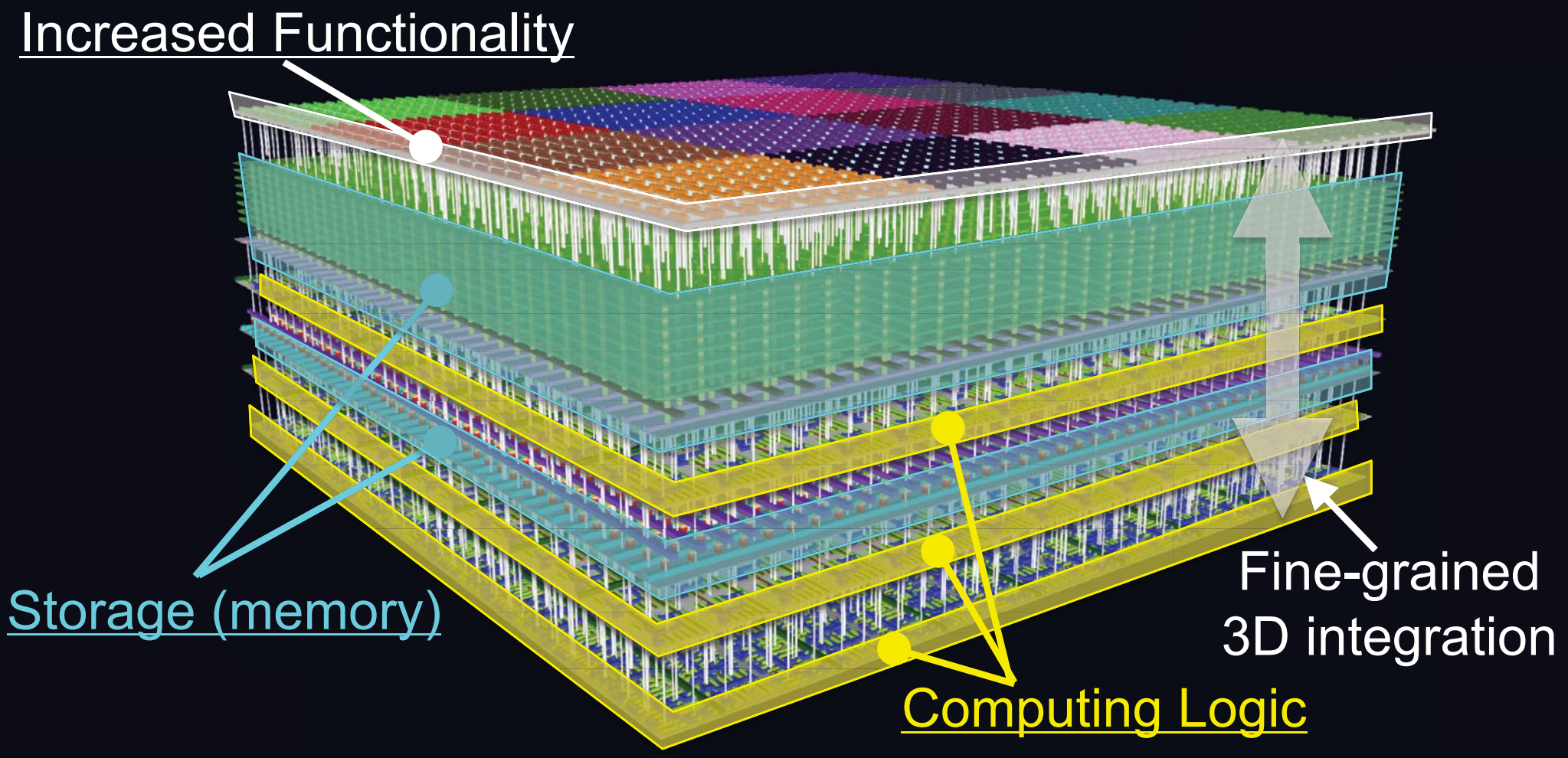
sensor

memory

Future Nanosystems

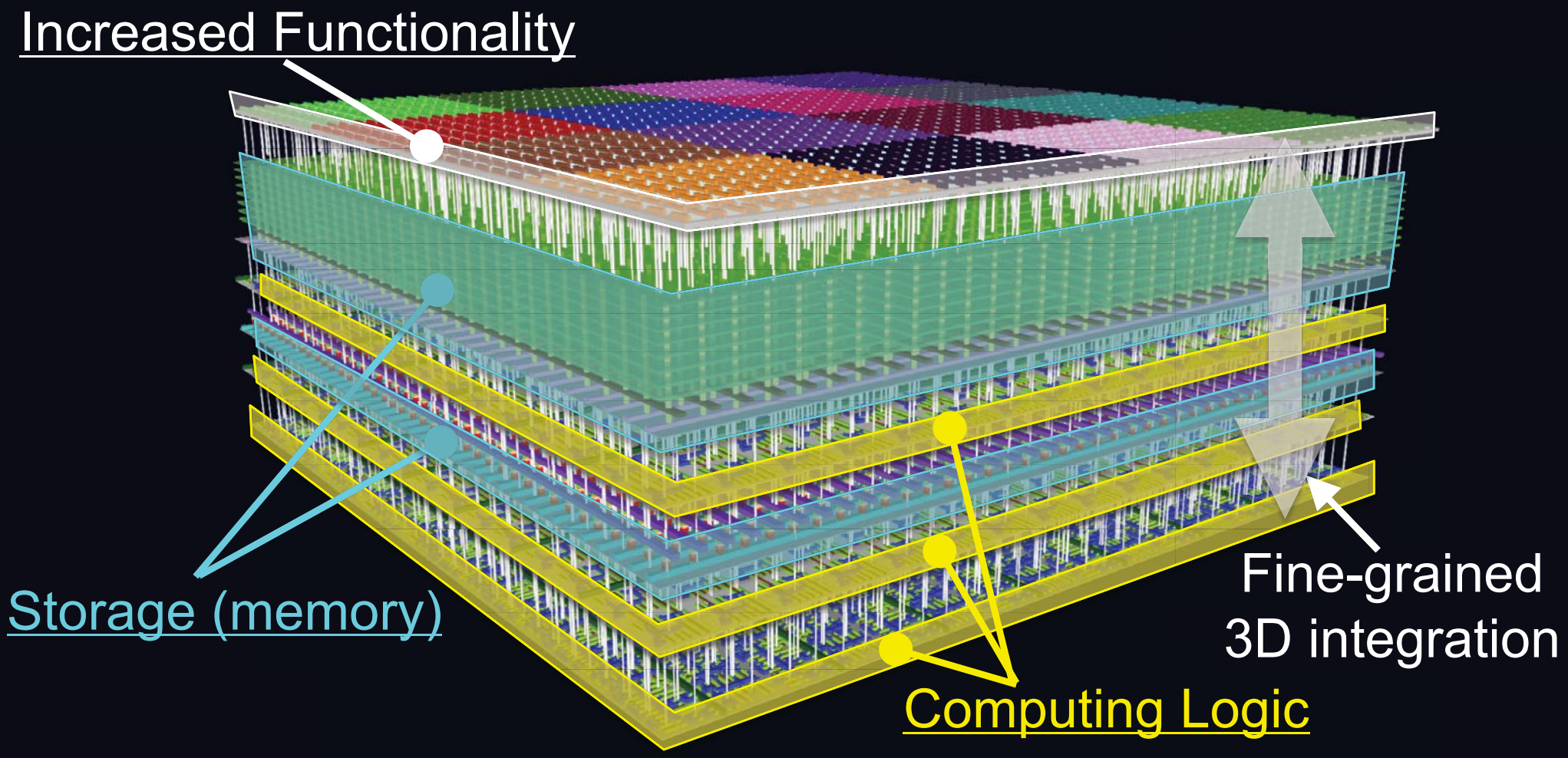


Future Nanosystems



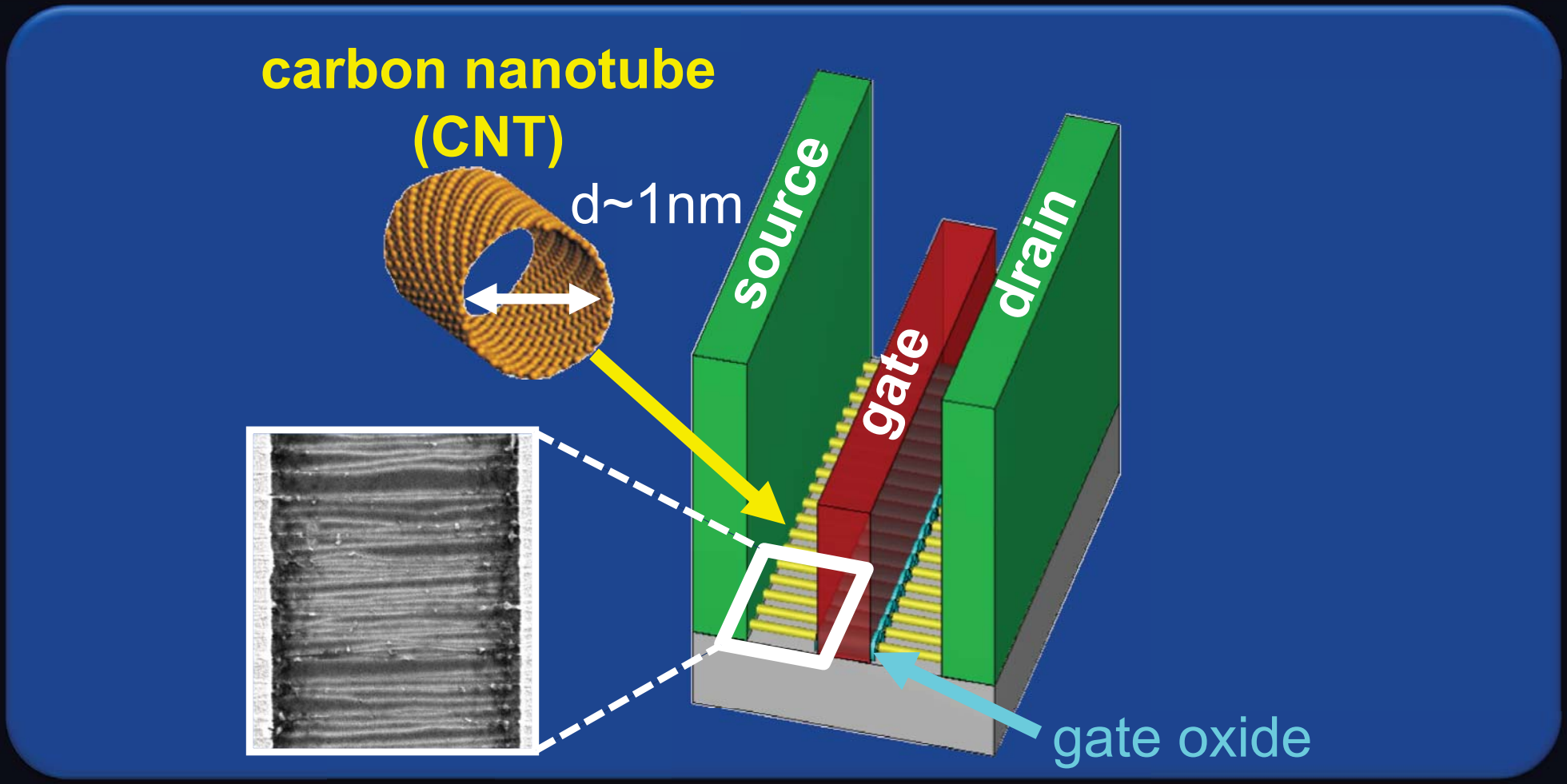
Impossible with today's technologies

Realizing Nanosystems TODAY
Enabled by Emerging Nanotechnologies



Case Study: Carbon Nanotube FETs (CNFETs)

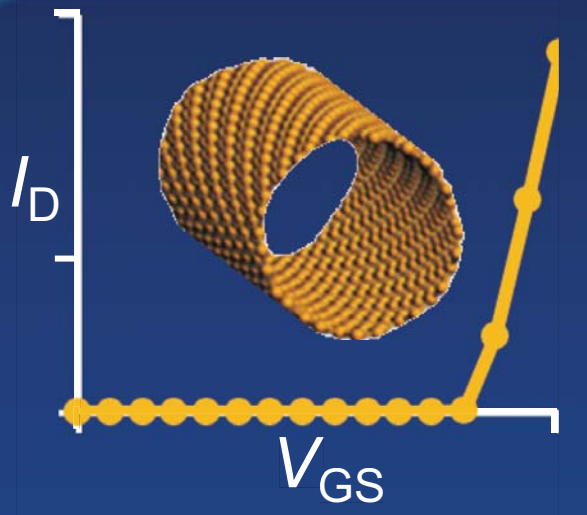
- Energy-efficient VLSI: **full-chip case studies**[1]
- Enable **monolithic 3D integrated systems**

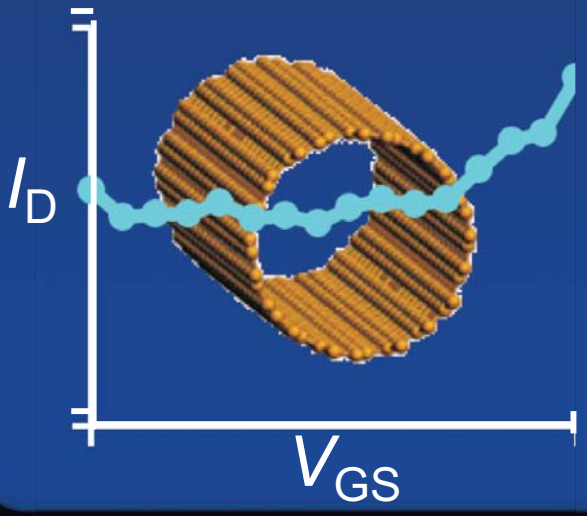


[1] IBM, imec, TSMC, Stanford, MIT

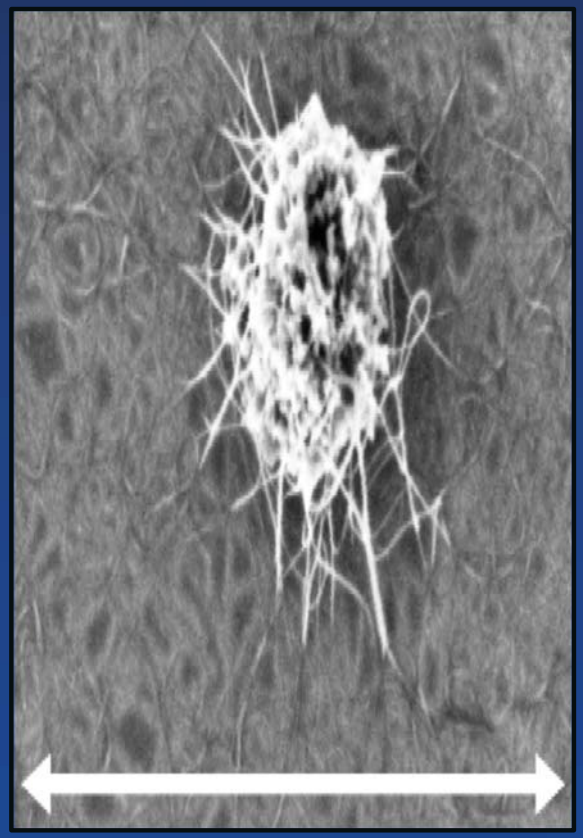
BIG Promise, BUT Major Obstacles

Materials

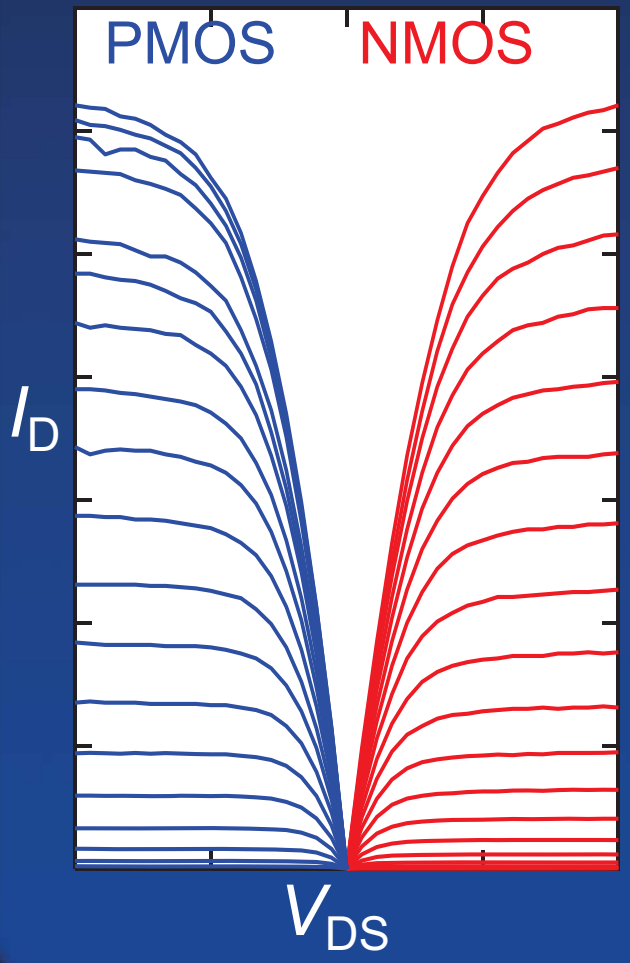




Manufacturing

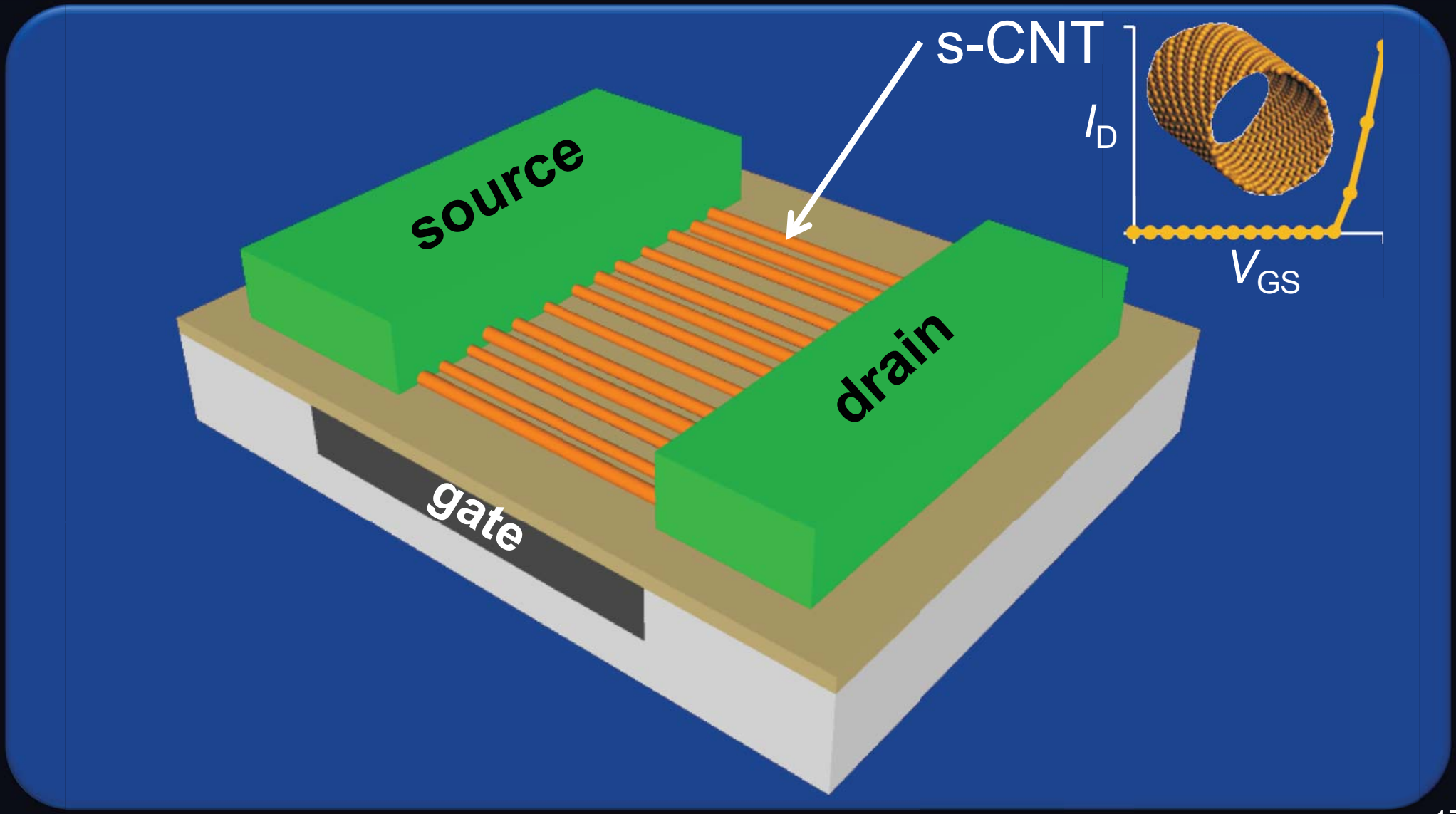


Variability



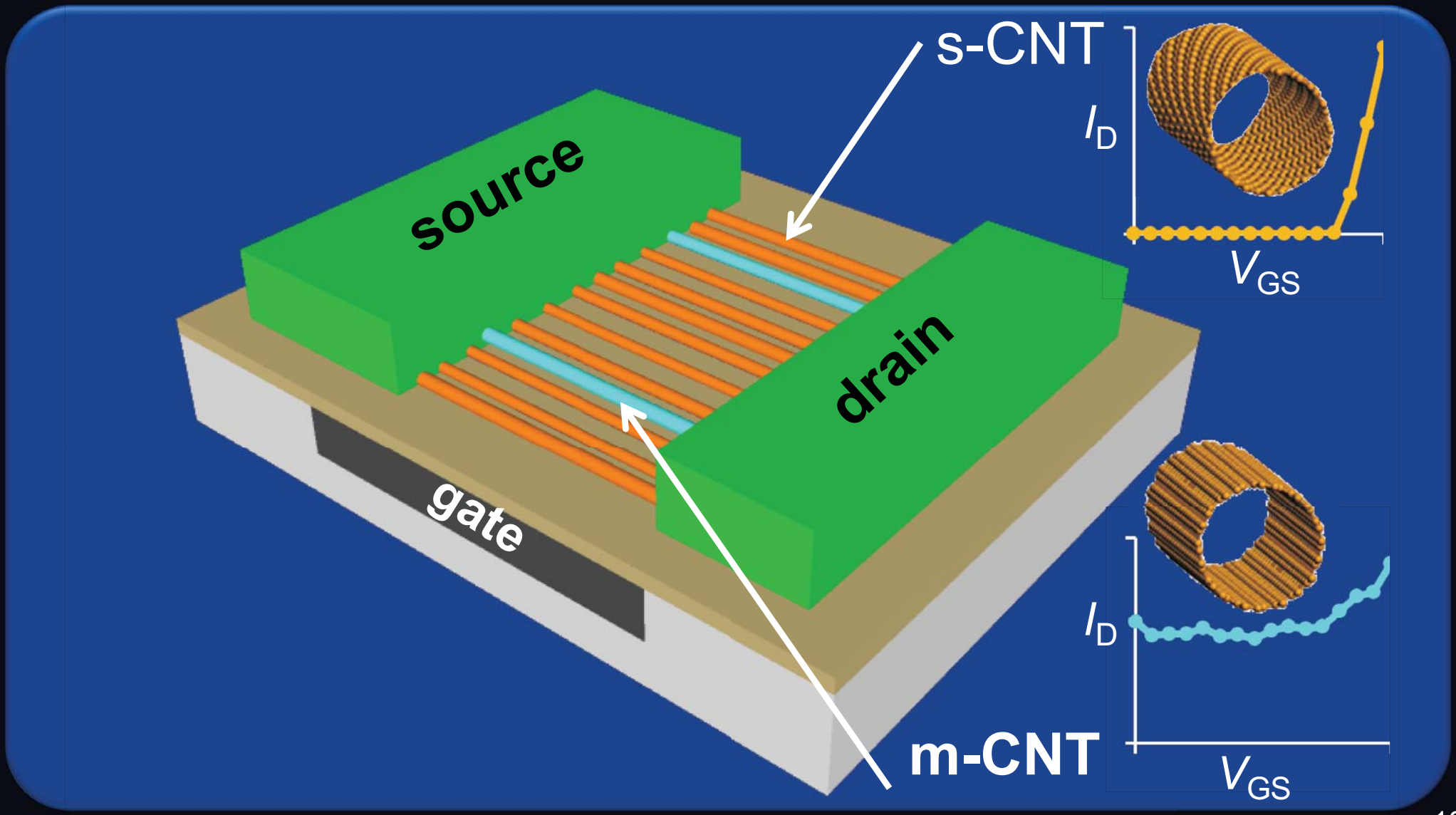
Imperfections: Metallic CNTs (m-CNTs)

- Ideally: all CNTs are semiconducting (s-CNT)



Metallic CNTs (m-CNTs)

- Random fraction of CNTs: **metallic (m-CNT)**



Metallic CNTs (m-CNTs)

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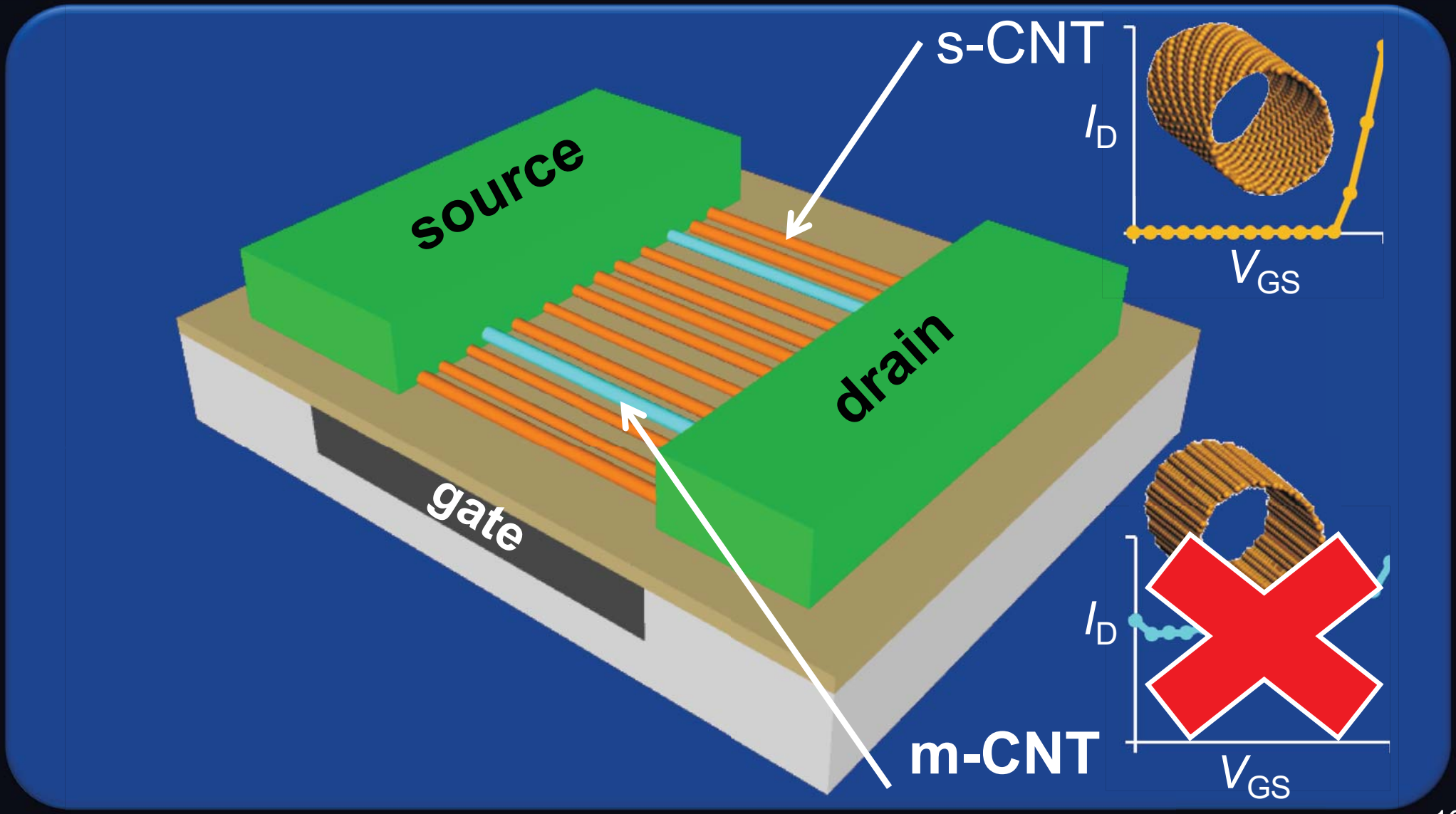
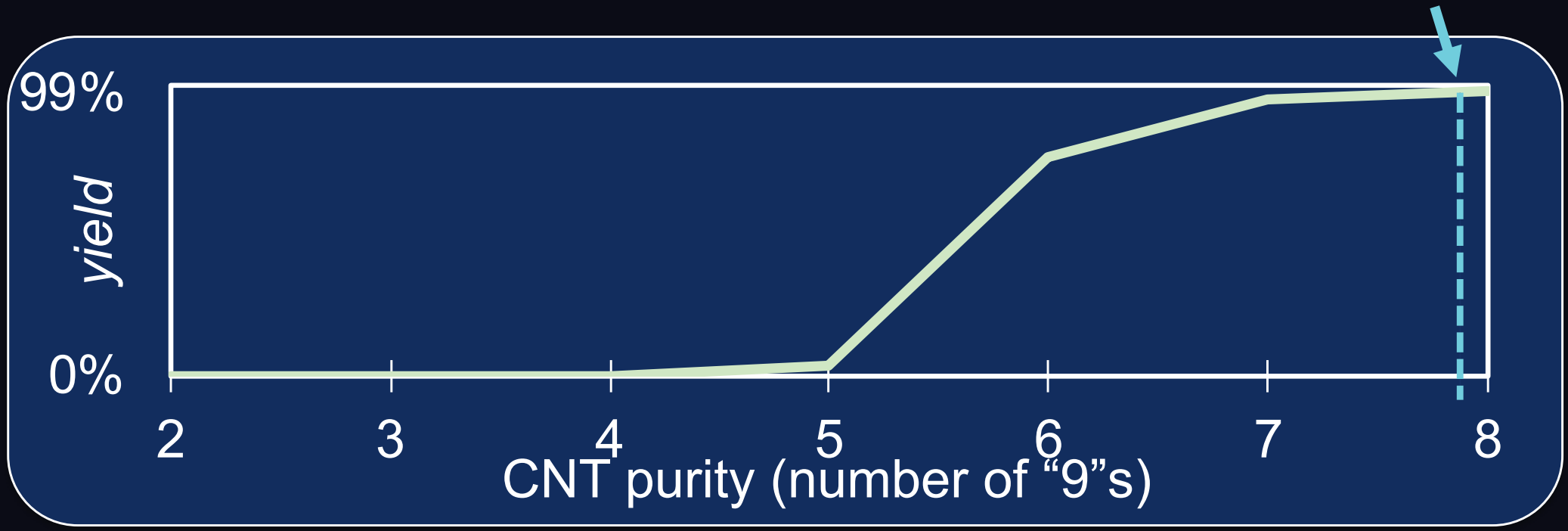


m-CNT Processing Options

- Grow 0% m-CNTs
  - Open challenge
- Remove m-CNTs after growth
  - ~99.99%

Major Roadblock

- ~99.999999% purity required
  - infeasible!

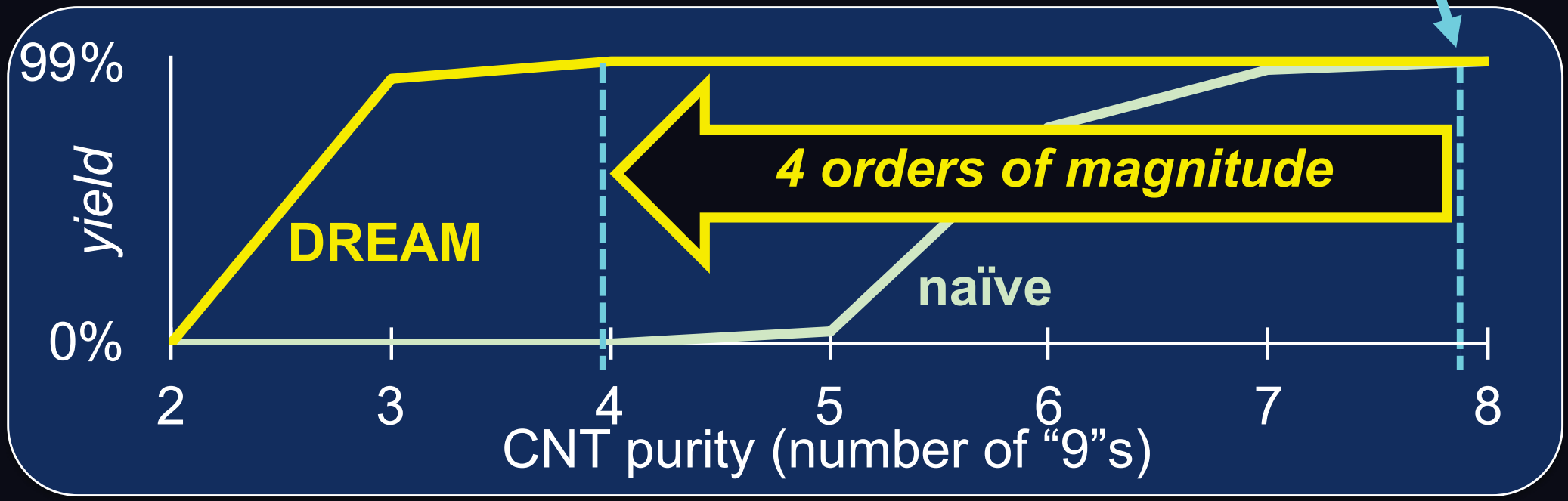


Yield = (1 – *PNMV*) for required SNM_R = VDD / 8

The "DREAM" Solution

- Designing REsiliency Against Metallic CNTs:
  - Achievable ***today*** !

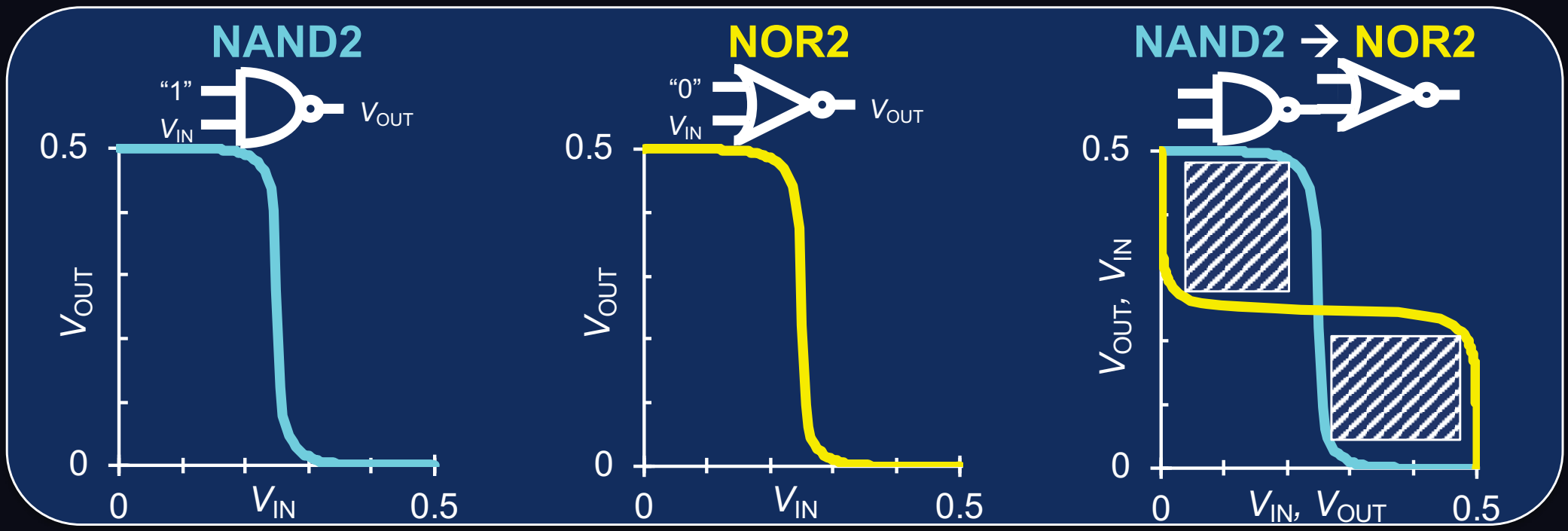
99% yield target:
~8Ns required



Yield = (1 – *PNMV*) for required SNM_R = VDD / 8

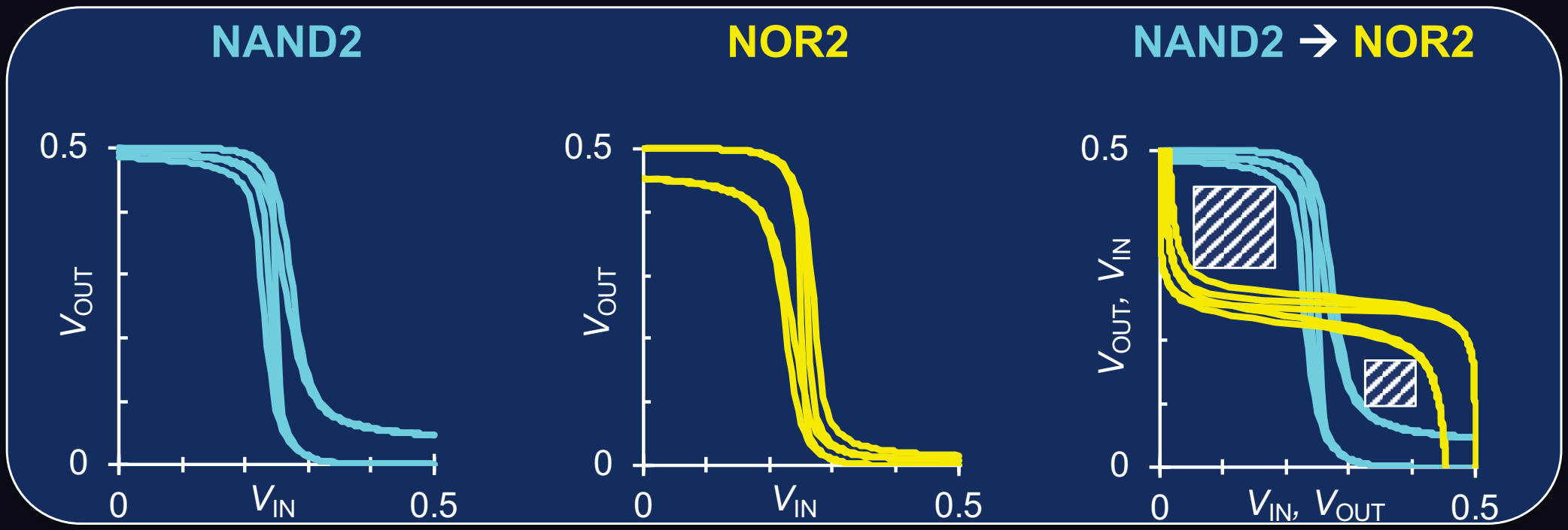
Metallic CNTs: Impact

- Example: no m-CNTs



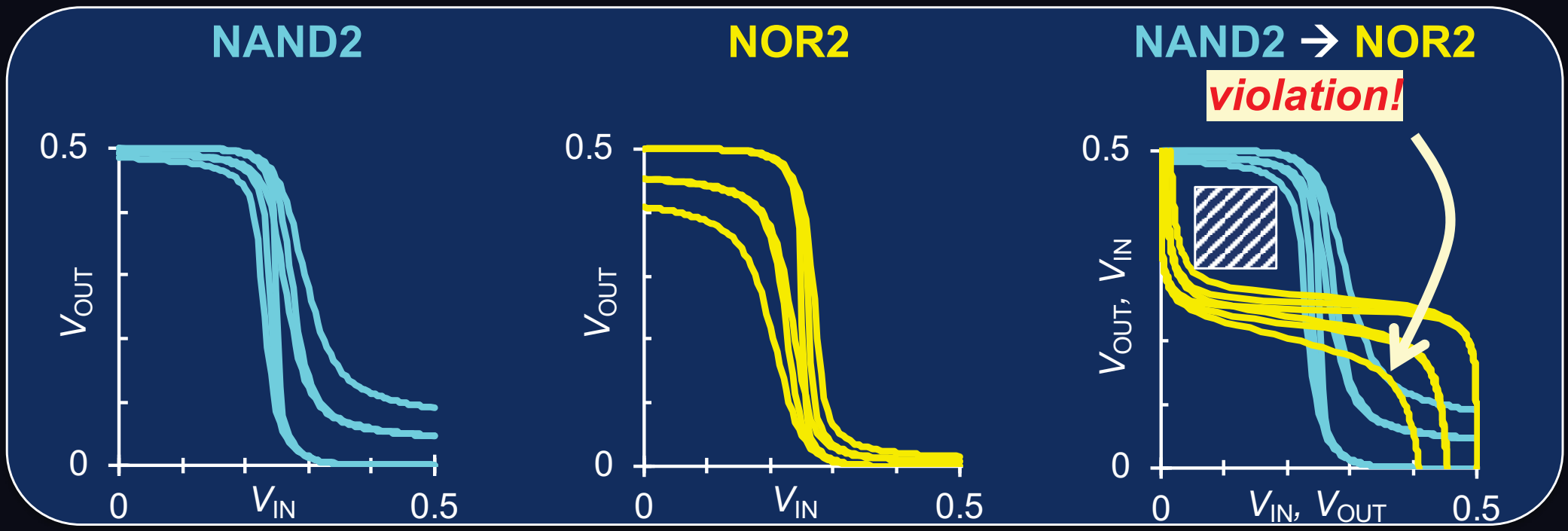
Metallic CNTs: Impact

- Example: ≤1 m-CNT per logic gate
  - degraded logic values



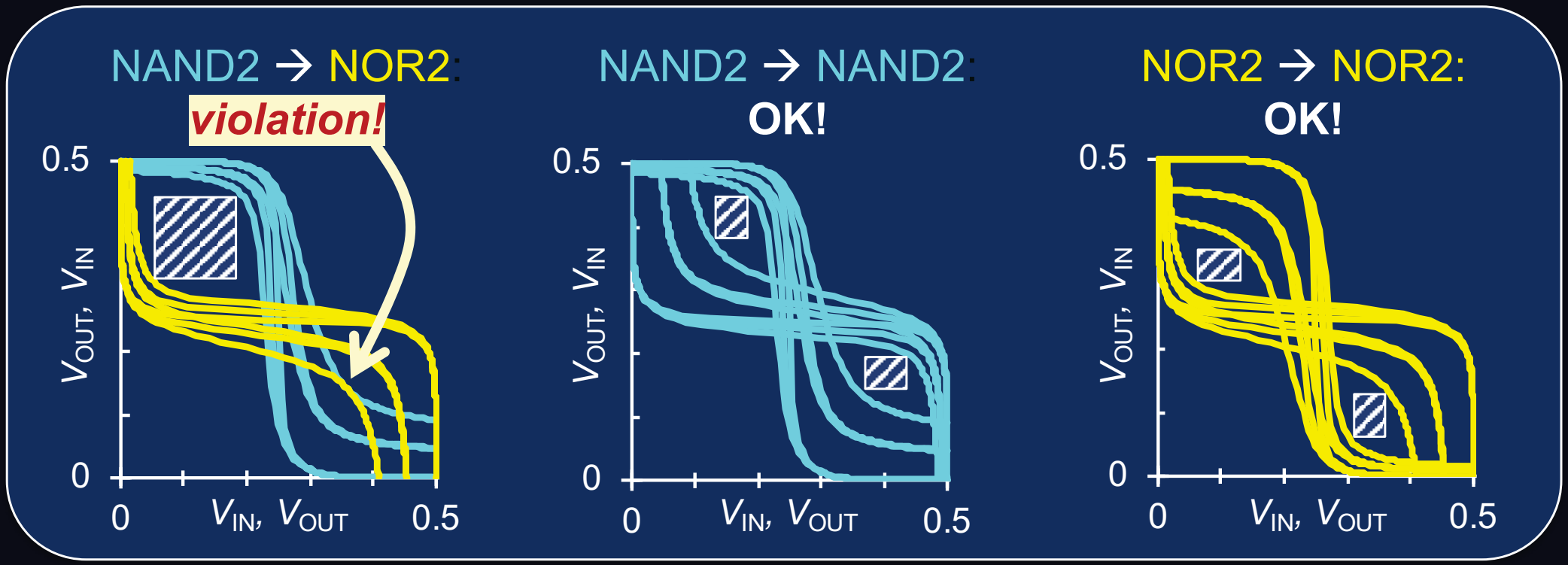
Metallic CNTs: Impact

- Example: ≤2 m-CNT per logic gate
  - incorrect logic functionality!



The “TRICK”

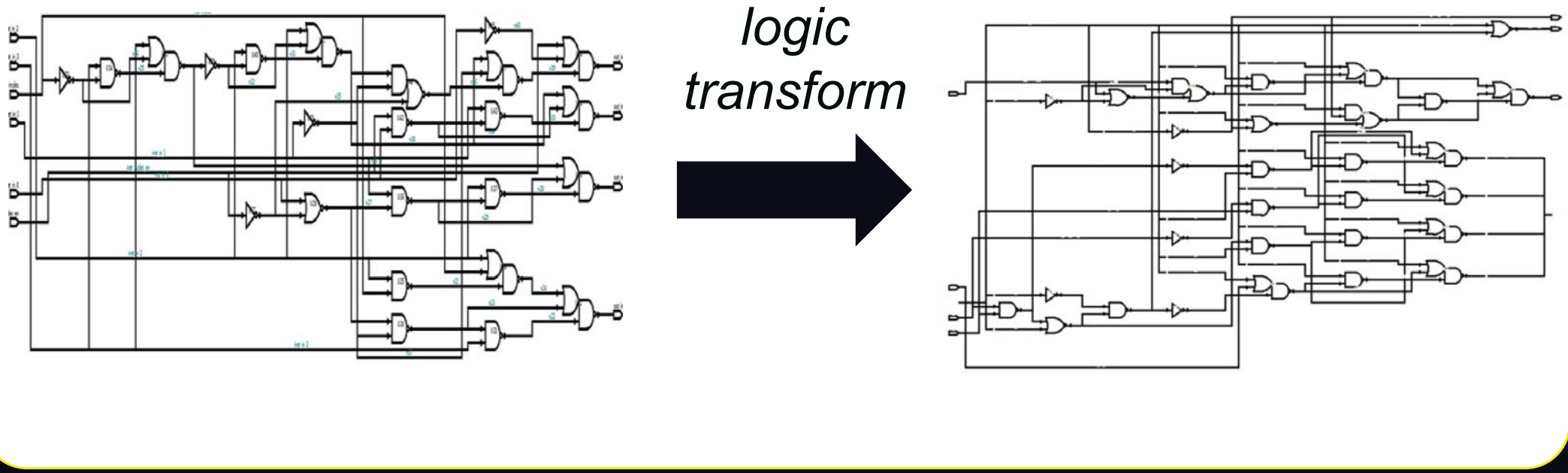
- m-CNTs degrade <u>specific combinations</u>



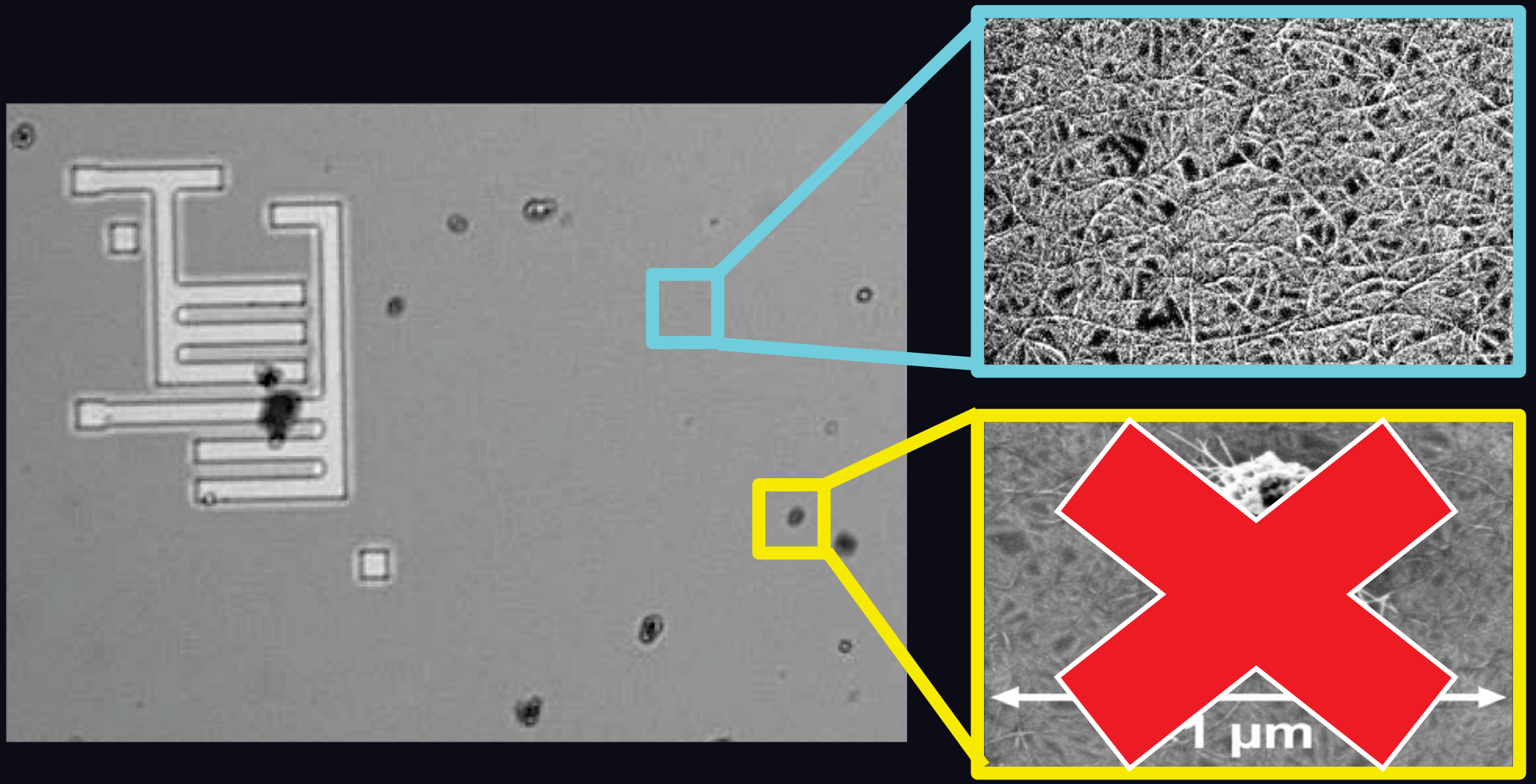
Yield = (1 – *PNMV*) for required SNM_R = VDD / 8

The “DREAM” Technique

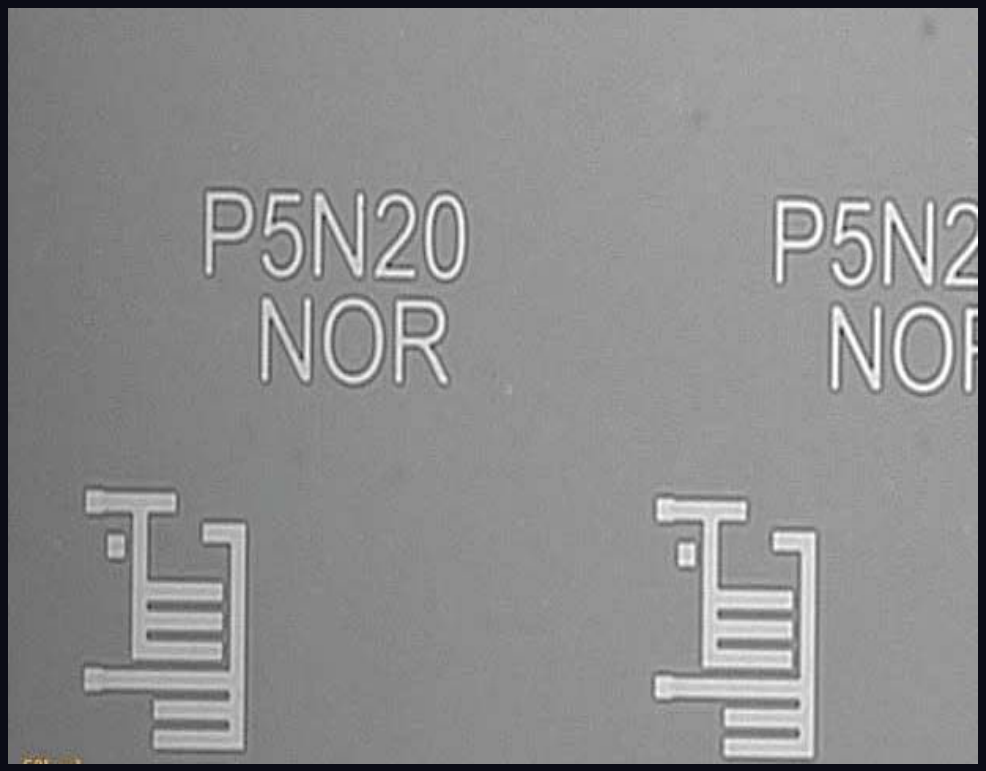
- Elegant solution:
  - apply logic transformation to avoid bad combinations
  - any arbitrary logic



Manufacturing Defects



Selective Exfoliation



- >250 × reduction in defects
- No damage to remaining CNTs

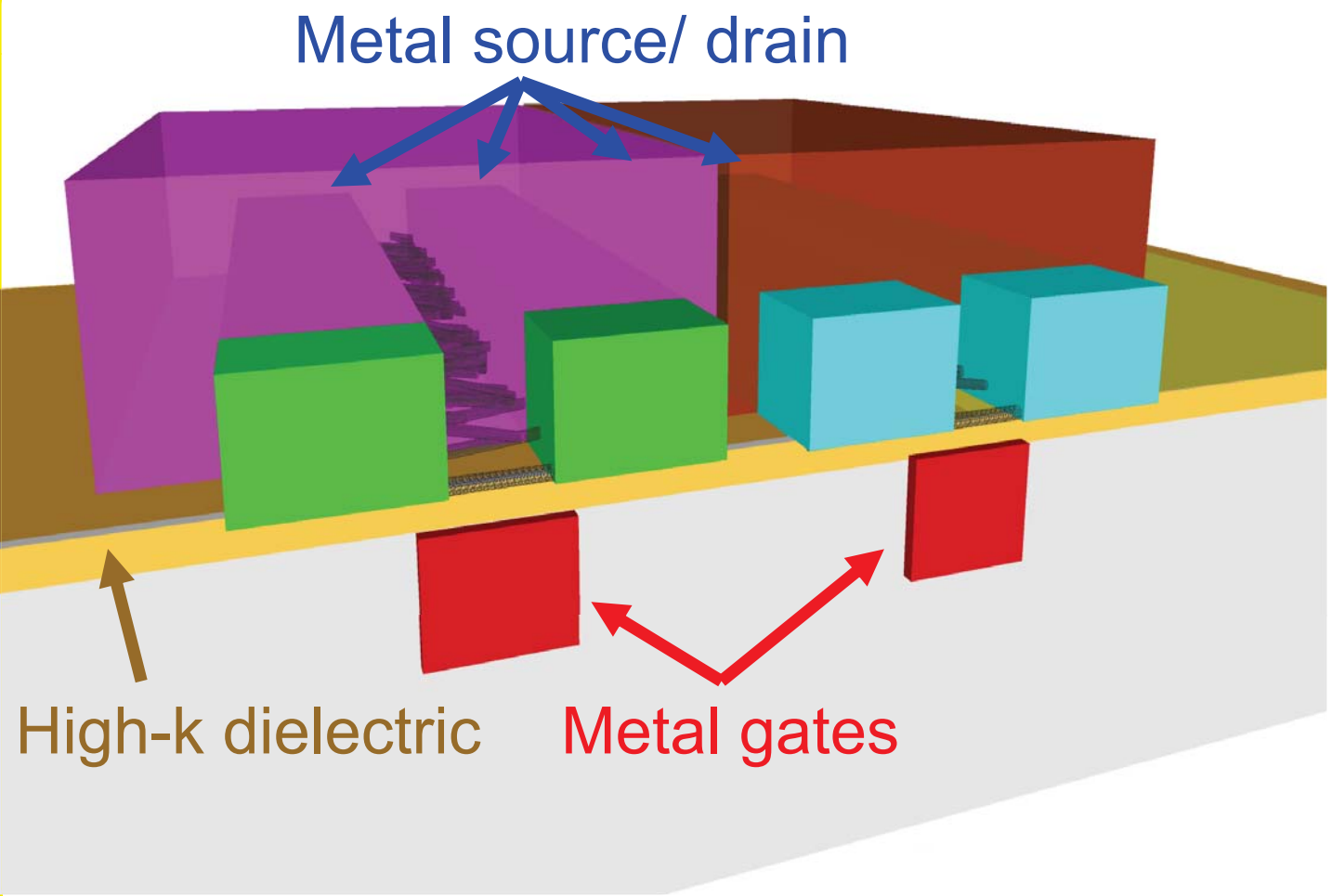
MIT, Nature ‘19

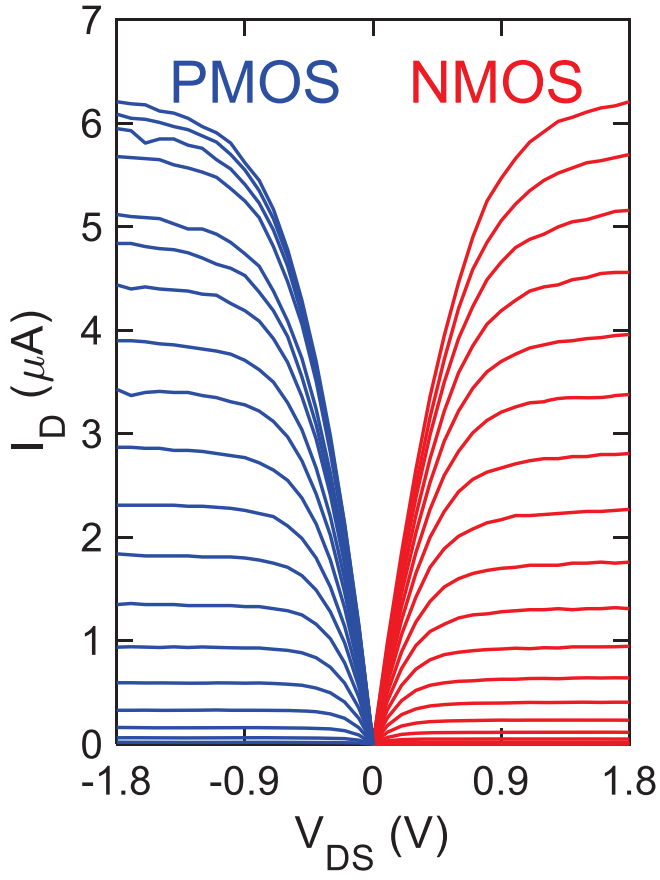
CNFET CMOS: P-type and N-type

- Major challenge:
  - solid-state + air-stable
  - silicon compatible + existing equipment
  - Reproducible + robust

CNFET CMOS: IN THE LAB

- Work function engineering + electrostatic doping



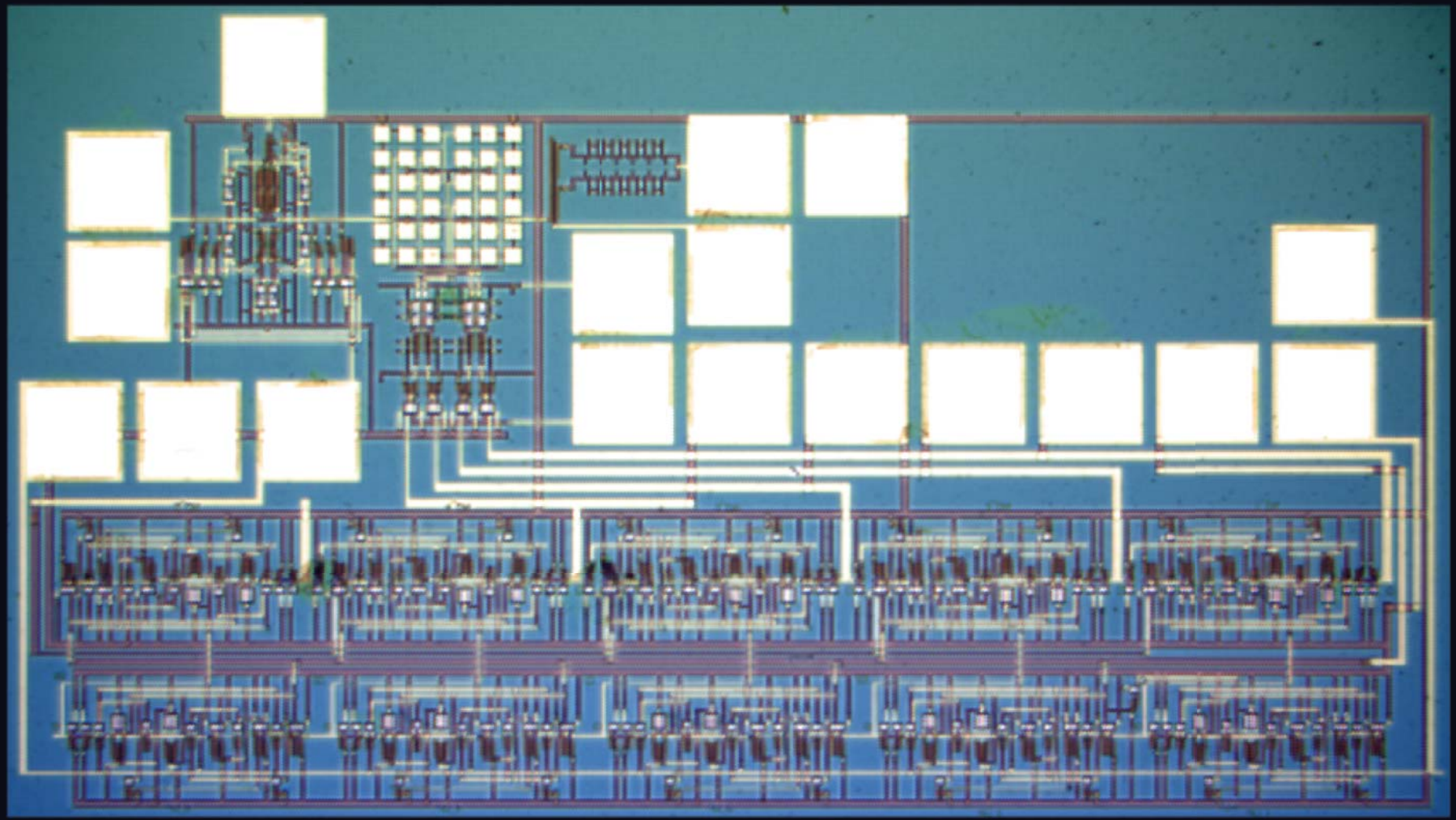


Most Importantly

- Combined processing + design solutions
  - Essential
- VLSI processing
  - No per-unit customization
- VLSI design flow
  - Immune CNT library

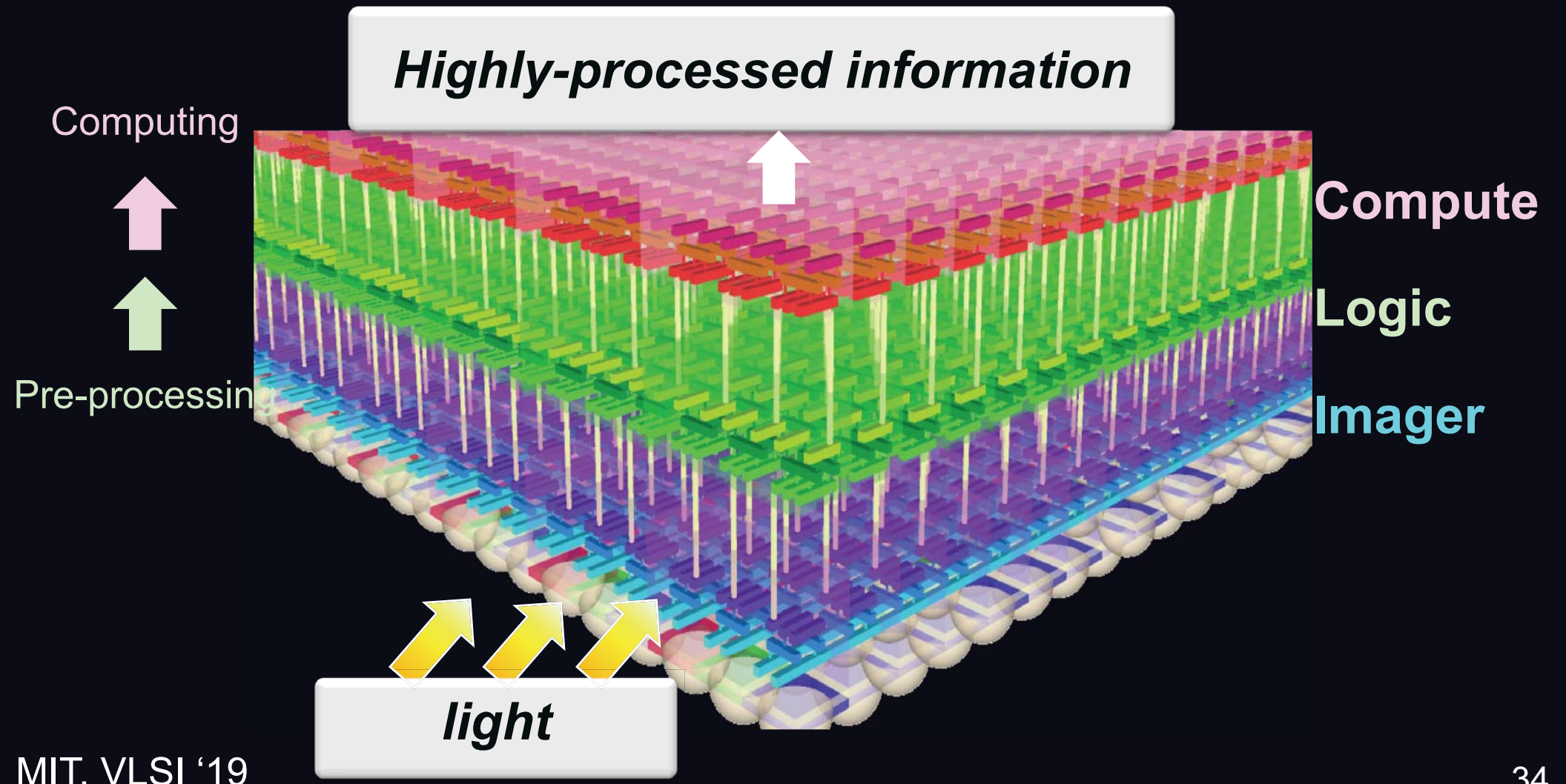
World's First: CNFET CMOS Analog + Mixed signal

SAR ADC (~100s CNFETs)



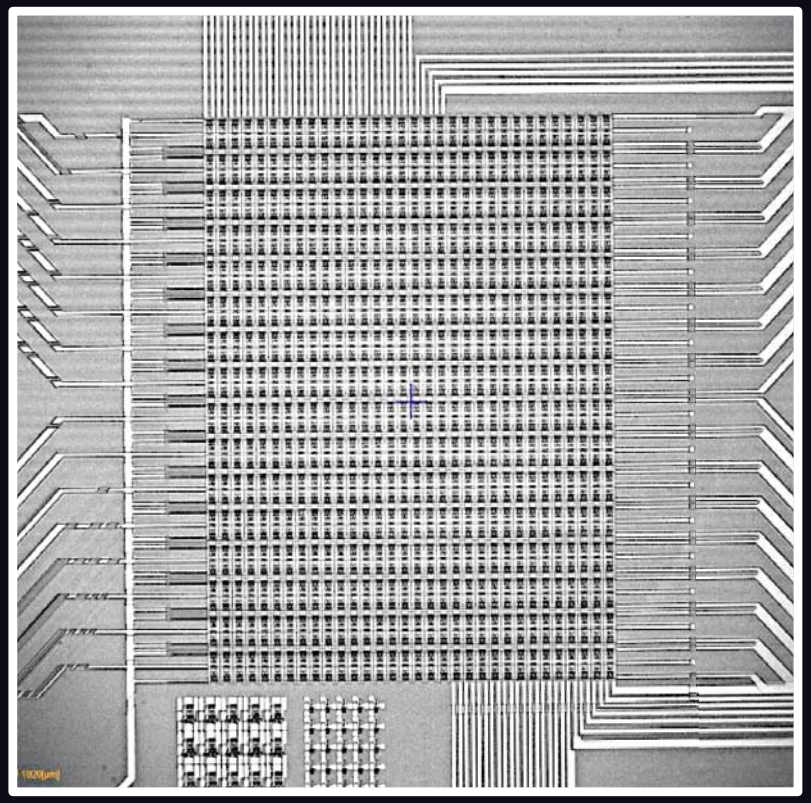
World's First: Monolithic 3D Imager

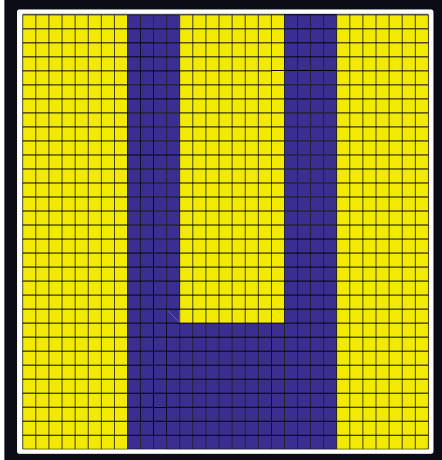
Transforms Raw Data ➔ Information (~2800 CNFETs)

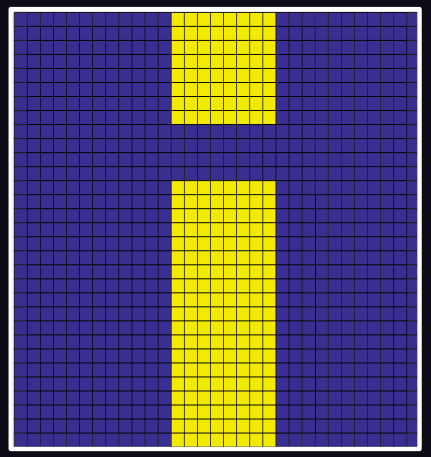


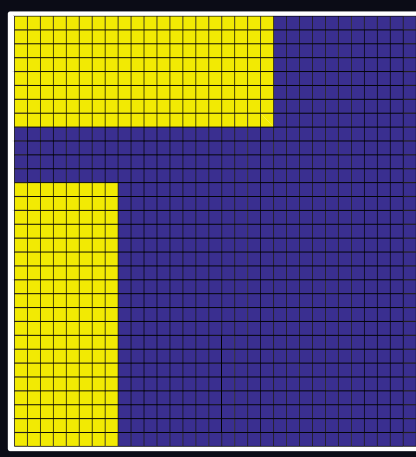
World's First: CNFET CMOS SRAM

Kbit SRAM (>6K CNFETs)

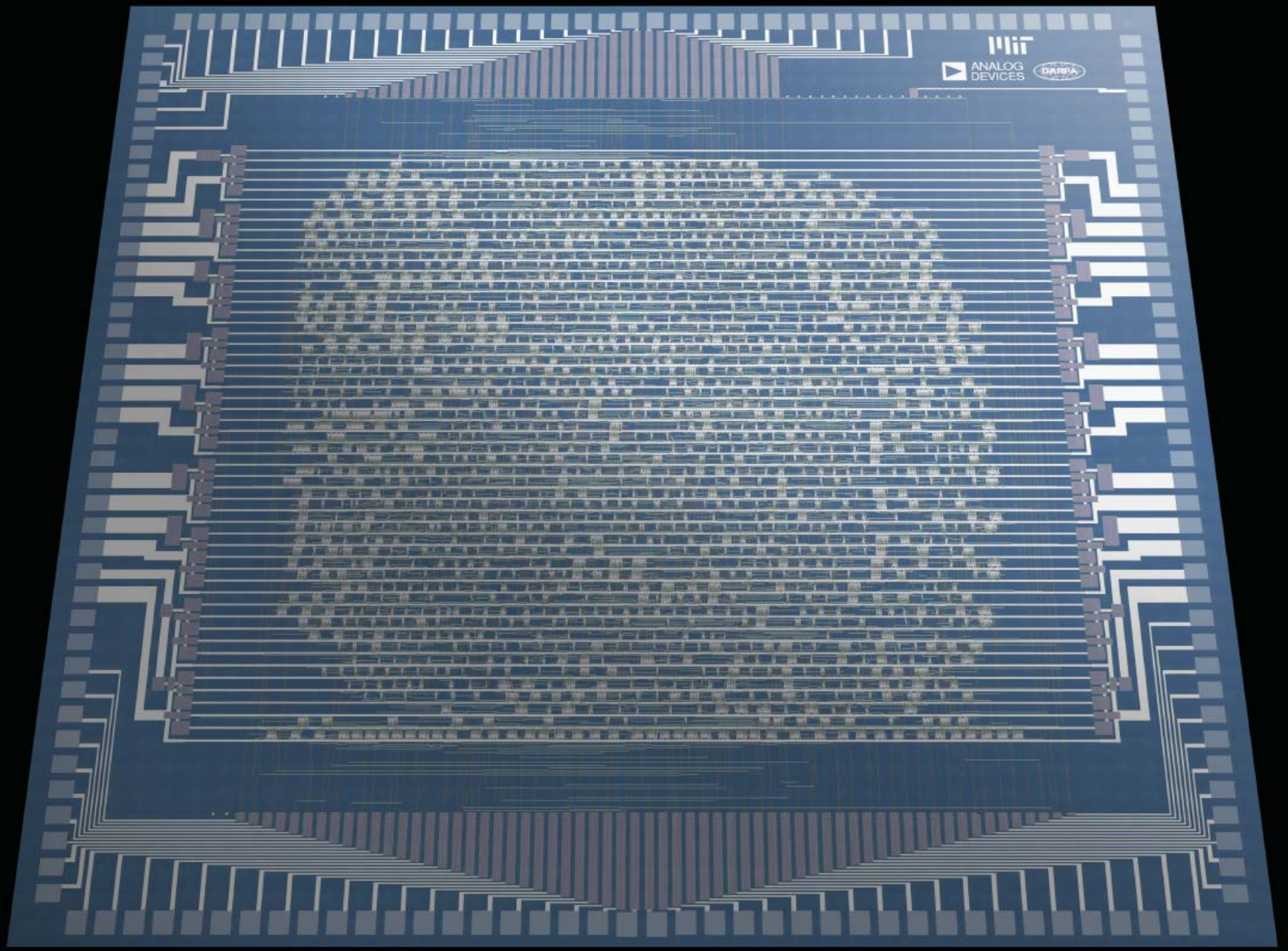




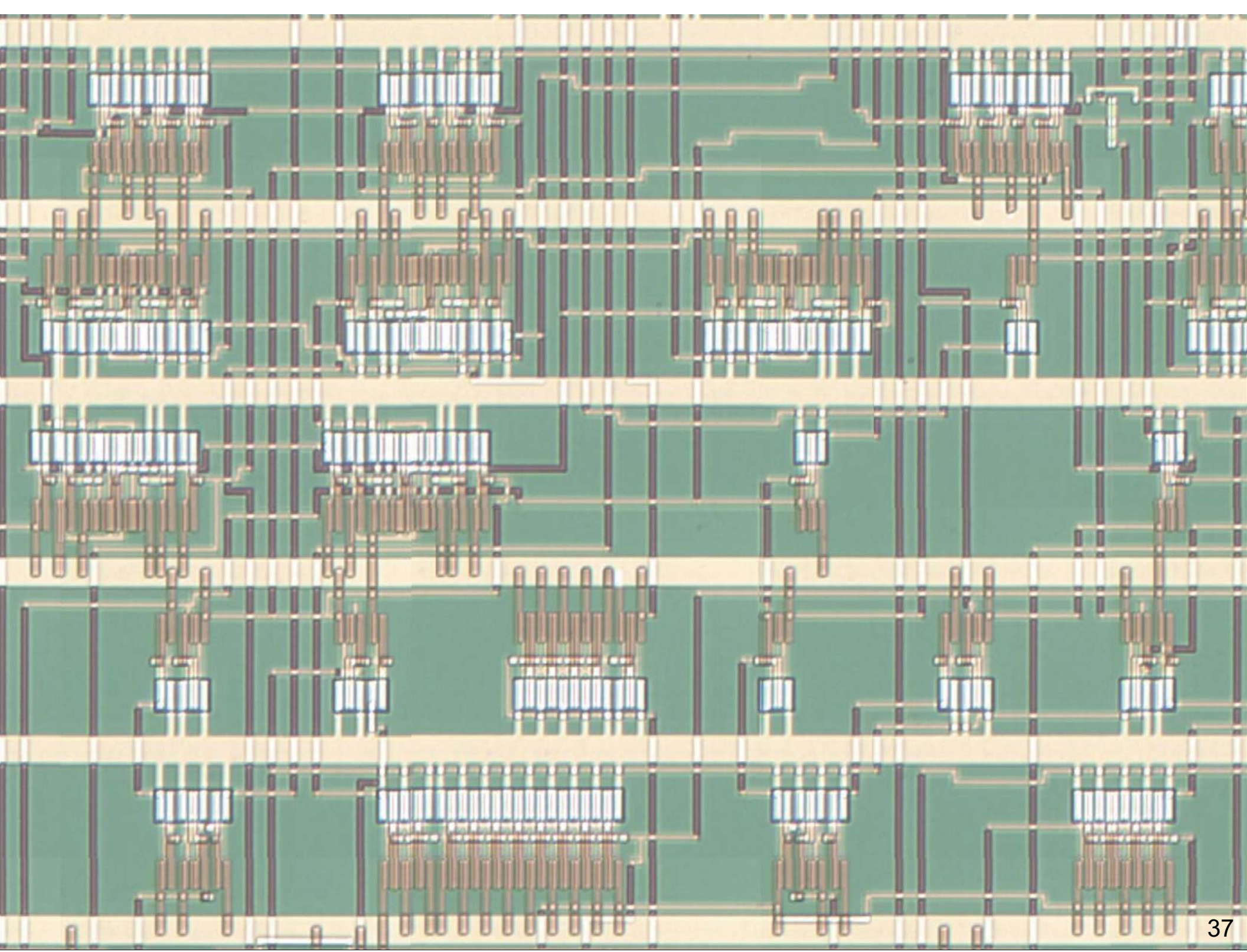




RISC-V Modern Microprocessor



MIT, Nature ’20. Collaborators: Arvind, Anantha Chandrakasan



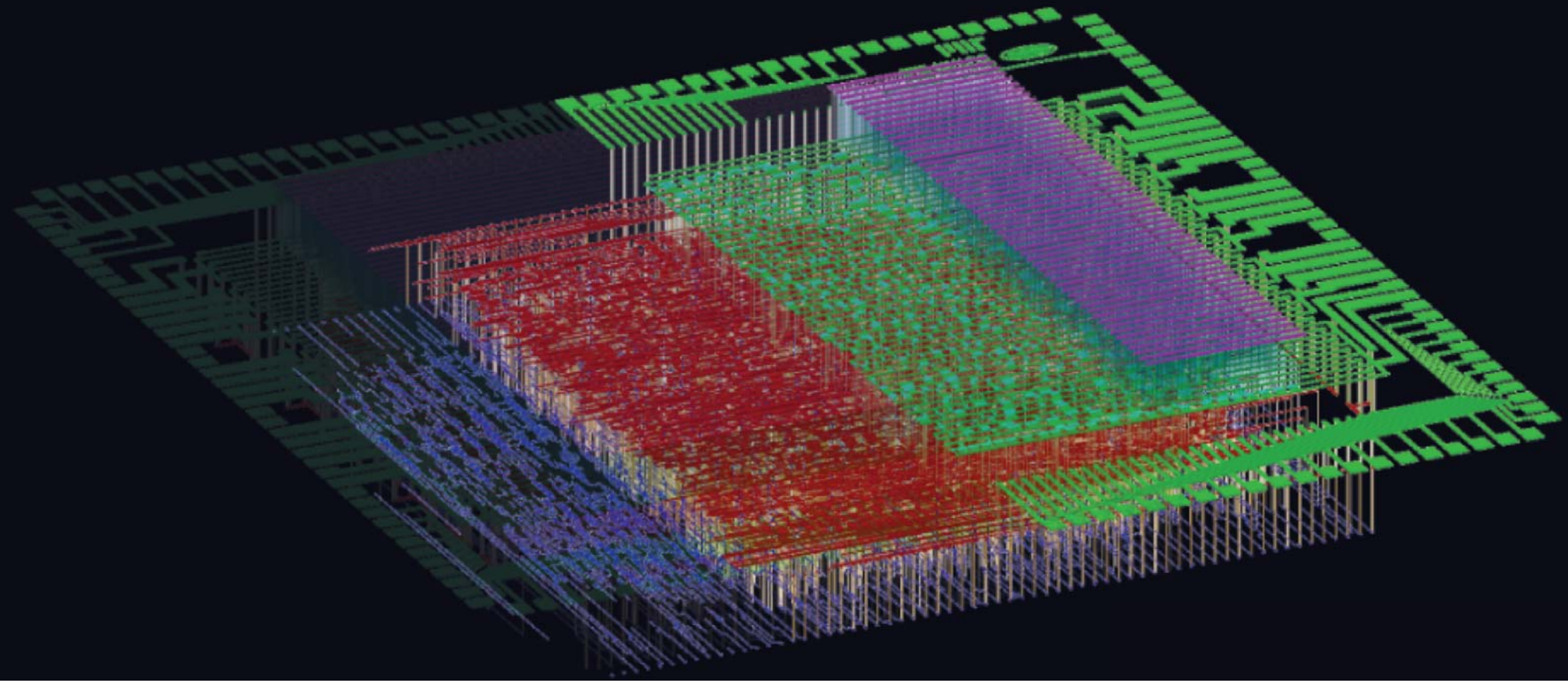
RV16X-NANO

- RISC-V processor
  - >14,700 PMOS + NMOS CNFETs
  - 32-bit instructions, 16-bit data
- VLSI compatible
  - Wafer-scale fabrication
  - Industry standard design tools

MIT, Nature ’19. Collaborators: Arvind, Anantha Chandrakasan

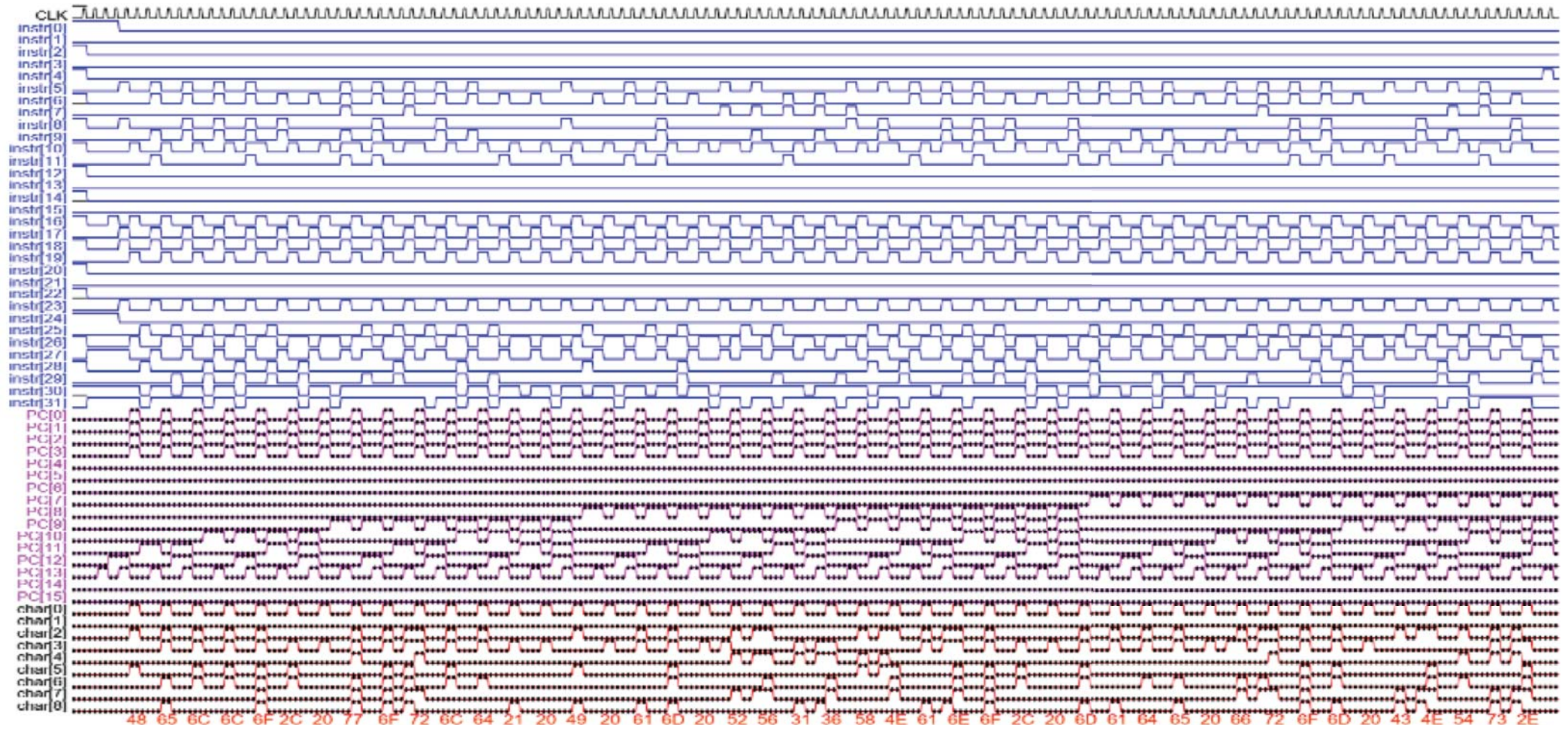
RV16X-NANO

- Industry-practice VLSI design flow
  - Calibrated compact models, PDKs, libraries
  - Enabled by emerging nano-design



RV16X-NANO

Measured Waveforms



RV16X-NANO

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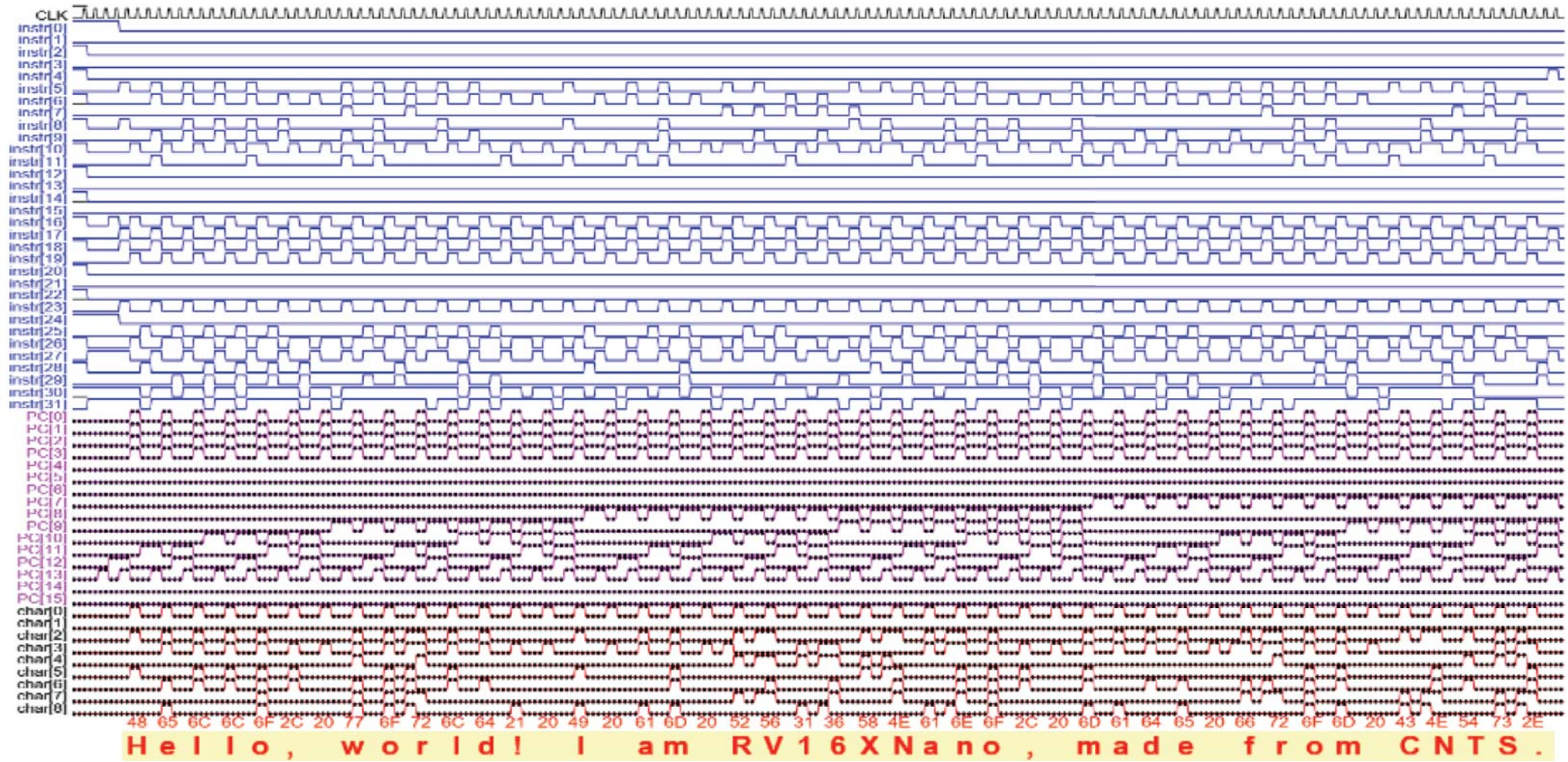


Key Take-Aways

- Wafer-scale
  - 150 – 200 mm wafer substrates
- Silicon CMOS compatible
  - Existing infrastructure (fabrication + design)
- Achievable *today*
  - combined processing + design solutions

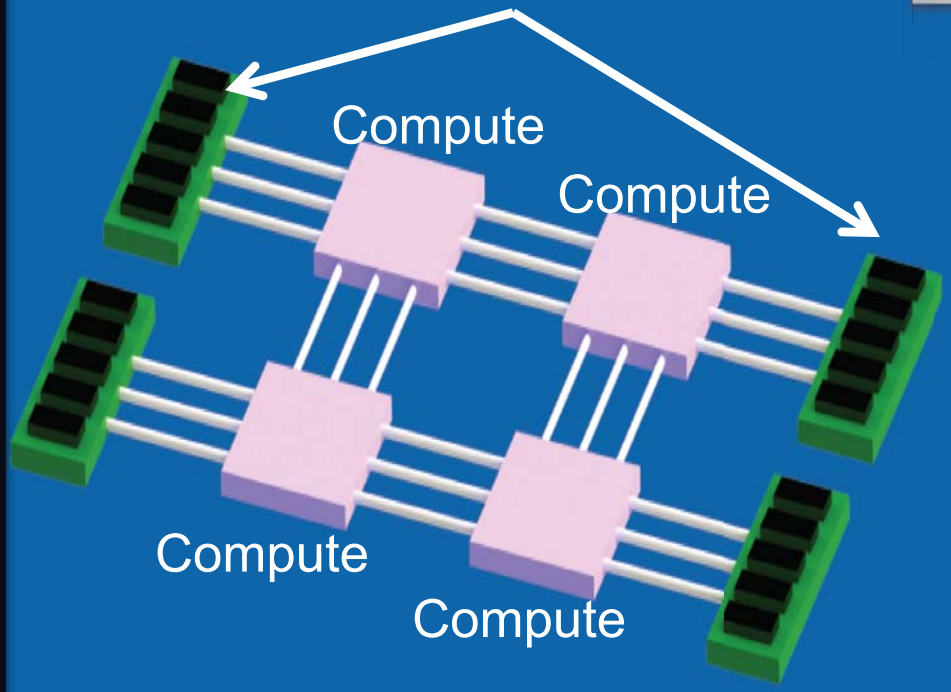
Transferring Into Commercial Foundry

Transferring Into Commercial Foundry

- SkyWater Technology: D.M.E.A. U.S. Foundry
  - Leveraging nanosystem PDK, DREAM, etc.
- DARPA 3DSoC (Electronics Resurgence Initiative)

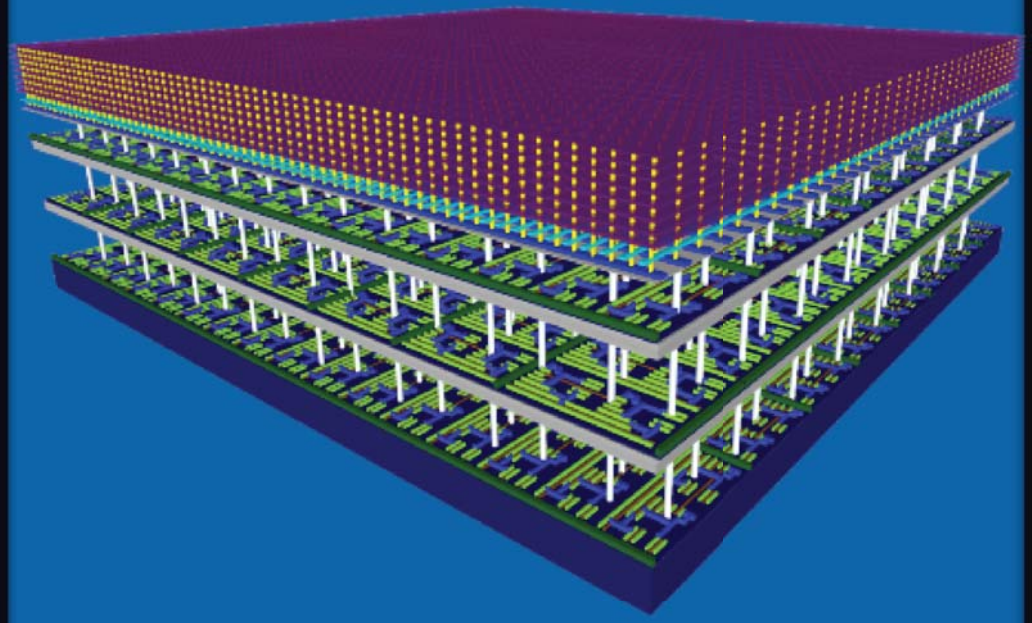
Three-Dimensional System-on-a-Chip (DARPA 3DSoC)

Baseline System



silicon + off-chip DRAM

3D Nanosystem

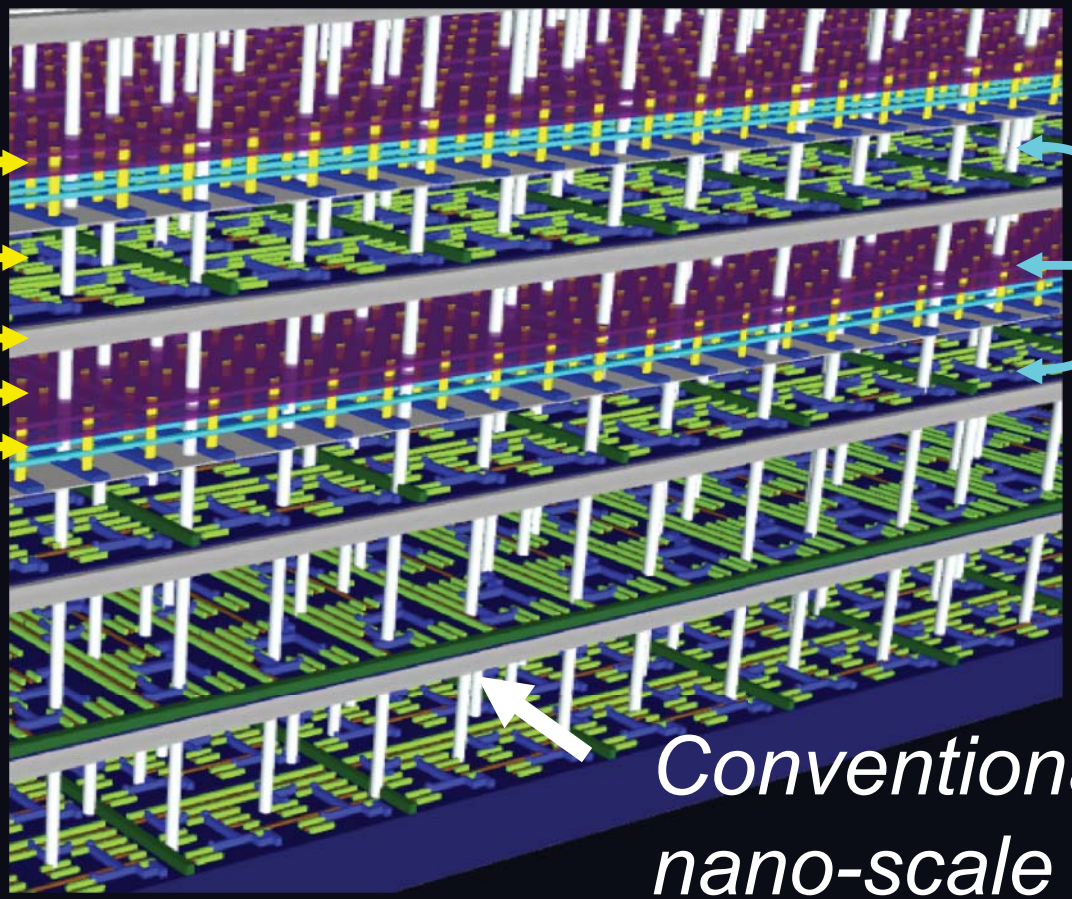


new tech. + monolithic 3D

Collaborators: Stanford University

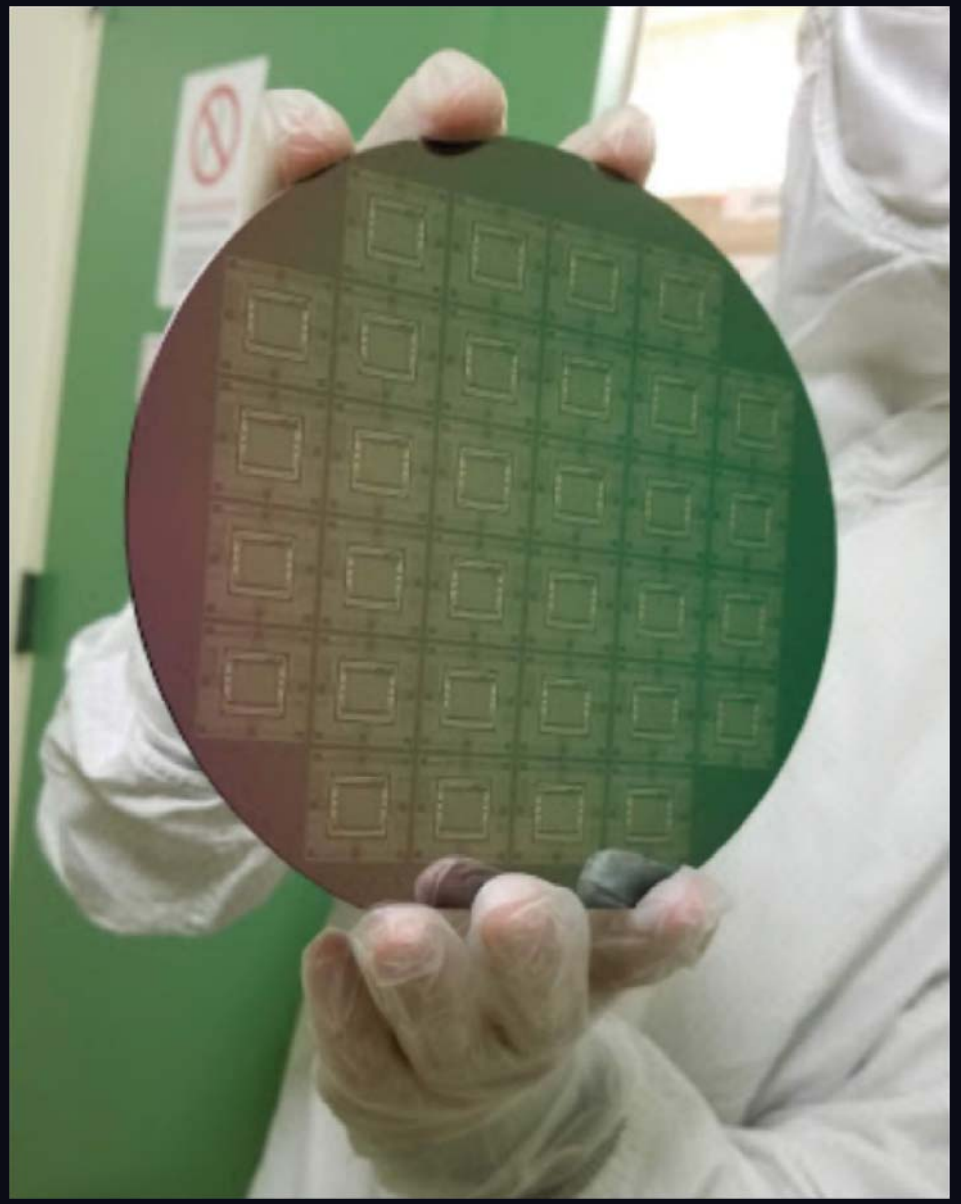
3DSoC: Our Approach

- **Monolithic 3D Integration:**
  - Fine-grained integration: logic + memory



Technology Transfer: U.S. Foundry

- **All process modules**
  - CNFETs + RRAM + 3D
- **Foundry MPWs**
  - End-to-end design tools
- **Wafers running today**



Acknowledgements

DARPA

ANALOG DEVICES

AIR FORCE RESEARCH LABORATORY

ARL

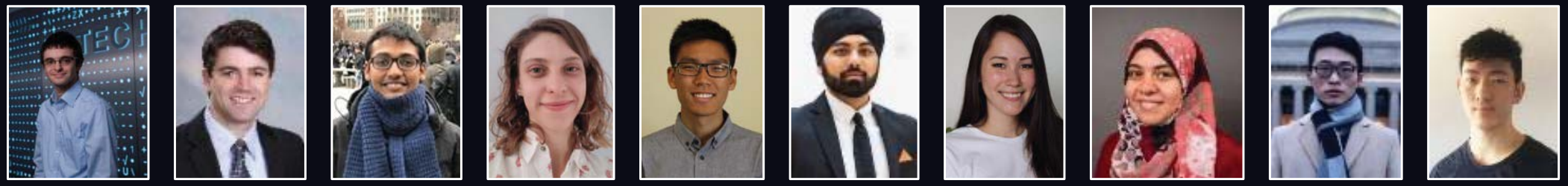
MEDRC
MEDICAL ELECTRONIC DEVICE REALIZATION CENTER

MGH 1811

NSF

SAMSUNG

Novel Electronic Systems (NOVELS) Group at MIT:

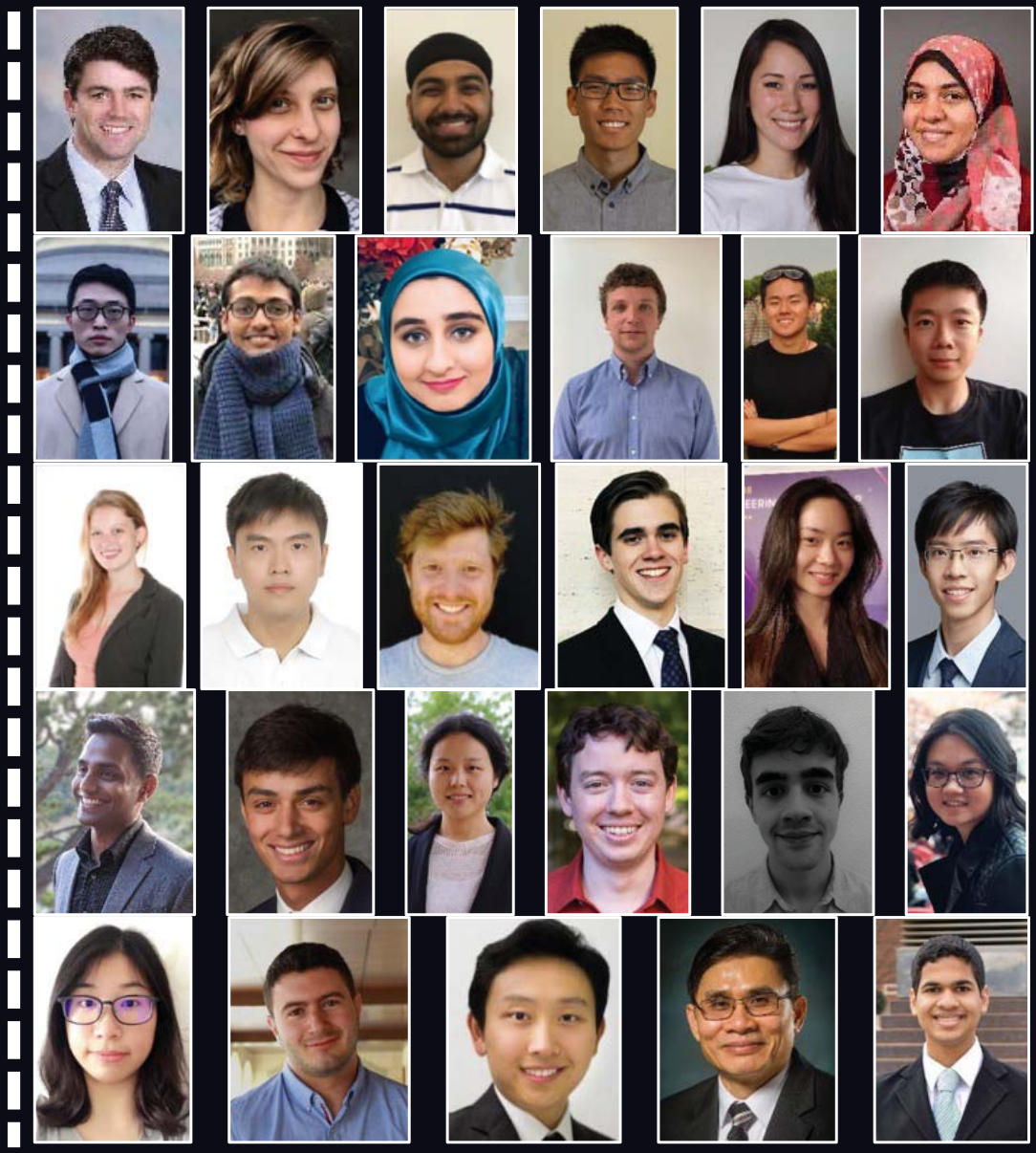


Acknowledgements

DARPA ERI 3DSoC







Thank you