ALiGN

Machine Learning Techniques in Analog Layout Automation

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✧ Intel Labs

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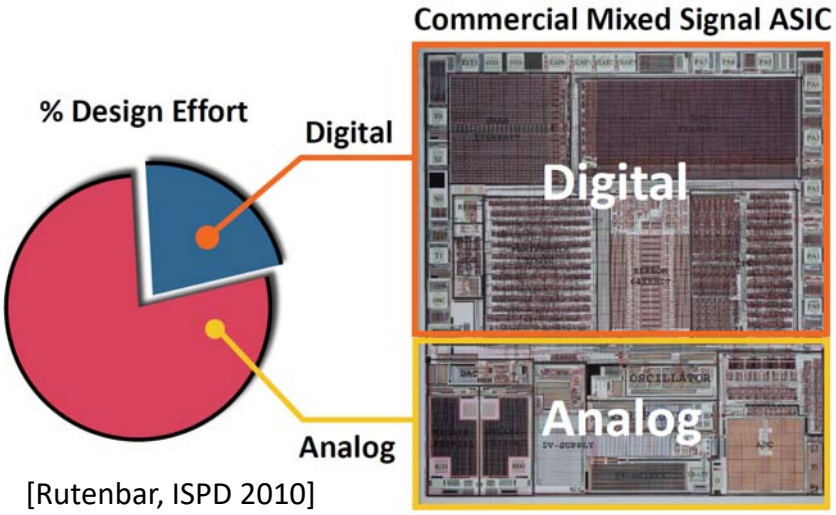
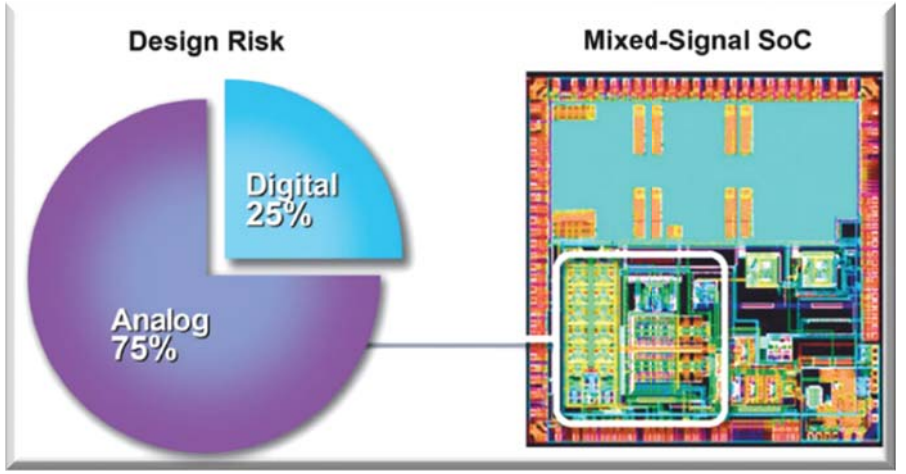
The criticality of analog circuits



[Rutenbar, ISPD 2010]



[Mentor, via semiengineering.com]

EDA360 Insider

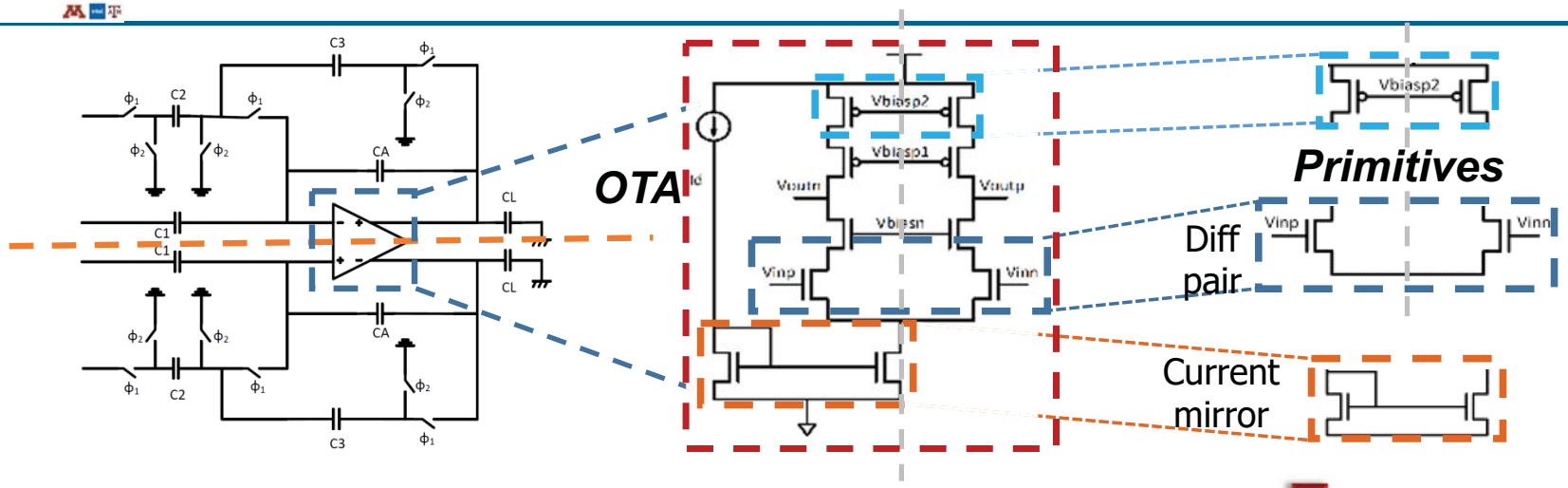
70% of re-spin issues are AMS in nature: How mixed-signal design can mess up a perfectly good SoC

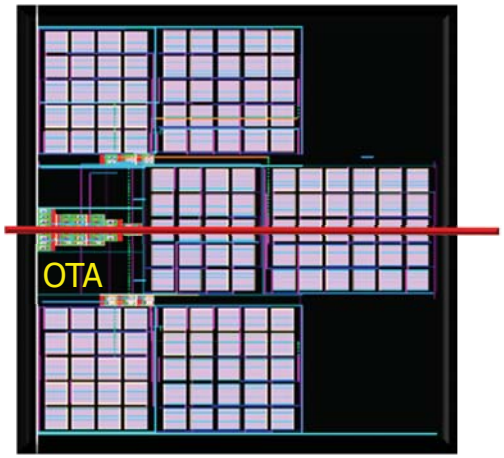
[https://eda360insider.wordpress.com]

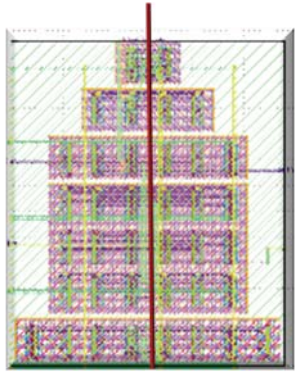
ALIGN = Efficient, automated high-quality layout synthesis

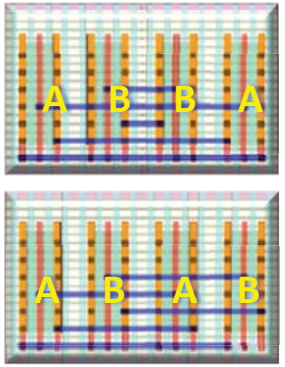
[Kunal *et al.*, DAC19; Dhar *et al.*, IEEE D&T]

Using the ALIGN layout generator on a switched capacitor filter







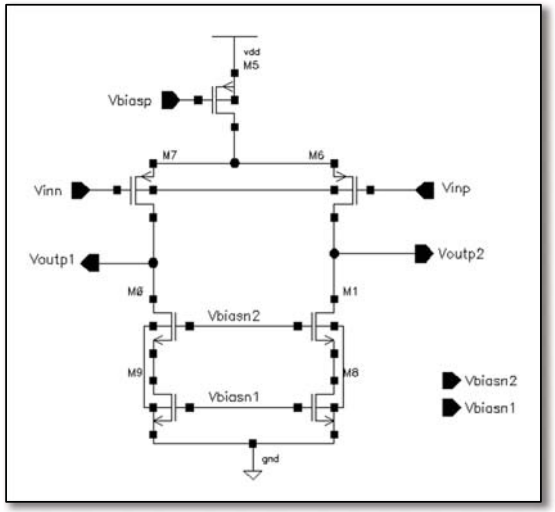


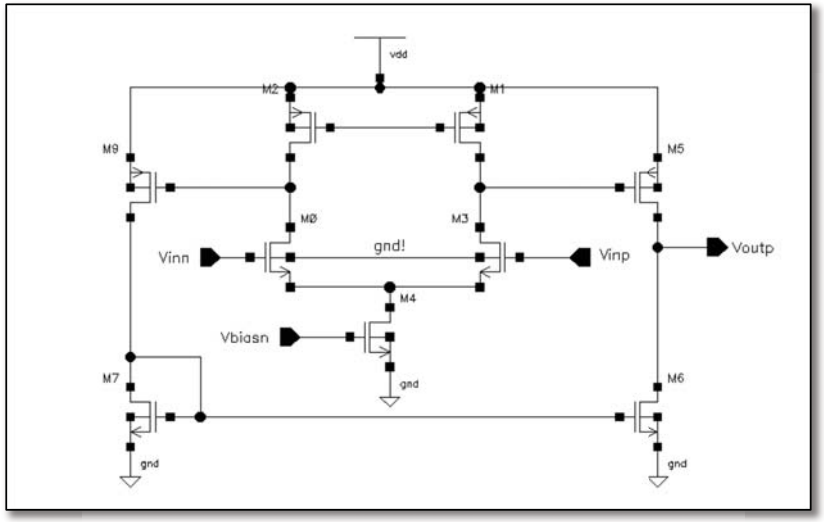
Design rule abstraction (PDK)

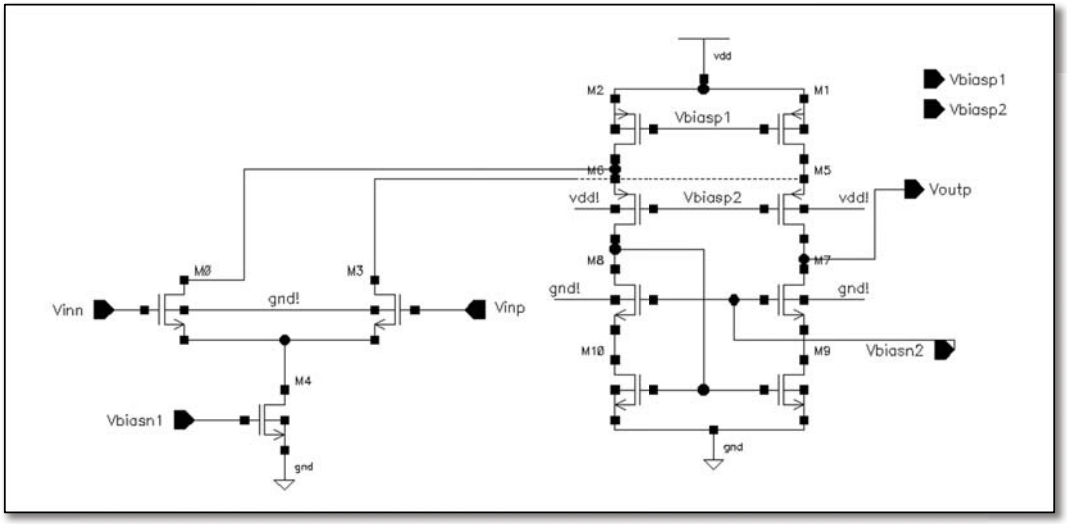
ALiGN

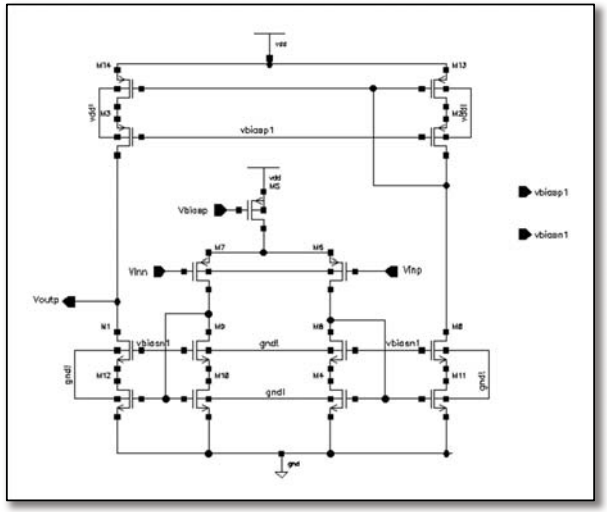
Application 1: Circuit auto-annotation

Recognizing components is hard: Example OTA layouts

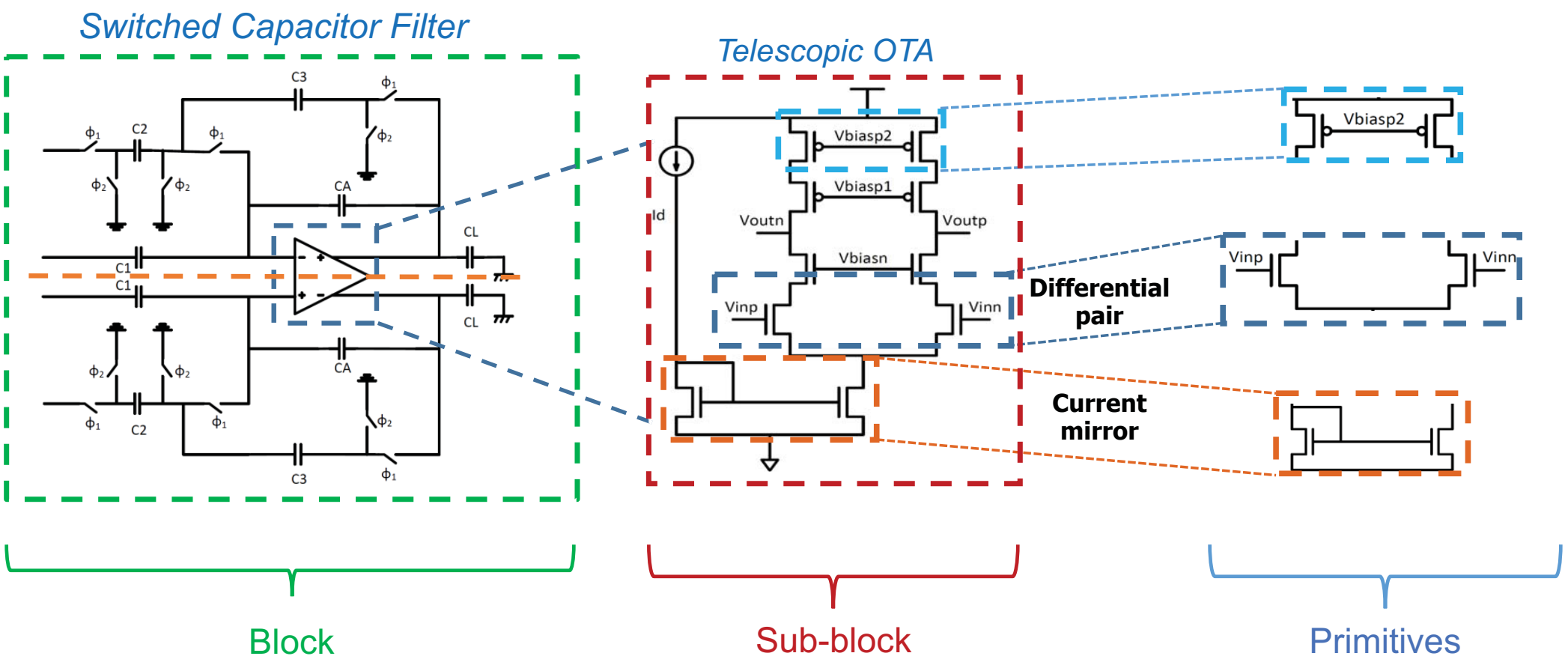






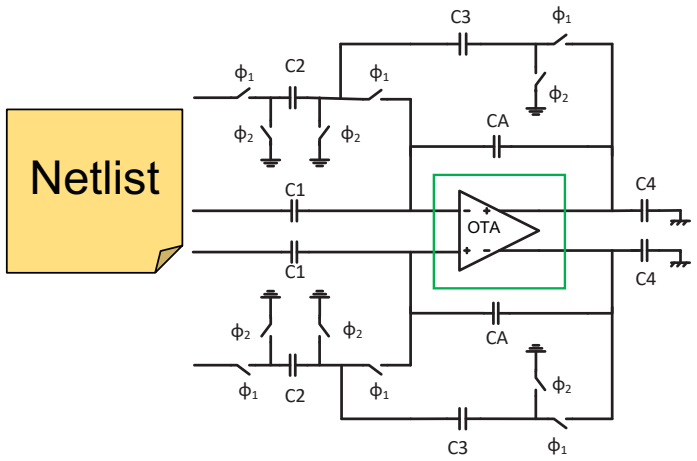


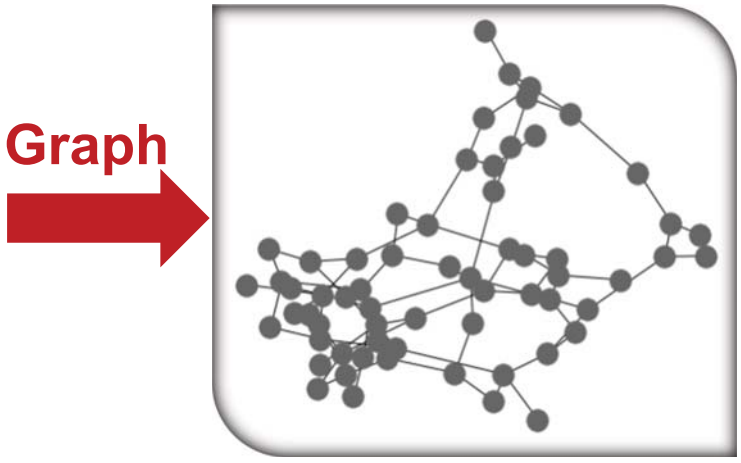
Recognizing sub-blocks in switched capacitor filter

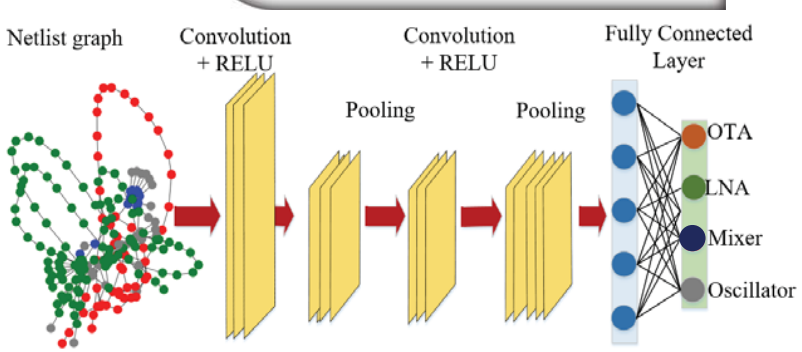


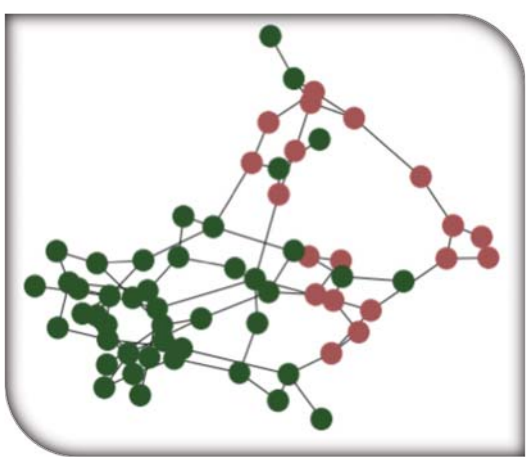
Recognizing sub-blocks in switched capacitor filter

- Model the circuit netlist as a graph and perform approximate subgraph isomorphism
- Graph convolutional networks (GCN) for graph-structured data







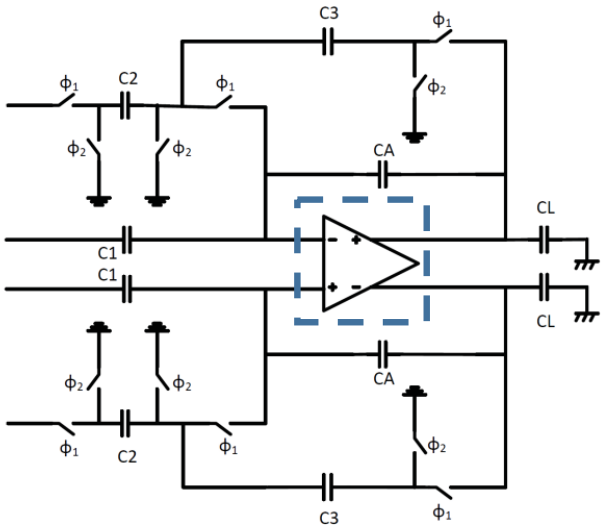


Node features:
- Device/net info
- Connection type

Frequency-domain graph convolution [Defferrard et al., NeurIPS 2016]

[Kunal *et al.*, DATE20]

GCN-based recognition: Switched capacitor filter



Switched capacitor filter circuit

Actual class

Predicted class	OTA	BIAS
OTA	21	0
BIAS	1	35

Postprocessing

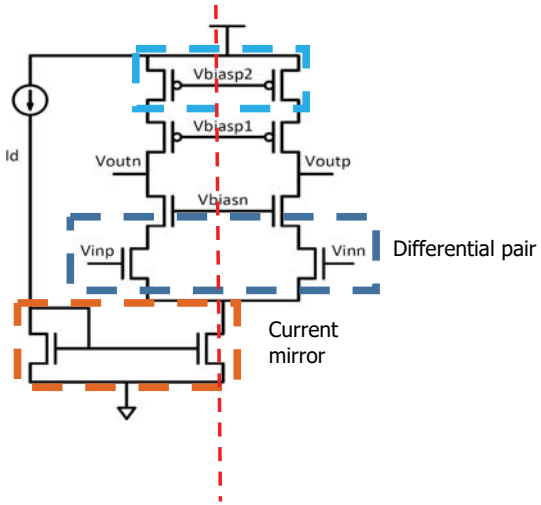
Actual class

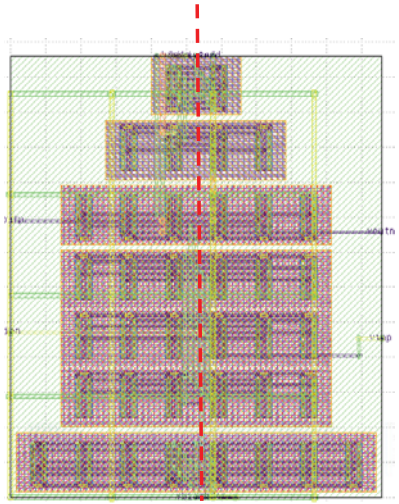
Predicted class	OTA	BIAS
OTA	22	0
BIAS	0	35

Layout based on annotated constraint

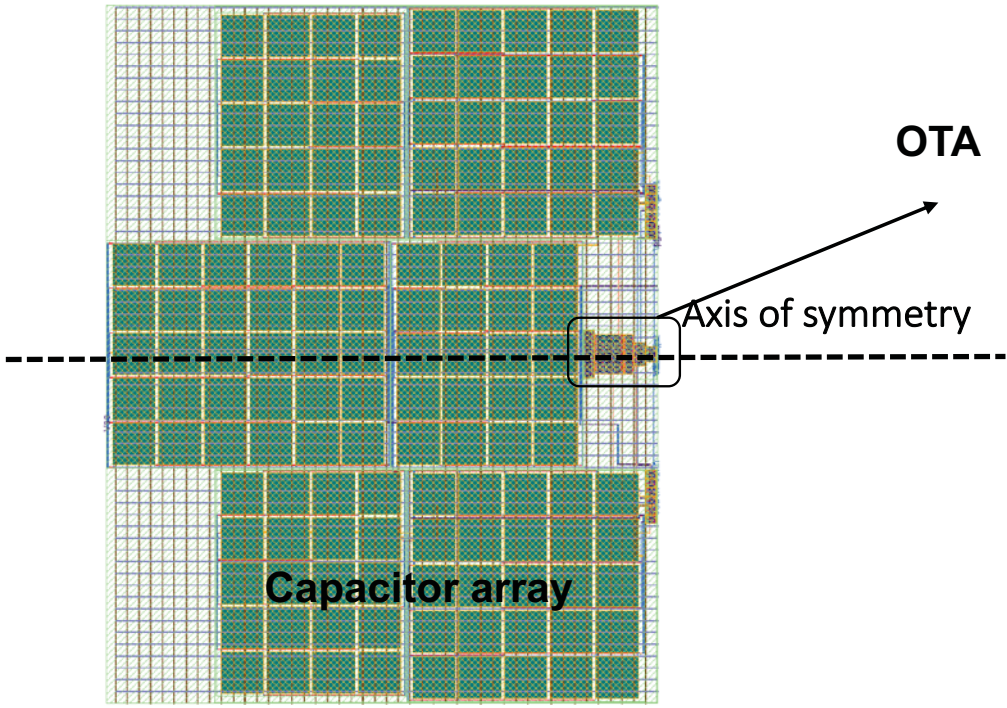
Annotated constraints

- Constraints on primitives
  - Differential pair (DP) → symmetry
  - Current mirror → matching
- Constraints on sub-blocks
  - OTA → symmetric about DP axis
  - C array → common centroid



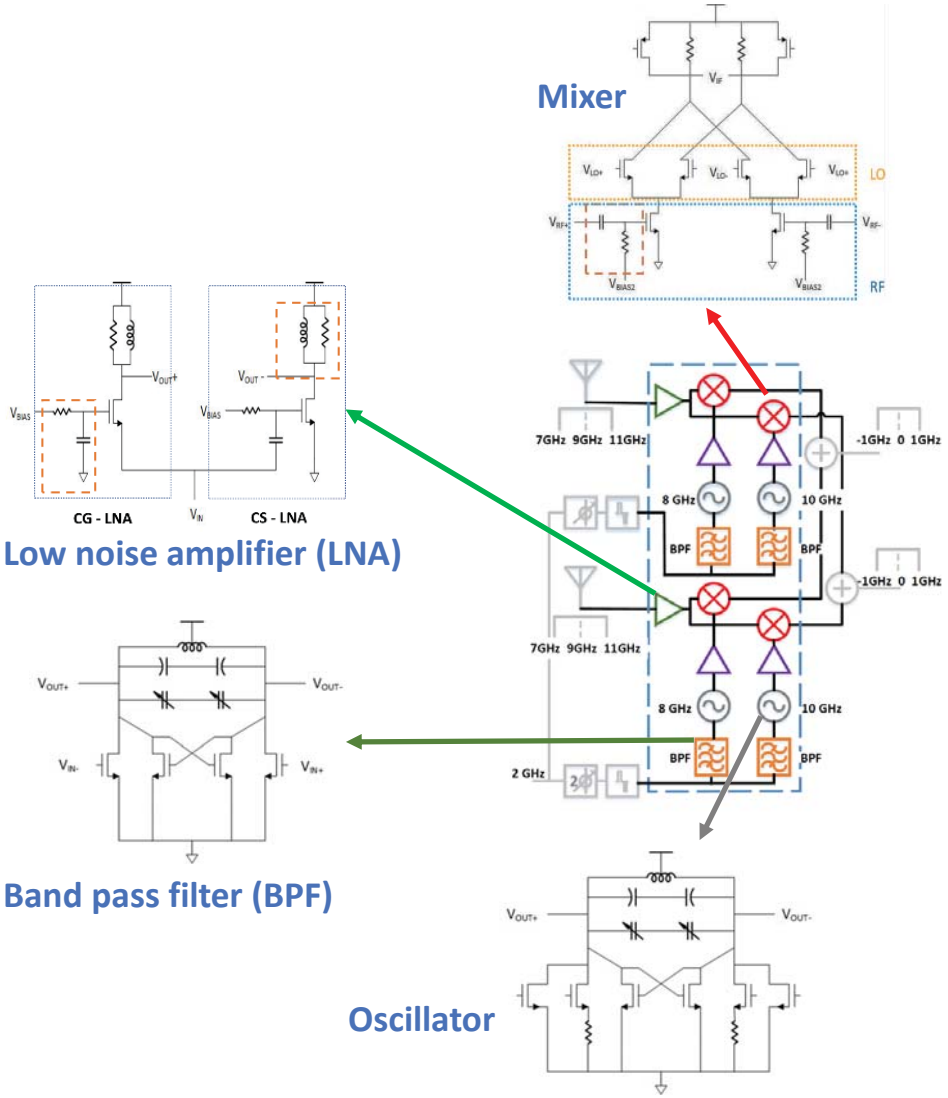


OTA



Switched cap filter

Phased array receiver



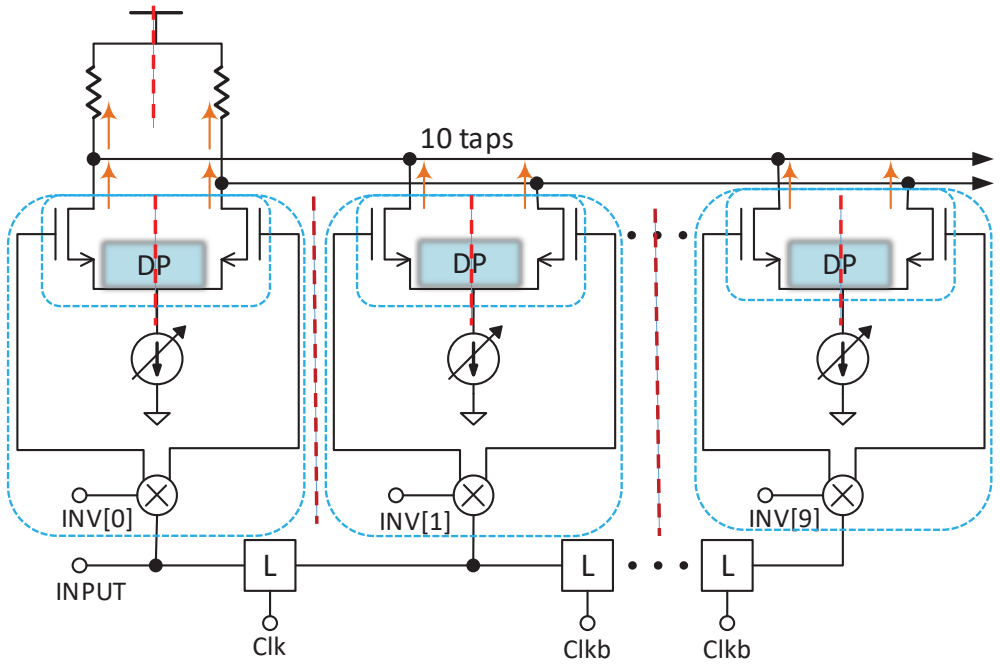
Actual class

Predicted class	LNA	Mixer	OSC	BPF	BUF	INV
LNA	78	0	0	0	0	0
Mixer	0	120	0	0	0	0
OSC	0	0	132	0	0	0
BPF	0	0	0	136	0	0
BUF	0	0	0	0	32	0
INV	0	0	0	0	0	24

Classification results after postprocessing

Approach 2: Annotation and hierarchical symmetry detection

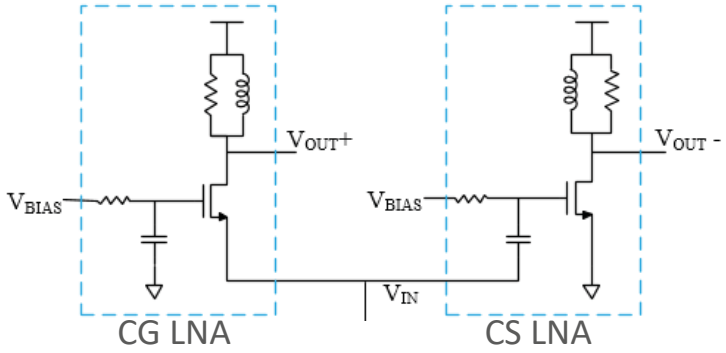
- Can be applied without a training set
- Bottom-up approach
- Multiple lines of symmetry
  - Identify matching blocks
- Multiple symmetry levels
  - Identify repeating structure
  - Create array hierarchy
- Matching between blocks
  - Instance type matching for primitives
  - Error-tolerant matching using graph edit distance (GED)



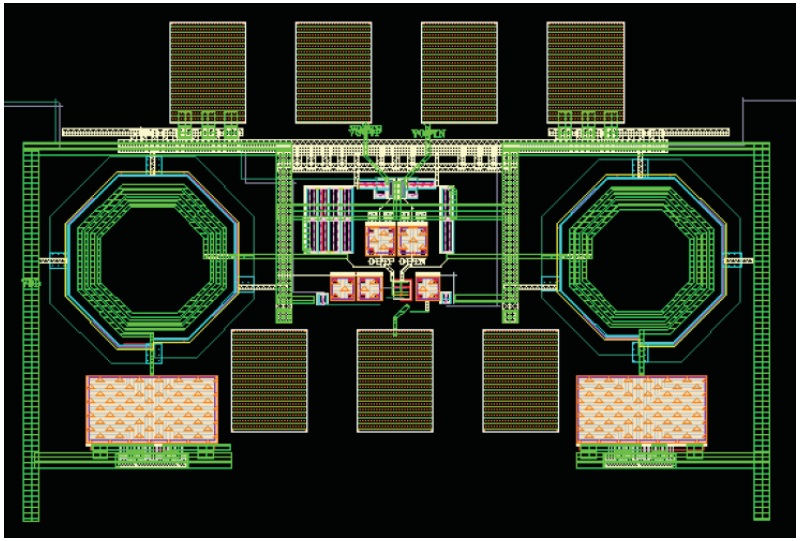
FIR equalizer

[Kunal *et al.*, ICCAD20]

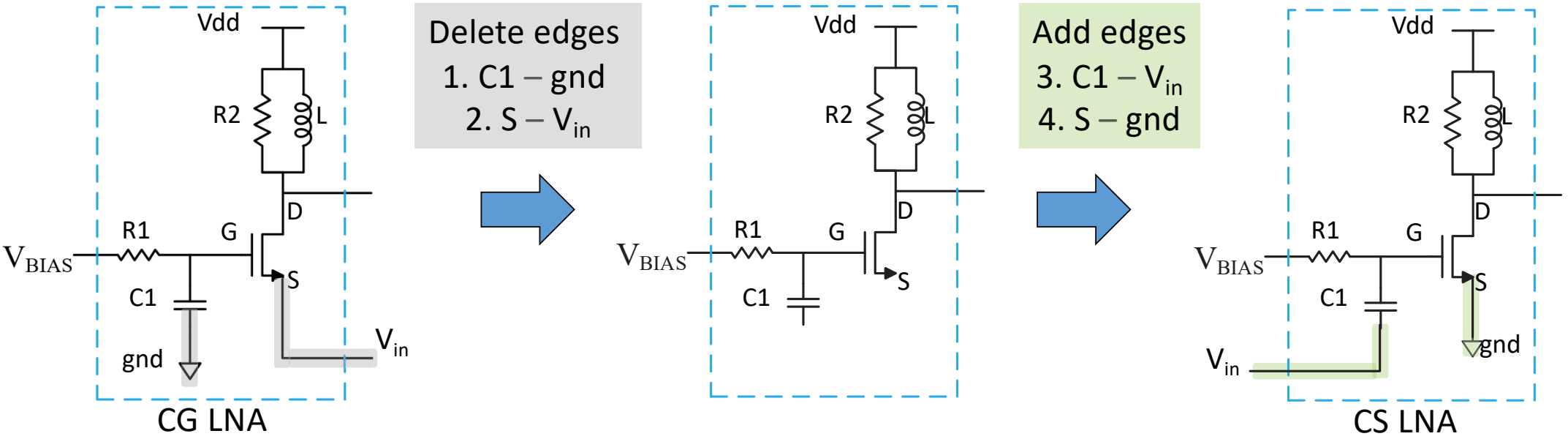
Error-tolerant matching



Differential LNA configuration



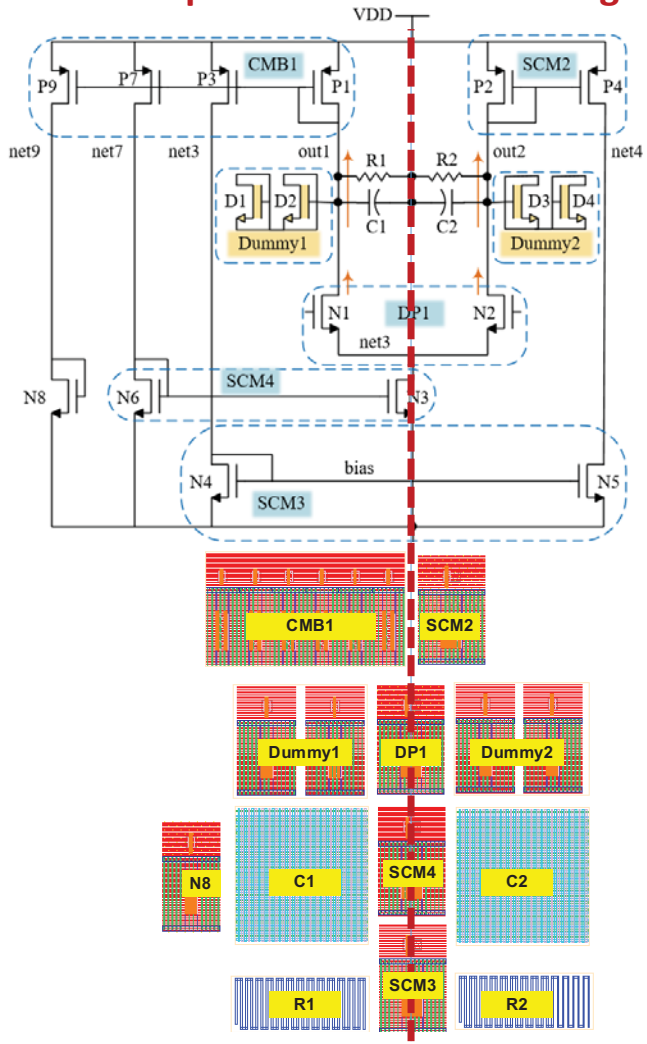
Graph edit distance (GED): An Example



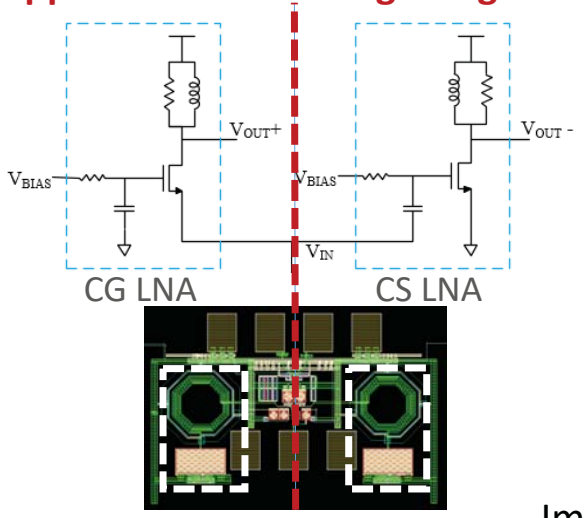
GED=4

Array recognition and geometric constraint annotation

Graph-based exact matching



Approximate matching using ML

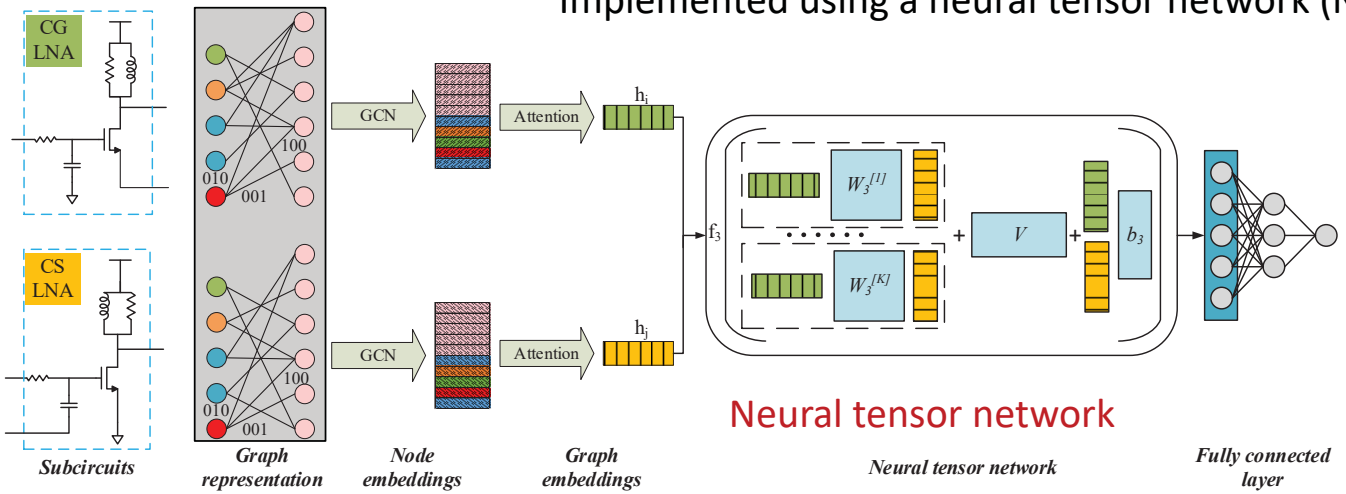


Auto-annotation requires recognition of

- Block structure
- Lines of symmetry
- Nested hierarchies

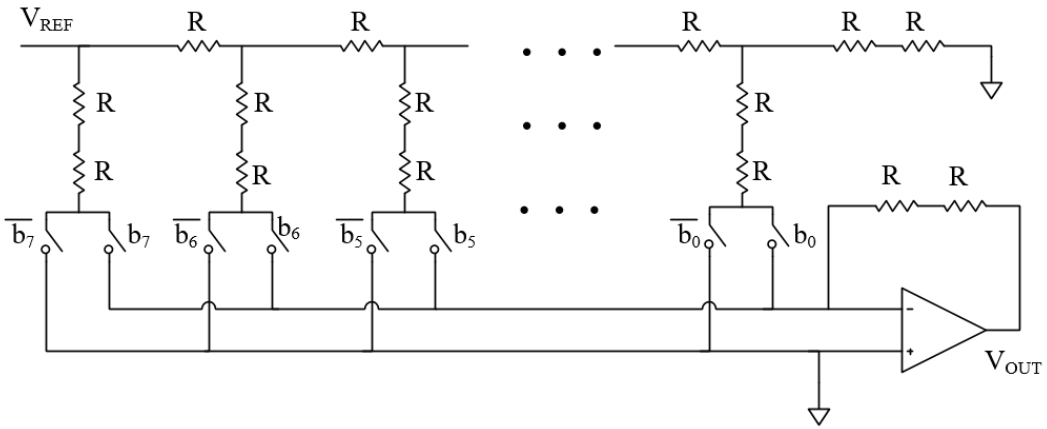
[K. Kunal *et al.*, ICCAD'20]

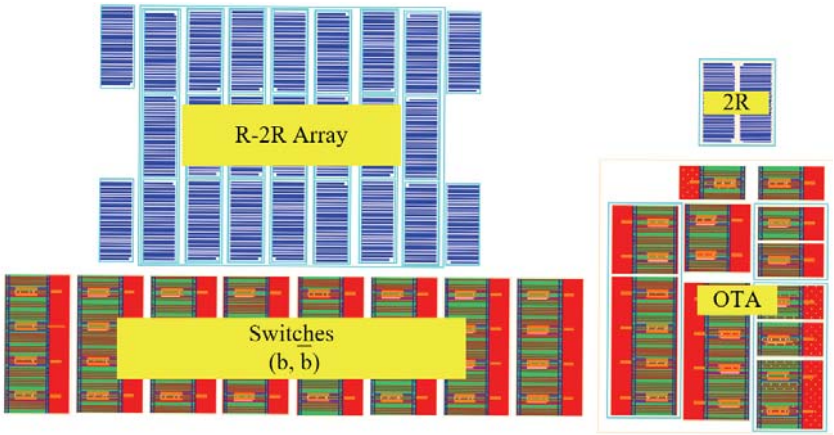
Identification of "graph edit distance"
Implemented using a neural tensor network (NTN)



From auto-annotation to layout

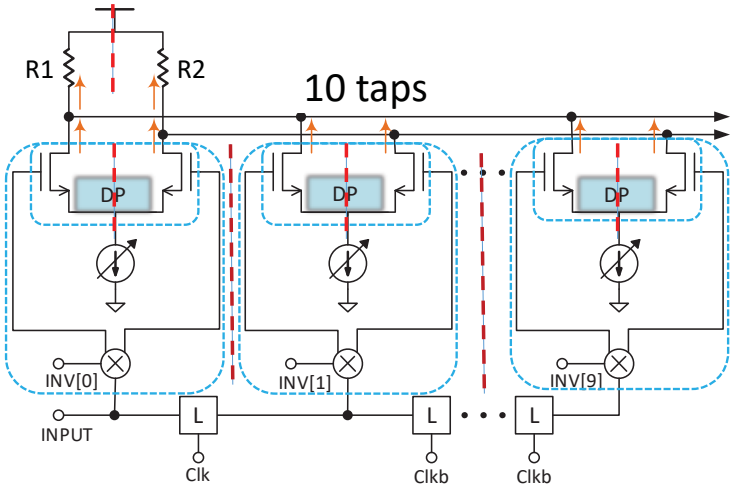
R-2R DAC

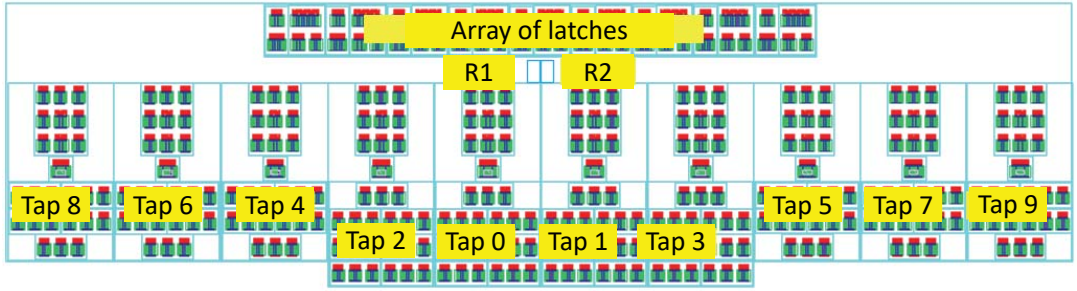




10-tap FIR Equalizer

- Taps symmetric wrt each other; wrt R1 and R2
- Approximate matching: 5-bit/7-bit current sources





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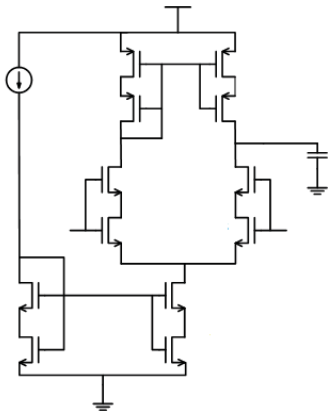
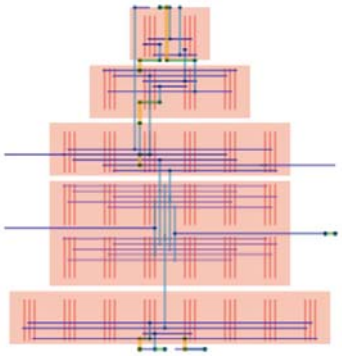
Application 2: Circuit Performance Optimization

Performance-driven placement guided by machine learning

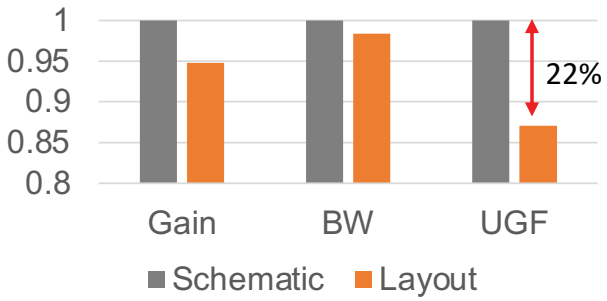
Telescopic OTA

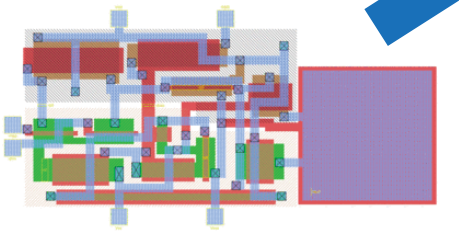


Schematic



Layout





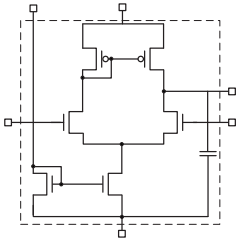
Analog IC placement

Machine learning

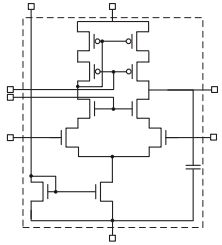
Performance good enough?

Approach 1: Constraint boundary discovery

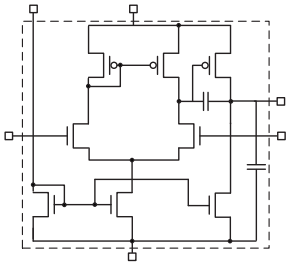
5T OTA

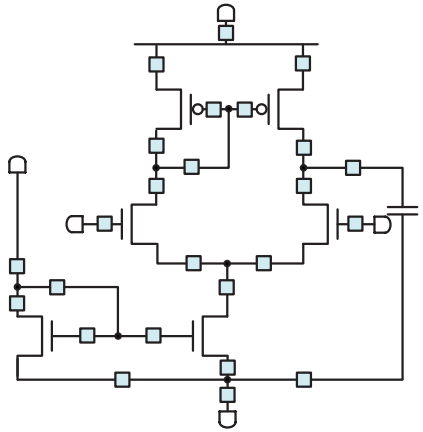


Telescopic OTA



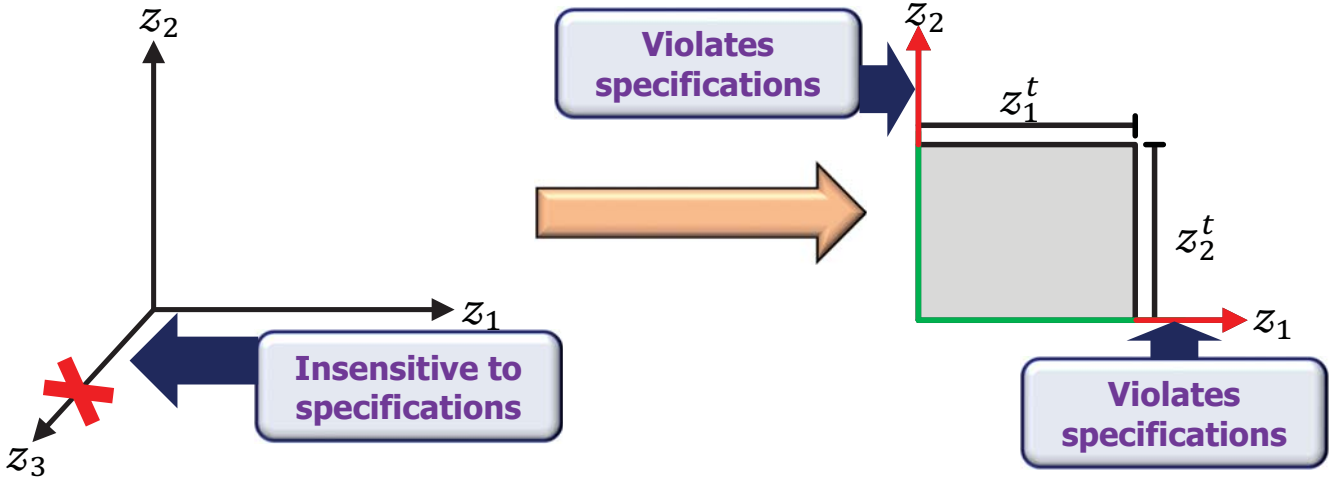
2-stage OTA





Performance / Specification	Critical values		
	5T OTA	Telescopic OTA	2-stage OTA
Gain (dB)	≥ 19	≥ 42	≥ 25
BW (MHz)	≥ 100	≥ 5	≥ 40
UGF (GHz)	≥ 1	≥ 0.7	≥ 0.95
PM (°)	≥ 60	≥ 60	≥ 60
CMRR (dB)	≥ 48	≥ 64	≥ 30
PSRR (dB)	≥ 19	≥ 42	≥ 25
SR (V/μS)	≥ 150	≥ 400	≥ 300
ICMR (V)	0.60 − 0.75	0.55 − 0.85	0.60 − 0.75

Feature space pruning

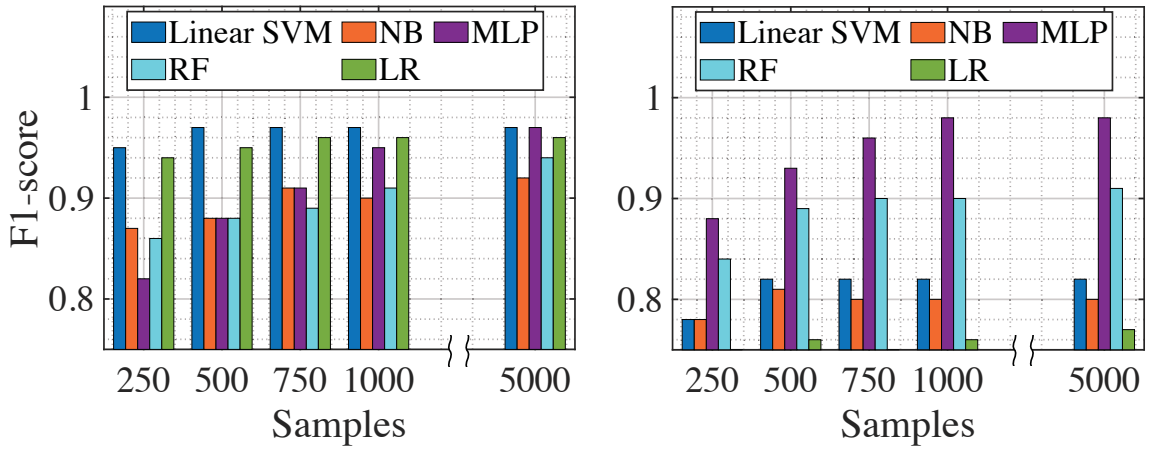


[Dhar *et al.*, ASPDAC21]

Classifier comparison

$$\text{Precision} = \frac{TP}{TP+FP} \qquad \text{Recall} = \frac{TP}{TP+FN} \qquad F1-\text{score} = \frac{2.\text{Precision}.\text{Recall}}{\text{Precision}+\text{Recall}}$$

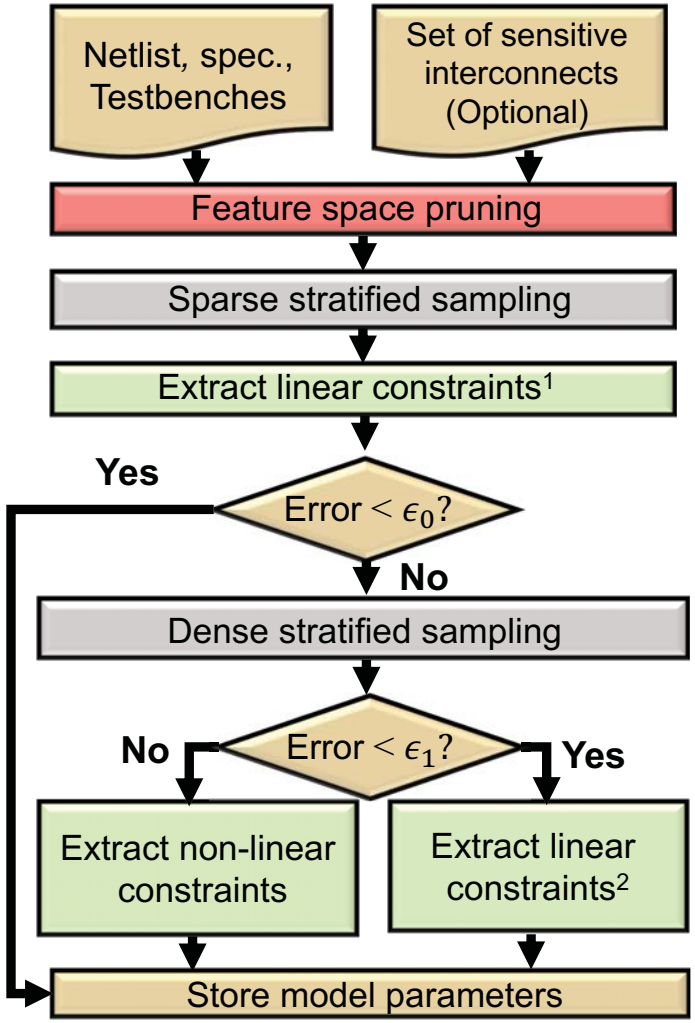
NB: Naïve Bayes, **RF**: Random Forest, **LR**: Logistic Regression
MLP: Multilayer Perceptron, **SVM**: Support Vector Machine

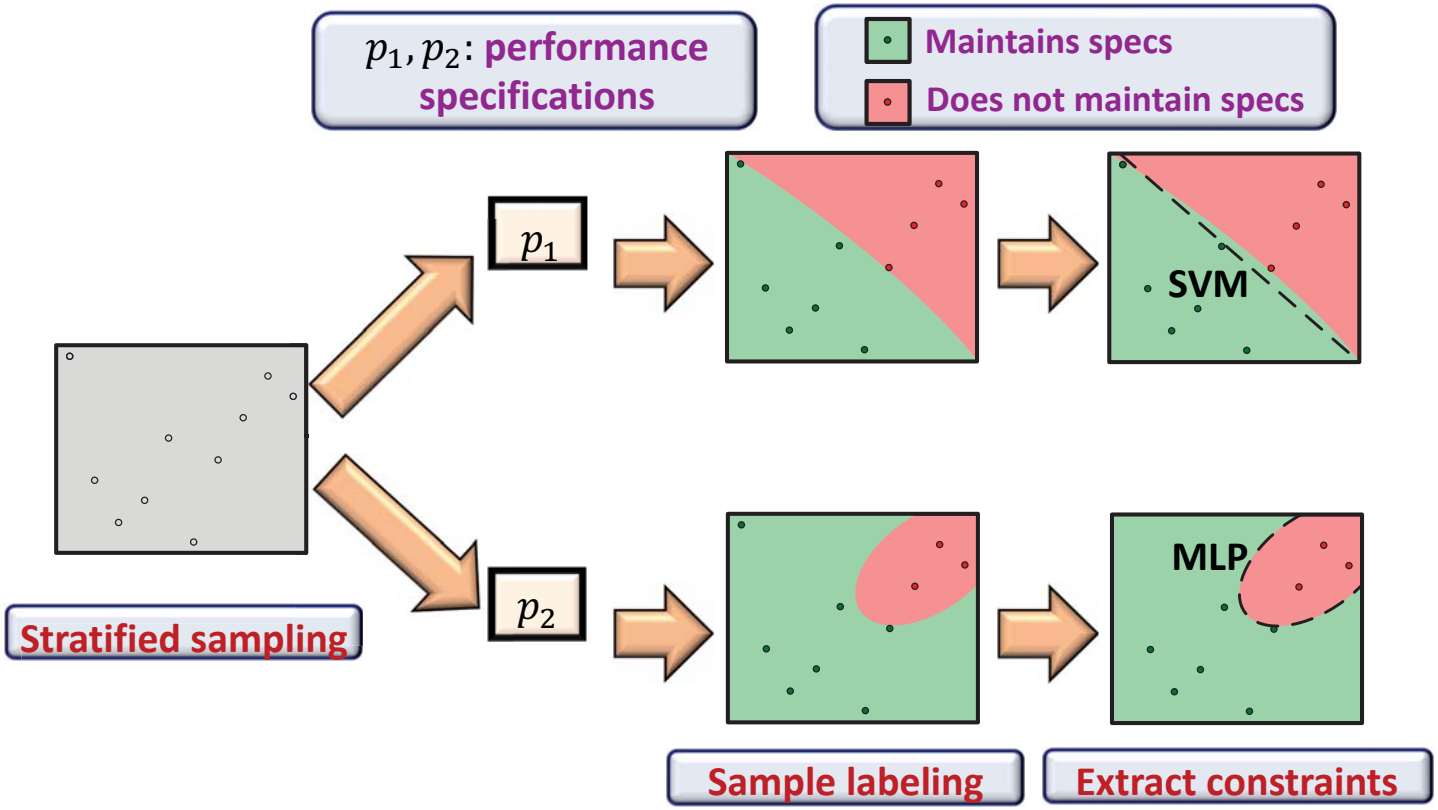


If a sample space is

- **Linearly separable, linear SVM is fast and efficient way** to extract constraints
- **Not linearly separable, multilayer perceptron** shows best accuracy

Extract constraints





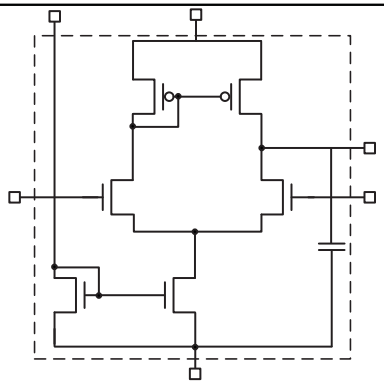
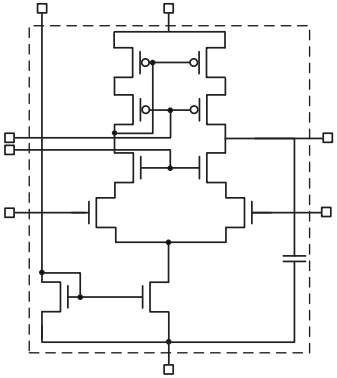
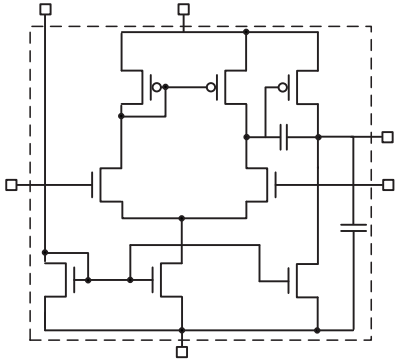
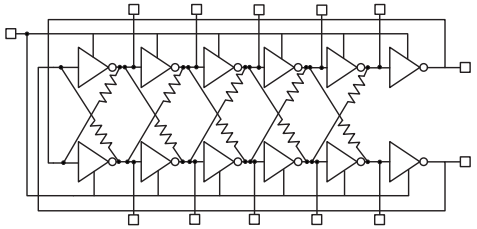
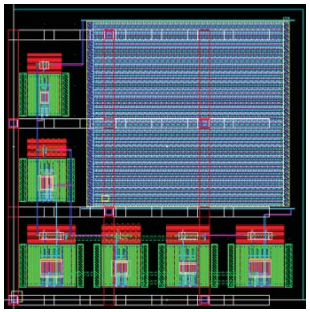
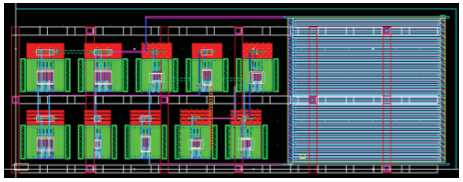
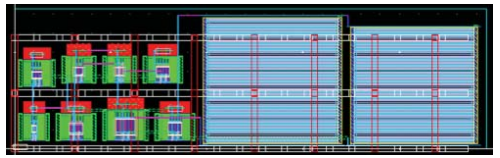
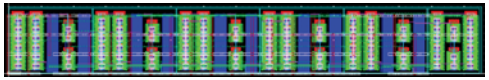
Classification accuracy

High classification accuracies are facilitated by feature space pruning

P	5T OTA				Telescopic OTA				2-stage OTA			
	$\mathcal{P}$	$\mathcal{R}$	F1	ML	$\mathcal{P}$	$\mathcal{R}$	F1	ML	$\mathcal{P}$	$\mathcal{R}$	F1	ML
Gain	0.95	0.84	0.90	$LSVM_2$	0.95	0.91	0.93	$LSVM_2$	0.99	0.99	0.99	MLP
BW	0.98	0.97	0.98	$LSVM_1$	0.99	0.99	0.99	$LSVM_1$	0.98	0.97	0.98	MLP
UGF	0.99	0.96	0.98	$LSVM_1$	0.99	0.98	0.97	$LSVM_1$	0.95	0.95	0.95	$LSVM_1$
PM	0.99	0.99	0.99	$LSVM_1$	0.99	0.99	0.99	$LSVM_1$	0.99	0.98	0.99	$LSVM_1$
CMRR	0.92	0.95	0.94	MLP	0.91	0.89	0.90	MLP	0.99	0.98	0.98	$LSVM_1$
PSRR	0.99	0.99	0.99	$LSVM_1$	0.98	0.99	0.99	$LSVM_1$	0.95	0.91	0.93	$LSVM_2$
SR	0.99	0.99	0.99	$LSVM_1$	0.98	0.97	0.98	$LSVM_1$	0.99	0.98	0.98	$LSVM_1$
ICMR	0.99	0.99	0.99	$LSVM_1$	0.99	0.99	0.99	$LSVM_1$	0.89	0.93	0.91	MLP

$LSVM_1$ ($LSVM_2$): Linear SVM with sparse (dense) sample set,
$\mathcal{P}$: Precision, $\mathcal{R}$: Recall, F1: F1−score.

Layouts of testcases

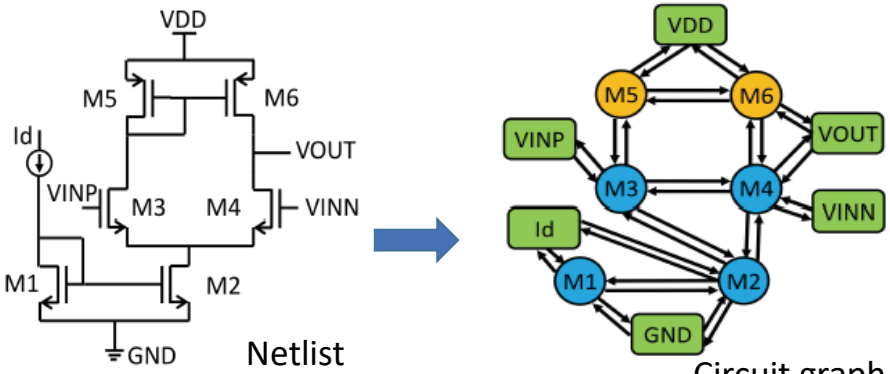
5T OTA	Telescopic OTA	2-stage OTA	VCO
			
			
9.63µm x 9.60µm	**6.85µm x 18.65µm**	**7.42µm x 24.49µm**	**10.11µm x 72.78µm**

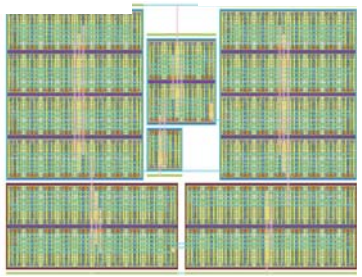
(Layouts are not drawn to scale)

Post-layout performance

P	5T OTA				Telescopic OTA				2-stage OTA			
	SVM+MLP		Conventional		SVM+MLP		Conventional		SVM+MLP		Conventional	
Gain (dB)	20.57	✓	19.09	✓	42.13	✓	38.12	✗	26.57	✓	24.38	✗
BW (MHz)	103.26	✓	126.20	✓	5.49	✓	7.64	✓	46.84	✓	41.22	✓
UGF (GHz)	1.17	✓	1.14	✓	0.70	✓	0.61	✗	1.00	✓	0.92	✗
PM (°)	110.33	✓	116.77	✓	133.41	✓	106.50	✓	94.43	✓	82.05	✓
CMRR (dB)	52.08	✓	52.92	✓	69.15	✓	62.14	✗	32.71	✓	38.27	✓
PSRR (dB)	21.39	✓	18.47	✗	42.45	✓	53.52	✓	26.94	✓	24.37	✗
SR (V/µS)	156.62	✓	156.63	✓	414.24	✓	424.23	✓	408.19	✓	386.07	✓
ICMR (V)	0.60-0.75	✓	0.60-0.75	✓	0.55-0.85	✓	0.55-0.85	✓	0.60-0.75	✓	0.60-0.75	✓

Approach 2: A GCN-based approach



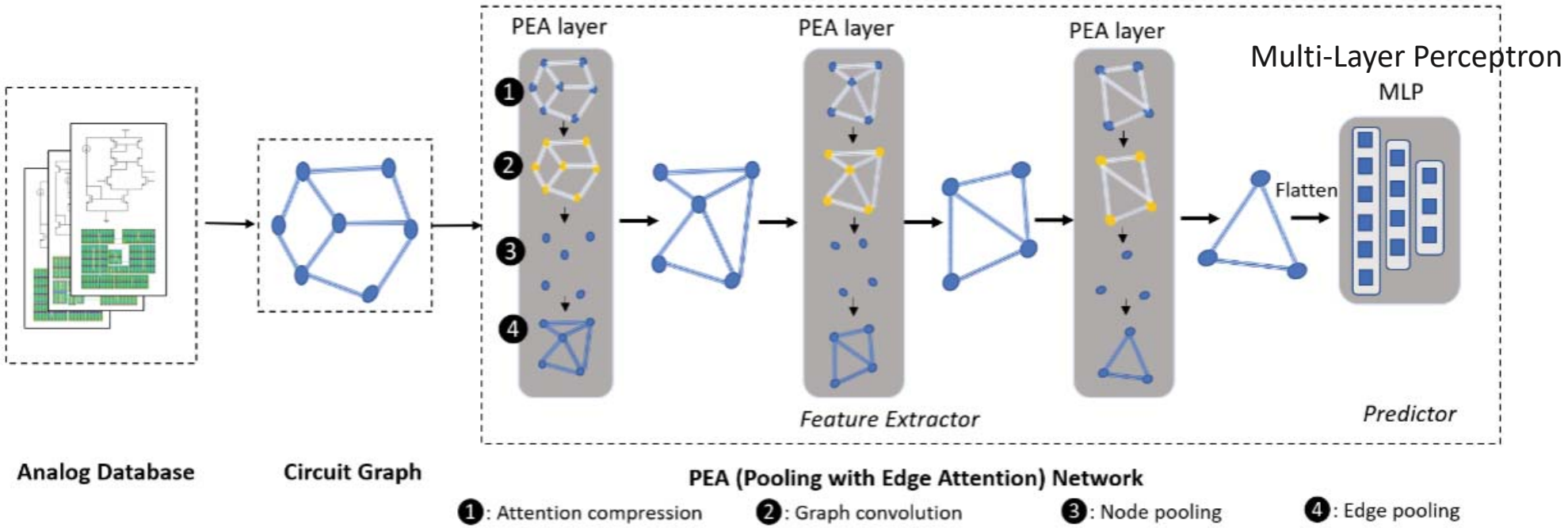


Placement

- Node features matrix $X \in R^{n \times d}$
  - $X_i \in R^d$: node feature for device i including device type, functional module, device dimension and position
- Adjacency matrix $A \in R^{n \times n}$
- Edge feature tensor $E \in R^{n \times n \times p}$ *Channel*
  - $E_{ij} \in R^p$: edge feature between pin j and pin i, including distance, metal layer…

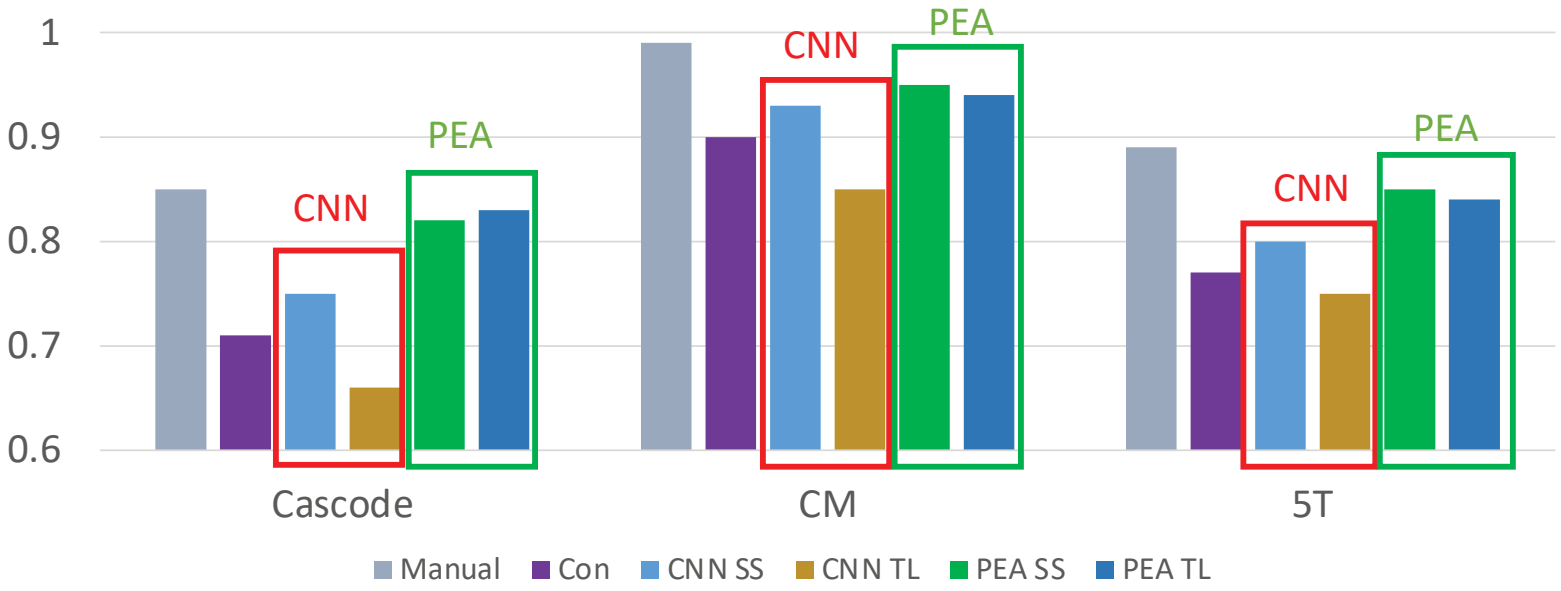
[Li *et al.*, ICCAD20]

PEA (Pooling with Edge Attention) network



Post-layout performance

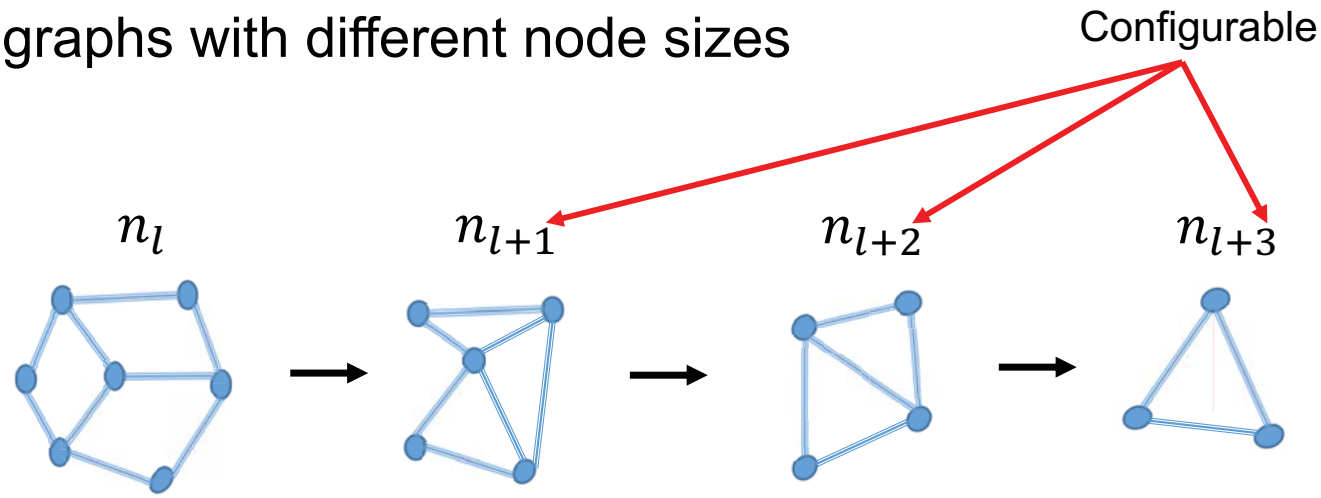
Layout score: close to 1
means close to spec



Con: conventional automatic placement without considering performance

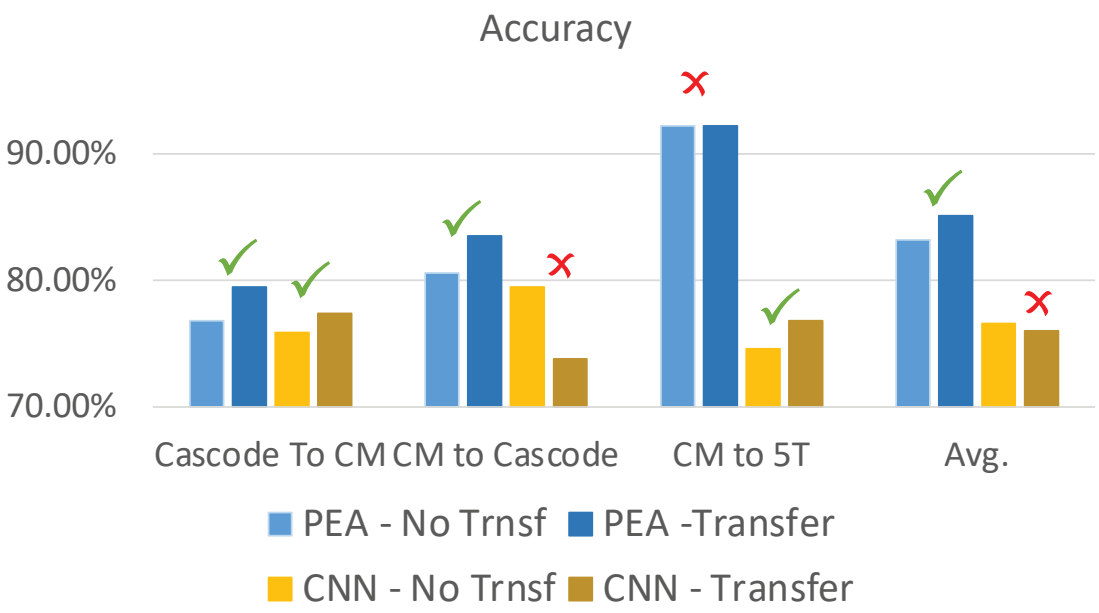
Advantages of the PEA model

- Handling graphs with different node sizes



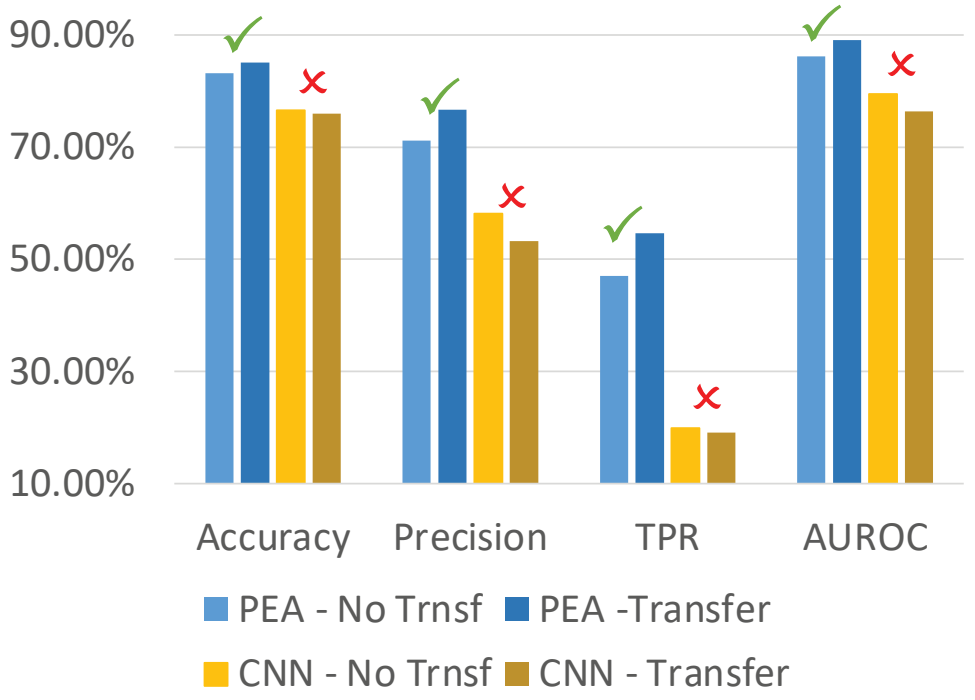
- Transferable for different topologies of circuits

Transfer learning using PEA



✓: successful transfer

×: failure to transfer



Conclusion

- ML techniques can be a game-changer in a field such as analog design

- What makes ML particularly attractive?
  - Trying to replace human intuition
  - Numerous circuit-specific metrics (not just “PPA” as in digital circuits)
  - Design in FinFET technologies makes layout automation more tractable
    - May be too complex for the human designer
    - Layout degrees of freedom are more restricted

ALiGN