ISPD 2016-2017 FPGA Placement Contests

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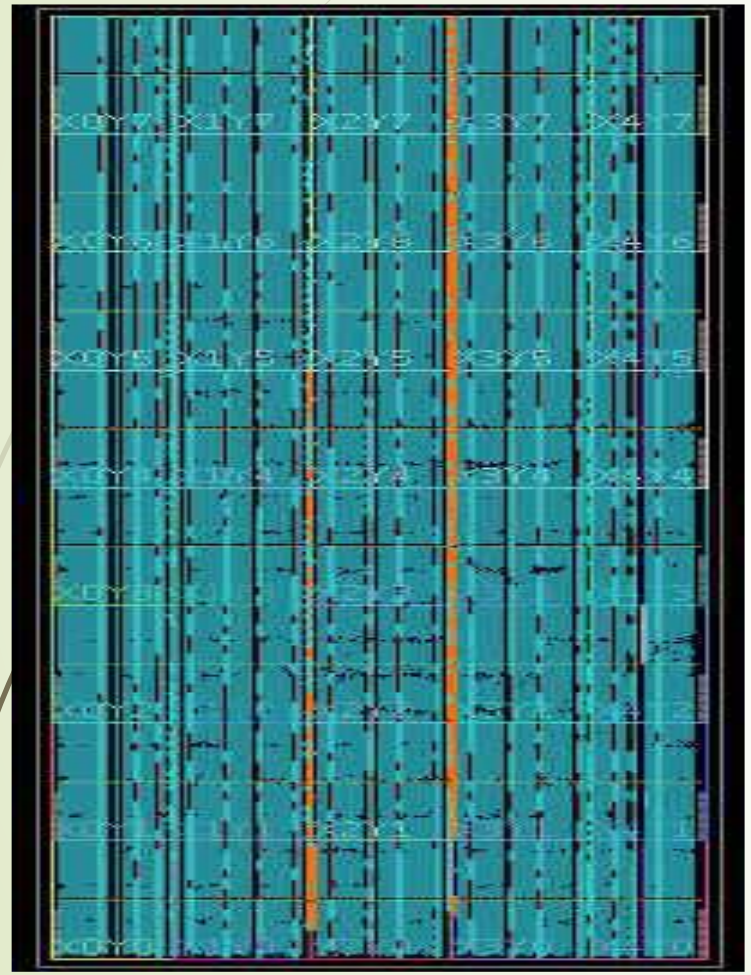
First FPGA Placement Contest

- State-of-the-art FPGA architecture
- Bookshelf format: Academic benchmark format
- Vivado: Industrial tool integration for evaluation
- 2016 Focus: FPGA legalization rule and routing congestion
- 2017 Focus: Clock legalization constraint

Target FPGA: Xilinx UltraScale VU095

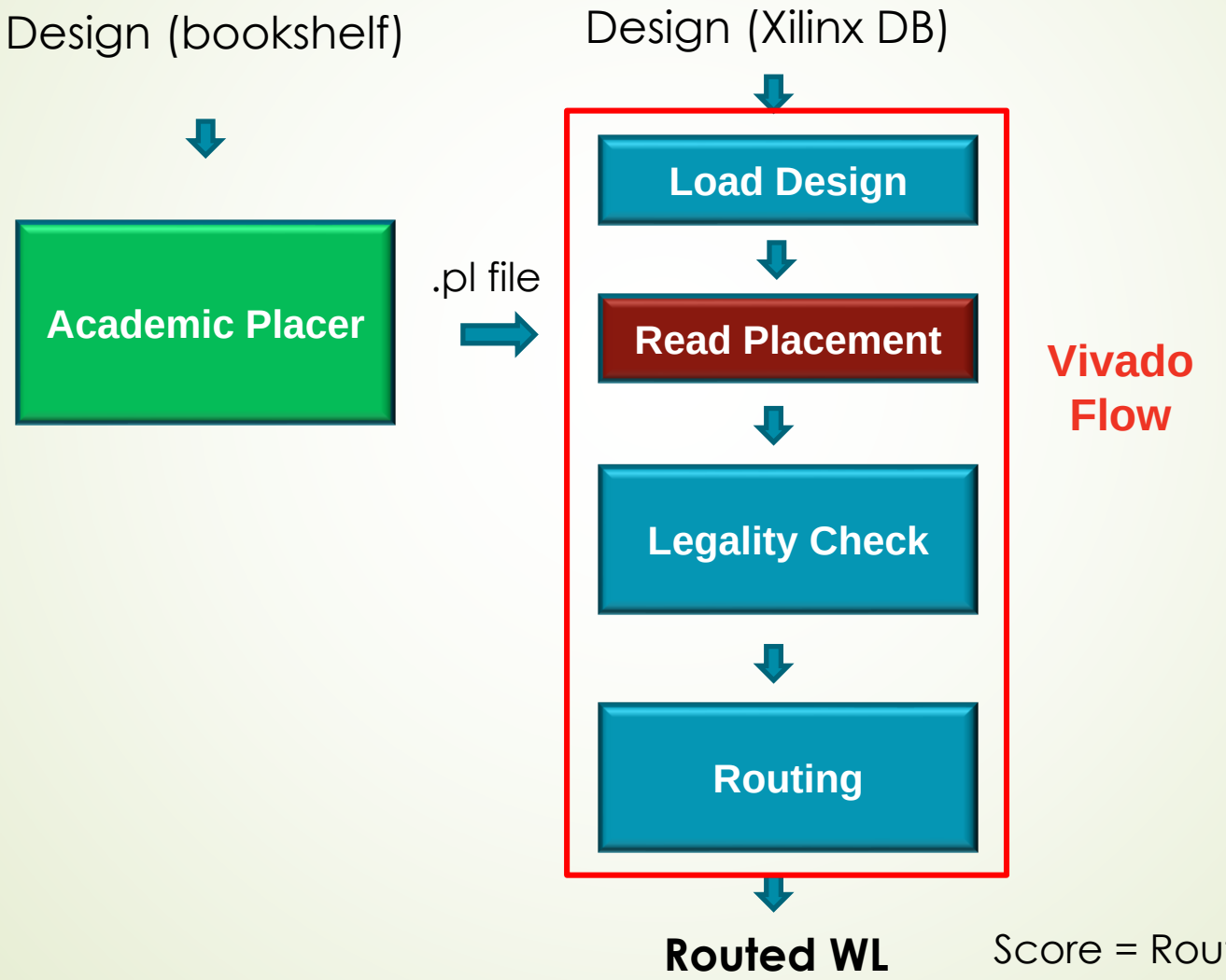


- 20nm Technology
- 1.2 million logic cells
- Heterogeneous architecture

Benchmarks

Design	#LUTs (util)	#Flops (util)	#RAMB36	#DSPs	#control sets
FPGA-1	50K (9%)	55K (5%)	0 (0%)	0 (0%)	12
FPGA-2	100K (19%)	66K (6%)	100 (6%)	100 (13%)	121
FPGA-3	250K (47%)	170K (16%)	600 (35%)	500 (65%)	1281
FPGA-4	250K (47%)	172K (16%)	600 (35%)	500 (65%)	1281
FPGA-5	250K (47%)	174K (16%)	600 (35%)	500 (65%)	1281
FPGA-6	350K (65%)	352K (33%)	1000 (58%)	600 (78%)	2541
FPGA-7	350K (65%)	355K (33%)	1000 (58%)	600 (78%)	2541
FPGA-8	500K (93%)	216K (20%)	600 (35%)	500 (65%)	1281
FPGA-9	500K (93%)	366K (34%)	1000 (58%)	600 (78%)	2541
FPGA-10	350K (65%)	600K (56%)	1000 (58%)	600 (78%)	2541
FPGA-11	480K (89%)	363K (34%)	1000 (58%)	400 (52%)	2091
FPGA-12	500K (65%)	602K (56%)	600 (35%)	500 (65%)	1281

Benchmarking Setup



Score = Routed-WL * (1 + Runtime_Factor)

Contest Winners

	2016 Routability-Driven	2017 Clock-Aware
First Place	UTPlace	UTPlaceF 2.0
Second Place	RippleFPGA	NTUfplace
Third Place	GPlace	RippleFPGA

Impact: Paper Citations

Contest Paper	Number of Citations	Number of Downloads
2016: Routability-Driven FPGA Placement Contest	22	373
2017: Clock-Aware FPGA Placement Contest	12	269

Motivated Research

FPGA Placement Papers	Conference / Journal
UTPlaceF: a routability-driven FPGA placer with physical and congestion aware packing	ICCAD
GPlace3.0: Routability-Driven Analytic Placer for UltraScale FPGA Architectures	TODAES
RippleFPGA: Routability-Driven Simultaneous Packing and Placement for Modern FPGAs	TCAD
Clock-aware ultrascale FPGA placement with machine learning routability prediction	ICCAD
UTPlaceF 3.0: a parallelization framework for modern FPGA global placement	ICCAD
Simultaneous Placement and Clock Tree Construction for Modern FPGAs	FPGA

Summary

- Motivated academic researchers
- Released realistic benchmarks
- Industry benefit out of the contests and research