ISPD 2014 & 2015
Detailed Routing-Driven Placement Contests - A Retrospective

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www.ispd.cc/contests/14/ispd2014_contest.html
www.ispd.cc/contests/15/ispd2

Contests were sponsored by

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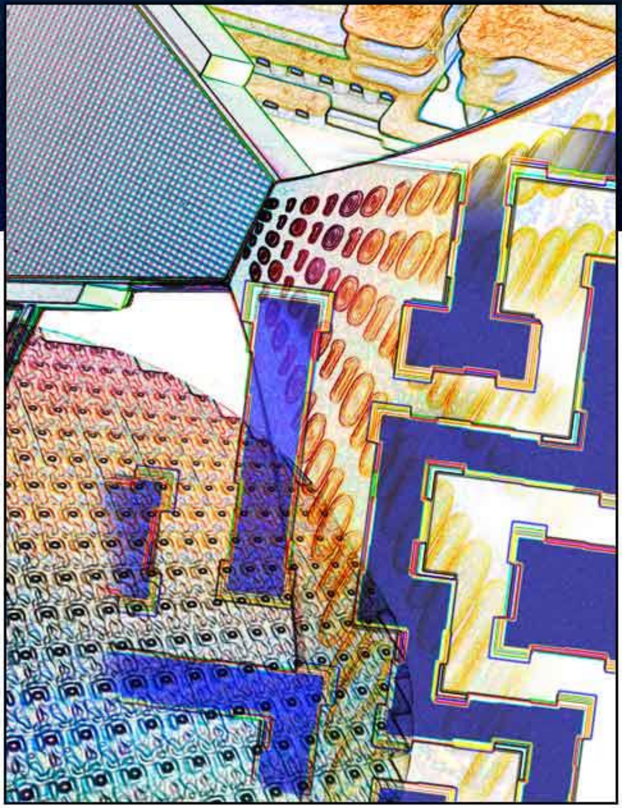


1. Motivation

Motivation

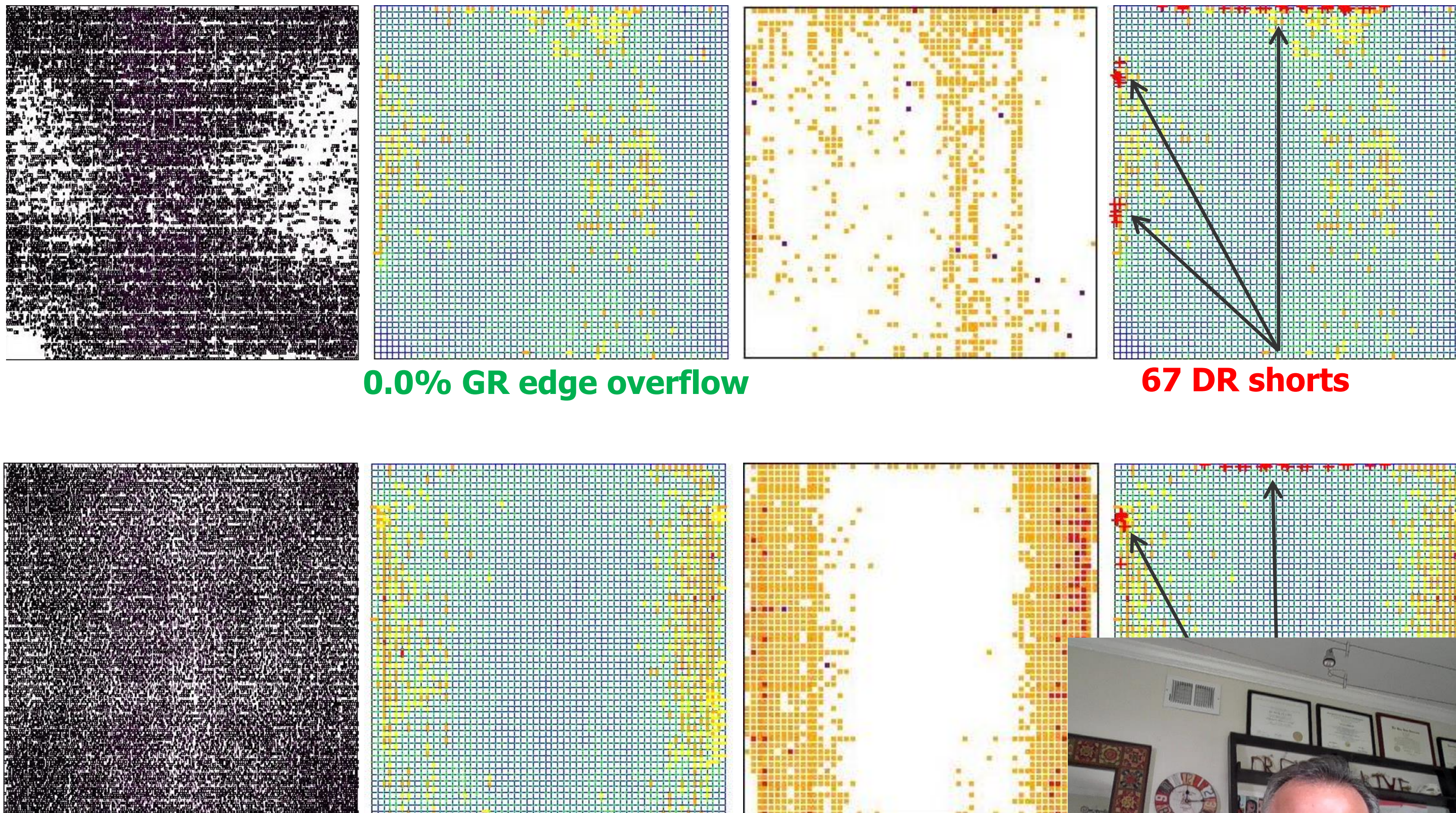
- Increasing complexity of design rules
  - Miscorrelation between global routing (GR) and detailed routing (DR)
  - Global routing may not adequately model short nets within coarse GR bin
- Placement constraints impacting routability
  - Floorplan: Irregular placeable area, narrow channels between blocks
  - Design rules: Min-spacing, pin geometry, edge-type, end-of-line, etc.
- Routing constraints
  - Non-default rules, routing layer restrictions and blockages, timing constraints, …

Is global routing congestion map a sufficient metric?

Placement | GR edge overflow | node congestion | DR violations

with GR congestion response

evenly spread



0.0% GR edge overflow

67 DR shorts

0.4% GR edge overflow

Since then, many excellent works that improved routing congestion prediction during placement

Painting on placement: Forecasting routing congestion using conditional generative adversarial nets
C Yu, Z Zhang - Proceedings of the 56th Annual Design Automation …, 2019 - dl.acm.org

High-definition routing congestion prediction for large-scale FPGAs
MB Alawieh, W Li, Y Lin, L Singhal… - 2020 25th Asia and …, 2020 - ieeexplore.ieee.org

prediction for mixed-size designs using convolutional neural network
Z Xie, YH Huang, GQ Fang, H Ren… - 2018 IEEE/ACM …, 2018 - ieeexplore.ieee.org

DRC hotspot prediction at sub-10nm process nodes using customized convolutional network
R Liang, H Xiang, D Pandey, L Reddy, S Ramji… - Proceedings of the …, 2020 - dl.acm.org

GPlace3. 0: Routability-driven analytic placer for UltraScale FPGA architectures
Z Abuowaimer, D Maarouf, T Martin, J Foxcroft… - ACM Transactions on …, 2018 - dl.acm.org

A machine learning framework to identify detailed routing short violations from a placed netlist
AF Tabrizi, L Rakai, NK Darav, I Bustany… - 2018 55th ACM …, 2018 - ieeexplore.ieee.org

RouteNet: Routability prediction for mixed-size designs using convolutional neural network
Z Xie, YH Huang, GQ Fang, H Ren… - 2018 IEEE/ACM …, 2018 - ieeexplore.ieee.org

Routability-driven macro placement with embedded cnn-based prediction model
YH Huang, Z Xie, GQ Fang, TC Yu… - … , Automation & Test …, 2019 - ieeexplore.ieee.org

Are adversarial perturbations a showstopper for ml-based cad? a case study on cnn-based lithographic hotspot detection
K Liu, H Yang, Y Ma, B Tan, B Yu, EFY Young… - arXiv preprint arXiv …, 2019 - arxiv.org

prediction and optimization with deep learning-based pin pattern recognition
TC Yu, SY Fang, HS Chiu, KS Hu… - … on Computer-Aided …, 2020 - ieeexplore.ieee.org

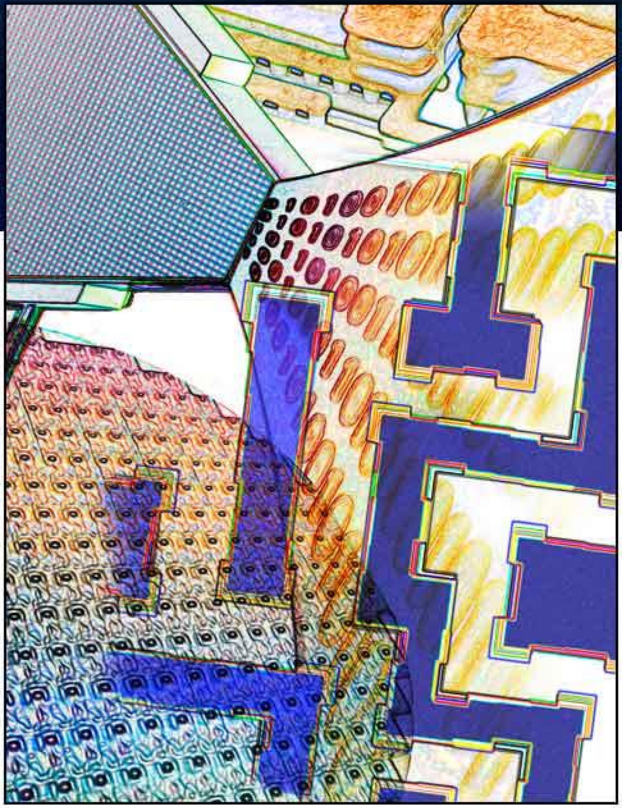
Design rule violation hotspot prediction based on neural network ensembles
W Zeng, A Davoodi, YH Hu - arXiv preprint arXiv:1811.04151, 2018 - arxiv.org

Supervised-learning congestion predictor for routability-driven global routing
Z Zhou, S Chahal, TY Ho… - … Symposium on VLSI …, 2019 - ieeexplore.ieee.org

Eh? predictor: A deep learning framework to identify detailed routing short violations from a placed netlist
AF Tabrizi, NK Darav, L Rakai, I Bustany… - … on Computer-Aided …, 2019 - ieeexplore.ieee.org

CongestionNet: Routing congestion prediction using deep graph neural networks
R Kirby, S Godil, R Roy… - 2019 IFIP/IEEE 27th …, 2019 - ieeexplore.ieee.org

…



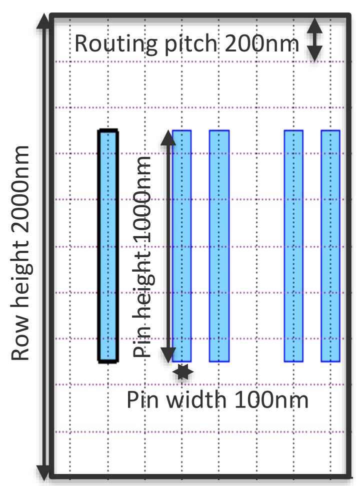
2. Benchmark Suites

Benchmark Suites

- 20 designs from 65nm and 28nm technology nodes
  - 16 available to contestants
  - 4 blind
- Adapted from designs originally provided by
  - Intel in the ISPD 2013 gate sizing contest
  - IBM in the DAC 2012 routability-driven placement contest
- Industry standard **LEF/DEF** format

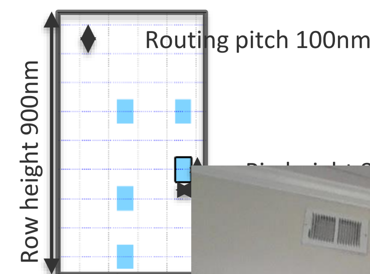
Suite A: mgc_edit_dist, mgc_des_perf, mgc_fft, mgc_pci_bridge32, & mgc_matrix_mult:
- 65nm technology
- Routing pitch 200nm
- 10 routing tracks per cell row
- All standard cells are one row high

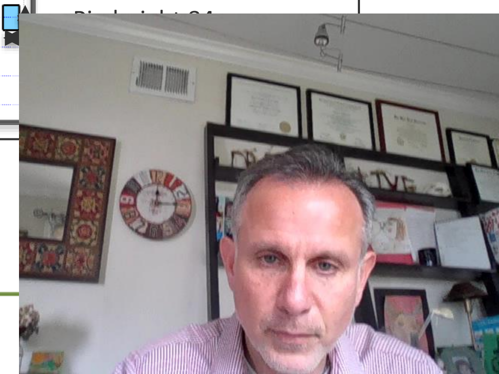
Typical 65nm standard cell



Suite B: mgc_superblue11_a, 12, 14, 16_a, and 19:
- 28nm technology
- routing pitch 100nm
- 9 routing tracks per cell row
- All standard cells are one row high

Typical 28nm standard cell





Benchmark design features

- **Realistic design rule constraints** (edge-type, min spacing, end-of-line, non-default routing, …)
- Rectilinear pin shapes, some metal2 pins
- Power and ground mesh
  - Pin access can be blocked by this if it is not considered

Design constraint features

- **Large macros with routing blockages and narrow placement channels** to the Intel benchmarks
  - To simulate top-level place-and-route problems
- **Exclusive fence placement regions** (e.g. voltage islands)
  - Only member cells allowed in
  - A region may be **disconnected**
- **Maximum cell utilization limit**
  - Some submitted 2014 ISPD placement contest solutions had local area utilization of 100% to minimize wirelength
  - To reserve space for cell sizing and buffering in a place-route flow
- **Routing layer blockages**

Retained 2014 benchmark characteristics

- Eight designs were retained from the 2014 ISPD contest, but we **added a maximum density limit constraint – NEW!**

Design	# Macros	# Cells	# Nets	# Fence Regions	# Primary Inputs & Outputs	%Area Utilization: Standard Cells	%Area Utilization: Standard Cells & Macros	Density Limit %
mgc_des_perf_1	0	112,644	112,878	0	374	90.6	Same	**90.6**
mgc_fft_1	0	32,281	33,307	0	3,010	83.5	Same	**83.5**
mgc_fft_2	0	32,281	33,307	0	3,010	49.9	Same	**65.0**
mgc_matrix_mult_1	0	155,325	158,527	0	4,802	80.2	Same	**80.2**
mgc_matrix_mult_2	0	155,325	158,527	0	4,802	79.0	Same	**80.0**
mgc_superblue12	89	1,286,948	1,293,413	0	5,908	44.0	57.0	**65.0**
mgc_superblue14	340	612,243	619,697	0	21,078	55%	77%	**56.0**
mgc_superblue19	286	506,097	511,606	0	15,422	[illegible]	[illegible]	[illegible]

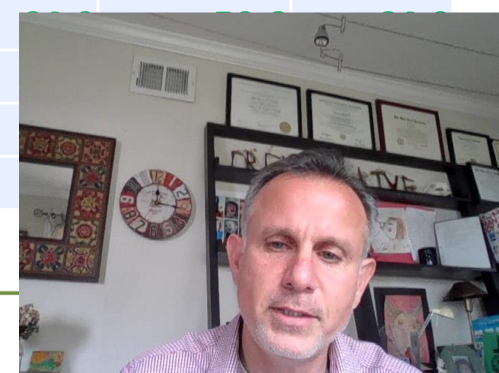
Blind benchmarks are shown in red!

Various design modifications for 2015 Contest

- These twelve designs incorporate the new modifications (**shown in green**) applied to the 2014 ISPD benchmarks

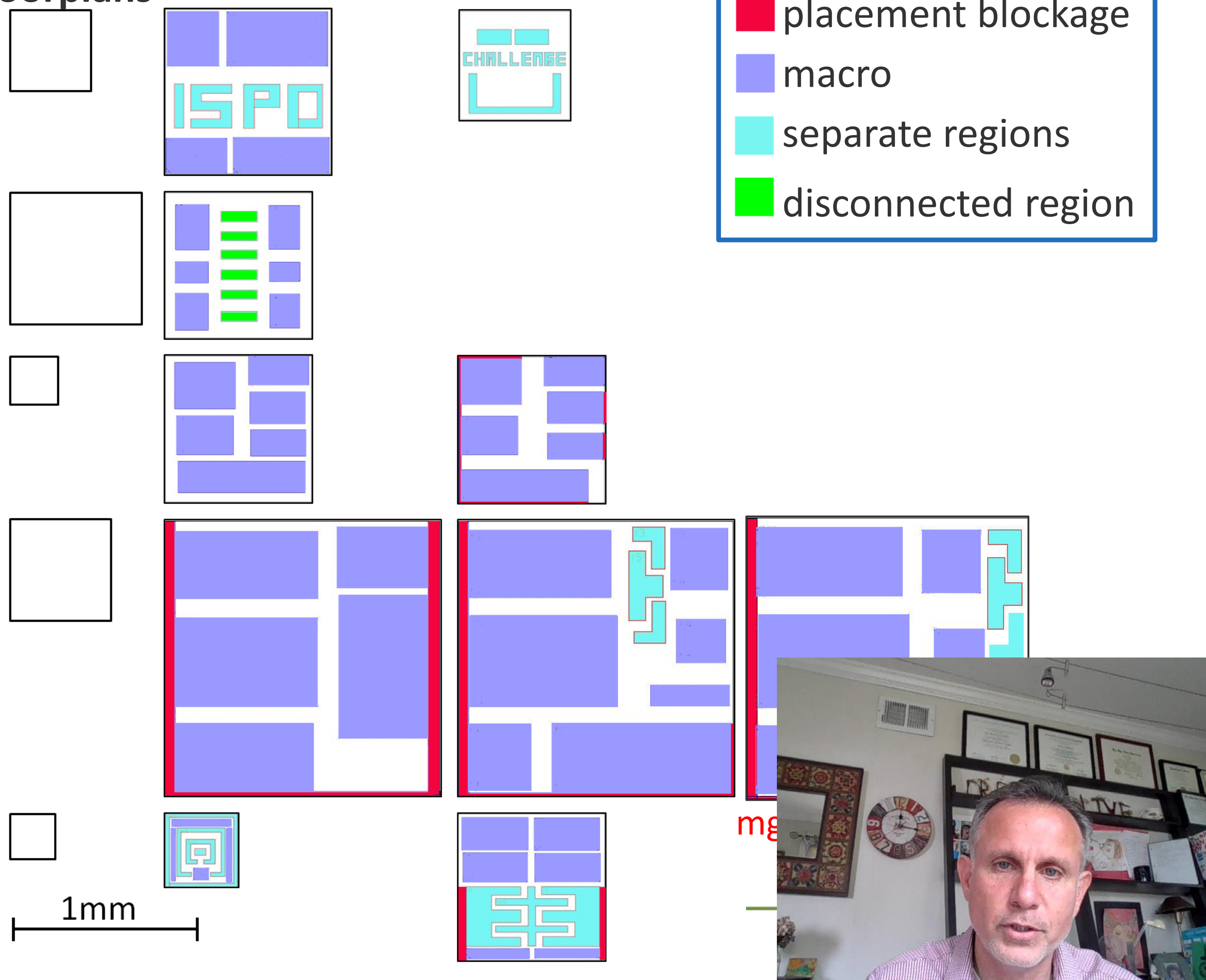
Design	# Macros	# Cells	# Nets	# Fence Regions	# Primary Inputs & Outputs	%Area Utilization: Standard Cells	%Area Utilization: Standard Cells & Macros	Density Limit %
mgc_des_perf_a	4	108,288	110,281	4	374	56.7	71.7	56.7
mgc_des_perf_b	0	112,644	112,878	12	374	56.3	49.7	56.3
mgc_edit_dist_a	6	127,413	131,134	1	2574	54.1	61.6	54.1
mgc_fft_a	6	30,625	32,088	0	3,010	28.5	74.0	50.0
mgc_fft_b	6	30,625	32,088	0	3,010	30.9	74.0	60.0
mgc_matrix_mult_a	5	149,650	154,284	0	4,802	44.9	76.8	60.0
mgc_matrix_mult_b	7	146,435	151,612	3	4,802	34.2	72.6	60.0
mgc_matrix_mult_c	7	146,435	151,612	3	4,802	32.7	72.6	60.0
mgc_pci_bridge32_a	4	29,517	29,985	4	361	[illegible]	[illegible]	[illegible]
mgc_pci_bridge32_b	6	28,914	29,417	3	361	[illegible]	[illegible]	[illegible]
mgc_superblue11_a	1,458	925,616	935,613	4	27,371	[illegible]	[illegible]	[illegible]
mgc_superblue16_a	419	680,450	697,303	2	17,498	[illegible]	[illegible]	[illegible]

Blind benchmarks are shown in red.



ISPD 2015 floorplans – Suite A

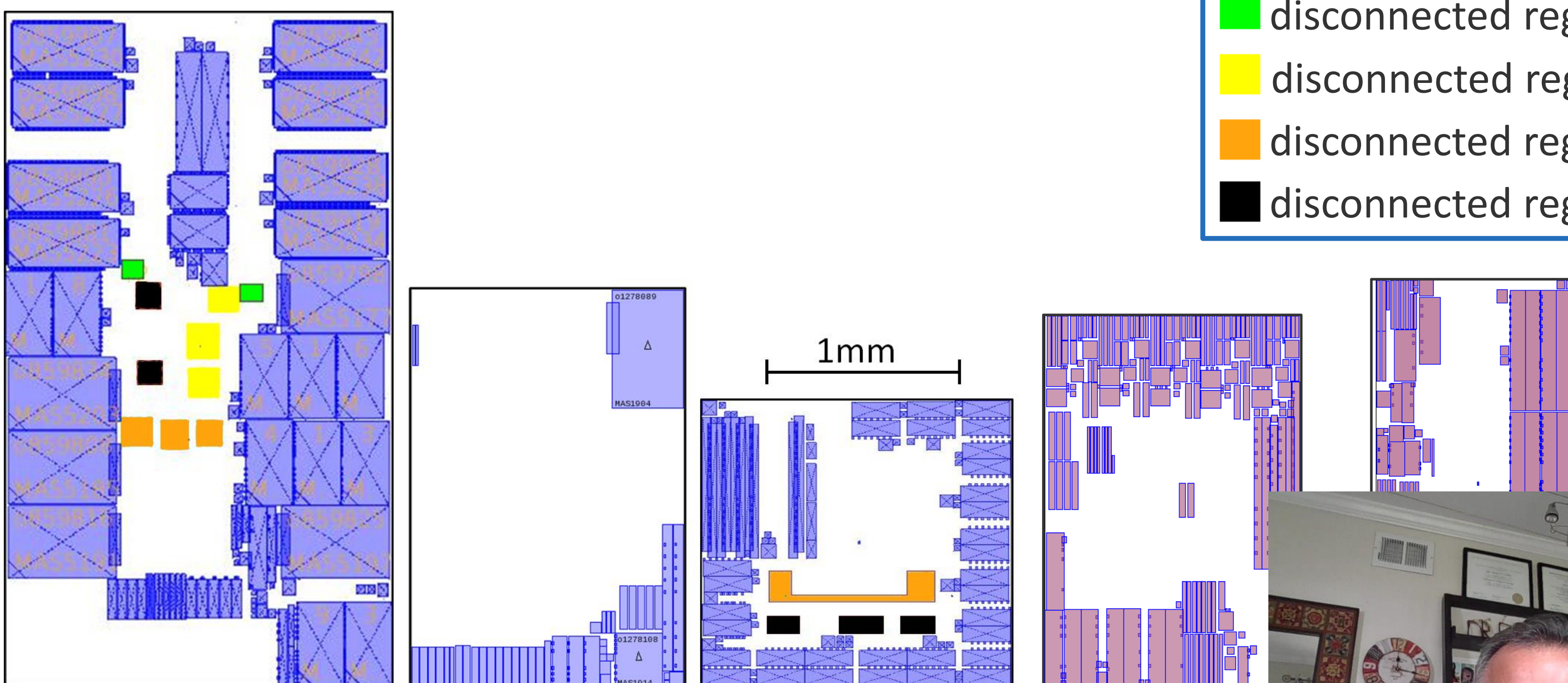
Benchmark	ISPD 2014 Floorplans	ISPD 2015 Floorplans Variant A	ISPD 2015 Floorplans Variant B
mgc_des_perf			
mgc_edit_dist			
mgc_fft			
mgc_matrix_mult			
mgc_pci_bridge32			



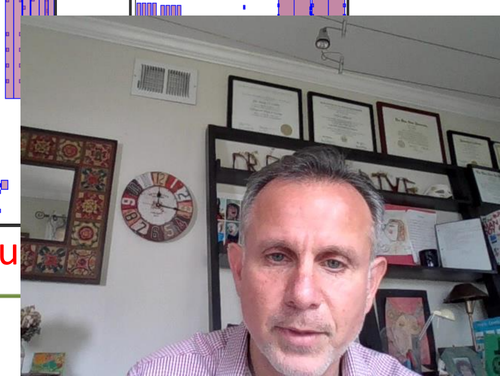
LEGEND:
- placement blockage
- macro
- separate regions
- disconnected region

ISPD 2015 floorplans – Suite B

LEGEND:
- placement blockage
- macro
- separate regions
- disconnected region1
- disconnected region2
- disconnected region3
- disconnected region4

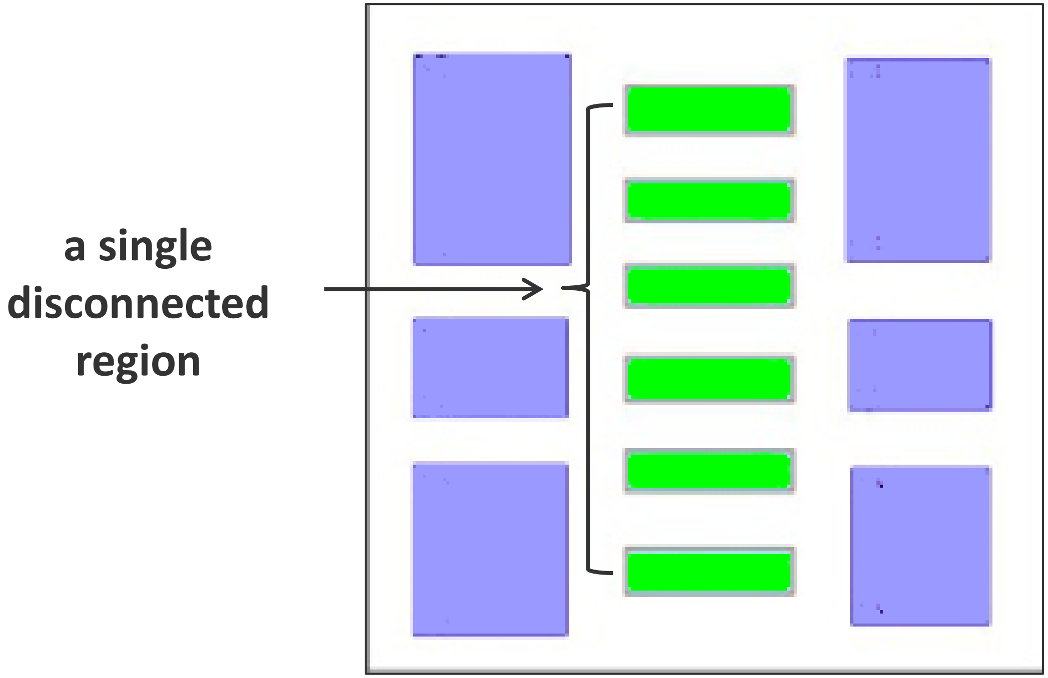


mgc_superblue11_a   mgc_superblue12   mgc_superblue16_a   mgc_superblu



Sample benchmark design

- Disconnected regions pose a challenging cell assignment problem



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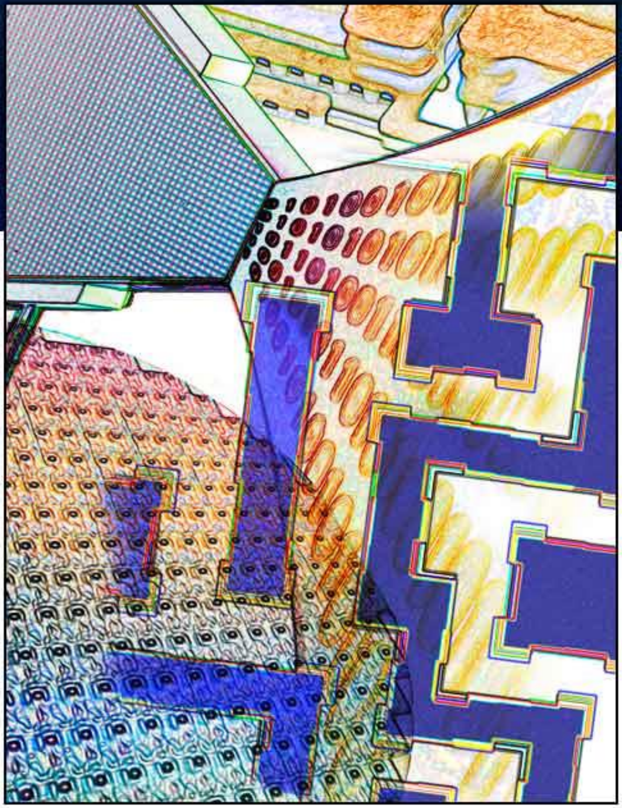
Design	# Cells	# Nets	#Regions	Cells
mgc_edit_dist_a	127,413	131,134	1	



3. Evaluation metrics

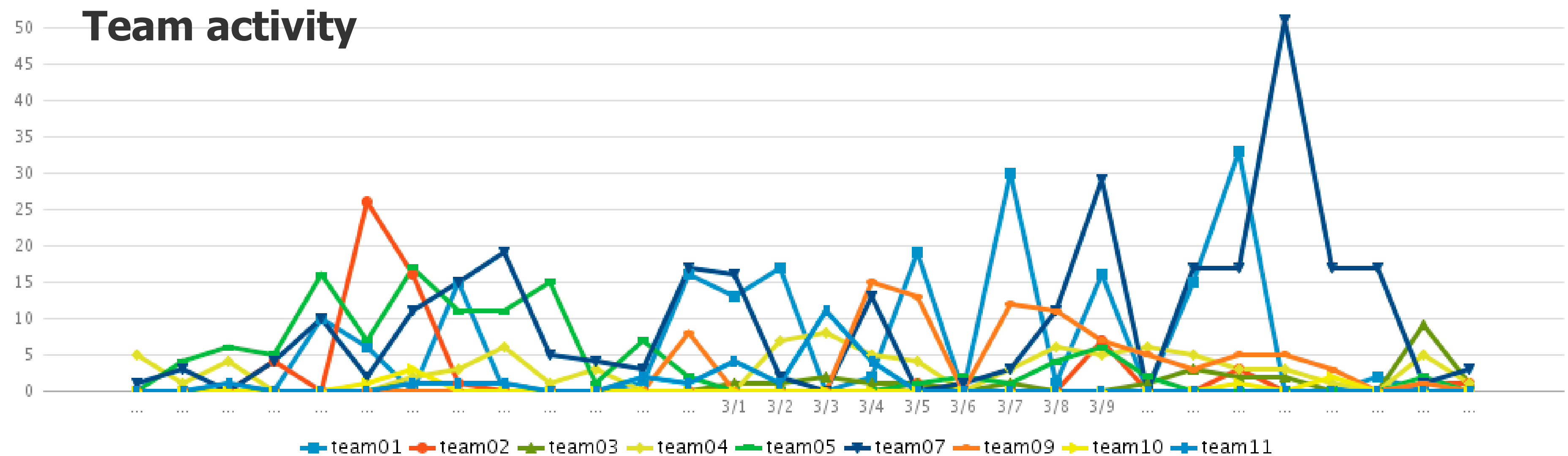
Total score $S = \min\{S_{DP} + S_{WL} + S_{DR} + , 50\}$ (larger is worse)

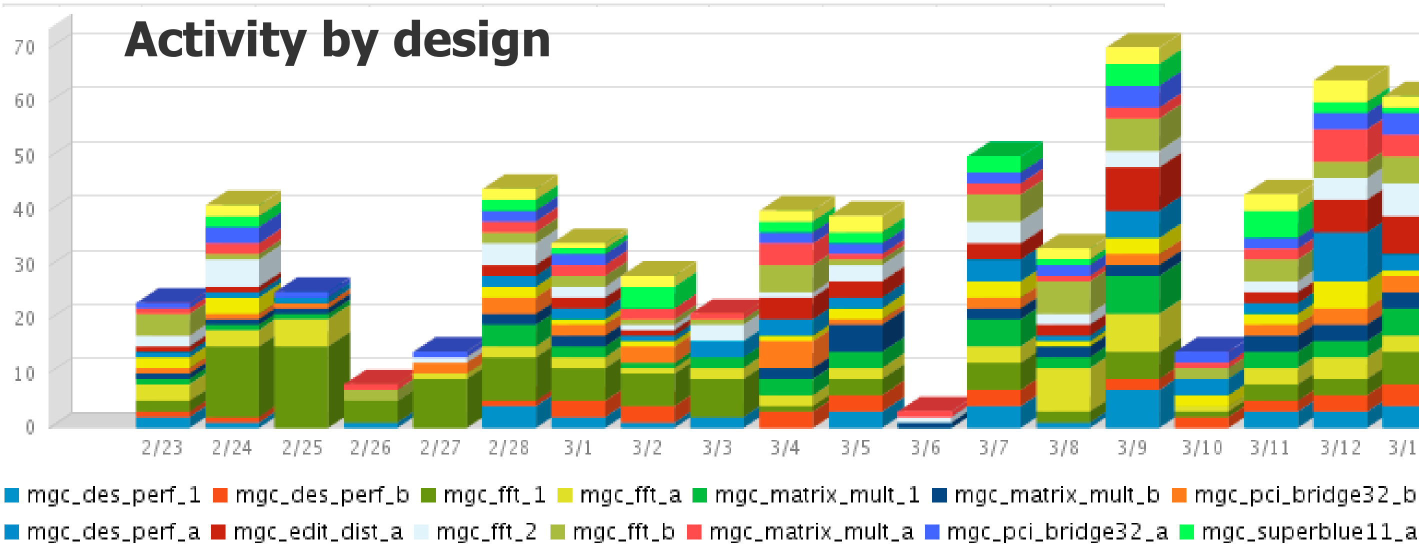
- S_{DP}: Average **legalization displacement** in standard cell row heights of the 10% most displaced of all cells
- S_{WL}: **Detail-routed wire-length** weighted by a density limit violation penalty
  - Scaled linearly from WL_{min} to 1.5xWL_{median} to [0,25]
- S_{DR}: **Number of detailed-routing violations,**
  - *DR* from 0 to 10,000 is scaled logarithmically to [0,25] by $S_{DR} = 12.475(\log_{10}(DR + 100) - 2)$
  - Detailed router used as final arbiter of quality
- Maximum score *S* = 50 if
  - There are fence region violations
  - $S_{DP} \geq 25$ standard cell rows
  - S_{DR} violations exceed 10,000
  - GR edge overflow exceeds GR_{edge_max} of 0.3% for mgc_superb
    3% for the other benchmarks

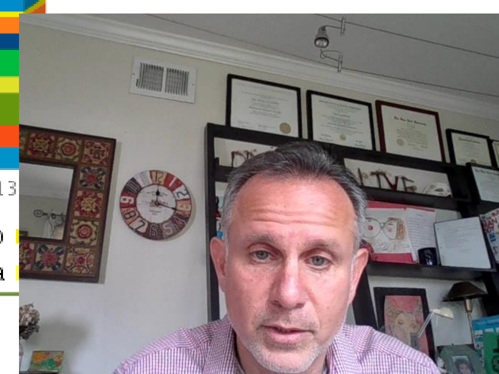
Contest scores were published daily – heavy competition among teams!

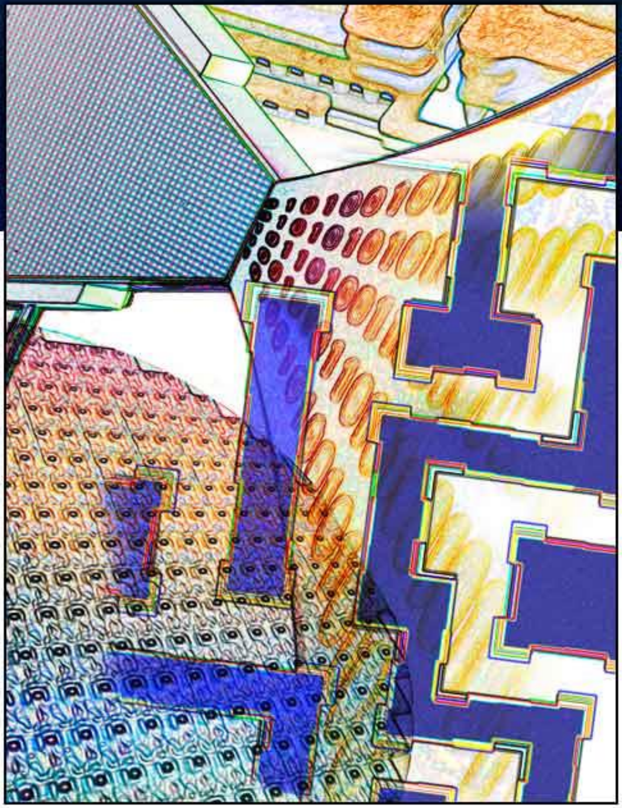
Density Overflow Factor	Global Routing			Detailed Routing		Scaled Scores			Total Score	Team
	%Edge Overflows	Node Overflows	Wire Length (m)	Wire Length (m)	Detailed Routing Violations	SDP	SWL	SDR		
0.017	0.001	84	4.50	4.66	7.0	0.00	0.00	0.37	0.4	ispd07
0.009	0.023	933	5.00	5.20	111.8	0.00	4.04	4.07	8.1	ispd01
0.088	0.015	1,080	4.43	4.61	179.0	0.84	2.22	5.56	8.6	ispd11
0.150	0.127	2,657	4.70	4.93	1713.8	0.00	7.47	15.70	23.2	ispd04
0.069	0.238	4,625	6.16	6.36	8853.4	0.00	16.42	24.35	40.8	ispd10
0.066	10.399	66,123	29.08						50.0	ispd02

Team activity during the contest









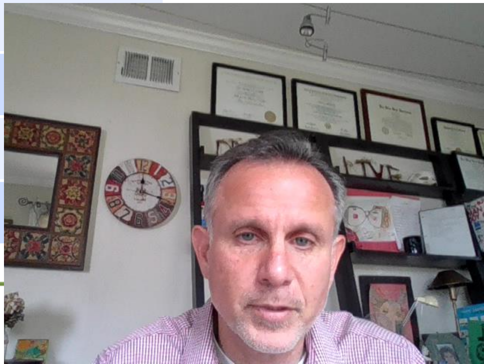
4. Results

2014 participation statistics

- 18 initial registrations:
  - Asia: China, Hong Kong, Taiwan
  - Europe: Germany
  - North America: Canada, USA
  - South America: Brazil

- 9 final binary submissions

ID	University	Country
1	National Chai Tung Univ	Taiwan
3	National Central Univ	China
5	National Taiwan Univ	Taiwan
8	National Taiwan Univ	Taiwan
9	Chinese Univ of Hong Kong	Hong Kong
10	Univ of Calgary & Univ of Waterloo	Canada
16	Tsinghua Univ	China
17	Univ of Texas at Austin	USA
18	Univ of Michigan	USA

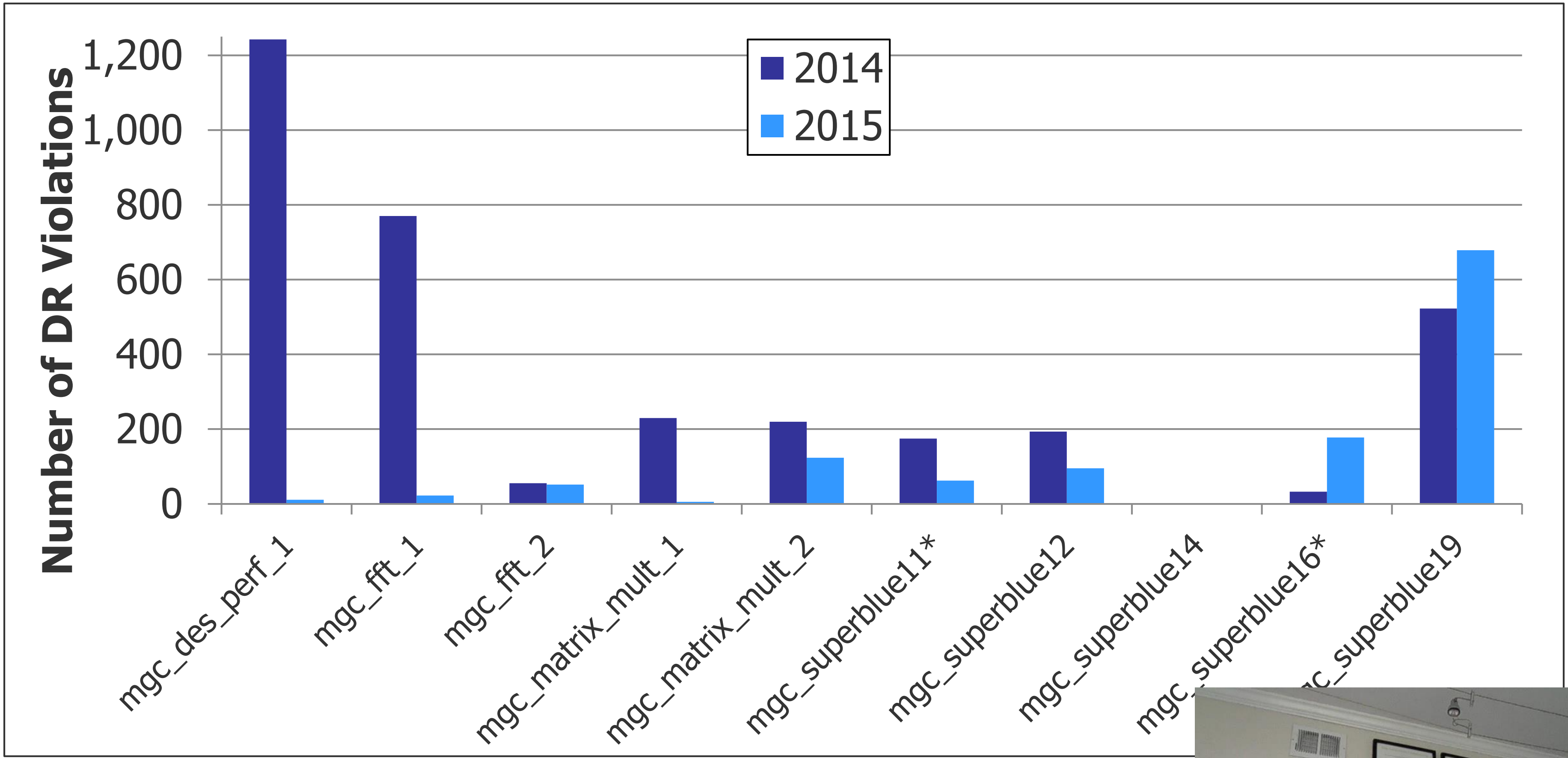


2015 participation statistics

- 12 teams initially participated:
  - Asia: China, Hong Kong, Taiwan
  - Europe: France, Germany
  - North America: Canada, USA

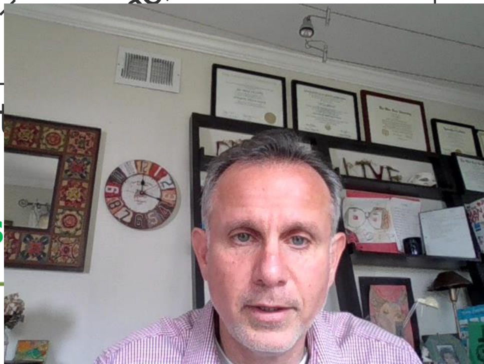
ID	University	Team Lead and Members	Advisor
1	University of Calgary and University of Waterloo	Nima Karimpour Darav, Aysa Fakheri Tabrizi, David Westwick	Lalah Behjat Andrew Kennings
2	Dresden University of Technology	Andreas Krinke,Sergii Osmolovskyi, Johann Kenctel, Matthias Thiele, Steve Bigalke	Jens Lienig
4	Chinese University of Hong Kong	Wing-Kai Chow, Peisahn Tu, Jian Kuang, Zhiqing Liu	Evangeline Young
5	University of Illinois	Chun-Xun Lin, Zigang Xiao, Haitong Tian, Daifeng Guo	Martin Wong
7	National Taiwan University	Chau-Chin Huang, Sheng-Wei Yang, Chin-Hao Chang, Hsin-Ying Lee, Szu-To Chen, Bo-Qiao Lin	Yao-Wen Chang
10	National Chiao Tung University	Ching-Yu Chin	
11	National Chung Cheng University	Xin-Yuan Su	

Comparison of detailed routing violations for best placement results in 2015 vs. 2014



*mgc_superblue11_a and mgc_superblue16_a have fence region const
contest, but still have comparable results.

2 Outliers, but significant improvement in most results versus

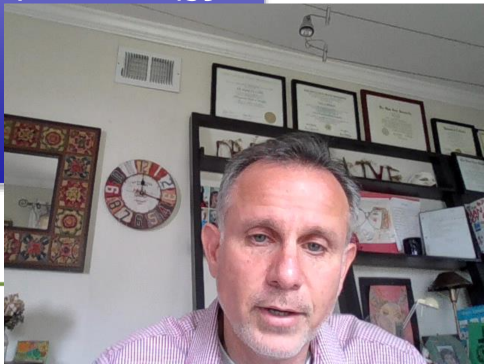


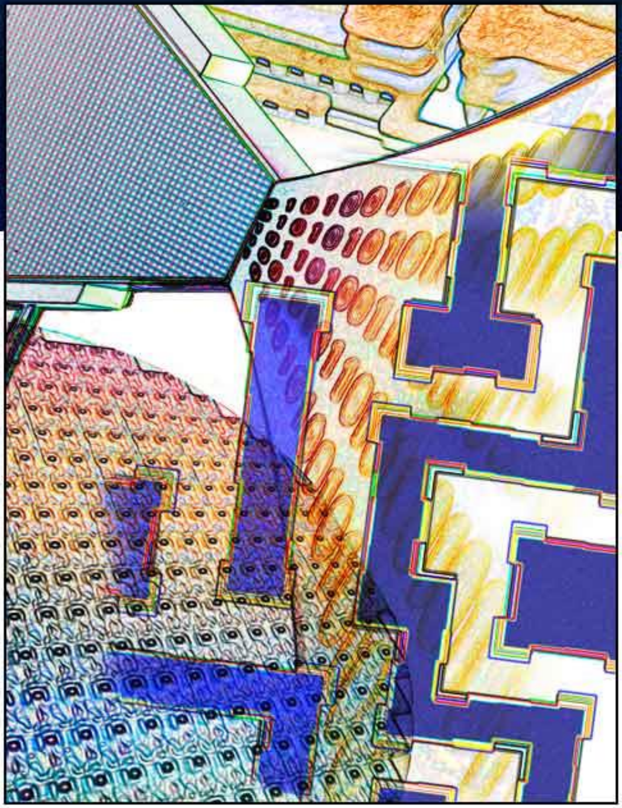
Final rankings!

- Competitive results with significant improvements as the contest progressed

ISPD 2014		Number of designs	
Rank	Team	Unroutable	Best DR Score
1st	UC & UW	0	2
	NCTU	2	5
3rd	NTU	2	4
4th	CUHK	5	2
5th	UTA	6	1
6th	NCU	11	0
	TU	11	0

ISPD 2015		Number of Designs				
Rank	Team	Unroutable	Fewest Detailed Routing Violations	Shortest Detail Routed Wire Length Scaled by Density Overflow	Best Score for Design	Total Score
1st	NTU	3	9	7	9	299
2nd	UC & UW	3	6	5	3	357
3rd	CUHK	4	5	5	7	439
4th	NCCU	11	1	2	[illegible]	[illegible]
5th	NCTU	13	0	0	[illegible]	[illegible]
6th	UI	17	0	0	[illegible]	[illegible]
7th	DUT	20	0	0	[illegible]	[illegible]





5. Research Impact

Research Impact

ISPD 2014 benchmarks with sub-45nm technology rules for detailed-routing-driven placement

Authors: Vladimir Yutsis, Ismail S Bustany, David Chinnery, Joseph R Shinnerl, Wen-Hao Liu

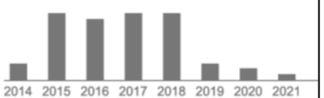
Publication date: 2014/3/30

Book: Proceedings of the 2014 on International symposium on physical design

Pages: 161-168

Description: The public release of realistic industrial placement benchmarks by IBM and Intel Corporations from 1998--2013 has been crucial to the progress in physical-design algorithms during those years. Direct comparisons of academic tools on these test cases, including widely publicized contests, have spurred researchers to discover faster, more scalable algorithms with significantly improved quality of results.

Total citations: Cited by 59



ISPD 2015 benchmarks with fence regions and routing blockages for detailed-routing-driven placement

Authors: Ismail S Bustany, David Chinnery, Joseph R Shinnerl, Vladimir Yutsis

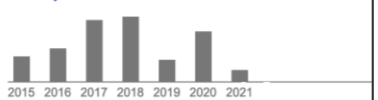
Publication date: 2015/3/29

Book: Proceedings of the 2015 Symposium on International Symposium on Physical Design

Pages: 157-164

Description: The ISPD~ 2015 placement-contest benchmarks include all the detailed pin, cell, and wire geometry constraints from the 2014 release, plus

Total citations: Cited by 76



ICCAD-2017 CAD contest in multi-deck standard cell legalization and benchmarks

Authors: Nima Karimpour Darav, Ismail S Bustany, Andrew Kennings, Ravi Mamidi

Publication date: 2017/11/13

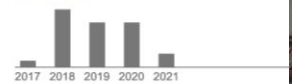
Conference: 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

Pages: 867-871

Publisher: IEEE

Description: An increasing number of multi-deck cells occupying multiple rows (e.g. multi-bit registers) are used in advanced node technologies to a
The multi-deck standard cell legalization not c
cells but also should satisfy delicate and com
quality of the given placement by applying the
process must be fast and robust to handle the
art designs. For this purpose, we have define
average cell movements, and Half Perimeter
the legalization algorithm. In addition, we hav
include multi-deck cells with a range of heigh

Total citations: Cited by 26



6. Acknowledgements

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- Mustafa Ozdal
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- Natarajan Viswanathan
- Alexander Volkov
- Yi Wang
- Benny Winefeld

- Professor Evangeline Young and her student Wing-Kai Chow generously provided their **RippleDP** detailed placer to the contest.
- Dr. Wen-Hao Liu generously provided his **NCTUgr** global router to the contest.