ISPD 2011 ROUTABILITY-DRIVEN PLACEMENT CONTEST

NATARAJAN VISWANATHAN

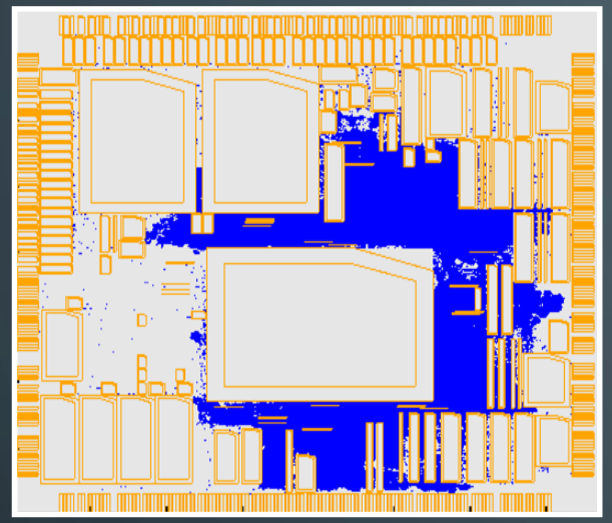
CADENCE DESIGN SYSTEMS, INC.

ISPD 2011 CONTEST AND BENCHMARK SUITE

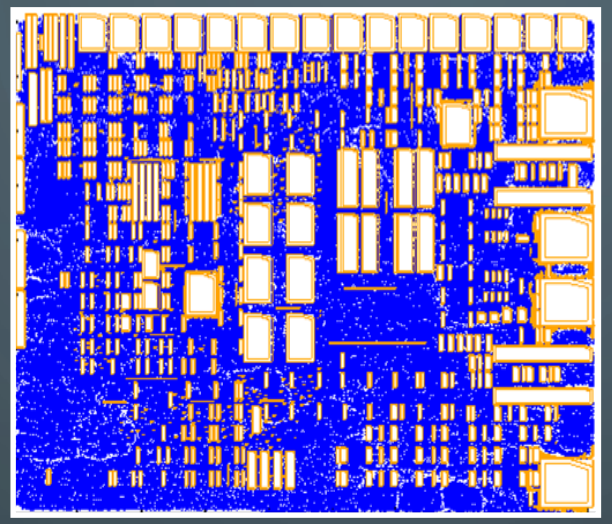
- Contest Organizers
  - Natarajan Viswanathan, Charles J. Alpert, Cliff Sze, Zhuo Li, Gi-Joon Nam, and Jarrod A. Roy
  - IBM Corporation, Austin, TX

MOTIVATION AND KEY OBJECTIVES

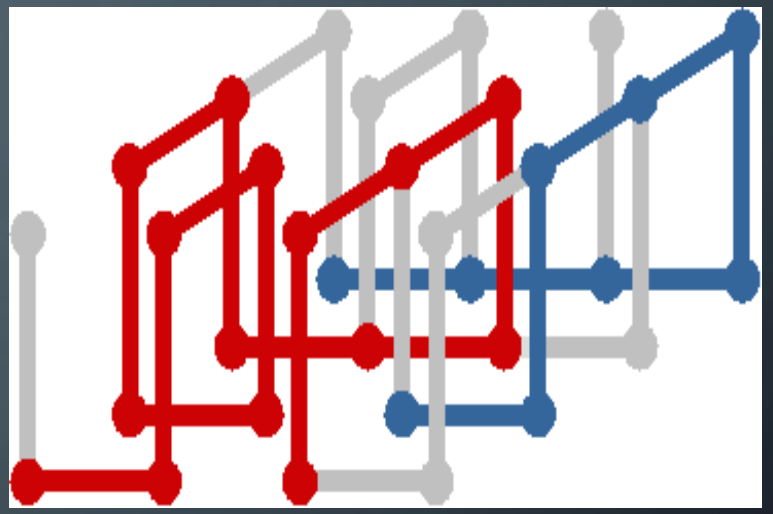
MOTIVATION



ISPD 2005: Placement
- Wire length



ISPD 2006: Placement
- Wire length and cell density

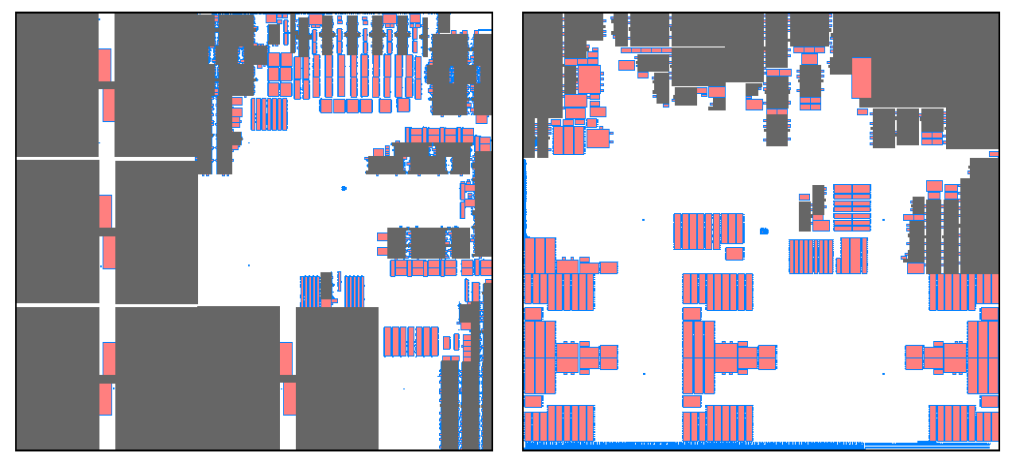


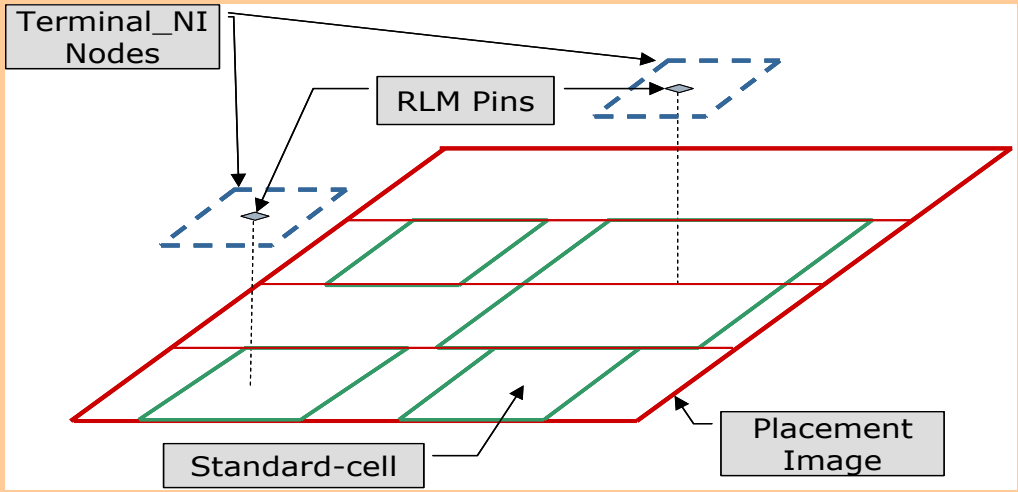
ISPD 2007/2008: Global Routing
- Multi-layer global routing – overflow minimization

- Ultimately designs need to be routable!
- How do we evaluate routability?
- Can placement and routing be completely independent?
- Routability-driven Placement: How do we effectively combine placement and routing?

ISPD 2011 CONTEST: OBJECTIVE 1

Advanced Industrial Benchmarks

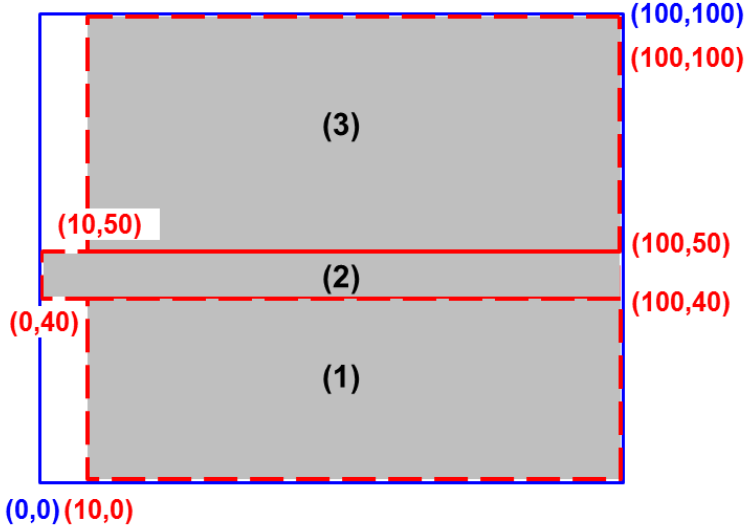




M1 – M4: 1x width and spacing

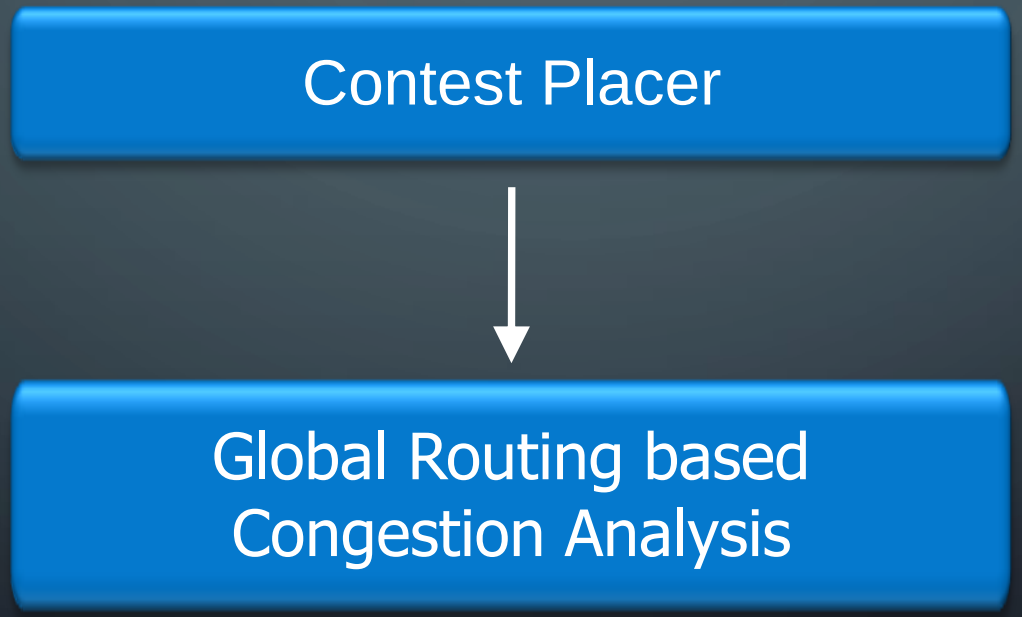
M5 – M7: 2x width and spacing

M8 – M9: 4x width and spacing



ISPD 2011 CONTEST: OBJECTIVE 2

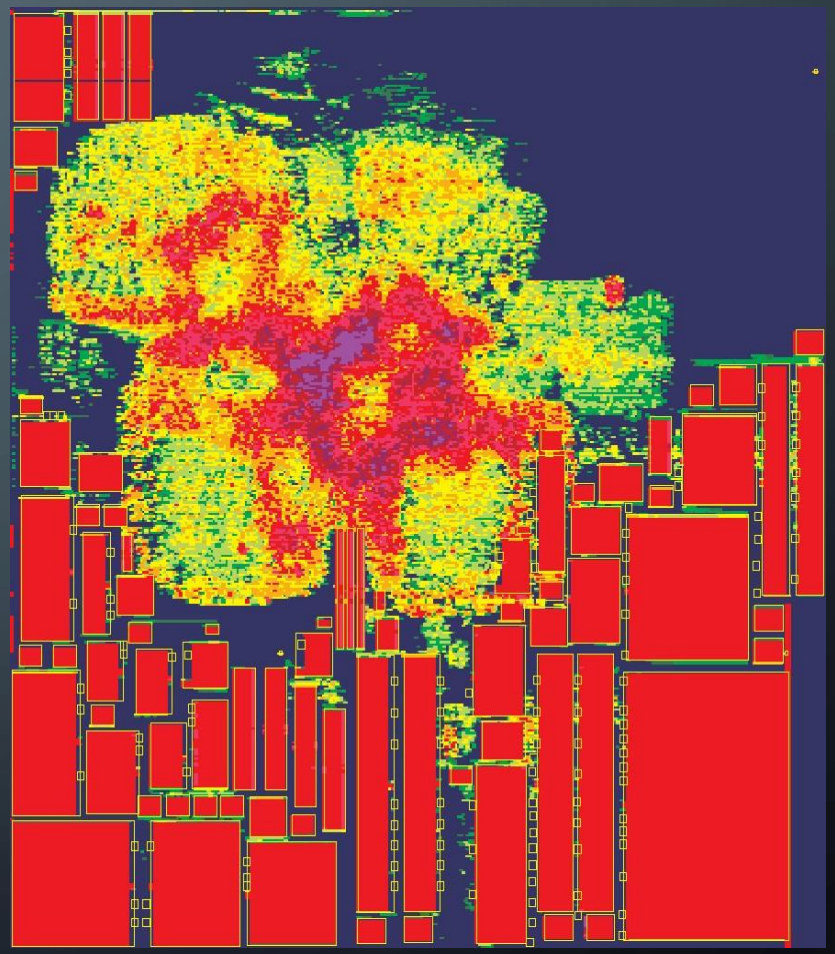
Accurate Congestion Analysis Framework



ISPD 2011 BENCHMARK SUITE

HIGHLIGHTS

- Real industrial ASIC designs from IBM
- Extended the Bookshelf design format
  - Enable placement and routing
- Placement blockages
  - Fragmented image space
- Routing blockages
  - Detouring during global route
  - Capacity overflow calculation
- Varying metal width and spacing
  - Layer assignment
  - Capacity overflow calculation



STATISTICS

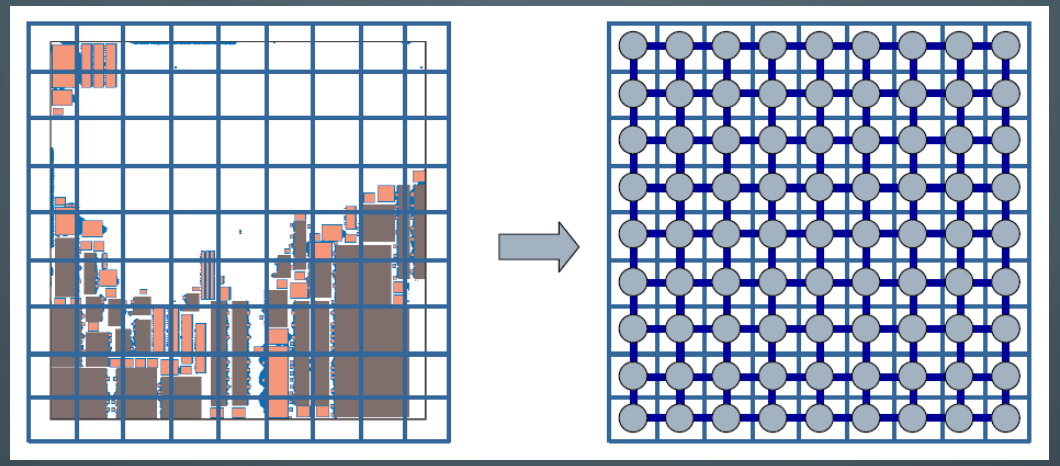
Design	Total Nodes	Movable Nodes	Terminal Nodes	Terminal_NI Nodes	Total Nets	Total Pins	Design Util.(%)	Design Den.(%)
superblue18	483452	442405	25063	15984	468918	1864306	67	47
superblue4	600220	521466	40550	38204	567607	1884008	70	44
superblue5	772457	677416	74365	20676	786999	2500306	77	37
superblue1	847441	765102	52627	29712	822744	2861188	69	35
superblue2	1014029	921273	59312	33444	990899	3228345	76	28
superblue15	1123963	829614	252053	42296	1080409	3816680	73	60
superblue10	1129144	914921	153595	60628	1085737	3665711	75	35
superblue12	1293433	1278084	8953	6396	1293436	4774069	56	44

CONTEST EVALUATION

EVALUATION TOOL

- Used an actual global routing tool for congestion analysis
- Requirements
  - Handle the new benchmarks with a complex layer stack
  - Reasonable runtime
  - Moderate overflow reduction
  - Stable
- Contest within a contest!
  - Evaluated five academic global routing tools on multiple designs / placements with varying congestion profiles
  - Calibrated using in-house congestion analysis tool

EVALUATION METRIC: TOTAL OVERFLOW OF ROUTING SOLUTION

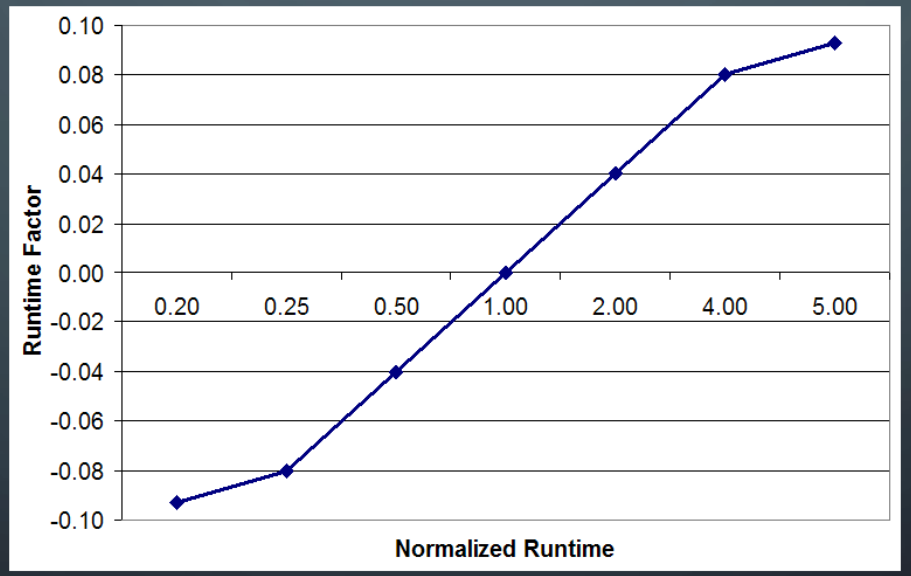


- For a tile edge on a particular layer
  - Capacity: Max allowed number of tracks
  - Demand: Actual routing demand in tracks
  - Edge_Overflow = MAX(0, (Demand – Capacity)) × (Wire_Width + Wire_Spacing)
- Total_Overflow = $\sum$ Edge_Overflow

EVALUATION METRIC: RUNTIME

- Normalized Runtime = $\frac{\text{Placer\_Wall\_Time}}{\text{Median\_Wall\_Time}}$

- Runtime Factor



±4% advantage for a 2X speed-up/slow-down
(capped at ±10% advantage)

OVERALL QUALITY METRIC

- Primary Metric
  - Scaled Total Overflow = Total_Overflow × (1 + Runtime_Factor)
- Secondary Metric
  - Scaled Tile-to-tile Routed Wire Length = Routed_WL × (1 + Runtime_Factor)

EXTENSIONS AND IMPACT

EXTENSIONS

- DAC 2012 Contest – Routability-driven Placement
  - More benchmark designs
  - Improved metric to measure global routing congestion
  - Quality metric based on scaled wire length considering routing congestion and runtime
- ICCAD 2012 Contest – Routability-driven Placement
  - Also model pin density and local wiring congestion
  - Released the design hierarchy

IMPACT

The ISPD-2011 routability-driven placement contest and benchmark suite

Authors: Natarajan Viswanathan, Charles J Alpert, Cliff Sze, Zhuo Li, Gi-Joon Nam, Jarrod A Roy

Publication date: 2011/3/27

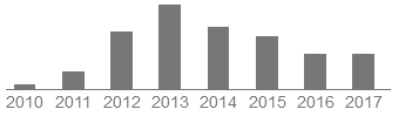
Conference: 2011 ACM International Symposium on Physical Design

Pages: 141-146

Publisher: ACM

Description: The last few years have seen significant adva
This is in part due to the availability of large, c
ISPD-2005 [17] and ISPD-2006 [16] placemer
evaluated the placers based on the half-perim
length is an important metric, it still does not a
placement algorithms, namely, the ability to pr

Total citations: Cited by 100



The DAC 2012 Routability-driven placement contest and benchmark suite

Authors: Natarajan Viswanathan, Charles Alpert, Cliff Sze, Zhuo Li, Yaoguang Wei

Publication date: 2012/6/3

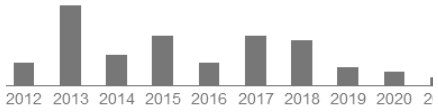
Conference: 49th ACM/EDAC/IEEE Design Automation Conference, 2012

Pages: 774-782

Publisher: ACM

Description: Existing routability-driven placers mostly employ rudi
models that fail to account for the complexities in mo
non-uniform wiring stacks, layer directives, partial an
etc. In addition, they are hampered by congestion me
represent design congestion. This is in large part due
designs depicting industrial wiring stacks and other c
routability. The aim of the DAC 2012 routability-driver
these issues, by way of the following: (a) release cha
are derived from modern industrial ASICs, and conta
placement and routing, (b) present a new congestion
congestion analysis framework to evaluate and comp

Total citations: Cited by 78



ICCAD-2012 CAD contest in design hierarchy aware routability-driven placement

Authors: Natarajan Viswanathan, Charles Alpert, Cliff Sze, Zhuo Li, Yaoguang Wei

Publication date: 2012/11

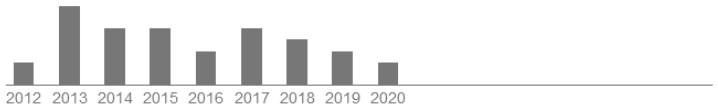
Conference: 2012 IEEE/ACM International Conference on Computer-Aided Design

Pages: 345-348

Publisher: IEEE

Description: The impact of considering design hierarchy during physical synthesis remains a fairly under-researched area. This is especially true for large-scale circuit placement. This is in large part due to the non-availability of realistic public designs with the design hierarchy information. Additionally, modern designs are fairly complex with numerous placement blockages, non-uniform wiring stacks, partial and/or complete routing blockages, etc. This significantly complicates both, the placement and routing steps of physical synthesis. The aim of the ICCAD-2012 contest is to evaluate the impact of considering design hierarchy on the wire length and routability of placement. This is addressed by way of the following: (a) release industrial-strength place-and-route benchmarks that contain the design hierarchy information, (b) present an accurate congestion analysis framework to evaluate and compare the routability of various ...

Total citations: Cited by 37



CONCLUSIONS

- Industrial benchmarks reflecting complexity of nanometer-scale placement & routing
- Standardized and accurate framework to evaluate routability of placement solutions
- Advanced academic research in multiple areas
  - Global and detailed routability-driven placement
  - Global routing
  - Fast and accurate congestion analysis / routability prediction
- Better aligned academic research with industry requirements