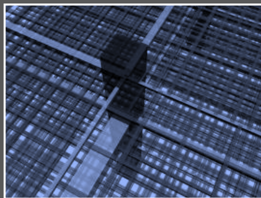
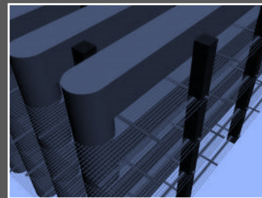
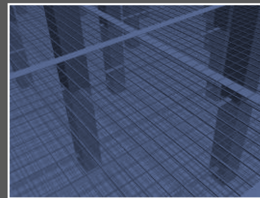
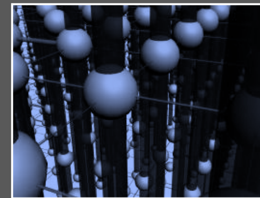
Physical Design Challenges and Solutions for Emerging Heterogeneous 3D Integration Technologies

Lingjun Zhu and Sung Kyu Lim (Presenter)

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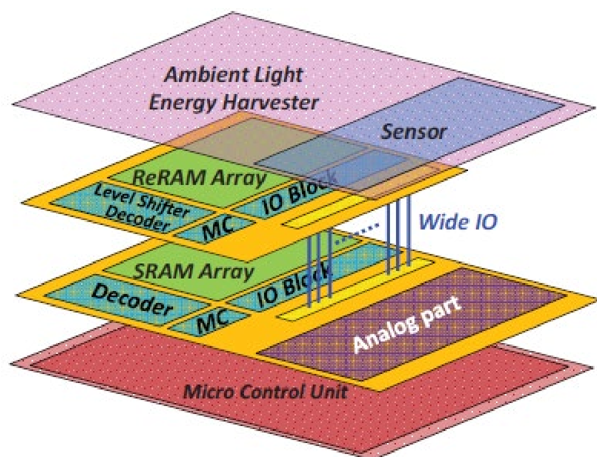
Outline

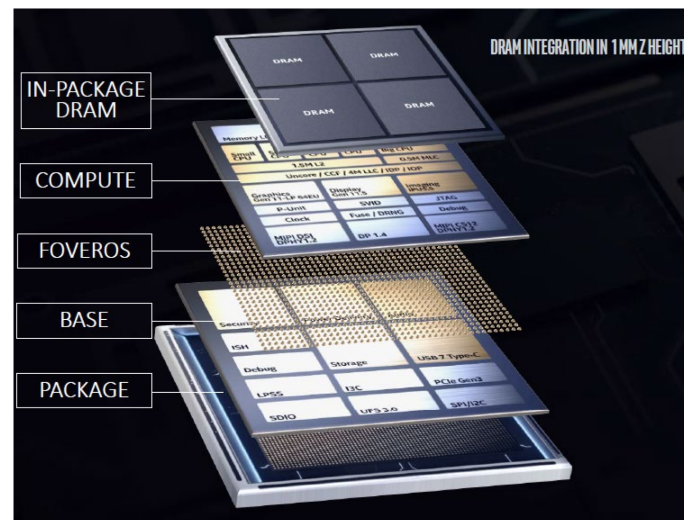
- Introduction
- Overview of Heterogeneous 3D Integration Technologies
- Physical Design Challenges in Heterogeneous 3D
- Physical Design Solutions in Heterogeneous 3D
- Future studies
- Conclusions

Motivations
Heterogeneous 3D has come

- Heterogeneous 3D is ready for commercial-level products
  - Provides benefits in system performance, leakage power, package area…
- Are physical design methodologies ready?



▲ Heterogeneous monolithic 3D IC proposed in [1]



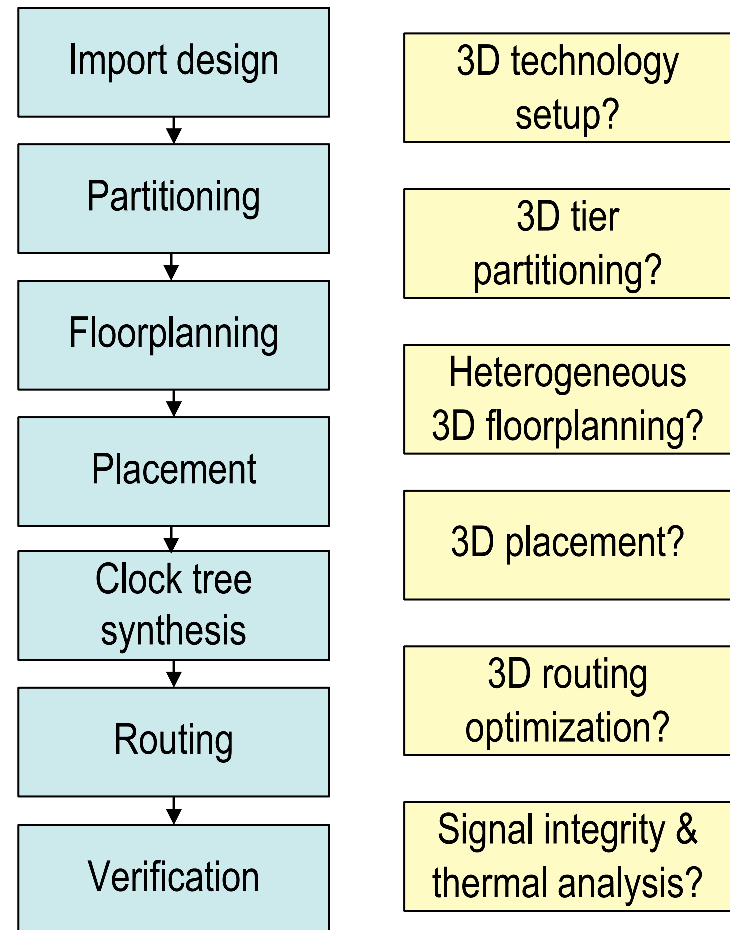
▲ Intel Lakefield heterogeneous 3D chip [2]

[1] Wu, Tsung-Ta, et al. "Low-cost and TSV-free monolithic 3D-IC with heterogeneous integration of logic, memory and sensor analogy circuitry for Internet of Things." 2015 IEEE International Electron Devices Meeting (IEDM). IEEE, 2015.

[2] S. Khushu, W. Gomes, Lakefield: Hybrid cores in 3D Package, Intel, Accessed on: Feb. 28, 2021. Available: https://newsroom.intel.com/wp-content/uploads/sites/11/2019/08/Intel-Lakefield-HotChips-presentation.pdf

Motivations
Physical design challenges

- **Existing physical design flows mainly target 2D/homogeneous 3D**
  - **Most of the tool cannot handle multiple process nodes**
  - **2D P&R engine cannot be used directly for heterogeneous 3D**
    - **Cell placement is optimized based on XY dimensions only**
    - **Routing is more complicated with the heterogeneous BEOL stack**
  - **High-density 3D interconnects are hard to handle manually**
  - **In need of EDA tools for signal integrity and thermal verifications**

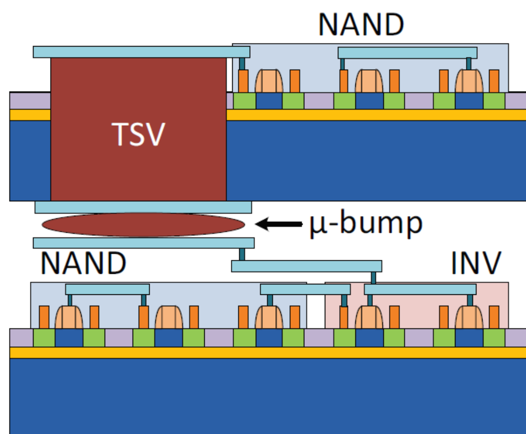


▲ A conventional physical design flow and potential challenges

Introduction
3D integration technologies

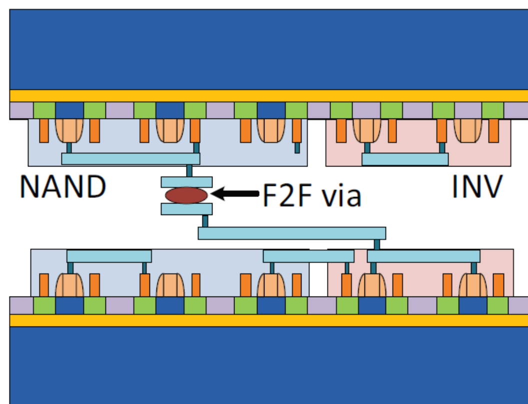
- Various 3D technologies can be used for heterogeneous 3D

higher interconnect density



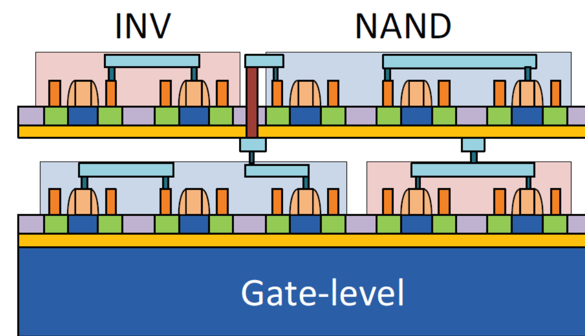
▲ TSV-based 3D

- ❑ Mature fabrication process
- ❑ High area overhead
- ❑ High RC parasitics



▲ F2F-bonded 3D

- ❑ No area overhead
- ❑ Low fabrication cost
- ❑ Electrical and thermal coupling issues



▲ Monolithic 3D [3]

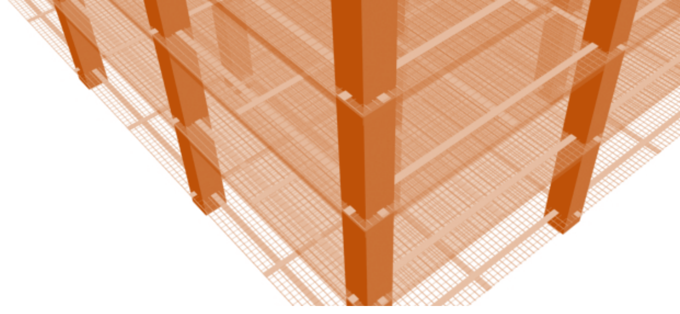
- ❑ High integration density
- ❑ Small RC parasitics
- ❑ High manufacturing requirements

[3] Panth, Shreepad A., et al. "Design and CAD methodologies for low power gate-level monolithic 3D ICs." Proceedings of the 2014 international symposium on Low power electronics and design. 2014.

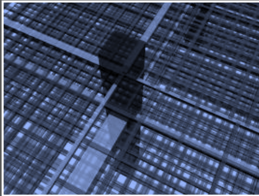
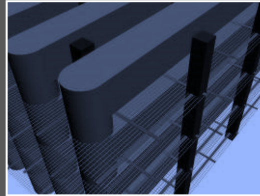
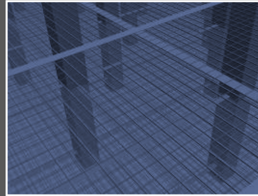
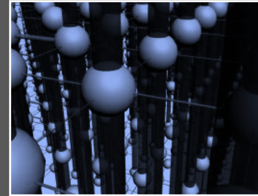
Introduction
3D integration technologies

- **Different levels of heterogeneous integration**
  - **Heterogeneous architecture: integrate heterogeneous cores in 3D**
  - **Heterogeneous technology nodes: integrate multiple process nodes**
  - **Heterogeneous floorplan: separate logic and memory blocks to two tiers**

▲ A conceptual view of different levels of heterogeneous 3D integration

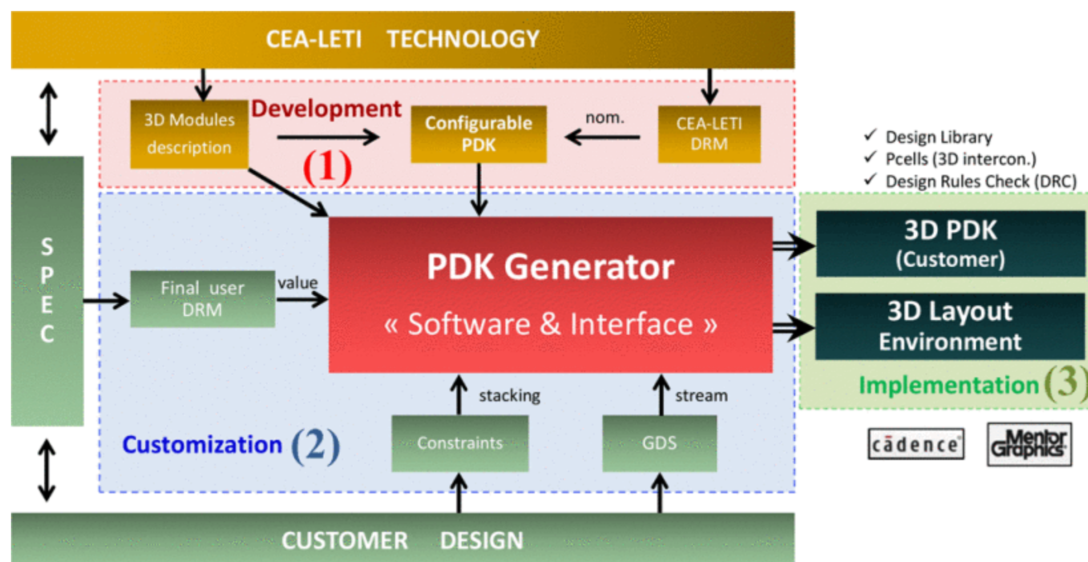


Physical Design Challenges in Heterogeneous 3D

Physical Design Challenges
Heterogeneous 3D technology setup

- It is challenging to represent heterogeneous 3D FEOL and BEOL
  - Multiple device layers, different process nodes, 3D metal stack
- Conventional 2D EDA tools do not support 3D technology natively
  - E.g., DEF and LEF formats support only one device layer
- Hard to create a real 3D PDK: require complete SPEC and cell design

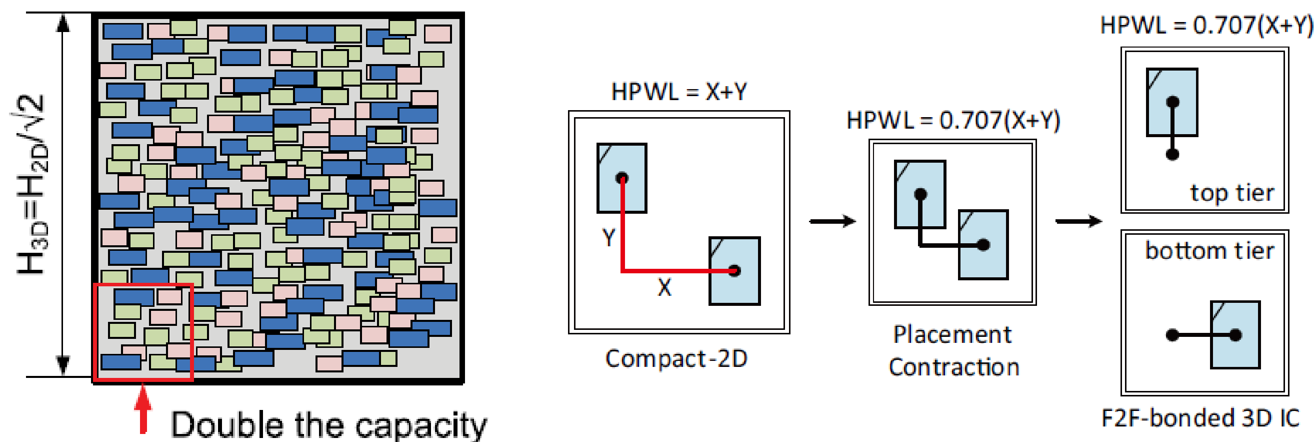


▲ A flow to generate 3D PDK proposed in [4]

[4] Cibrario, Gerald, et al. "A 3D process design kit generator based on customizable 3D layout design environment." 2013 IEEE International 3D Systems Integration Conference (3DIC). IEEE, 2013.

Physical Design Challenges
Heterogeneous 3D technology setup

- Technology setup in existing pseudo-3D flows may introduce errors
  - Pseudo-3D flows trick the 2D EDA tools into implementing 3D ICs by modifying the technology files
    - Shrunk-2D flow [1] shrinks the cell and wire dimensions by 0.7
    - Compact-2D flow [2] uses the original cells and wires, but scale unit RC by 0.7
  - Dimension and RC scaling introduces errors in placement and parasitic extraction, and cannot represent multiple process nodes directly



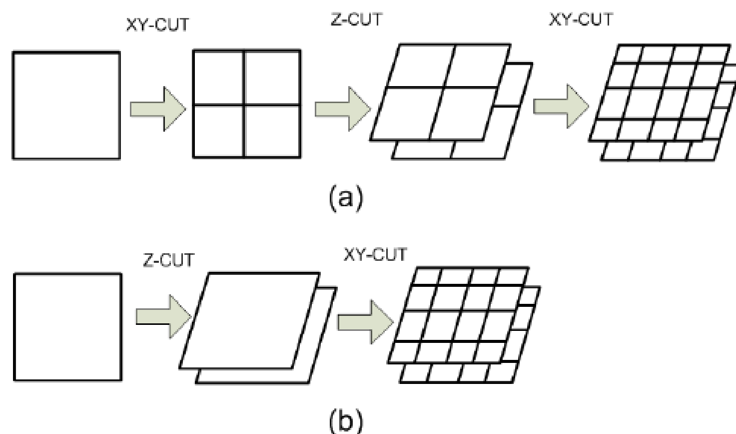
[4] Panth, S. et al. (2015). Placement-driven partitioning for congestion mitigation in monolithic 3D IC designs. IEEE Trans. Computer-Aided Design, 34(4), 540-553.

[5] Ku, B. W. et al. (2018, March). Compact-2D: A physical design methodology to build commercial-quality face-to-face-bonded 3D ICs. In Proceedings of the 2018 Int. Symp. Physical Design (pp. 90-97).

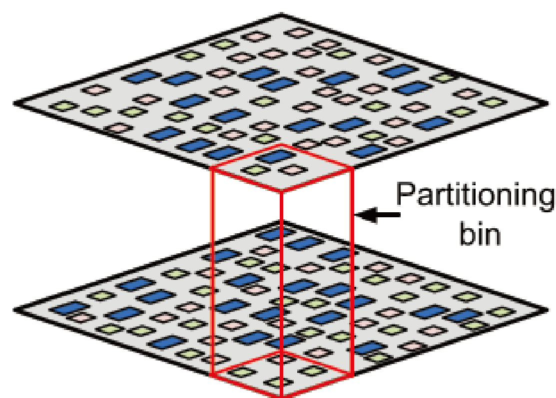
▲ Shrunk-2D technology setup [4] ▲ Compact-2D technology setup [5]

Physical Design Challenges
Heterogeneous 3D tier partitioning

- Conventional partitioning approaches do not distinguish cells
  - They cannot separate logic from memory and do not consider process nodes
    - Recursive partitioning [6] can control the cutsize but not cell type on each tier
    - Bin-based min-cut partitioning [4] applies the area-balance constraint, but does not consider the process node or function of the cells
  - Need to incorporate more cell metrics for heterogeneous 3D tier partitioning
    - Microarchitecture, process node, cell timing, etc.



▲ Recursive partitioning procedures [6]

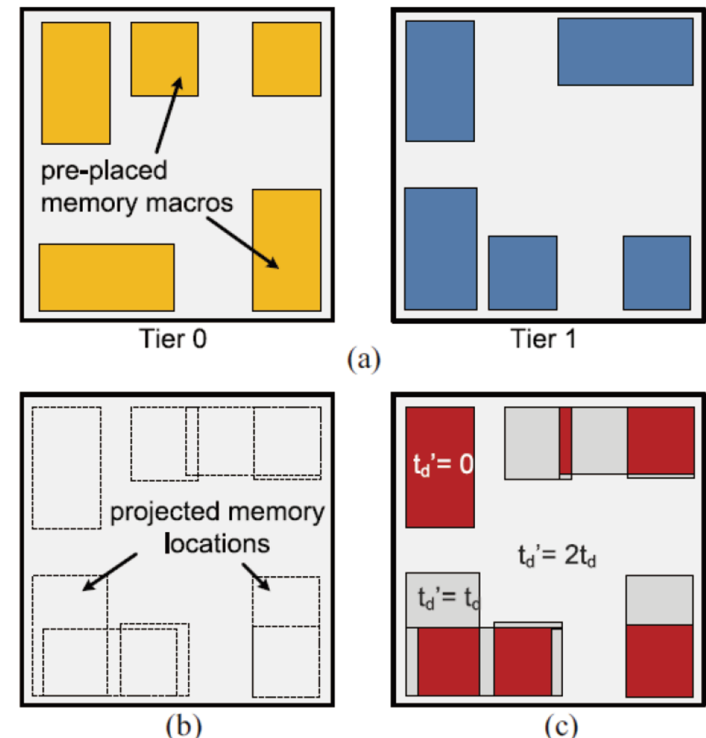


▲ Bin-based min-cut partitioning [4]

[6] Pathak, Mohit, et al. "Through-silicon-via management during 3D physical design: When to add and how many?." 2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2010.

Physical Design Challenges
Heterogeneous 3D P&R

- **Die-by-die routing leads to timing degradation**
  - In pseudo-3D flows, each die is routed separately after tier partitioning
  - Timing constraint and load cap. estimation can cause timing degradation
- **Heterogeneous floorplan proposes challenges for 3D P&R flows**
  - One tier is completely occupied by memory blocks, the other tier is for cell placement
  - If using partial placement blockage,
    - Blockage is not strictly honored in P&R
    - Cell may overlap after rescaling and worsen timing

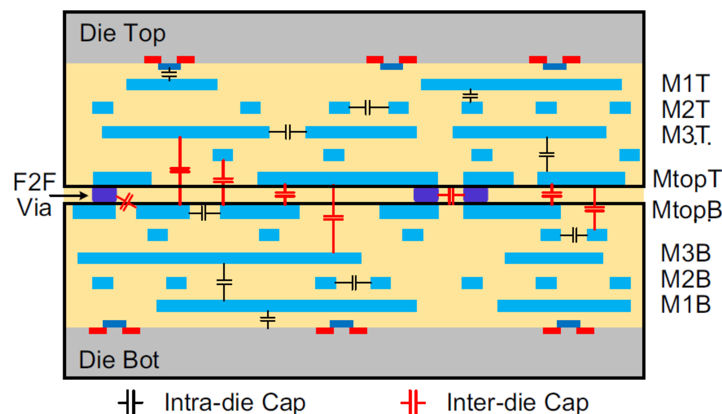


▲ Handling memory in Shrunk-2D [4]

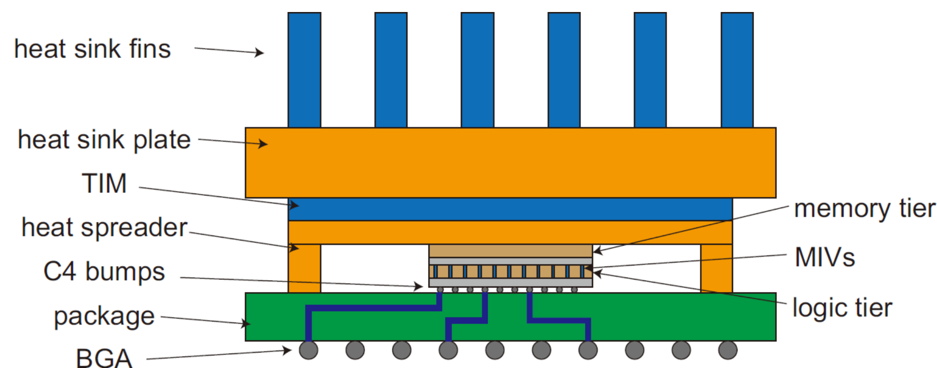
[4] Panth, S. et al. (2015). Placement-driven partitioning for congestion mitigation in monolithic 3D IC designs. IEEE Trans. Computer-Aided Design, 34(4), 540-553.

Physical Design Challenges
Heterogeneous 3D verification

- **Signal integrity and thermal analysis are crucial for 3D ICs**
  - Inter-die coupling and crosstalk are non-negligible for F2F 3D ICs
    - Conventional die-by-die parasitic extraction cannot capture inter-die coupling
  - Temperature increases in 3D due to higher power density and smaller area
    - Need a complete 3D thermal model to analyze the entire system
  - Power and temperature distribution is unbalanced with heterogeneous technology nodes and floorplan



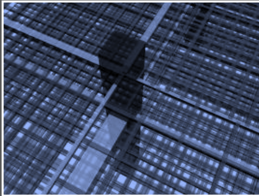
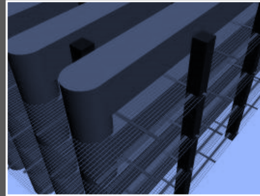
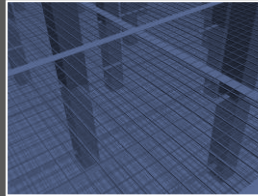
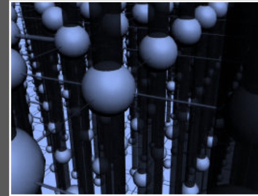
▲ Electrical coupling in a F2F 3D IC [7]



▲ A thermal model for memory-on-logic 3D ICs

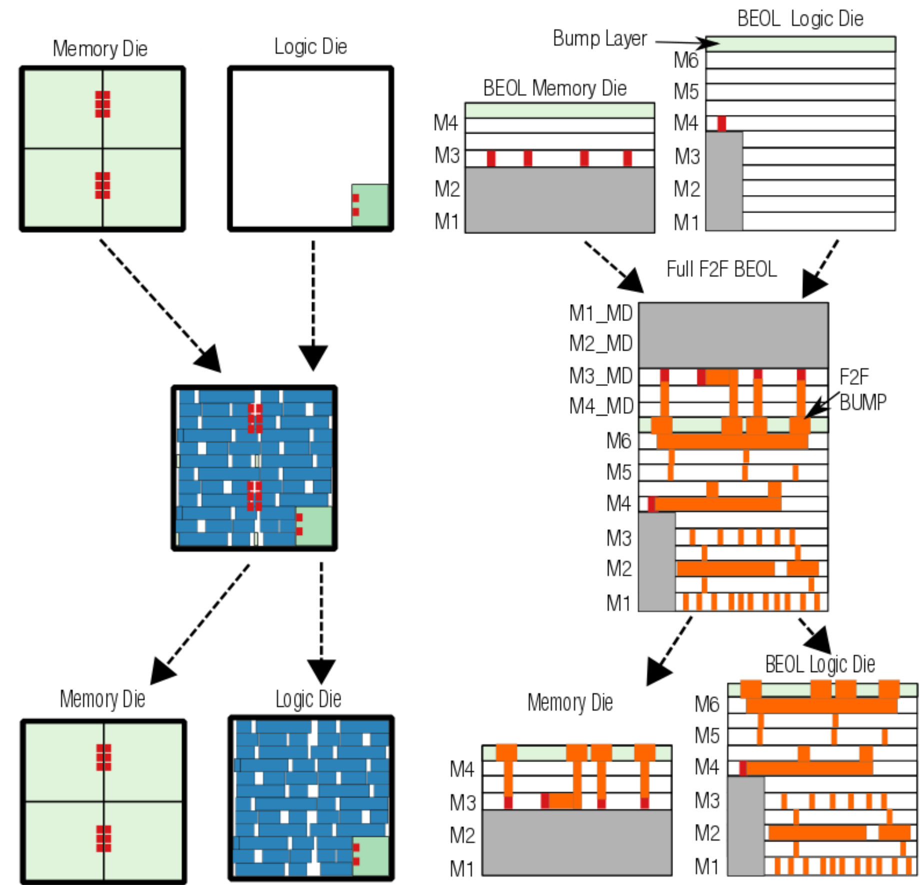
[7] Peng, Yarui, et al. "Full-chip inter-die parasitic extraction in face-to-face-bonded 3D ICs." 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2015.

Physical Design Solutions for Heterogeneous 3D

Physical Design Solutions
Heterogeneous 3D technology setup

- Create memory-on-logic stack
  - Combine BEOL from both dies
    - Use the info from LEF and ICT
    - Add F2F bump layer in between
  - Minimize memory macros
    - Memory pins remain untouched
    - They can be placed along with standard cells on a 2D plane
  - Enable heterogeneous 3D
    - Utilize different materials for top and bottom BEOL
    - Create unbalanced BEOL stack
      - E.g. 4 layers for the memory die, 6 layers for the logic die

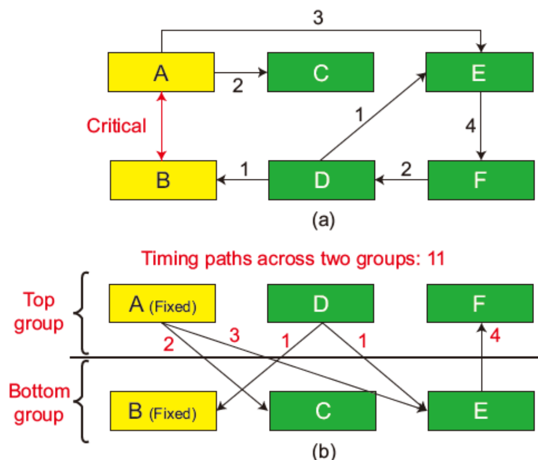


▲ Heterogeneous 3D technology setup in [8]

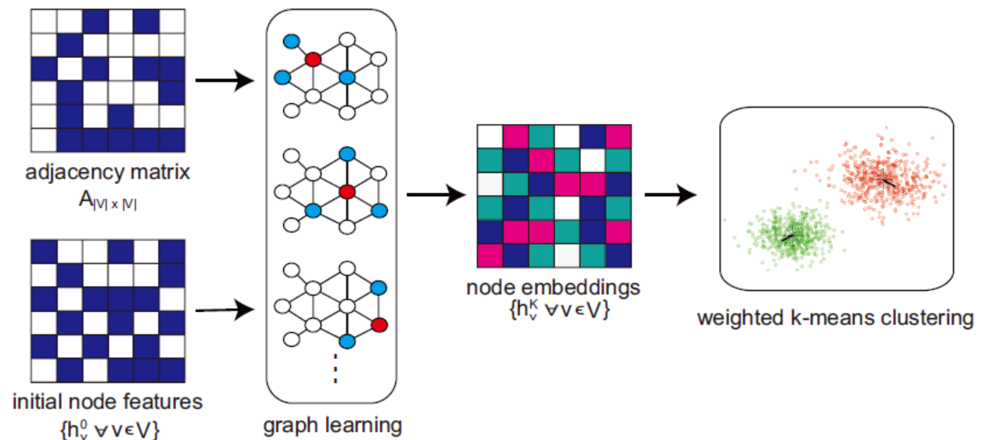
[8] Bamberg, Lennart, et al. "Macro-3D: A physical design methodology for face-to-face-stacked heterogeneous 3D ICs." 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2020.

Physical Design Solutions
Heterogeneous 3D tier partitioning

- **Memory-on-logic partitioning is straightforward**
  - **But it only applies to designs with more than 50% memory area**
- **Cascade-2D [9] uses 2D connection info to optimize partitioning**
- **TP-GNN [10] uses a graph neural network for tier partitioning**
  - **The feature vector incorporates hierarchy, timing, & connection info**



▲ **Cascade-2D partitioner [9]**



▲ **TP-GNN framework for tier partitioning [10]**

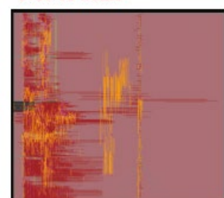
[9] Chang, Kyungwook, et al. "Cascade2D: A design-aware partitioning approach to monolithic 3D IC with 2D commercial tools." Proceedings of the 35th International Conference on Computer-Aided Design. 2016.

[10] Lu, Yi-Chen, et al. "TP-GNN: a graph neural network framework for tier partitioning in monolithic 3D ICs." 2020 57th ACM/IEEE Design Automation Conference (DAC). IEEE, 2020.

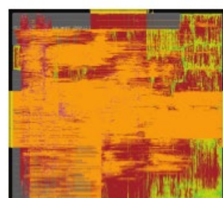
Physical Design Solutions
Heterogeneous 3D P&R

- **Macro-3D [7] is dedicated to P&R for memory-on-logic 3D**
  - Cell placement and signal routing are done by 2D tools with exact pin location
  - It achieves up to 28% frequency boost for a RISC-V core compared to 2D
- **Cascade-2D [9] overcomes timing degradation issues in Shrunk-2D**
  - Pseudo-3D routing is done for both dies simultaneously using anchor cells
  - Performance is improved by 25% at 14/16nm for a commercial processor

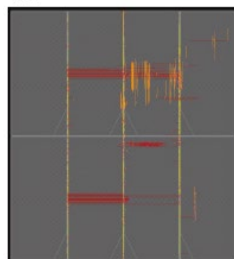
*Not to scale



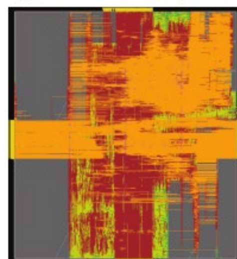
(a) Small-Cache Macro Die



(b) Small-Cache Logic Die

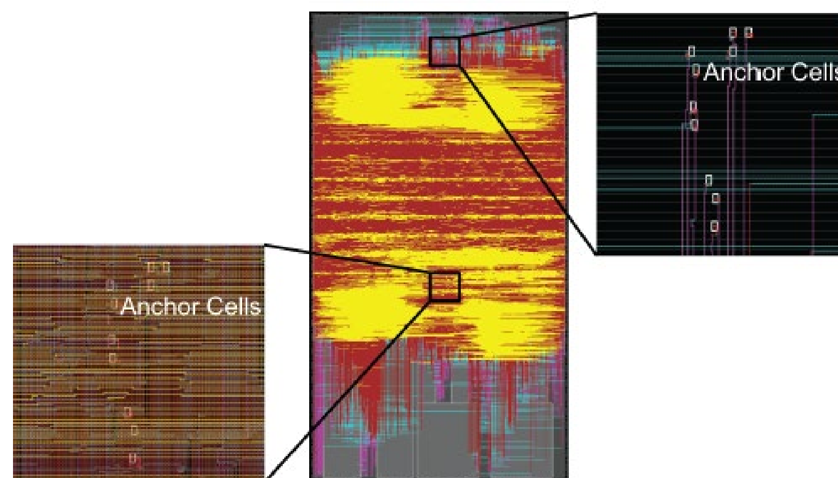


(c) Large-Cache Macro Die



(d) Large-Cache Logic Die

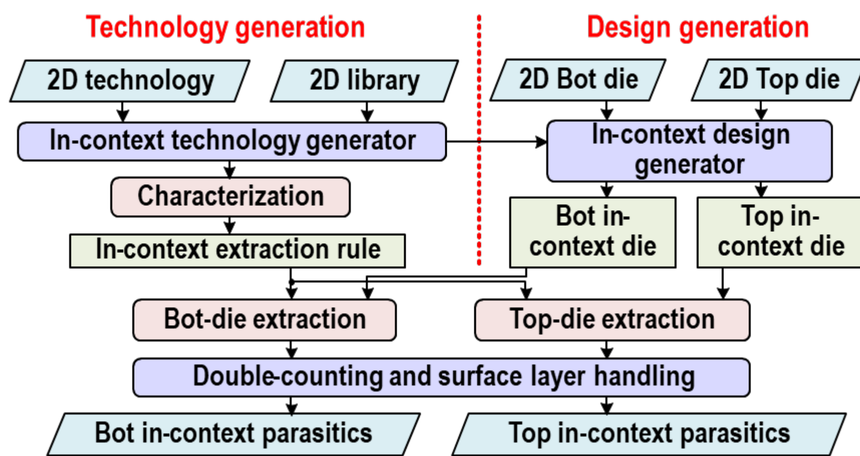
▲ Memory-on-logic 3D RISC-V core [8]



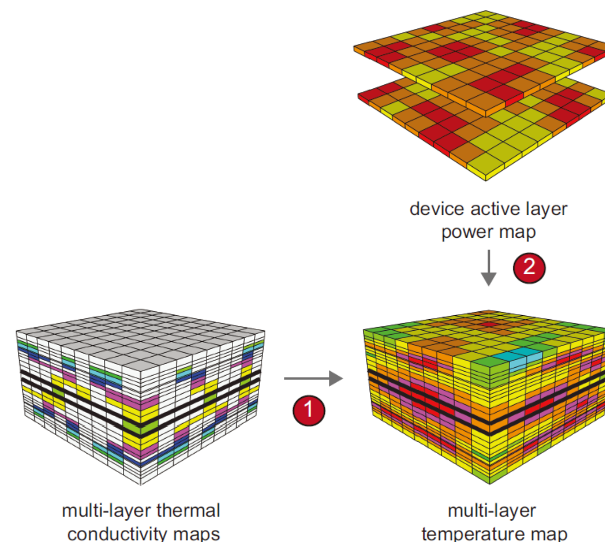
▲ Cascade-2D P&R [9]

Physical Design Solutions
Heterogeneous 3D verifications

- In-context method [7] extracts inter-die coupling with short runtime
  - Combine the interface layers to generate an in-context design for F2F 3D ICs
  - Signal integrity analysis shows capacitance and noise error is less than 6%
- Tile-based thermal analysis [11] considers thermal coupling in 3D
  - Power maps are generated for each die, and thermal conductivity is calculated for each tile

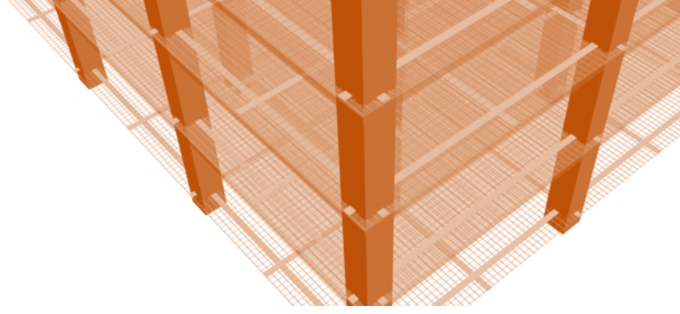


▲ In-context extraction method [7]

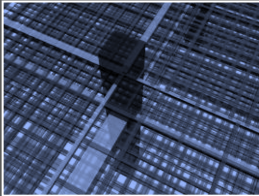
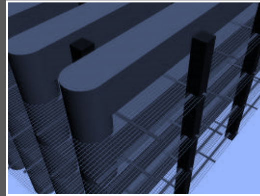
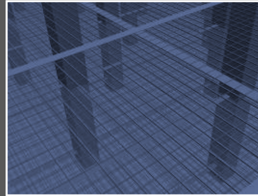
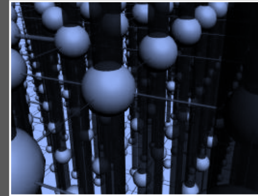


▲ Tile-based thermal analysis [11]

[11] Zhu, Lingjun, et al. "Full-Chip Electro-Thermal Coupling Extraction and Analysis for Face-to-Face Bonded 3D ICs." Proceedings of the 2020 International Symposium on Physical Design. 2020.



Future Studies and Summary

Future Studies

- Heterogeneous-3D-aware synthesis
  - Consider the heterogeneous configurations, technology nodes, and physical constraints at the synthesis stage
  - Optimize PPA using the flexibility provided by heterogeneous 3D
- True 3D PDK and placers
  - Create 3D PDK and cell libraries to provide native support for heterogeneous 3D ICs
  - Develop 3D placer to optimize cell placement with three dimensions

Summary

- Heterogeneous 3D proposes unique challenges for physical design flows due to the complex nature of the technology setup
- Previous 3D design flows do not work well with heterogeneous 3D because of low tier partitioning quality, timing degradation in P&R, and lack of verification tools
- State-of-the-art flows address these issues by modifying the technology files and tricking the 2D tools
- True 3D PDK, cell libraries, and placers are still in need for the future applications of heterogeneous 3D ICs