The EDA Lab, NTUSTEE

Lookahead Placement Optimization with Cell Library-based Pin Accessibility Prediction via Active Learning

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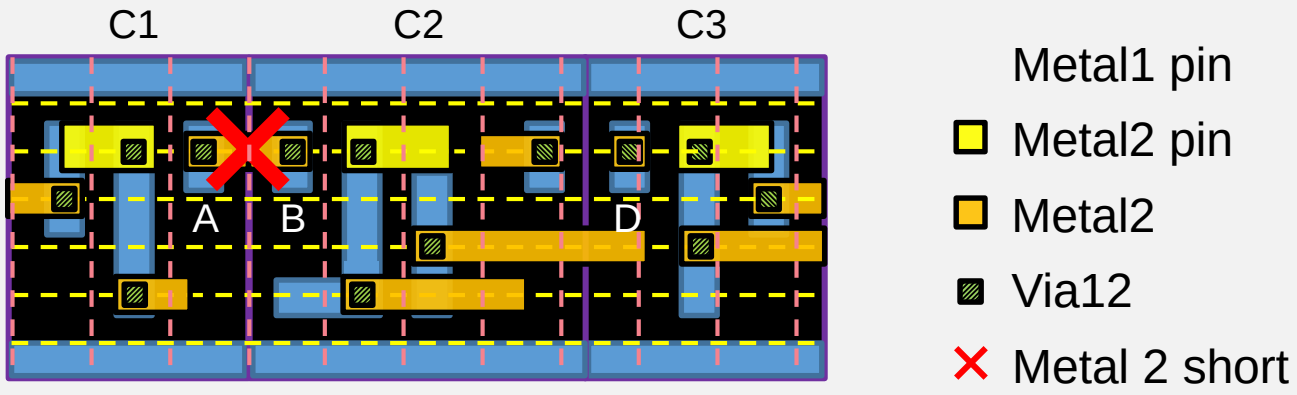
01 Introduction

DRV due to Pin Accessibility

- The trends of design features with process nodes:
  - The number of cells ↑, the sizes of standard cells ↓, routing resource ↓
- The analysis of design rule violation (DRV) occurrence in advanced nodes becomes much more challenging
  - Recent works resort to machine learning-based methods for DRV prediction
- **Poor pin accessibility** is one of the major causes resulting in DRVs

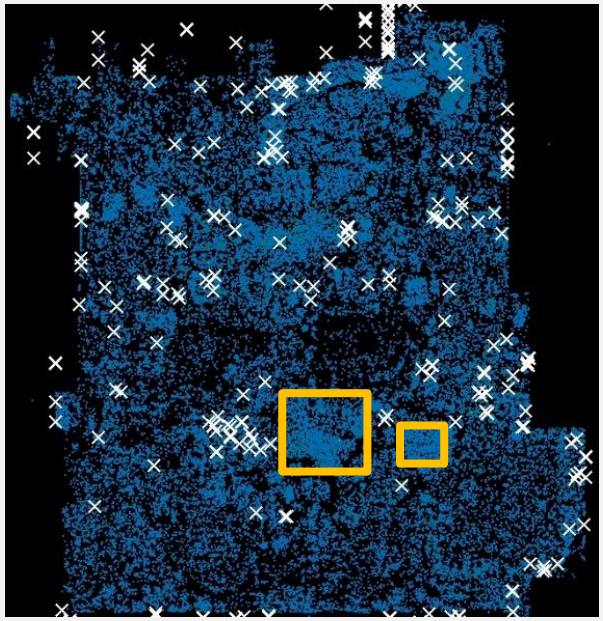


Existing Works and Methodologies

- Existing works
  - Chan et al., “BEOL stack-aware routability prediction from placement using data mining techniques,” ICCD’16
  - Tabrize et al., “Detailed routing violation prediction during placement using machine learning,” VLSI-DAT’17
  - Chan et al., “Routability optimization for industrial designs at sub-14nm process nodes using machine learning,” ISPD’17
  - Xie et al., “RouteNet: routability prediction for mixed-size designs using convolutional neural network,” ICCAD’18
  - Tabrizi et al., “A machine learning framework to identify detailed routing short violations from a placed netlist,” DAC,18
- ML models
  - Support vector machine, neural network, ensemble boosted trees, etc
- **Global routing (GR) congestion** and **pin density** are used as the main features

DRVs vs Congestion Map

- DRV occurrence may not have strong correlation with GR congestion map

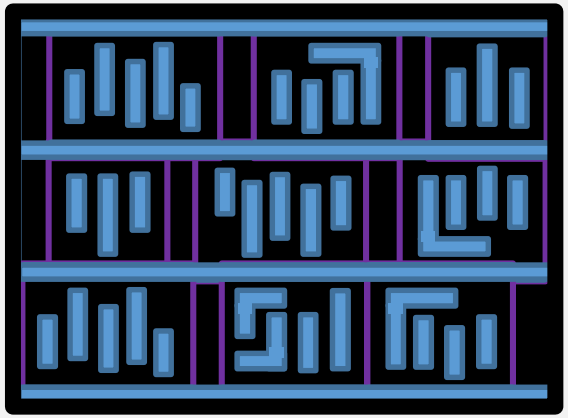


- Congested region
- Design rule violation

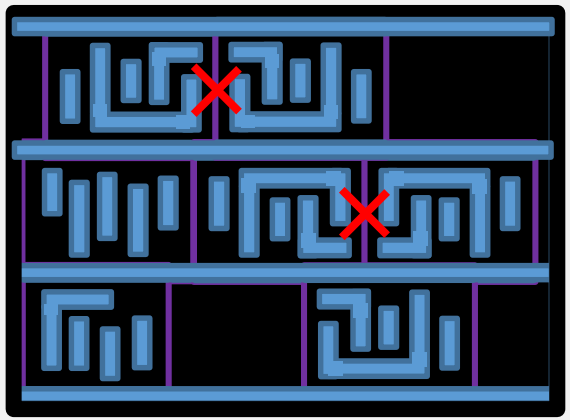
GR congestion map vs. DRV distribution

DRVs vs Pin Density

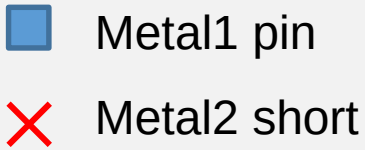
- DRVs are not dominated by the pin density
- Two windows consisting of the same set of cells (same pin density)



Pin density: 0.73



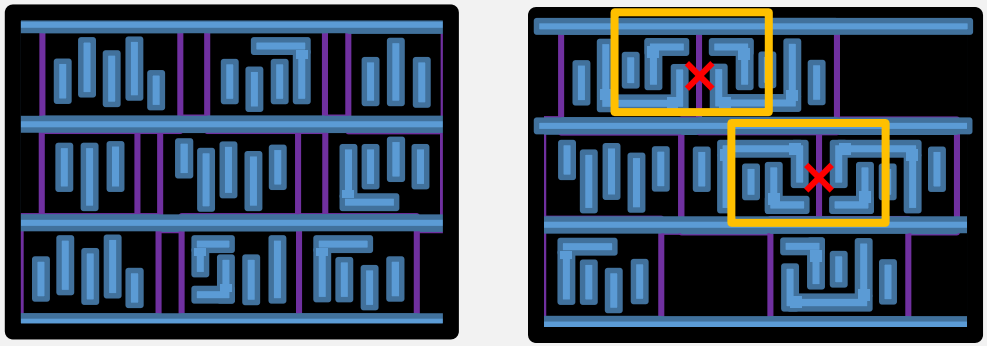
Pin density: 0.61



02 Preliminaries

DRV due to Pin Access

- Two windows consisting of the same set of cells (same pin density)

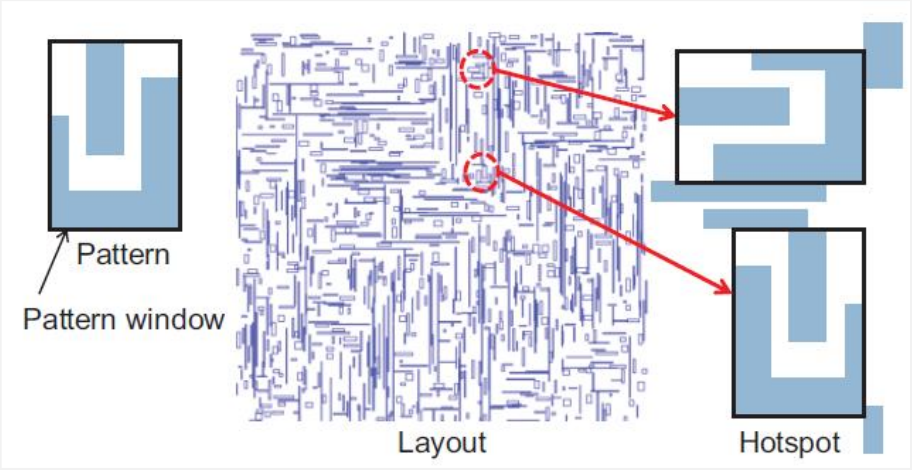


- DRVs are not dominated by the pin density
- But some **pin patterns** do have correlation with DRV occurrence
- Motivations
  - ***Predict pin access-induced DRVs using pin patterns***
  - ***Avoid generating pin patterns with bad accessibility during placement***

How to identify bad pin patterns?

Inspiration

- Identifying bad pin patterns is similar to identifying hotspots in a given layout

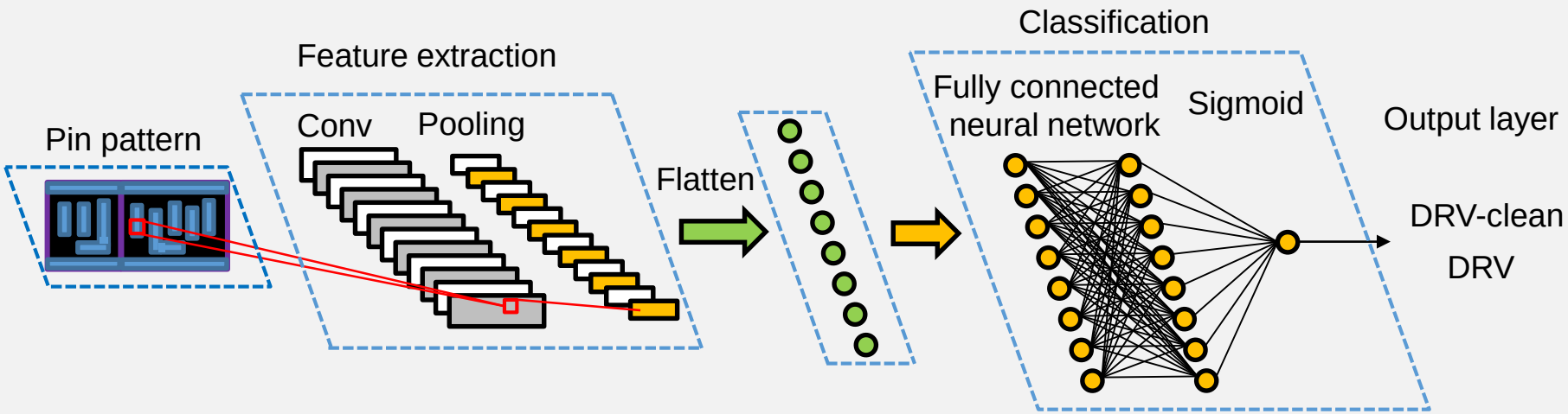


[Yu et al., DAC'12]

- Two methodologies have been adopted in hotspot detection
  - Exact pattern matching: identify layout clips exactly the same as **known hotspots**
  - **Machine learning-based methods**: able to predict **unseen hotspots** based on a prediction model trained by known hotspots

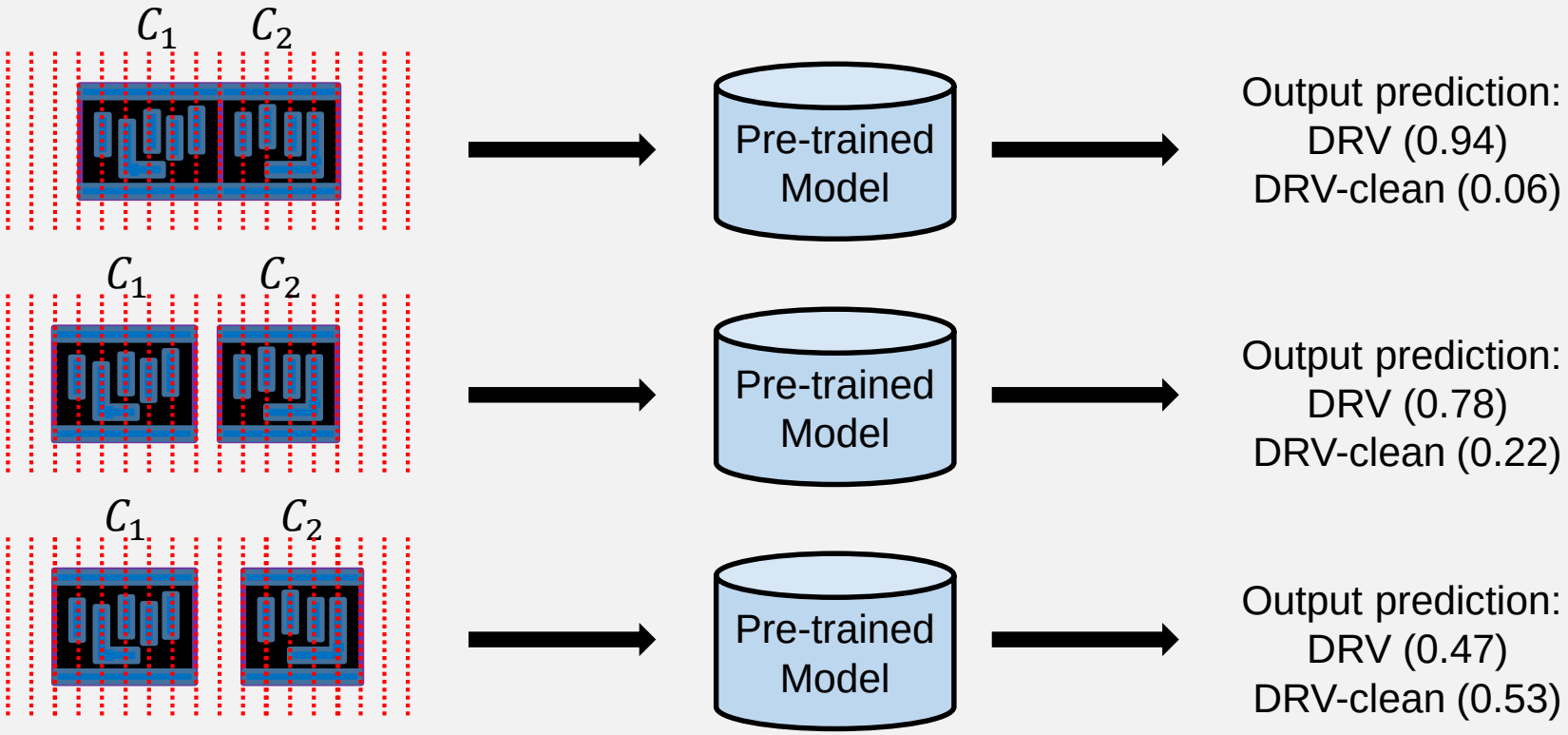
Model Training

- Convolutional neural network (CNN) is widely used in image recognition
  - Input layer: pin patterns collected from routed designs
  - Feature extraction: multiple convolution interleaved by pooling
  - Classification: neural network followed by sigmoid
  - Output layer: DRV or DRV-clean prediction



Placement Spacing Rule Generation

- Generate placement spacing rules (hard rules) to avoid generating bad pin patterns

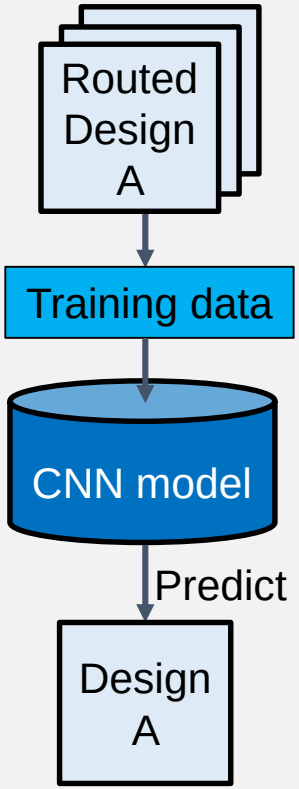


2 site of spacing is required between C_1 and C_2!!

03 Library-based DRV Prediction

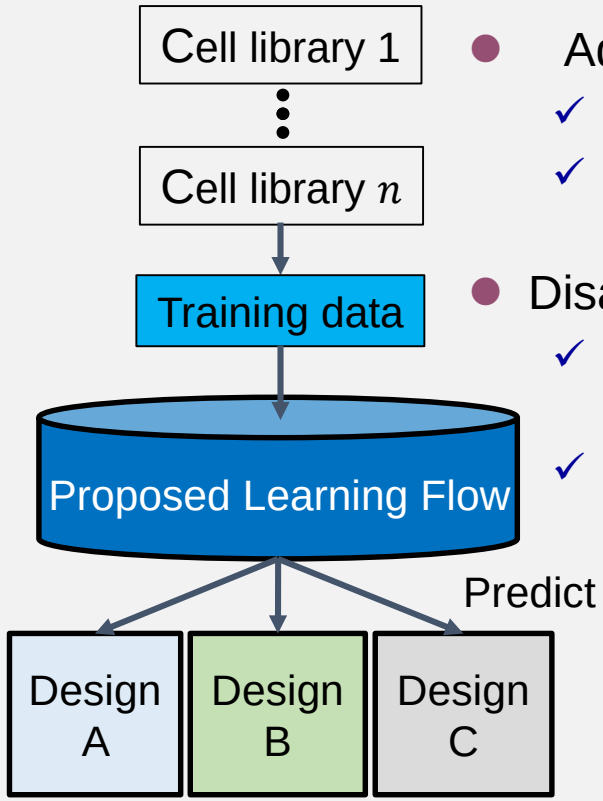
Design-specific vs Library-based Model

- Design-specific model training flow



- Advantage:
  - ✓ Intuitive in data collection
  - ✓ Less training time
- Disadvantage:
  - ✓ Large effort for data preparation
  - ✓ Design-specific

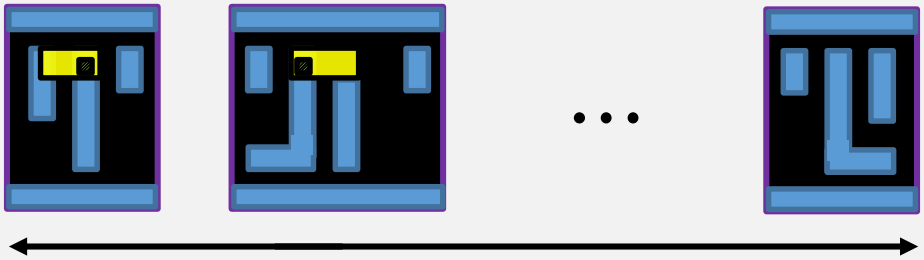
- Library-based model training flow

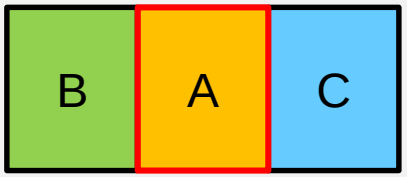


- Advantage:
  - ✓ Model reusable
  - ✓ Design-independent
- Disadvantage:
  - ✓ Long training time
  - ✓ Huge amount of data

Tackling Huge Data

- A cell library may contain thousand types of standard cells

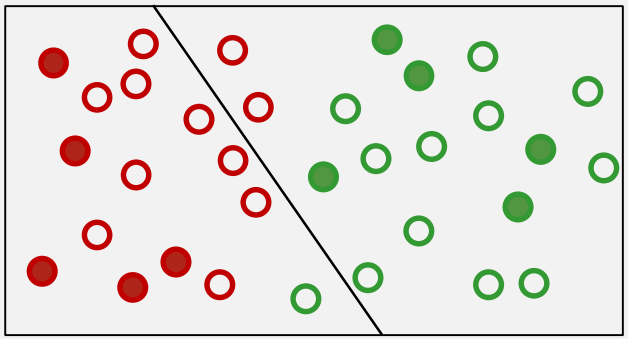




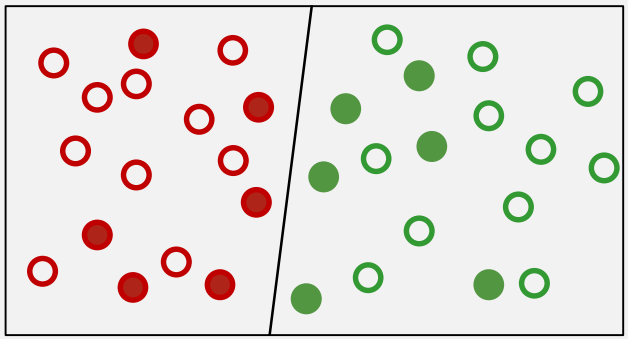
#Cell combinations: $> 1000^3$

Orientations…

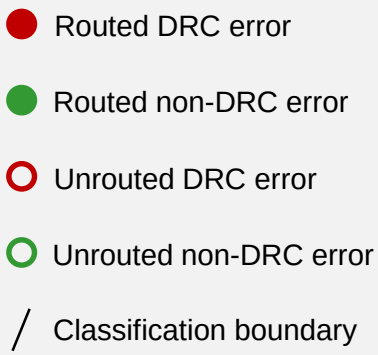
- It is desirable to develop a smart method for querying cell combinations → **Active learning!!**



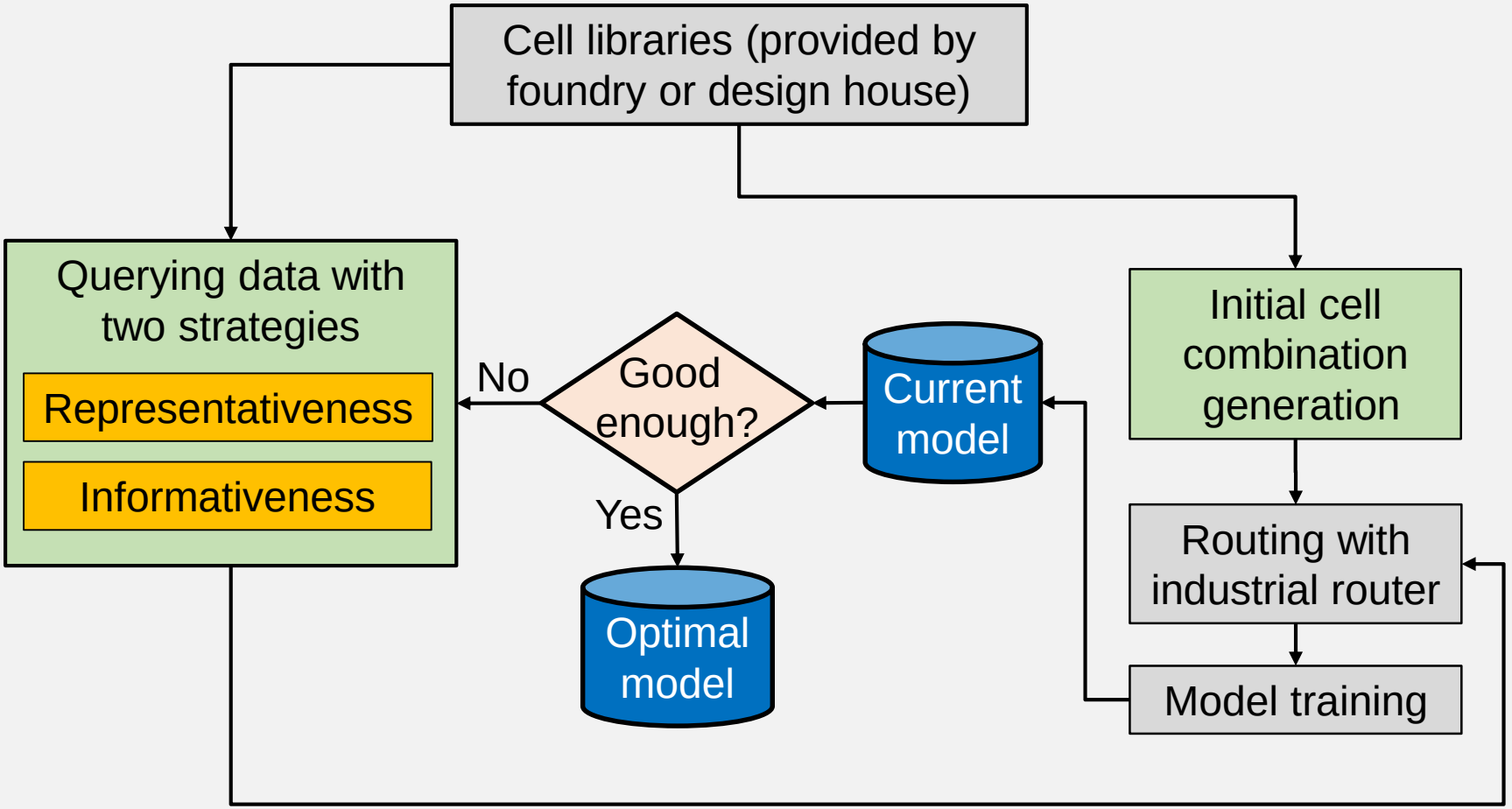
3 errors



Perfect classification

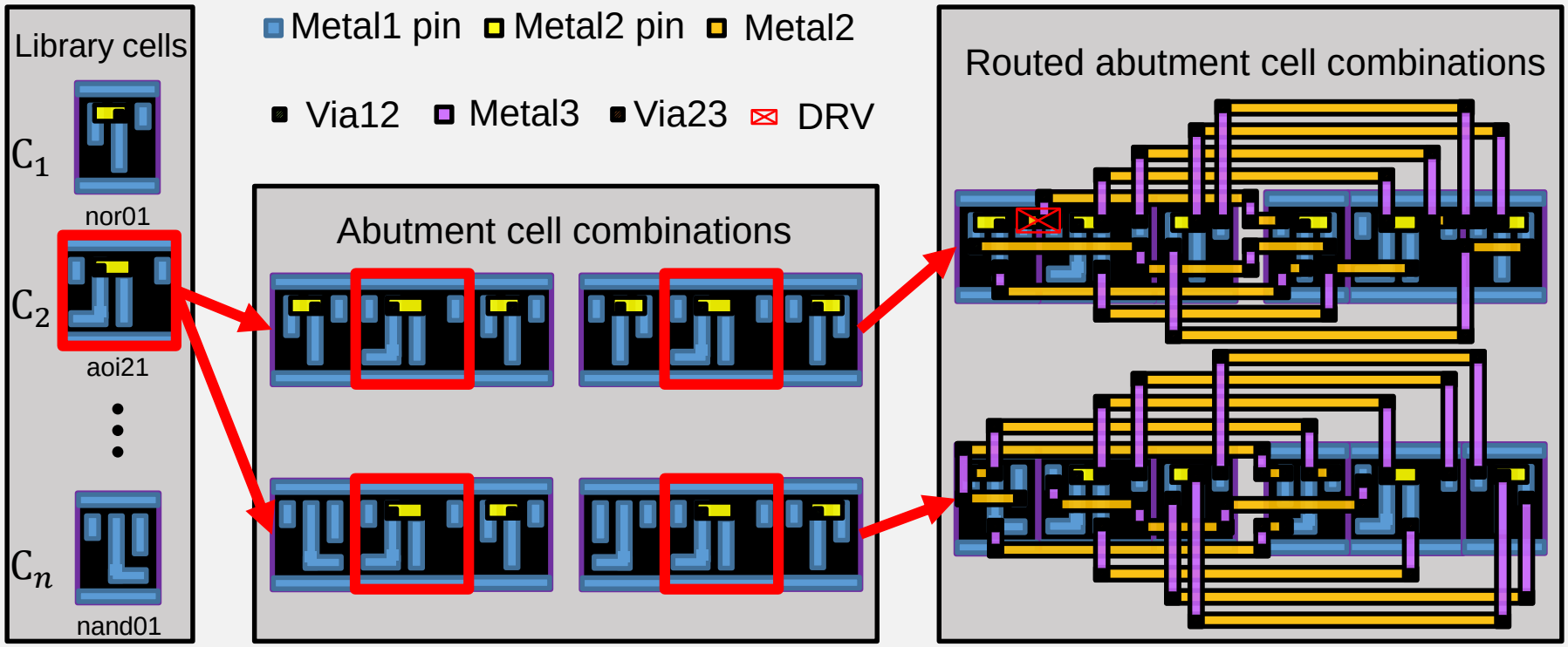


Proposed Active Learning Flow



Pin Accessibility Evaluator

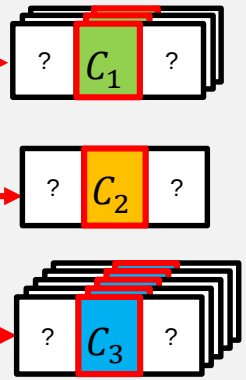
- Randomly query some cell combinations to train initial model



Representativenss

- Determine **the number of routing queries** for each library cell
- Higher DRV probability, more routing queries

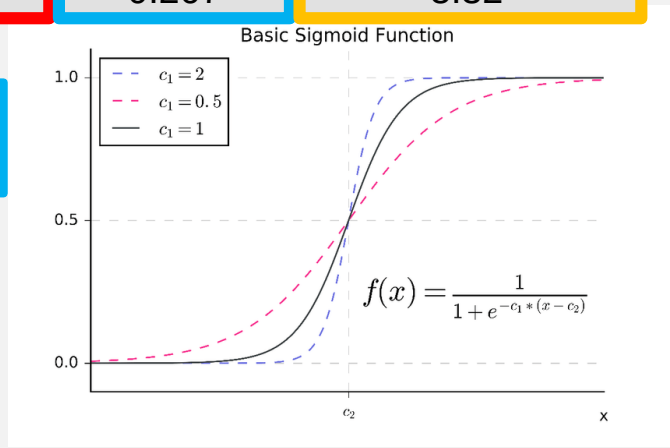
Cell	#Current Queries	#Drvs	#Non-drvs	DRV prob.	Query priority	#Queries in the next iteration
C_1	10	2	8	0.2	-0.033	3.08
C_2	2	0	2	0	-0.233	1.60
C_3	10	5	5	0.5	0.267	5.32



$$DP_i = \frac{D_i}{D_i + ND_i}$$

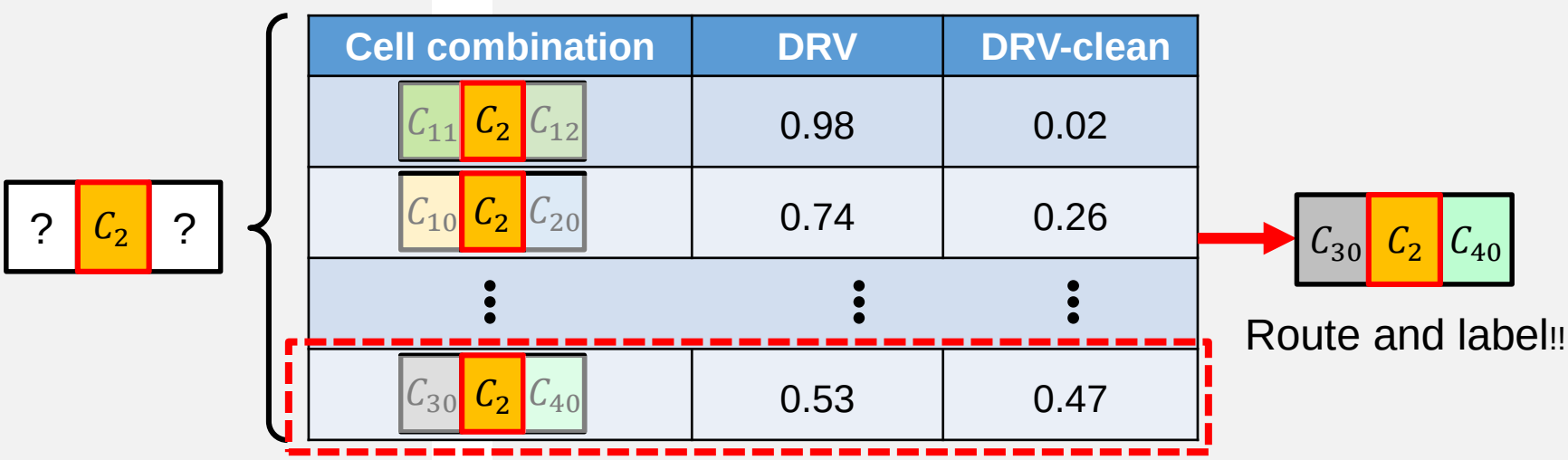
$$QP_i = DP_i - \frac{\sum_{j=1}^{N} DP_j}{N}$$

$$QN_i = R \times \frac{sig(QP_i)}{\sum_{j=1}^{N} sig(QP_i)}$$



Informativeness

- Predict a batch of unrouted cell combinations for each cell before its routing query
- Less confident candidates have higher priorities to be queried

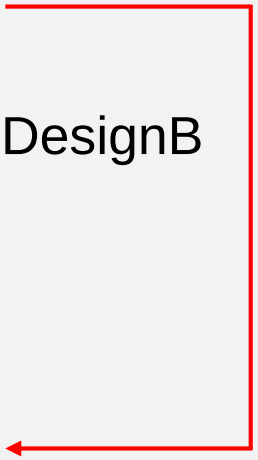


This cell combination with the smallest difference of the probabilities has the least confidence!!

04 Experimental Results

Benchmark Settings

- An industrial reference cell library set
  - Ref lib1
  - Ref lib2
  - Ref lib3
  - Ref lib4
  - Ref lib5
- The libraries used in DesignA
  - Ref lib1
  - Ref lib2
- The libraries used in DesignB
  - Ref lib1
  - Ref lib2
  - Ref lib3
  - Ref lib4
  - Ref lib5



DesignA uses a subset libraries of DesignB

DesignA QoR

- Compare the library-based model with DesignA-specific model (Model A)

	Default				Model A				Library-based model			
	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length
A0	7007	409	NA	34241091	684	58	0.02	34236770	195	18	0.04	34250660
A1	6313	404	NA	34242054	513	43	0.02	34238082	136	11	0.04	34256413
A2	6246	343	NA	34248936	431	33	0.02	34236562	188	8	0.04	34259169
A3	6138	359	NA	34242534	459	36	0.02	34232966	237	26	0.04	34250939
A4	7306	479	NA	34245913	531	42	0.02	34240628	148	12	0.04	34251859
A5	6138	362	NA	34238156	699	66	0.02	34235498	172	14	0.04	34252064
A6	6997	410	NA	34243955	473	36	0.02	34235820	116	9	0.04	34247673
A7	6314	399	NA	34241290	501	43	0.02	34234593	165	10	0.04	34250314
Avg	6557	395	NA	34242991	536	45	0.02	34236365	170	14	0.04	34252386
Comp	1.00	1.00	NA	1.00	0.08	0.11	1.00	1.00	**0.03**	**0.035**	2.00	1.00

Win 5% and 7.5%, respectively

DesignB QoR

- Compare the library-based model with DesignB-specific model (Model B)

	Default				Model B				Library-based model			
	#All drvs	#M2 shorts	Avg cell dis	Total wire length	#All drvs	#M2 shorts	Avg cell dis	Total wire length	#All drvs	#M2 shorts	Avg cell dis	Total wire length
B0	2348	126	NA	4760556	727	15	0.14	4757222	763	19	0.06	4750090
B1	1782	101	NA	4760927	987	31	0.14	4756902	223	6	0.06	4749916
B2	3937	157	NA	4746708	1893	48	0.13	4740258	468	10	0.06	4735521
B3	1646	116	NA	4753160	656	9	0.14	4749079	175	5	0.07	4742816
B4	1777	111	NA	4751883	1282	32	0.14	4748118	575	14	0.06	4741236
B5	3777	174	NA	4758590	926	27	0.13	4751806	677	12	0.07	4747759
B6	2055	128	NA	4757570	481	10	0.13	4750694	1991	54	0.07	4747662
B7	2262	130	NA	4766738	182	2	0.13	4759874	893	17	0.07	4754889
Avg	2448	130	NA	4757017	892	22	0.135	4751744	721	17	0.065	4746236
Comp	1.00	1.00	NA	1.00	0.36	0.17	1.00	1.00	**0.29**	**0.13**	0.48	1.00

Win 7% and 4%, respectively

Predict DesignA Model B

designA: ref1, ref2

designB: ref1, ref2, ref3, ref4, ref 5

	Default				Model A				Model B			
	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length
A0	7007	409	NA	34241091	684	58	0.02	34236770	1347	**27**	0.04	4751564
A1	6313	404	NA	34242054	513	43	0.02	34238082	1288	29	0.04	4750405
A2	6246	343	NA	34248936	431	33	0.02	34236562	853	17	0.04	4735285
A3	6138	359	NA	34242534	459	36	0.02	34232966	109	5	0.04	4742430
A4	7306	479	NA	34245913	531	42	0.02	34240628	473	15	0.04	4741054
A5	6138	362	NA	34238156	699	66	0.02	34235498	232	3	0.04	4747608
A6	6997	410	NA	34243955	473	36	0.02	34235820	307	8	0.04	4745988
A7	6314	399	NA	34241290	501	43	0.02	34234593	2352	70	0.04	4755889
Avg	6557	395	NA	34242991	536	45	0.02	34236365	870	22	0.04	4746278
Comp	1.00	1.00	NA	1.00	0.08	0.11	1.00	1.00	**0.36**	**0.17**	0.30	1.00

Still works!!

Predict Design B by Model A

designA: ref1, ref2

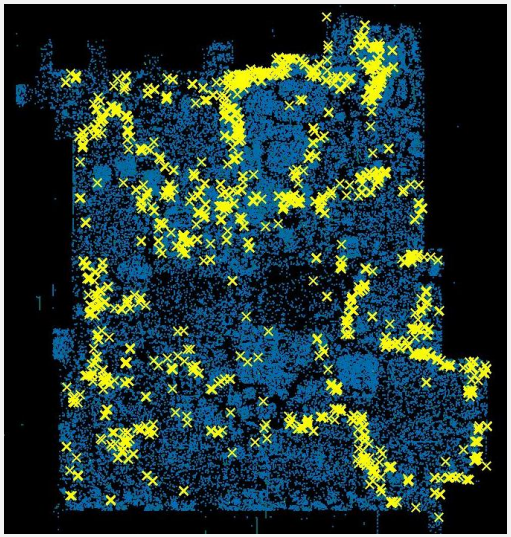
designB: ref1, ref2, ref3, ref4, ref 5

	Default				Model B				Model A			
	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length	#All drcs	#M2 shorts	Avg cell dis	Total wire length
B0	2348	126	NA	4760556	727	15	0.14	4757222	NA	NA	NA	NA
B1	1782	101	NA	4760927	987	31	0.14	4756902	NA	NA	NA	NA
B2	3937	157	NA	4746708	1893	48	0.13	4740258	NA	NA	NA	NA
B3	1646	116	NA	4753160	656	9	0.14	4749079	NA	NA	NA	NA
B4	1777	111	NA	4751883	1282	32	0.14	4748118	NA	NA	NA	NA
B5	3777	174	NA	4758590	926	27	0.13	4751806	NA	NA	NA	NA
B6	2055	128	NA	4757570	481	10	0.13	4750694	NA	NA	NA	NA
B7	2262	130	NA	4766738	182	2	0.13	4759874	NA	NA	NA	NA
Avg	2448	130	NA	4757017	892	22	0.135	4751744	NA	NA	NA	NA
Comp	1.00	1.00	NA	1.00	0.36	0.17	1.00	1.00	NA	NA	NA	NA

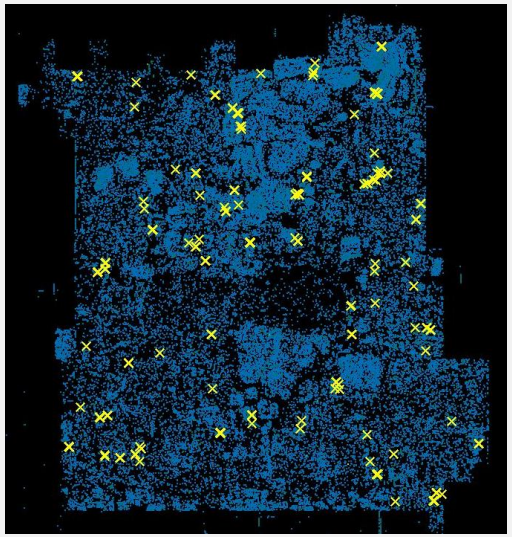
Generate a lot of spacing rules, legalization fails!!

Illustrations of DRV Reduction

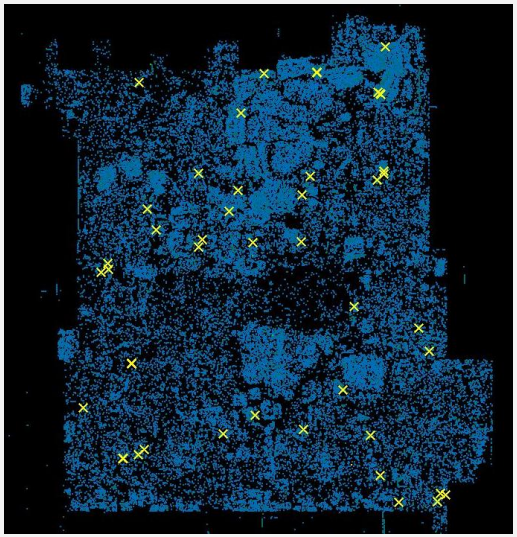
- Total DRV maps



Origin



Design-specific



Library-based

05 Conclusions

Conclusions and Discussion

- Pin pattern is an effective feature to train a DRV prediction model for a cell library that has the problem of pin access
- Compared to a design-specific training model, a library-based model may be more desirable
  - Can be trained at the earlier stage in a process development flow
  - Do not need to generate a lot of routed designs
  - Be applicable to any design referencing to the same cell library set
  - May achieve higher prediction performance because the queried data are more representative and informative
- Applying models to generate DRV-minimized designs instead of predicting DRVs should be the final goal of related researches

THANK YOU