# Construction of All Multilayer Monolithic Rectilinear Steiner Minimum Trees on the 3D Hanan Grid for Monolithic 3D IC Routing

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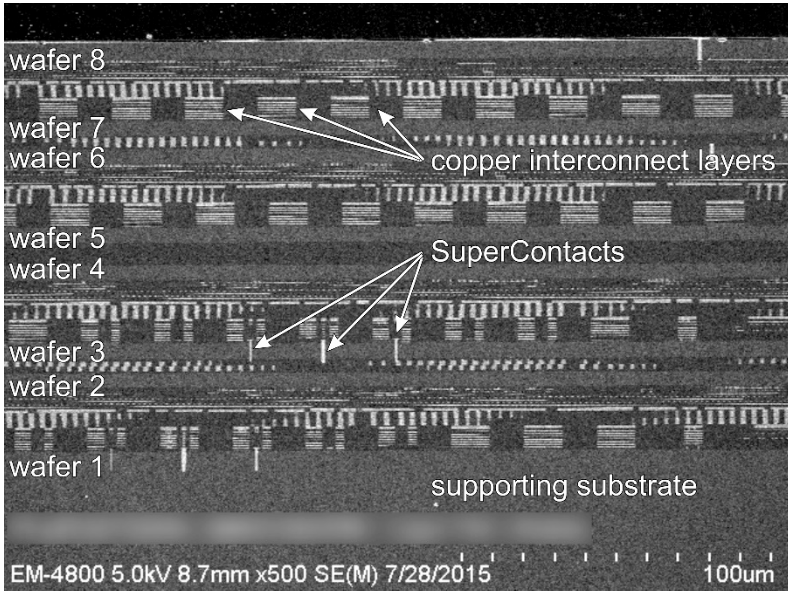
# Outline

- Monolithic 3D Integration – Technology and Design
- Monolithic 3D IC Routing
- Motivation / Goal / Review
- Algorithm
- Simulation Results
- Conclusion

# 3D Integration

- Benefits (compared to 2D ICs)
  - Shorter wire length
    - $\frac{1}{\sqrt{N}}$ ($N$: # tiers)
  - Higher performance
  - Lower power consumption
  - Wider bandwidth
  - Heterogeneous integration
  - ...



3D integration (Tezzaron)

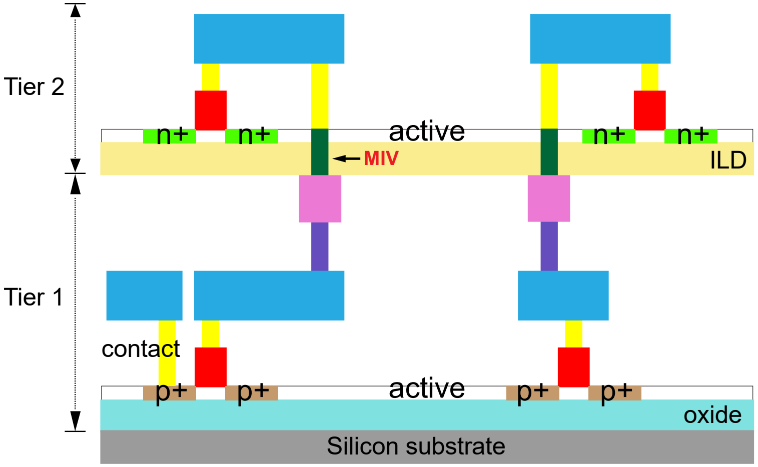
https://tezzaron.com/media/8layer-720x540.jpg

# Monolithic 3D Integration

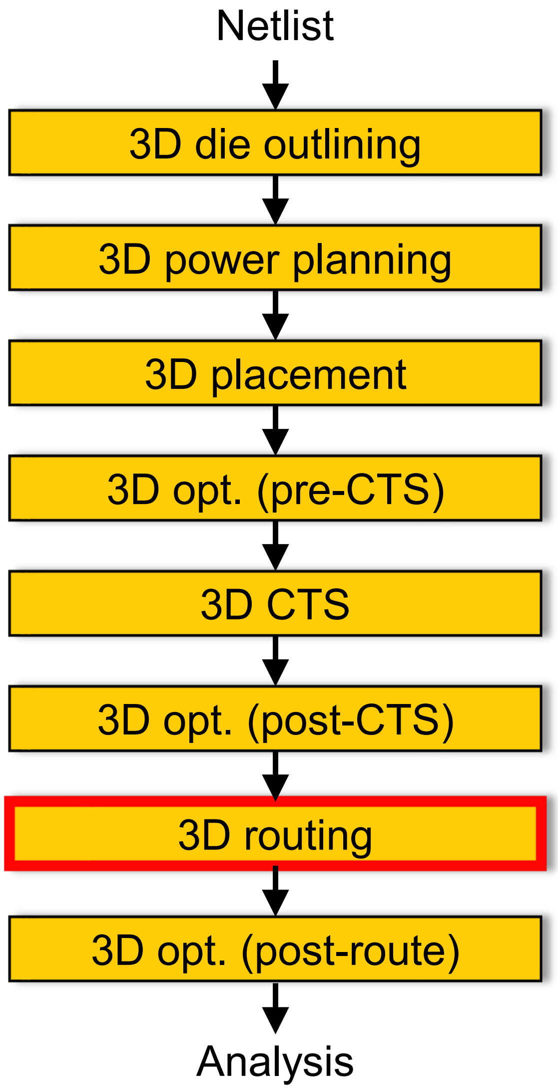
- Stack ultra-thin silicon tiers (0.1~0.2um)

- Ultra-small vertical via
  - Monolithic inter-tier via (MIV)
  - Comparable to local vias
  - Very low parasitic RC

- Maximizes the benefits of 3D integration.



# Monolithic 3D IC Design – Overall Flow

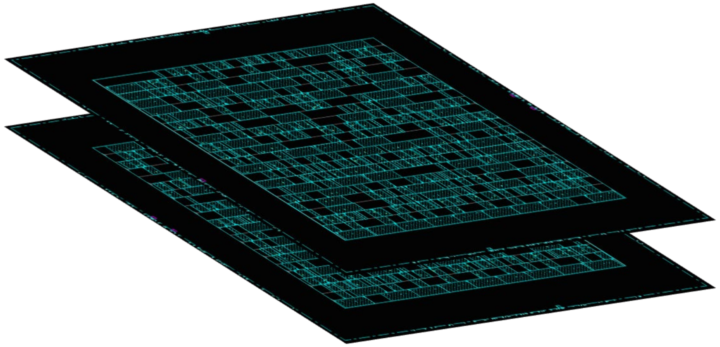


| | |
|---|---|
| Netlist | |
| 3D die outlining | |
| 3D power planning | TCAD’17 |
| 3D placement | ISQED’16, ICCAD’16, ISQED’17, TCAD’17, ISPD’18, TCAD’18 |
| 3D opt. (pre-CTS) | ISQED’12 |
| 3D CTS | TCAD’16, TCAD’17 |
| 3D opt. (post-CTS) | |
| **3D routing** | ISLPED’16, TCAD’16, TCAD’17, ISPD’18,<br>ISQED’19, ICCD’16 → TETC (accepted, early access) |
| 3D opt. (post-route) | |
| Analysis | |

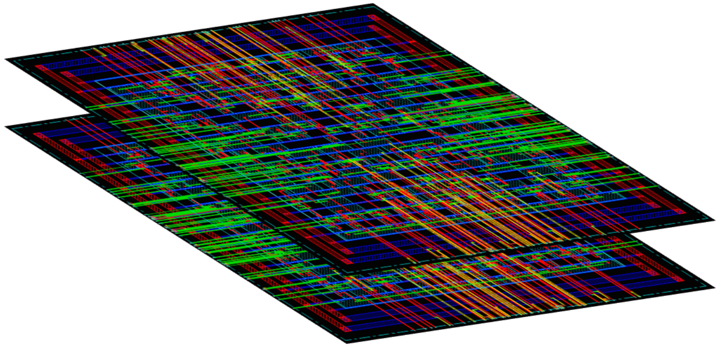
Cyan: our papers

# Monolithic 3D IC Design – 3D Routing

- Input
  - 3D placement (instance, I/O pin locations in multiple tiers)
- Output
  - Routed layouts (with MIVs inserted into the layouts)
  - Modified netlists
    - 3D nets are decomposed into 2D nets.
- Goal
  - Generate manufacturable layouts (i.e., not just globally-routed, but fully-routed)



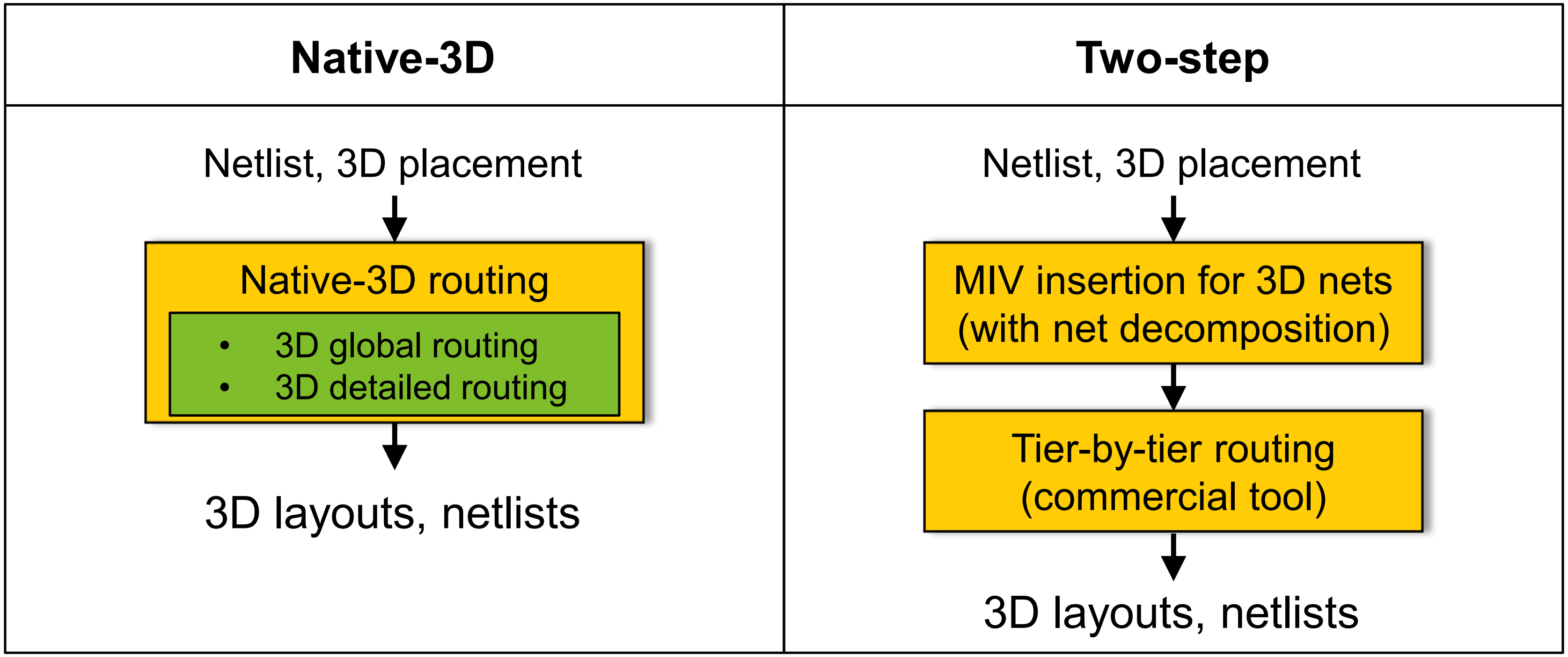
3D placement (two tiers)



3D routing

# Monolithic 3D IC Design – 3D Routing

- Comparison of two 3D routing methodologies



**Native-3D**

Netlist, 3D placement

Native-3D routing

- 3D global routing
- 3D detailed routing

3D layouts, netlists

**Two-step**

Netlist, 3D placement

MIV insertion for 3D nets (with net decomposition)

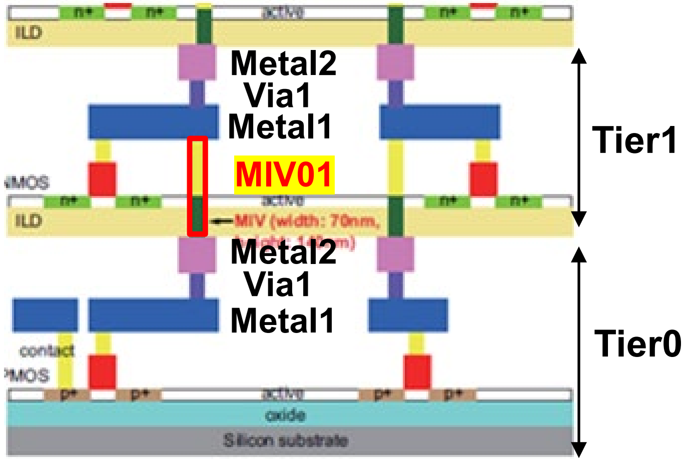
Tier-by-tier routing (commercial tool)

3D layouts, netlists

| | Native-3D | Two-step |
|---|---|---|
| Quality | ? | ? |
| Runtime | ? | ? |

# Monolithic 3D IC Design – 3D Routing

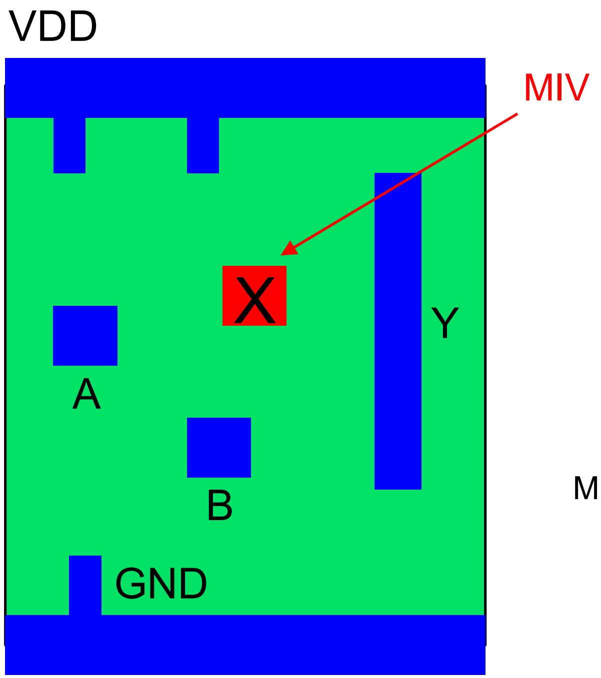
- Native-3D (using a commercial tool)
  - Modify physical library files (LEF).
    - Metal1 in Tier 0
      - M1_T0
    - Metal1 in Tier 1
      - M1_T1
    - Via12 in Tier 0
      - V1_T0
    - Via12 in Tier 1
      - V1_T1
    - MIV connecting Tier0 and Tier1
      - MIV_01 (defined as a via layer)
    - Cell in Tier 0
      - NAND2_X1_T0
      - Uses the metal and via layers in Tier 0
    - Cell in Tier 1
      - NAND2_X1_T1
      - Uses the metal and via layers in Tier 1



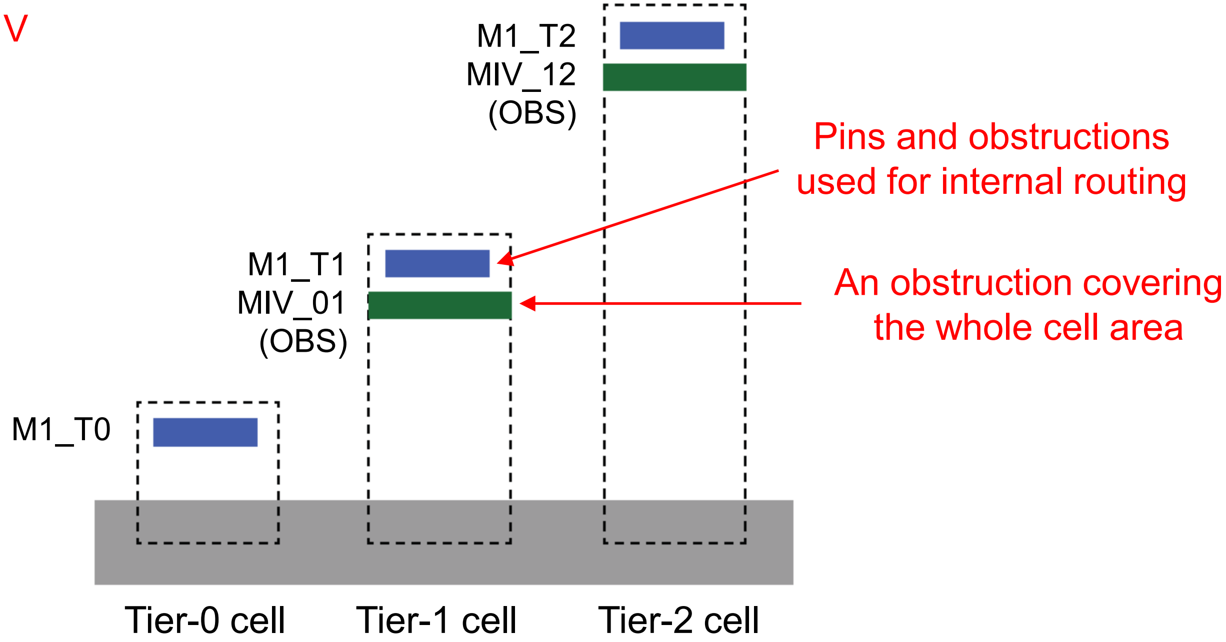
**<side view>**

# Monolithic 3D IC Design – 3D Routing

- Native-3D
  - To avoid inserting MIVs inside standard cells, we need to create an obstruct inside the standard cells.



<Top-down view>



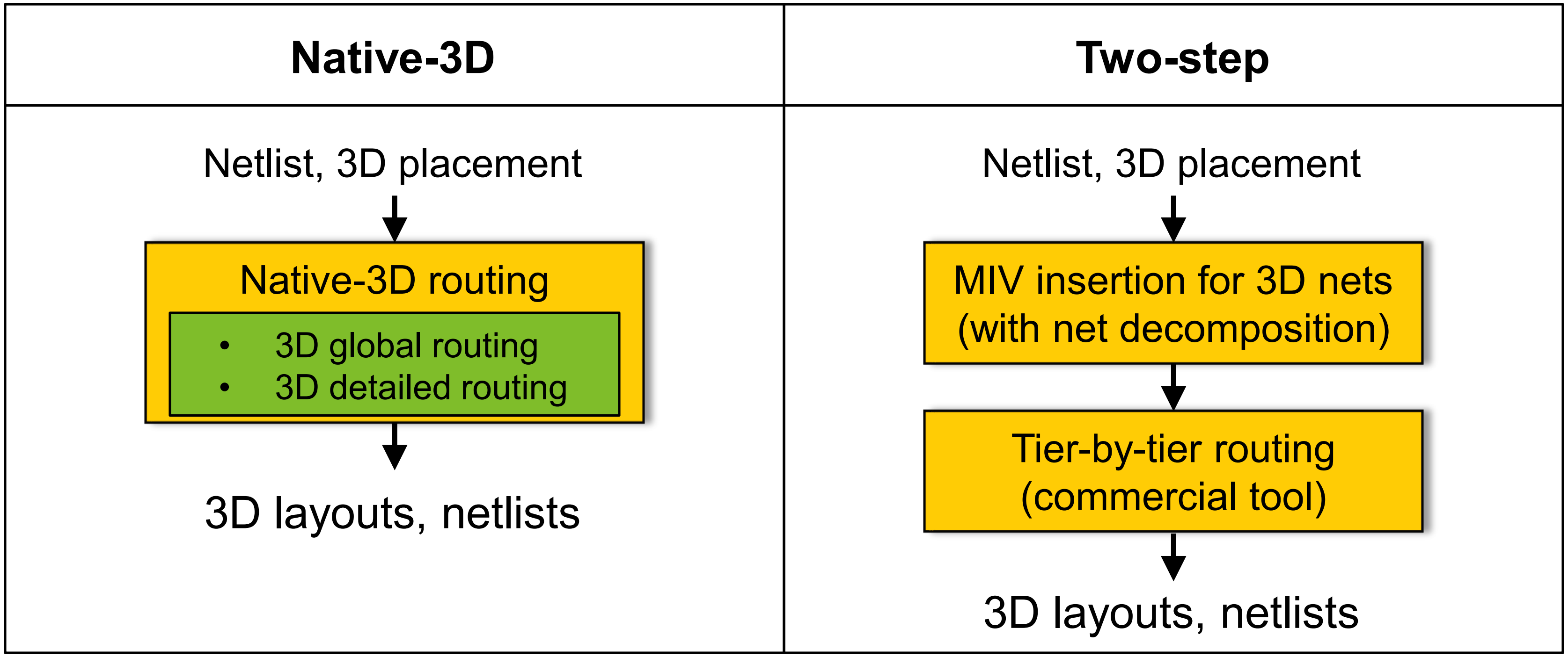
Pins and obstructions used for internal routing

An obstruction covering the whole cell area

<Side view>

# Monolithic 3D IC Design – 3D Routing

- Comparison of two 3D routing methodologies



**Native-3D**

Netlist, 3D placement

Native-3D routing
- 3D global routing
- 3D detailed routing

3D layouts, netlists

**Two-step**

Netlist, 3D placement

MIV insertion for 3D nets (with net decomposition)

Tier-by-tier routing (commercial tool)

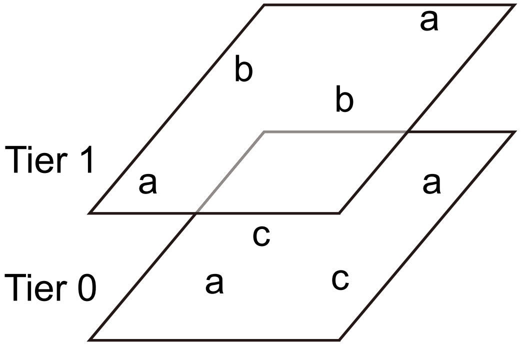
3D layouts, netlists

| | Native-3D | Two-step |
|---|---|---|
| Quality | High (commercial tool) | ? |
| Runtime | Slow* | ? |

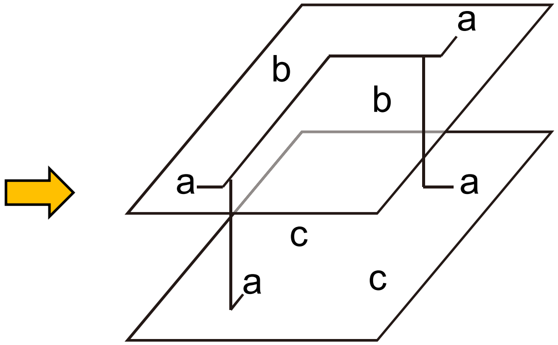
* Sheng-En Lin and Dae Hyun Kim, "Routing Complexity Minimization of Monolithic Three-Dimensional Integrated Circuits," ISQED'19.

# Monolithic 3D IC Design – 3D Routing

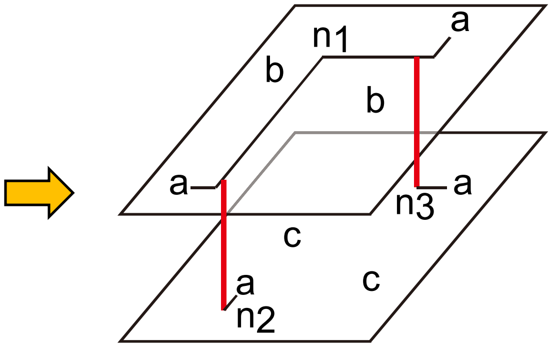
- Two-step approach
  - MIV insertion



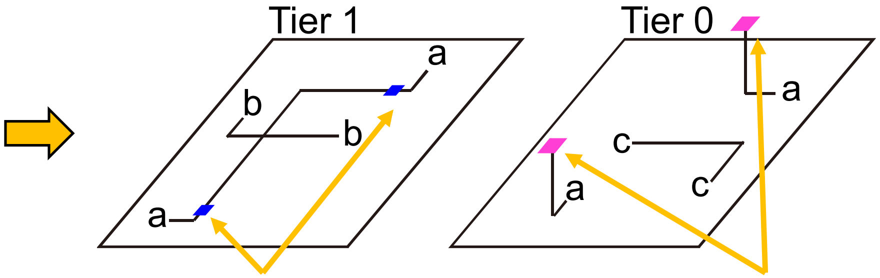
2D nets: b, c
3D net: a



3D routing topology generation

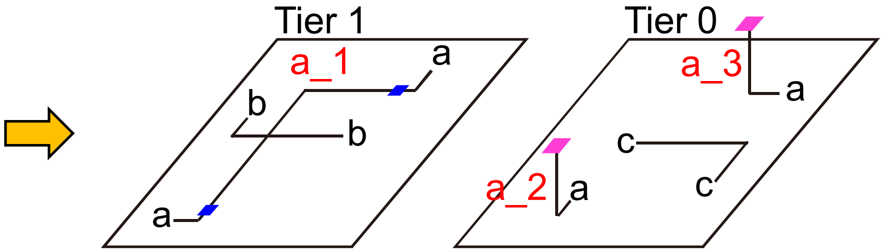


MIV insertion



MIV pad (metal 1, top tier)
- defined as an I/O pin

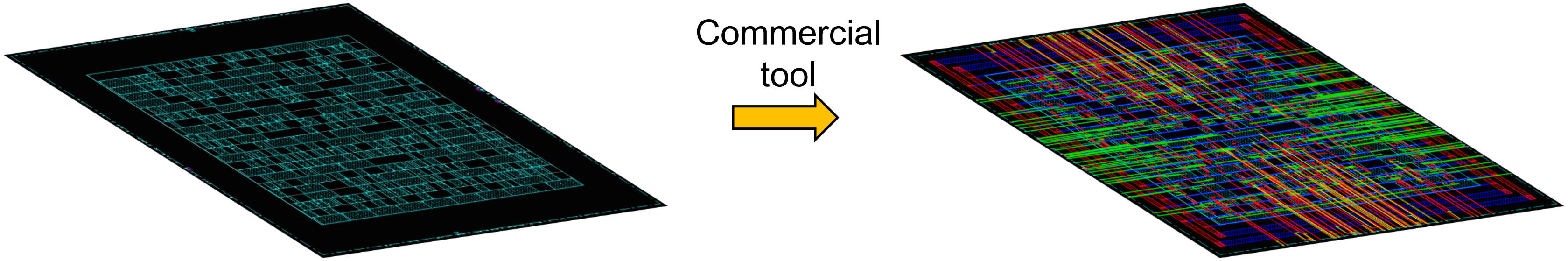
MIV pad (metal top, bottom)
- defined as an I/O pin



Net decomposition
(The final netlist has three subnets for a)

# Monolithic 3D IC Design – 3D Routing

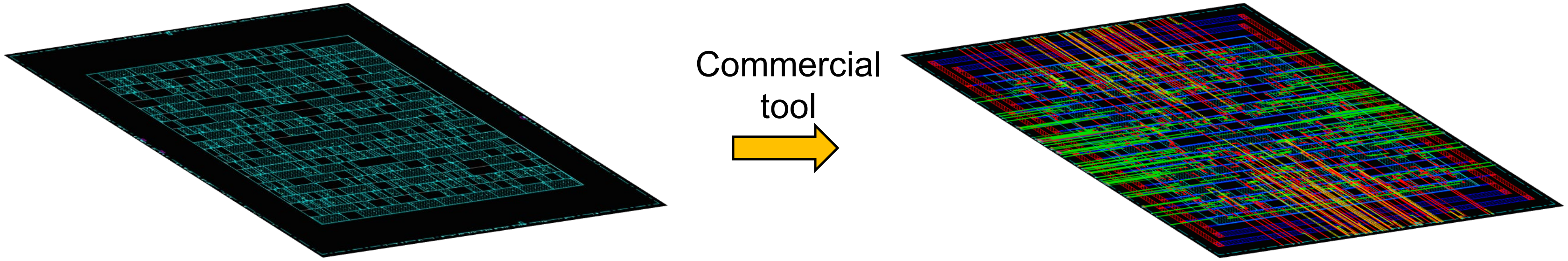
- Two-step approach
  - Tier-by-tier routing



Commercial tool

Tier 1

3D placement (top tier)
A modified netlist (top tier)



Commercial tool

3D placement (bottom tier)
A modified netlist (bottom tier)

Tier 0

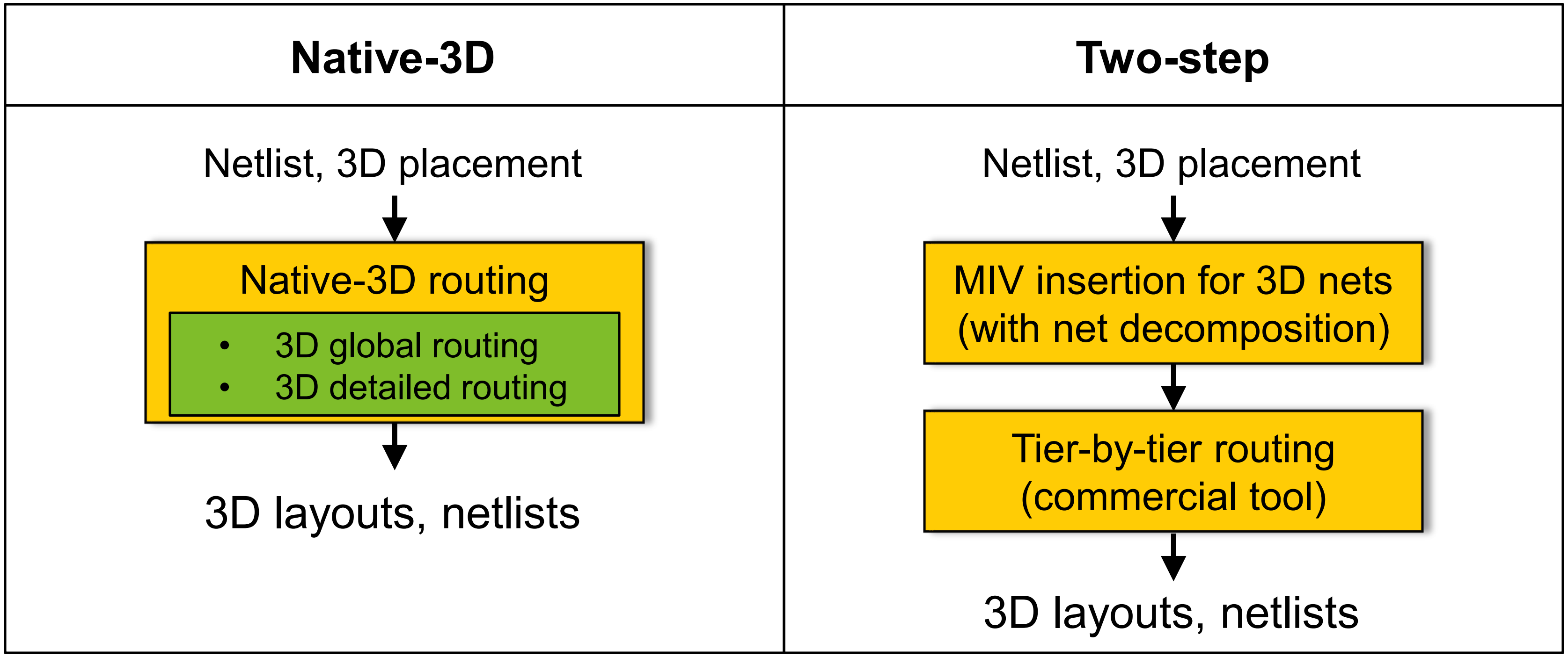
# Monolithic 3D IC Design – 3D Routing

- Native-3D vs. Two-step (ICCD'16, TETC early access)
  - MIV insertion: done by multilayer obstacle-avoiding rectilinear Steiner tree (MLOARST) construction.
    - Chung-Wei Lin, Shih-Lun Huang, Kai-Chi Hsu, Meng-Xiang Lee, and Yao-Wen Chang, TCAD'08.
  - Simulation results (scaled)
    - Enc: Cadence Encounter (now Innovus)

| Circuit | # tiers | # insts | WL (Enc) | WL (Two-step) | # MIVs (Enc) | # MIVs (Two-step) | Runtime (Enc) | Runtime (Two-step) |
|---|---|---|---|---|---|---|---|---|
| LDPC | 2 | 51K | 1.000 | 1.015 | 1.000 | 0.789 | 1.000 | 0.207 (5X) |
|  | 3 |  | 1.000 | 1.033 | 1.000 | 0.906 | 1.000 | 0.166 (6X) |
|  | 4 |  | 1.000 | 1.044 | 1.000 | 0.999 | 1.000 | 0.128 (8X) |
| FFT | 2 | 256K | 1.000 | 0.984 | 1.000 | 1.160 | 1.000 | 0.170 (6X) |
|  | 3 |  | 1.000 | 0.983 | 1.000 | 1.173 | 1.000 | 0.063 (16X) |
|  | 4 |  | 1.000 | 0.944 | 1.000 | 1.261 | 1.000 | 0.044 (23X) |

# Monolithic 3D IC Design – 3D Routing

- Comparison of two 3D routing methodologies



**Native-3D**

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Native-3D routing
- 3D global routing
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3D layouts, netlists

**Two-step**

Netlist, 3D placement

MIV insertion for 3D nets (with net decomposition)

Tier-by-tier routing (commercial tool)

3D layouts, netlists

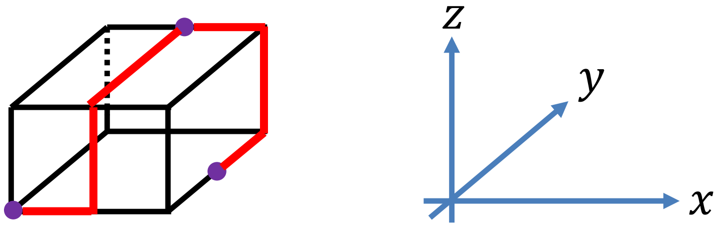
| | **Native-3D** | **Two-step** |
|---|---|---|
| Quality | High | **Need a better algorithm** |
| Runtime | Slow | **Fast** |

# MIV Insertion

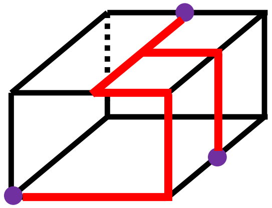
- How?
  - Let’s try to find all optimal 3D topologies and select a best one.
- How can we find all optimal 3D topologies?
  - We need something like FLUTE.
- What is FLUTE?
  - Let’s review some past work.

# Background

- Terminologies
  - 3D rectilinear tree (3D RT)
    - A tree having only x-, y-, and z-directional edges

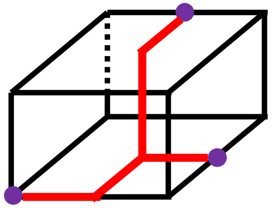


  - 3D rectilinear Steiner tree (3D RST)
    - A 3D RT with Steiner points.

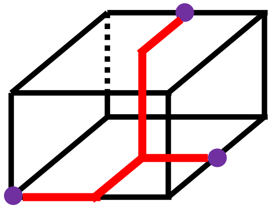


# Background

- Terminologies
  - 3D rectilinear Steiner minimum tree (3D RSMT)
    - A 3D RST having the minimum length ($L = \sum e_x + \sum e_y + \sum e_z$)

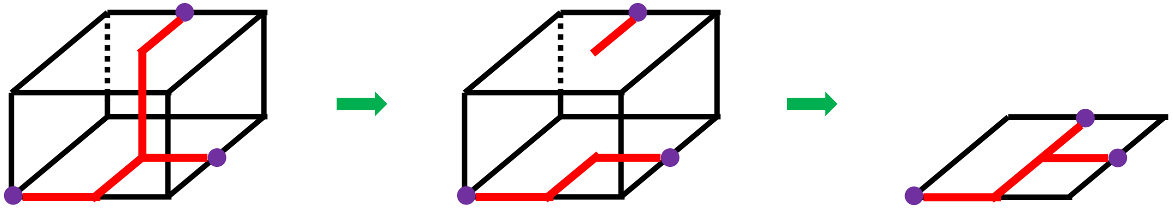


  - Multilayer monolithic rectilinear Steiner minimum tree (MMRSMT)
    - A 3D RST having the minimum planar length and the minimum number of z-directional edges (MIVs)
    - Why?
      - The length of an MIV is negligible. Do not consider the length itself.
      - However, # MIVs is important (inserting too many MIVs causes serious routing congestion).

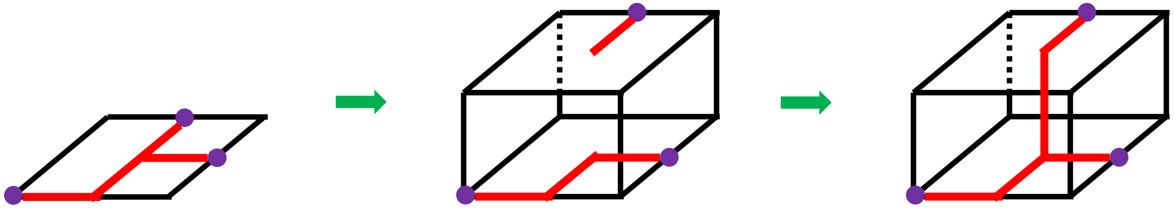


# Background

- We can construct MMRSMTs from 2D RSMTs.
- Why?
  - An MMRSMT has the minimum planar wire length.



- How?
  - Extend a 2D RSMT to 3D and insert z-directional edges properly.



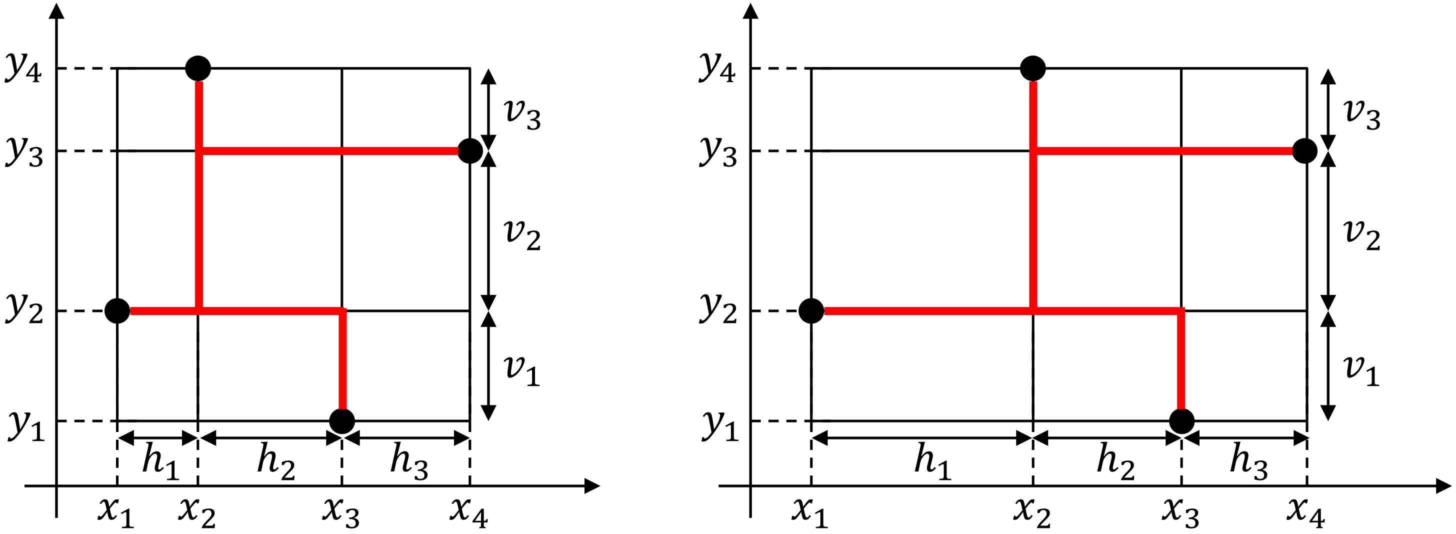
# Review – 2D RSMT Construction (FLUTE)

- FLUTE: Lookup-Table-Based RSMT Construction (Chu, TCAD'08)
- Wire length computation

$$L = 1 \cdot h_1 + 2 \cdot h_2 + 1 \cdot h_3 + 1 \cdot v_1 + 1 \cdot v_2 + 1 \cdot v_3$$
$$= (1,2,1,1,1,1) \cdot (h_1, h_2, h_3, v_1, v_2, v_3)$$

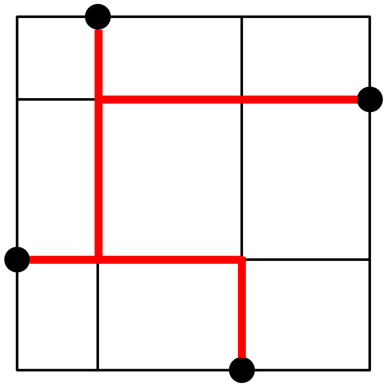
Wirelength Vector
(Topology-dependent, constant)

Edge-length Vector
(Coordinate-dependent, variable)



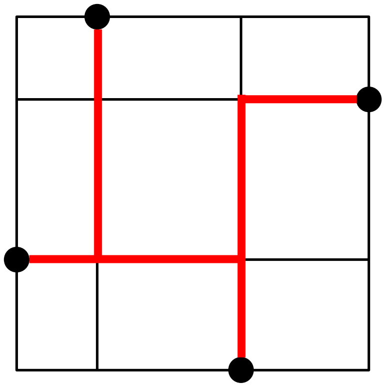
# Review – 2D RSMT Construction (FLUTE)

- Observation
  - The wirelength vectors (WV) of some topologies cannot generate RSMTs.
  - Example
    - (a, b, c, d, e, f): $L_1 = a \cdot h_1 + b \cdot h_2 + c \cdot h_3 + d \cdot v_1 + e \cdot v_2 + f \cdot v_3$
    - (a, b, c+1, d, e, f): $L_2 = a \cdot h_1 + b \cdot h_2 + (c+1) \cdot h_3 + d \cdot v_1 + e \cdot v_2 + f \cdot v_3$
    - $L_2 - L_1 = h_3 > 0$



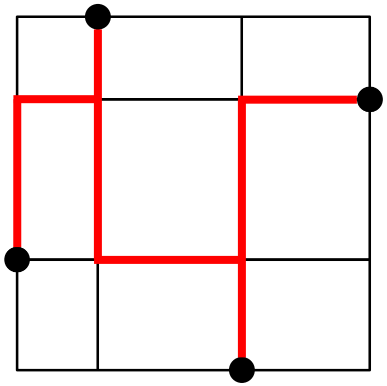
WV: $(1,2,1,1,1,1)$

Potentially optimal? YES



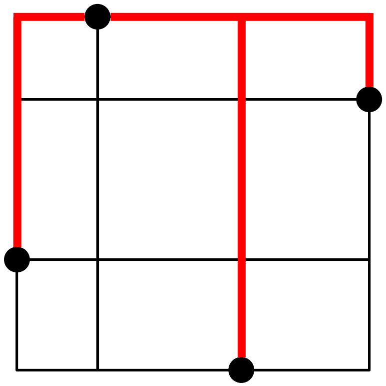
WV: $(1,1,1,1,2,1)$

YES



WV: $(1,1,1,1,\mathbf{3},1)$

NO

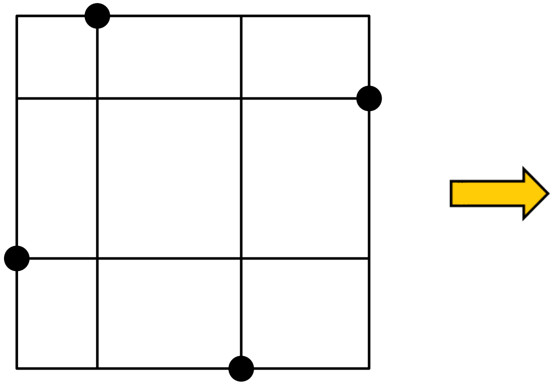


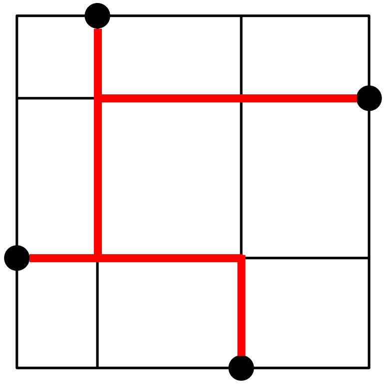
WV: $(1,1,1,1,\mathbf{2},\mathbf{3})$

NO

# Review – 2D RSMT Construction (FLUTE)

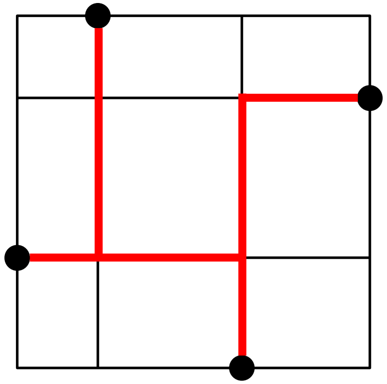
- Optimal topology
  - Once pin locations are given, compute the wire length by the dot product and return the shorter topology.





$(1,2,1,1,1,1) \cdot (h_1, h_2, h_3, v_1, v_2, v_3)$

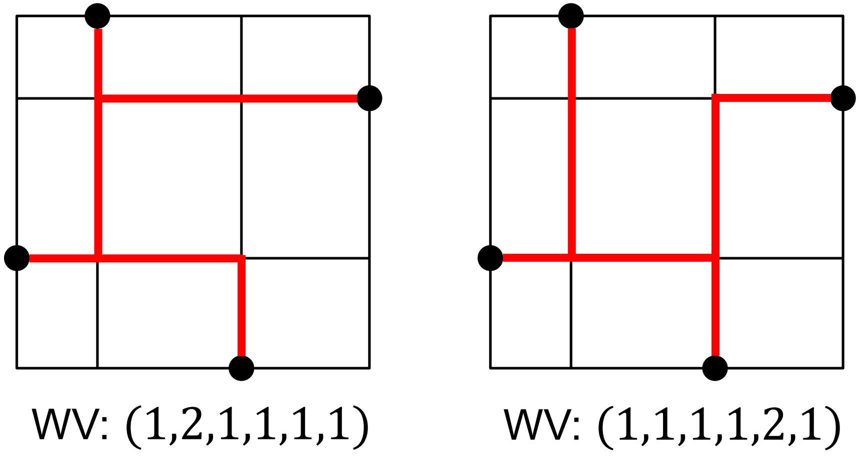
OR



$(1,1,1,1,2,1) \cdot (h_1, h_2, h_3, v_1, v_2, v_3)$

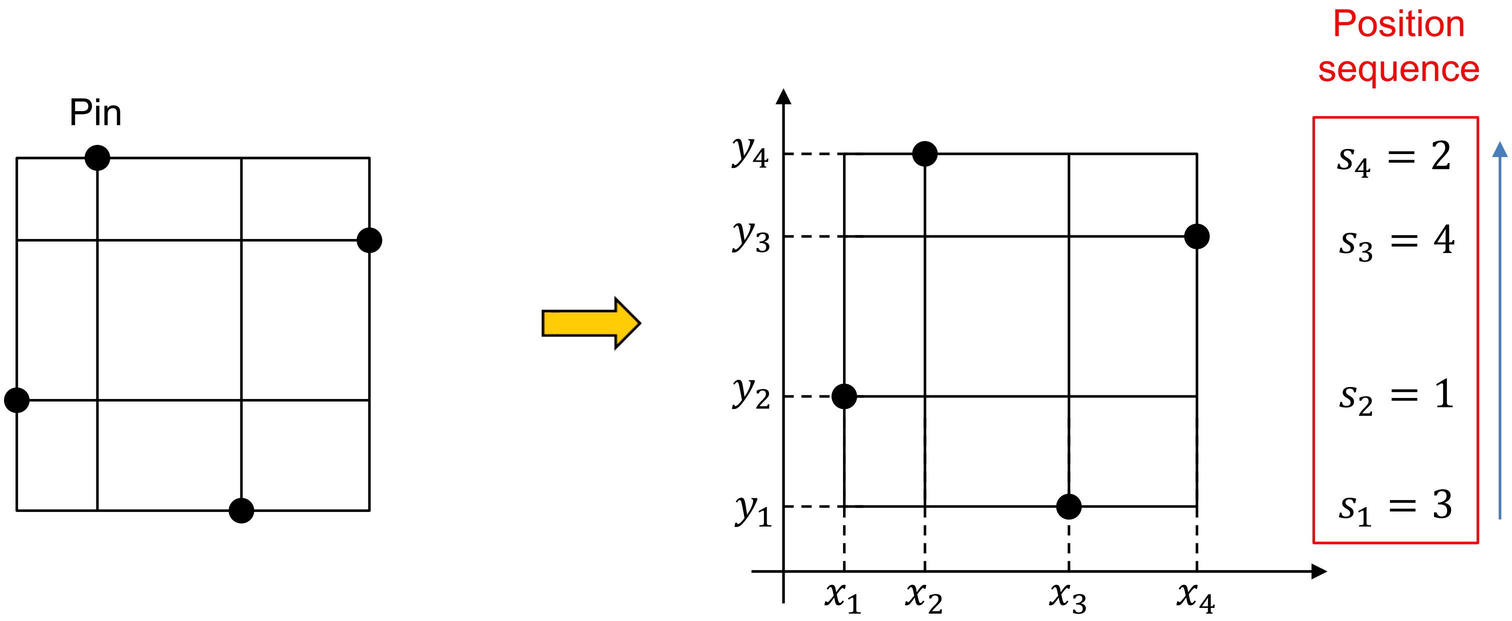
# Review – 2D RSMT Construction (FLUTE)

- FLUTE
  - Find all potentially optimal wirelength vectors (POWVs) for each set of relative pin locations.



# Review – 2D RSMT Construction (FLUTE)

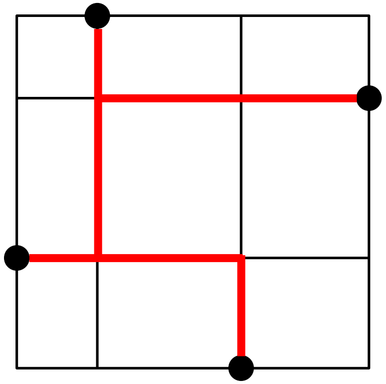
- Terminologies
  - Position sequence (relative pin locations)



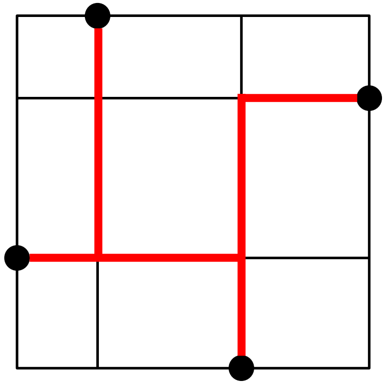
  - Sort the pins in the increasing order of the y-coordinates $(y_1, y_2, y_3, y_4)$.
  - Obtain their x-coordinates $(x_3, x_1, x_4, x_2)$.
  - Obtain the indices (3,1,4,2).

# Review – 2D RSMT Construction (FLUTE)

- Terminologies
  - Potentially Optimal Wirelength Vector (POWV)
    - Belongs to a position sequence
    - Example for position sequence (3142)
      - (1 2 1 1 1 1)
      - (1 1 1 1 2 1)
  - Potentially Optimal Steiner Tree (POST)
    - Belongs to a POWV



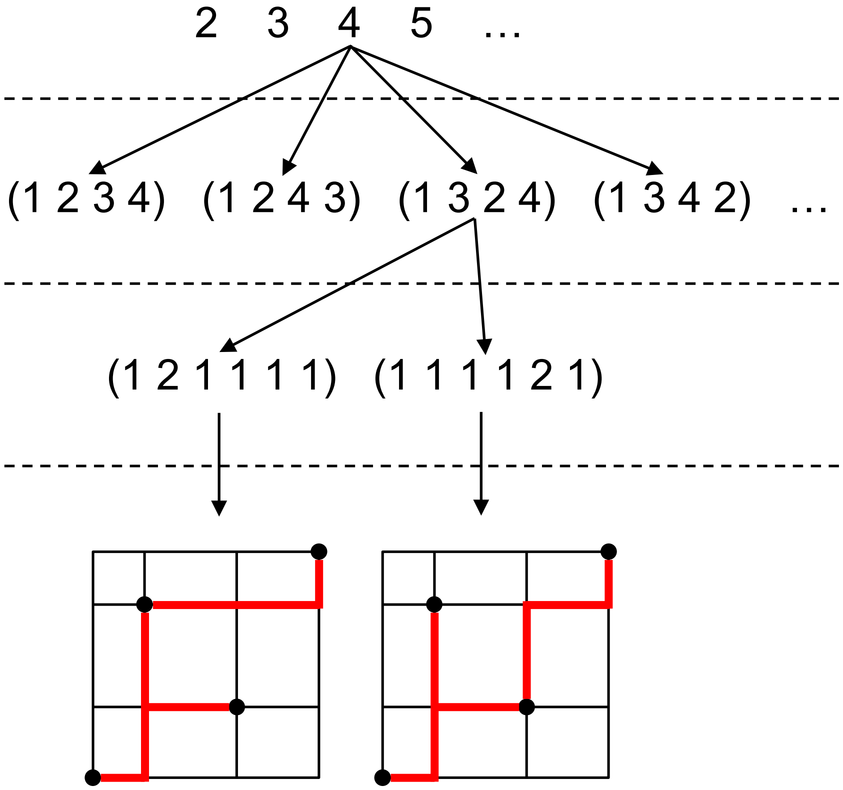
POWV: (1,2,1,1,1,1)



POWV: (1,1,1,1,2,1)

# Review – 2D RSMT Construction (FLUTE)

- Database structure



Pin count 2 3 4 5 …

Position sequence (1 2 3 4) (1 2 4 3) (1 3 2 4) (1 3 4 2) …

POWV (1 2 1 1 1 1) (1 1 1 1 2 1)

One POST for a POWV

# Review – 2D RSMT Construction (FLUTE)

- How to find POWVs and POSTs
  - Please see the FLUTE paper.

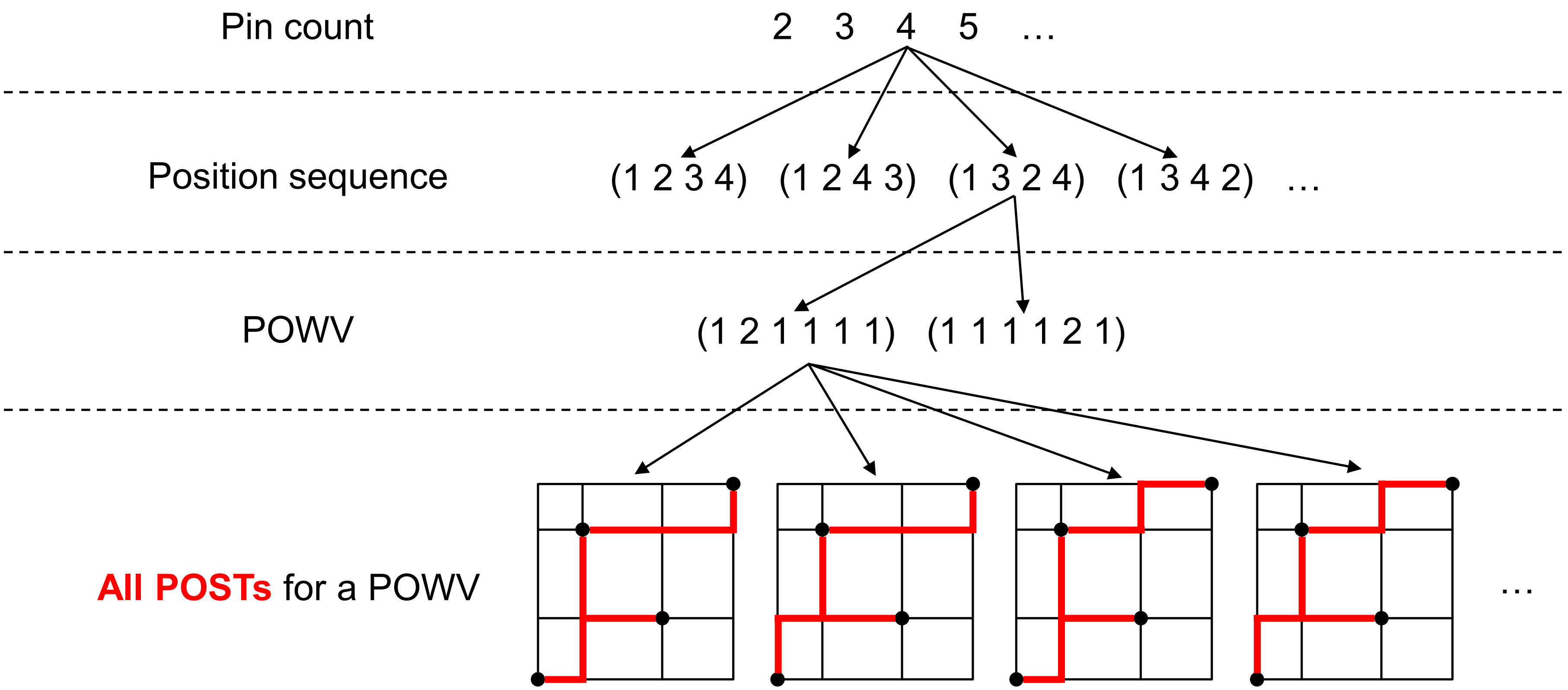
  - Chris Chu and Yiu-Chung Wong, “FLUTE: Fast Lookup Table Based Rectilinear Steiner Minimal Tree Algorithm for VLSI Design,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, Issue 1, Jan. 2008, pp. 70–83.

# Review – All 2D RSMT Construction (ISPD’18)

- Goal
  - Find **all** 2D POSTs for each POWV.
- Why?
  - We can try different 2D RSMTs to optimize various objectives such as
    - Routing congestion minimization
    - Path length minimization
    - Concurrent minimization of the wire length and source-to-critical-sink length
    - …
  - We can generate all MMRSMTs from all 2D POSTs for monolithic 3D IC routing.

# Review – All 2D RSMT Construction (ISPD'18)

- Database structure



Pin count 2 3 4 5 …

Position sequence (1 2 3 4) (1 2 4 3) (1 3 2 4) (1 3 4 2) …

POWV (1 2 1 1 1 1) (1 1 1 1 2 1)

**All POSTs** for a POWV …

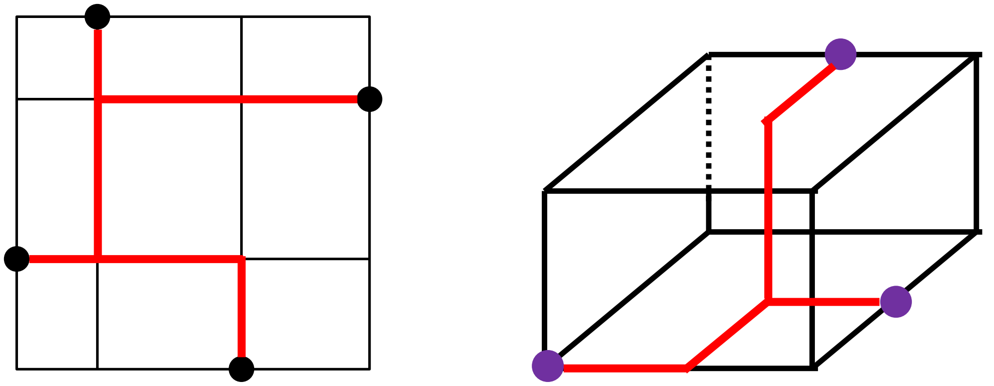
# Review – All 2D RSMT Construction (ISPD’18)

- How to find all POSTs
  - Please see the ISPD’18 paper.

  - Sheng-En Lin and Dae Hyun Kim, “Construction of All Rectilinear Steiner Minimum Trees on the Hanan Grid,” *ACM International Symposium on Physical Design (ISPD)*, pp. 18–25, 2018.

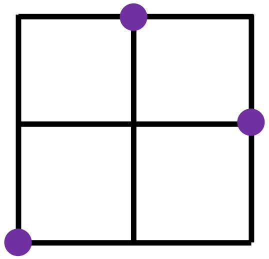
# 2D vs. 3D

| | 2D | Monolithic 3D |
|---|---|---|
| Optimal | 2D RSMT | MMRSMT |
| DB | 2D POST | 3D POST |
| How to construct the DB | FLUTE (TCAD'08),<br>ISPD'18 | This work<br>(From 2D POSTs) |

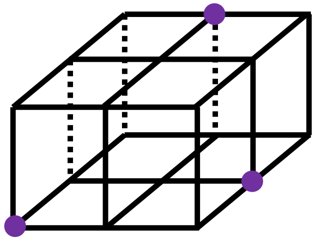


# Terminology

- 2D Hanan grid



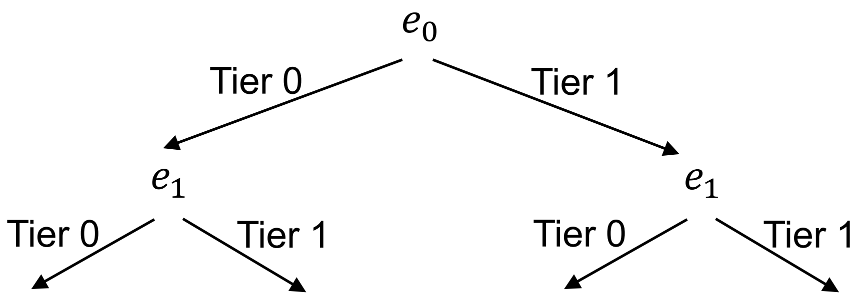
- 3D Hanan grid



- 3D Potentially Optimal Steiner Tree (3D POST)
  - 3D RST that could be an MMRSMT

# Our Algorithm for 3D POST Construction

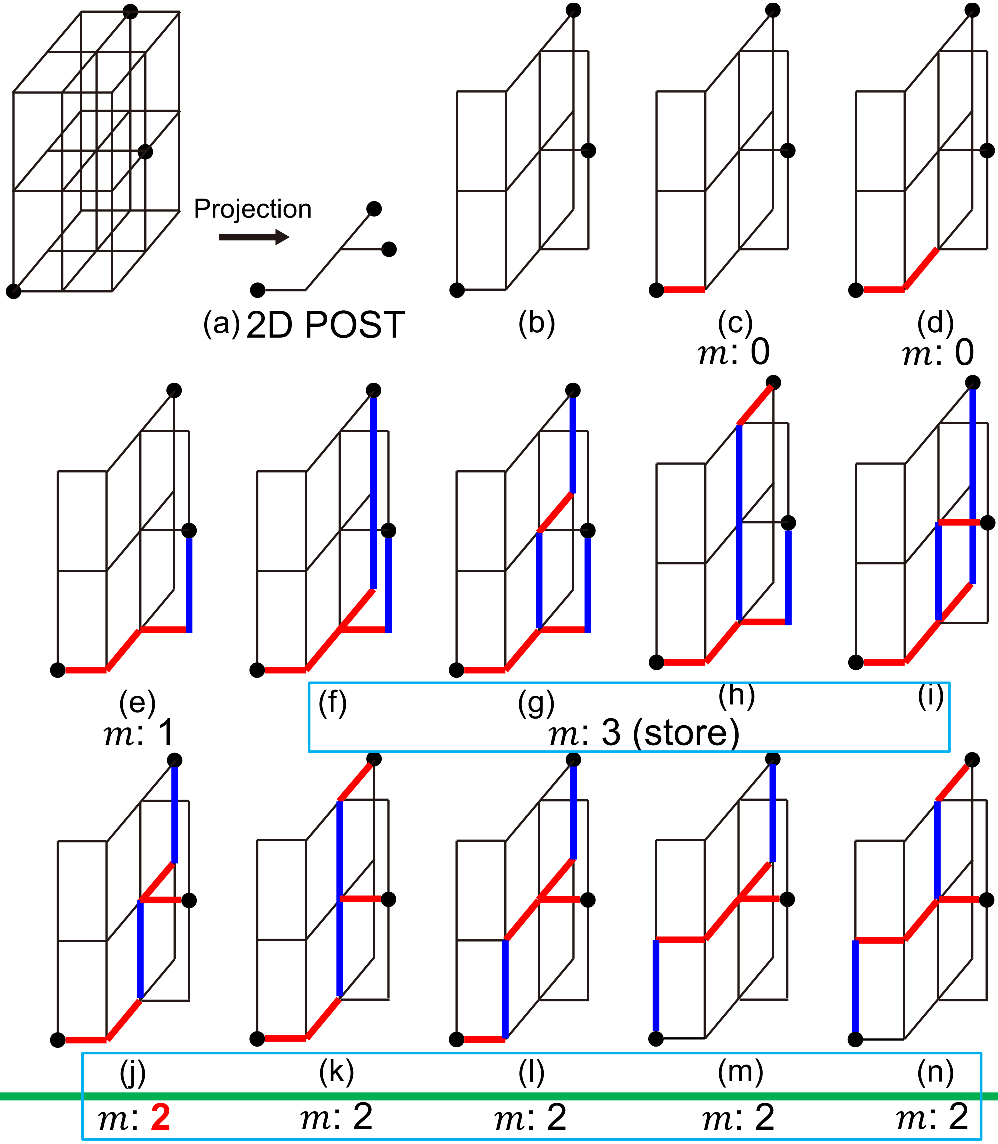
- Decision tree (for each 2D POST)



1. Place edge $e$ in Tier $k$.
2. Count the number of total z-directional edges (MIVs) in the current 3D RST.
3. If # MIVs of the current 3D RST $>$ # MIVs of the currently-best 3D RST, go back to the parent (discard placing $e$ in Tier $k$).
4. Move on to the next edge.

# Our Algorithm for 3D POST Construction

- Example
  - $m$: # MIVs



(a) 2D POST (b) (c) $m$: 0 (d) $m$: 0

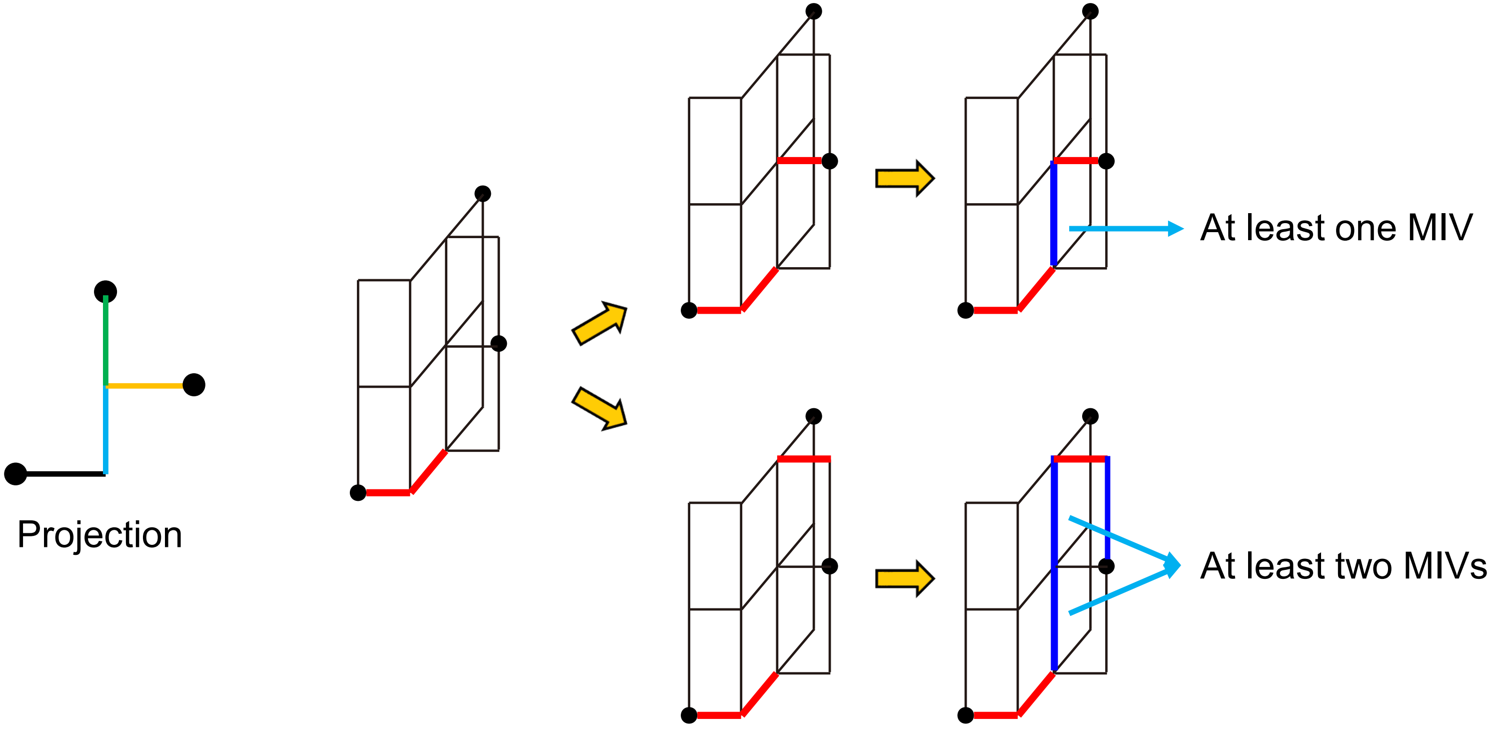
(e) $m$: 1 (f) (g) (h) (i) $m$: 3 (store)

(j) $m$: **2** (k) $m$: 2 (l) $m$: 2 (m) $m$: 2 (n) $m$: 2

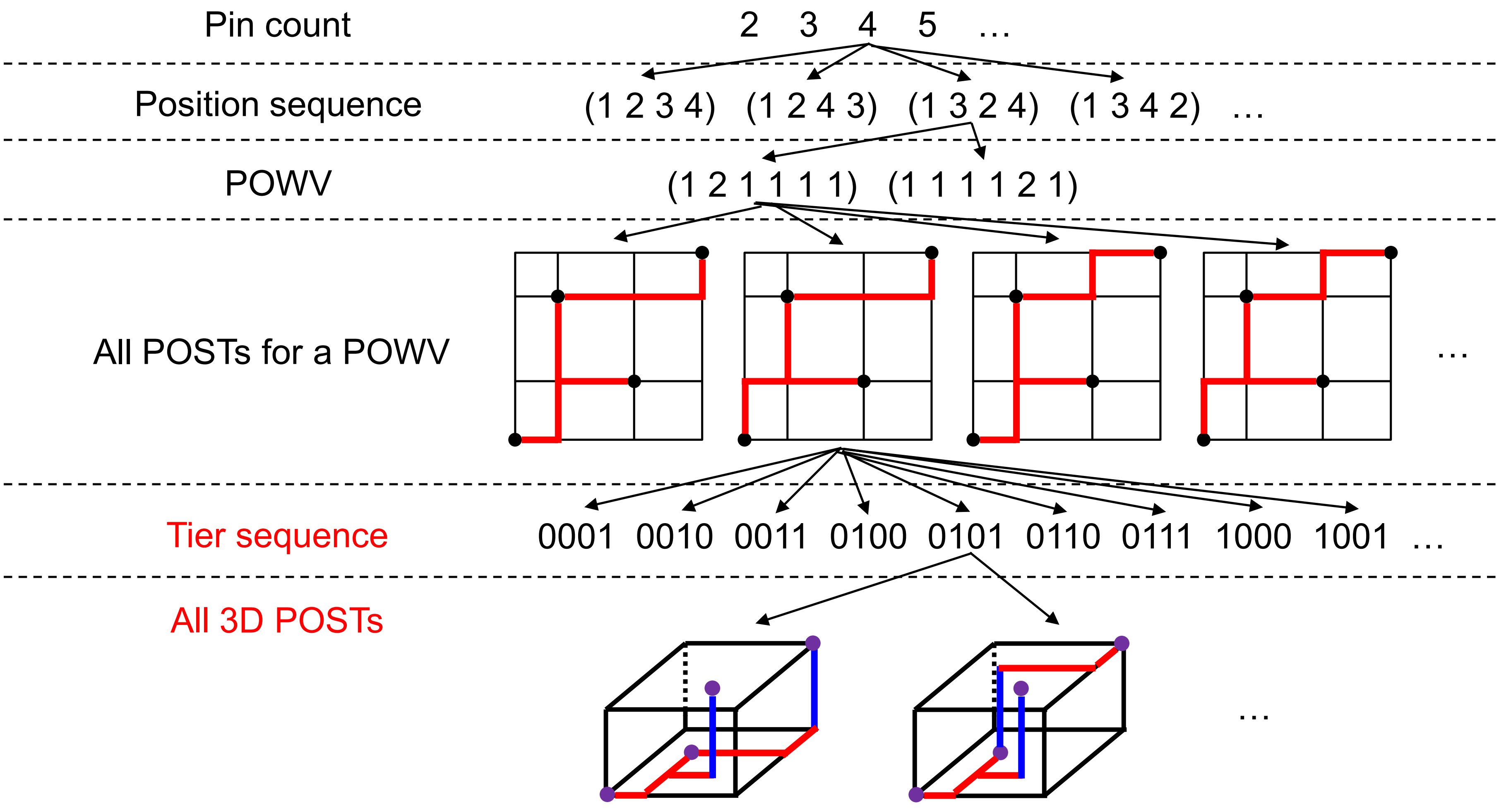
(Discard the topologies having three MIVs.)

# Our Algorithm for 3D POST Construction

- How to count (estimate) # MIVs
  - Whenever we place an edge $e$ in Tier $k$, update # MIVs at both nodes of $e$.



# 3D POST Database Structure



Pin count 2 3 4 5 …

Position sequence (1 2 3 4) (1 2 4 3) (1 3 2 4) (1 3 4 2) …

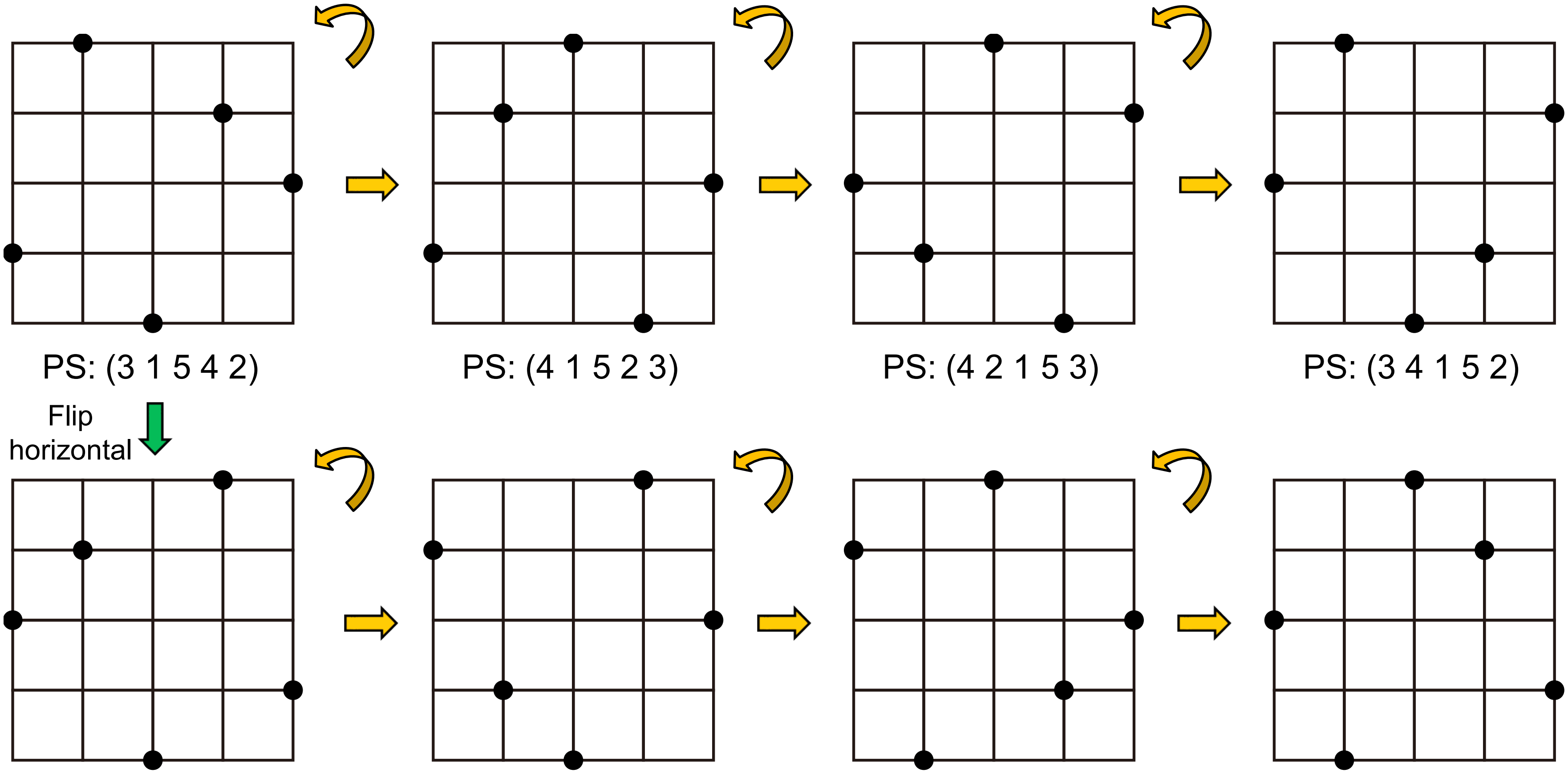
POWV (1 2 1 1 1 1) (1 1 1 1 2 1)

All POSTs for a POWV …

Tier sequence 0001 0010 0011 0100 0101 0110 0111 1000 1001 …

All 3D POSTs …

# Database Size Reduction by Congruence



Rotate counterclockwise

PS: (3 1 5 4 2)

PS: (4 1 5 2 3)

PS: (4 2 1 5 3)

PS: (3 4 1 5 2)

Flip horizontal

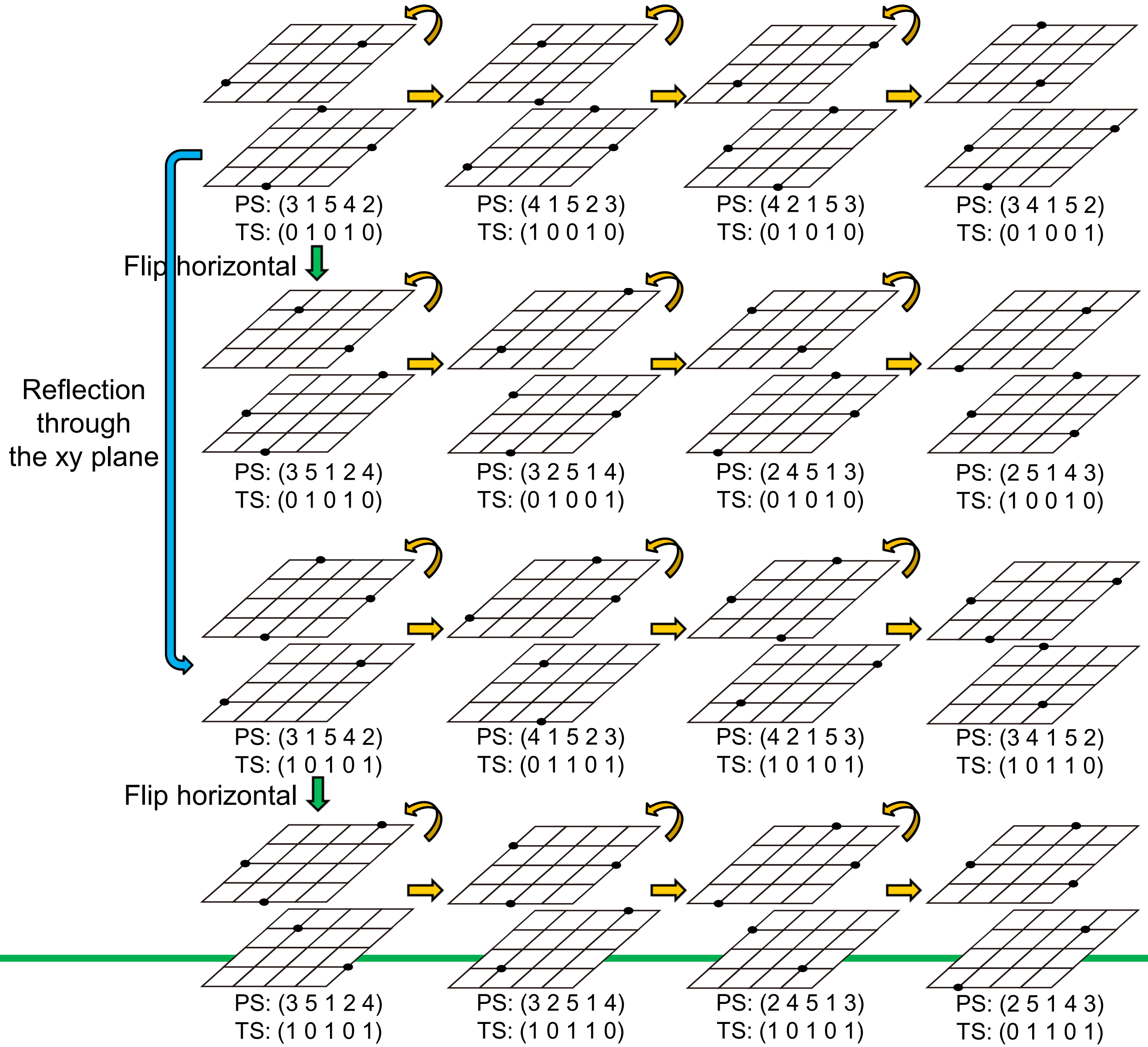
PS: (3 5 1 2 4)

PS: (3 2 5 1 4)

PS: (2 4 5 1 3)

PS: (2 5 1 4 3)

# Database Size Reduction by Congruence



PS: (3 1 5 4 2)
TS: (0 1 0 1 0)

PS: (4 1 5 2 3)
TS: (1 0 0 1 0)

PS: (4 2 1 5 3)
TS: (0 1 0 1 0)

PS: (3 4 1 5 2)
TS: (0 1 0 0 1)

Flip horizontal

Reflection through the xy plane

PS: (3 5 1 2 4)
TS: (0 1 0 1 0)

PS: (3 2 5 1 4)
TS: (0 1 0 0 1)

PS: (2 4 5 1 3)
TS: (0 1 0 1 0)

PS: (2 5 1 4 3)
TS: (1 0 0 1 0)

PS: (3 1 5 4 2)
TS: (1 0 1 0 1)

PS: (4 1 5 2 3)
TS: (0 1 1 0 1)

PS: (4 2 1 5 3)
TS: (1 0 1 0 1)

PS: (3 4 1 5 2)
TS: (1 0 1 1 0)

Flip horizontal

PS: (3 5 1 2 4)
TS: (1 0 1 0 1)

PS: (3 2 5 1 4)
TS: (1 0 1 1 0)

PS: (2 4 5 1 3)
TS: (1 0 1 0 1)

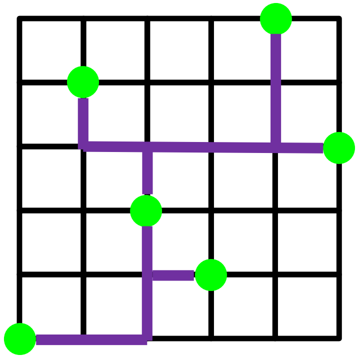
PS: (2 5 1 4 3)
TS: (0 1 1 0 1)

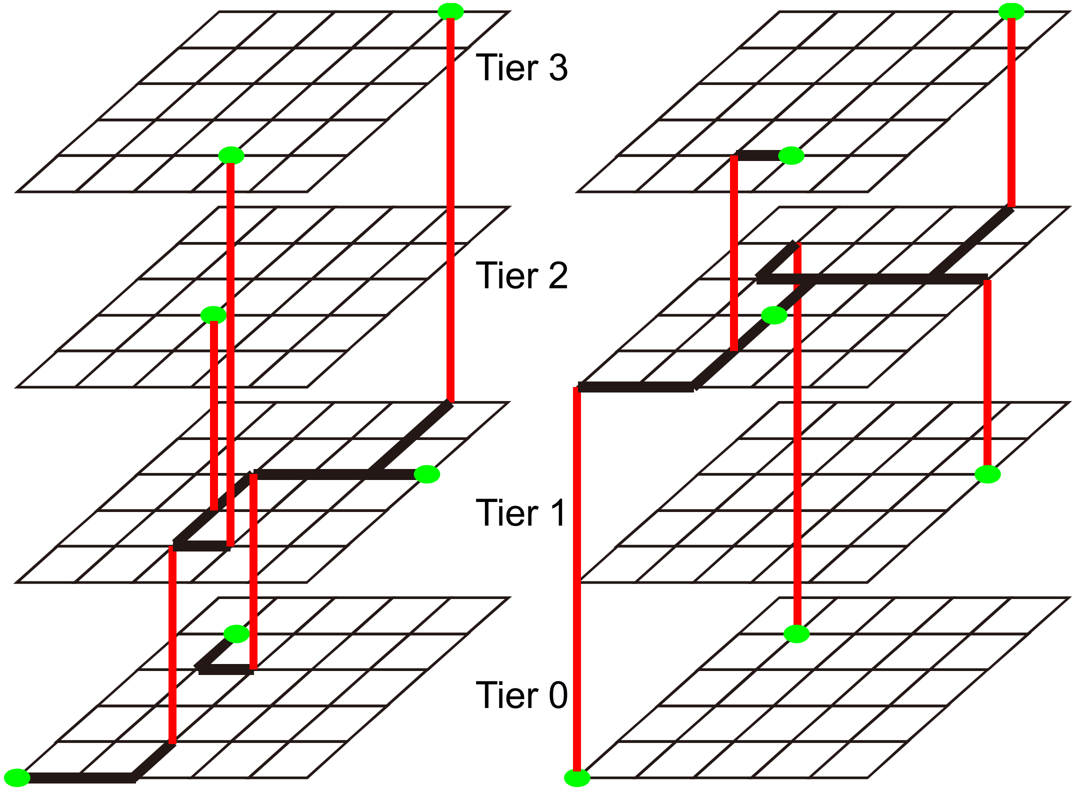
# Simulation Results – 3D POST DB Construction

| # pins | # pin groups (n!) | # 2D POSTs | # tiers | # all 3D POSTs (A) | # gen. 3D POSTs (B) | B/A | Time (C) | Eff. (B/C) | DB size |
|---|---|---|---|---|---|---|---|---|---|
| 2 | 2 | 4 | 2 | 24 | 12 | 0.5 | 0 | - | 0 |
| | | | 3 | 48 | 24 | 0.5 | | | |
| | | | 4 | 80 | 40 | 0.5 | | | |
| 3 | 6 | 16 | 2 | 224 | 84 | 0.375 | | | |
| | | | 3 | 896 | 336 | 0.375 | | | |
| | | | 4 | 2,352 | 888 | 0.378 | | | |
| 4 | 24 | 284 | 2 | 20,056 | 5,372 | 0.268 | | | |
| | | | 3 | 226,800 | 60,120 | 0.265 | | | |
| | | | 4 | 1,396,944 | 367,424 | 0.263 | | | |
| 5 | 120 | 4,260 | 2 | 719,864 | 125,360 | 0.174 | | | |
| | | | 3 | 14,876,928 | 2,575,092 | 0.173 | 5s | 491K | 16MB |
| | | | 4 | 142,195,680 | 24,482,354 | 0.172 | 96s | 256K | 167MB |
| 6 | 720 | 120,212 | 2 | 85,530,040 | 13,831,206 | 0.162 | 20s | 687K | 93MB |
| | | | 3 | 4,318,826,472 | 697,355,262 | 0.161 | 42m | 275K | 5GB |
| | | | 4 | 90,473,628,112 | 14,586,090,890 | 0.161 | **30h** | 134K | **129GB** |

# Simulation Results

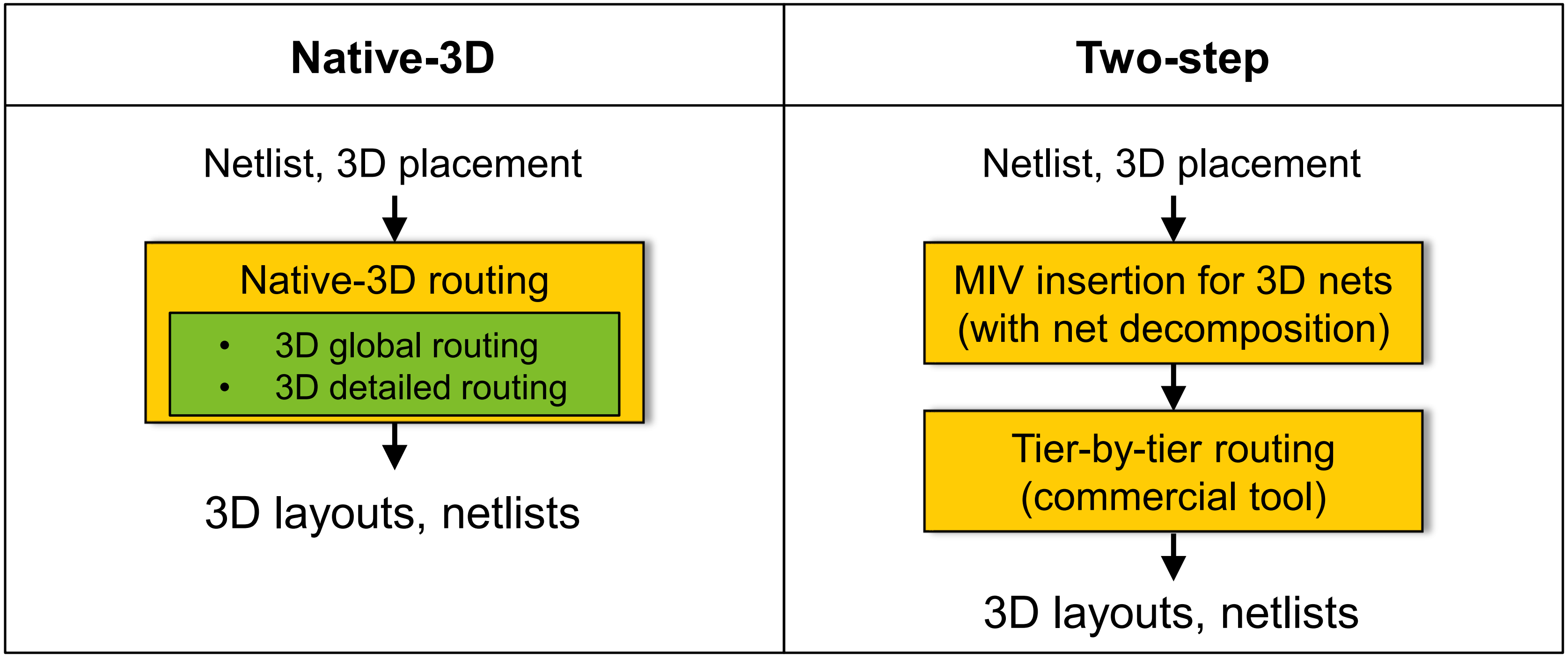
- Comparison of two 3D POSTs
  - Position sequence: 143625
  - Tier sequence: 032103
  - POWV: 1221111121
  - 2D POST





# Application – 3D Routing

- Comparison of two 3D routing methodologies



**Native-3D**

Netlist, 3D placement

Native-3D routing

- 3D global routing
- 3D detailed routing

3D layouts, netlists

**Two-step**

Netlist, 3D placement

MIV insertion for 3D nets
(with net decomposition)

Tier-by-tier routing
(commercial tool)

3D layouts, netlists

| | **Native-3D** | **Two-step** |
|---|---|---|
| Quality | High | **Optimal DB + MIV insertion** |
| Runtime | Slow | **Fast** |

# Application – 3D Routing

- Native-3D vs. (3D POST DB + Sequential MIV insertion)

| Circuit | # tiers | # insts | WL (Enc) | WL (Two-step) | # MIVs (Enc) | # MIVs (Two-step) |
|---|---|---|---|---|---|---|
| LDPC | 2 | 51K | 1.000 | 1.015 → 1.002 | 1.000 | 0.789 → 0.721 |
| | 3 | | 1.000 | 1.033 → 0.989 | 1.000 | 0.906 → 0.858 |
| | 4 | | 1.000 | 1.044 → 1.015 | 1.000 | 0.999 → 0.923 |
| FFT | 2 | 256K | 1.000 | 0.984 → 0.987 | 1.000 | 1.160 → 0.943 |
| | 3 | | 1.000 | 0.983 → 0.978 | 1.000 | 1.173 → 0.892 |
| | 4 | | 1.000 | 0.944 → 0.945 | 1.000 | 1.261 → 0.917 |

# Conclusion

- We built a database of all 3D POSTs for up to six pins and four tiers.
  - What about seven pins?
    - Two- and three-tier were doable.
    - Four-tier was not doable.

- The DB can be used for monolithic 3D IC design.
  - Placement
  - Routing
  - Optimization
  - …

- The DB shows that it can help generate many meaningfully-different MMRSMTs, which could improve the quality of 3D routing.

# Sponsors

- DARPA YFA D16AP00119

- Washington State University 125679-002

# Thank you

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(Please email me for the database)