Pin Access-Driven Design Rule Clean and DFM Optimized Routing of Standard Cells under Boolean Constraints

Nikolay Ryzhenko

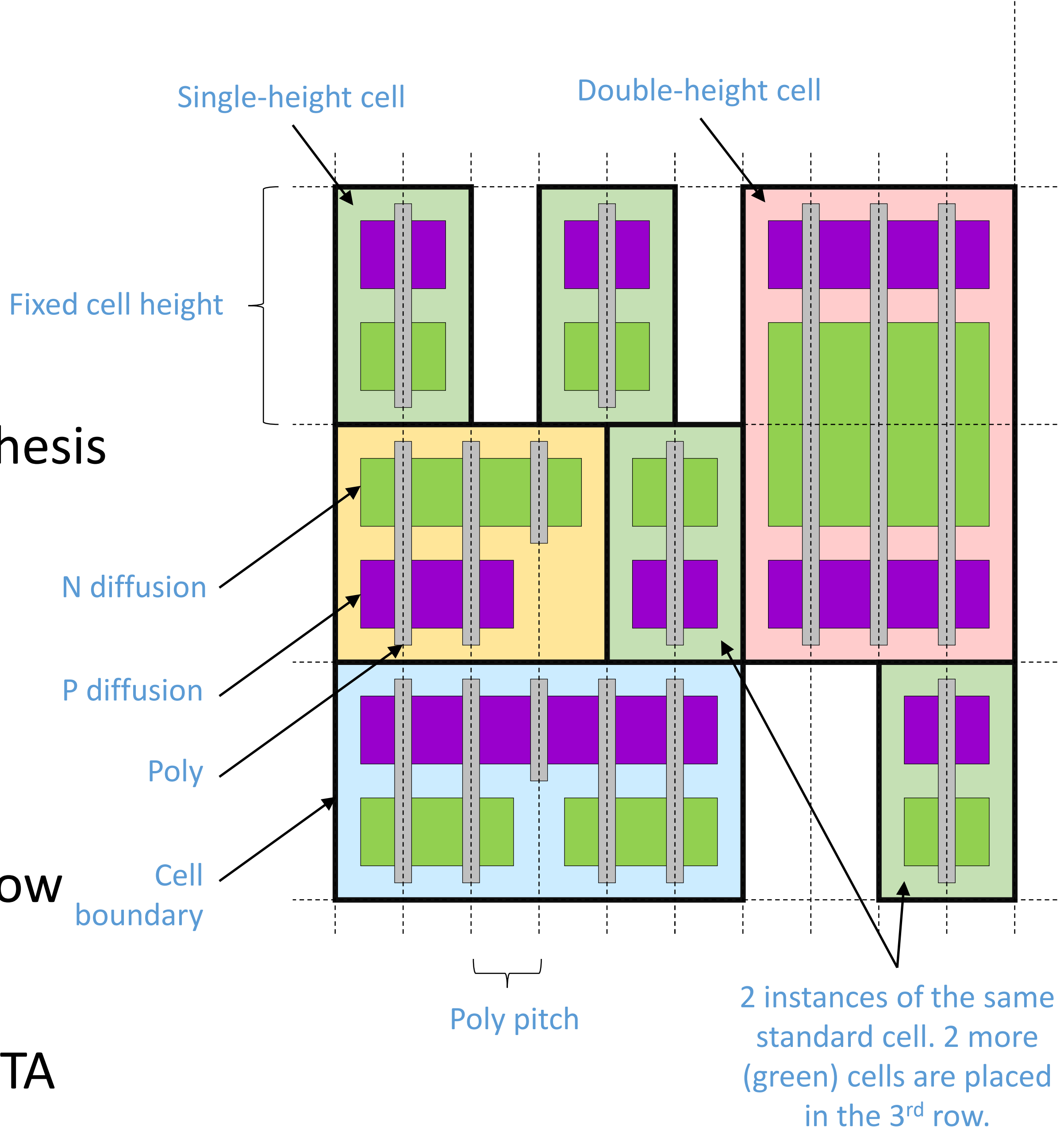
Steven Burns, Anton Sorokin, Mikhail Talalay

Intel corporation, Hillsboro, OR, USA

Introduction

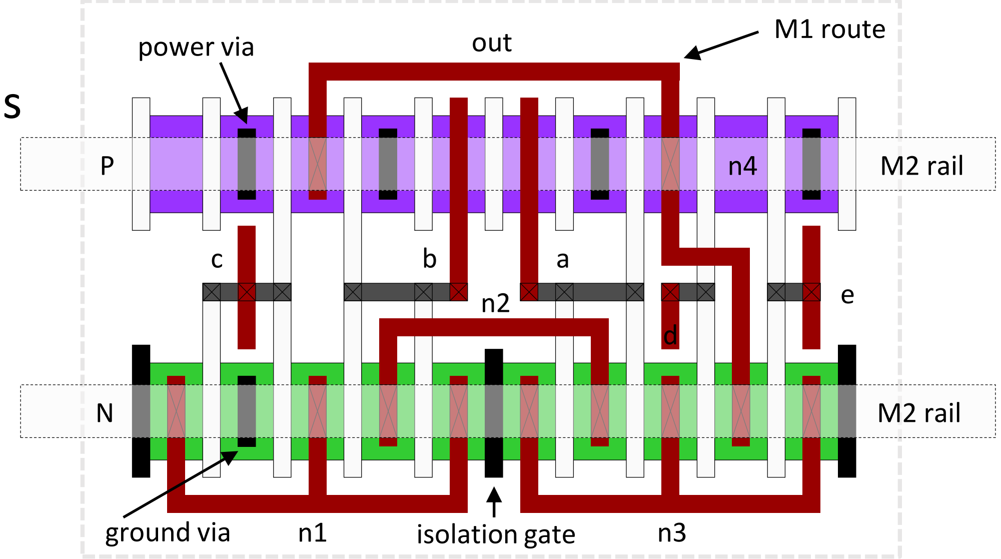
- Standard cell design:
  - The only way for Random Logic Synthesis
  - Fixed and discrete height of cells
  - Discrete cell width
  - Fixed power grid layout

- Encapsulation:
  - Layout: any cells can be placed anyhow next to each other
  - Logic: fixed logic function
  - Characterization: fast and accurate STA



Routing of Standard Cells

- Primary requirements:
  - DRC-clean and correct by abutment
  - All nets are to be routed: transistors are connected by wires and vias according to the netlist
  - Power/ground nets are connected to the rails
  - Pin access: I/O nets must have a specified number of feasible intersections with the upper metal layer
- Optimizations:
  - PPA: Power, performance, area
  - Reliability, extra pin hit points; pin density
- Emerging challenges:
  - Design for manufacturing
  - Metal fill & via density

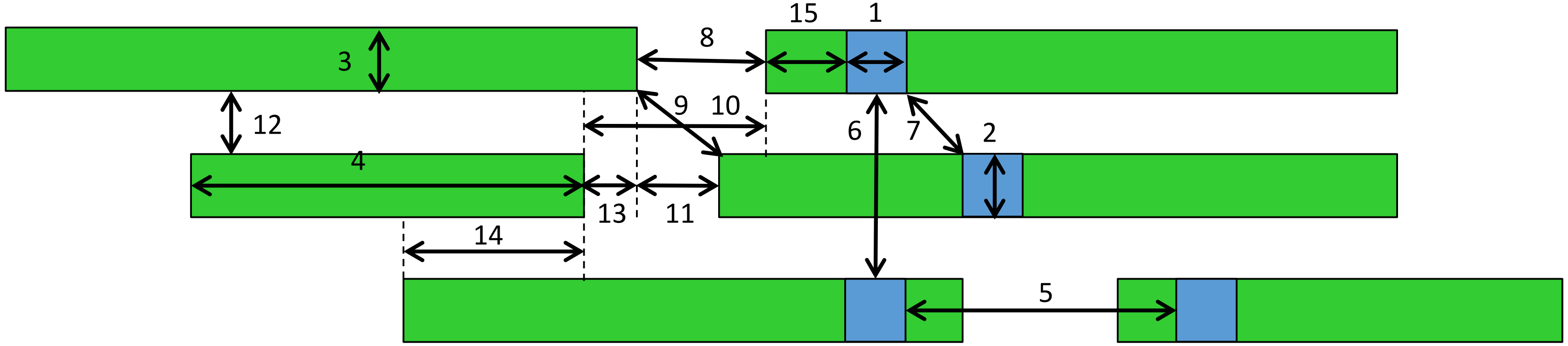


Design Rules

- A gap between the 193nm optical wave length and sub 20-nm layout objects makes design rules complex and non-local.
- The complexity of rules only grows with every technology node:
  - The number of involved objects;
  - The number of involved tracks in a design rule;
  - The number of corner cases (if then, if then, if then …).
- Neither traditional tools nor humans can handle such complex rules optimally

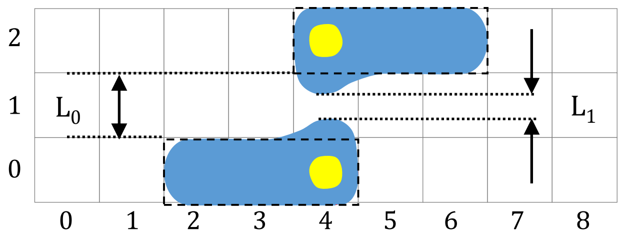
Design Rules

- Basic rules involve two objects: (1) some via/wire side/edge/corner to another (2) via/wire side/edge/corner
  - Legal (minimal) via/wire width/length (1, 2, 3, 4)
  - Via-2-via edge/side/diagonal spacing (5, 6, 7)
  - Wire-2-wire edge/side/corner spacing in the same and adjacent tracks (8, 9, 10, 11, 12)
  - Minimal offsets between wire end-lines (13, 14)
  - Minimal wire enclosure for a via edge (15)
- There can be multi-object DRs: forbidden placements of 3+ vias, forbidden configurations of 3+ wire cuts, different minimal wire lengths for different combinations of other wires and vias around, etc.



Design For Manufacturing

Design rules are always a tradeoff between manufacturability and marginality: yield vs. PPA, time to market, #masks.

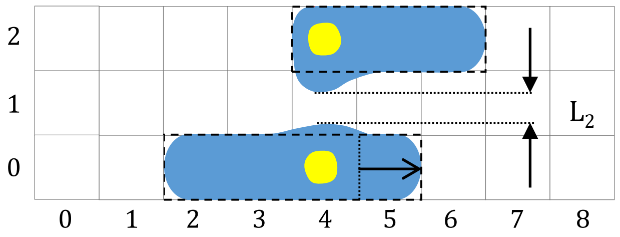


Design rule clean layout:
Two wires and two vias

L_0 is a minimal spacing (design rule value)
L_1 is an actual silicon spacing

$L_1 < L_0$

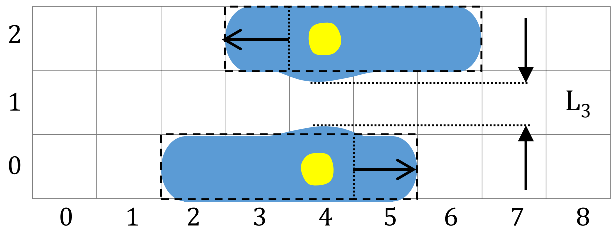
Litho-unfriendly layout pattern



Added extra wire length

$L_2 > L_1$

Layout becomes more sustainable



Added even more wire length

$L_3 > L_2$

Litho-friendly layout pattern may affect PPA due to longer wire length.

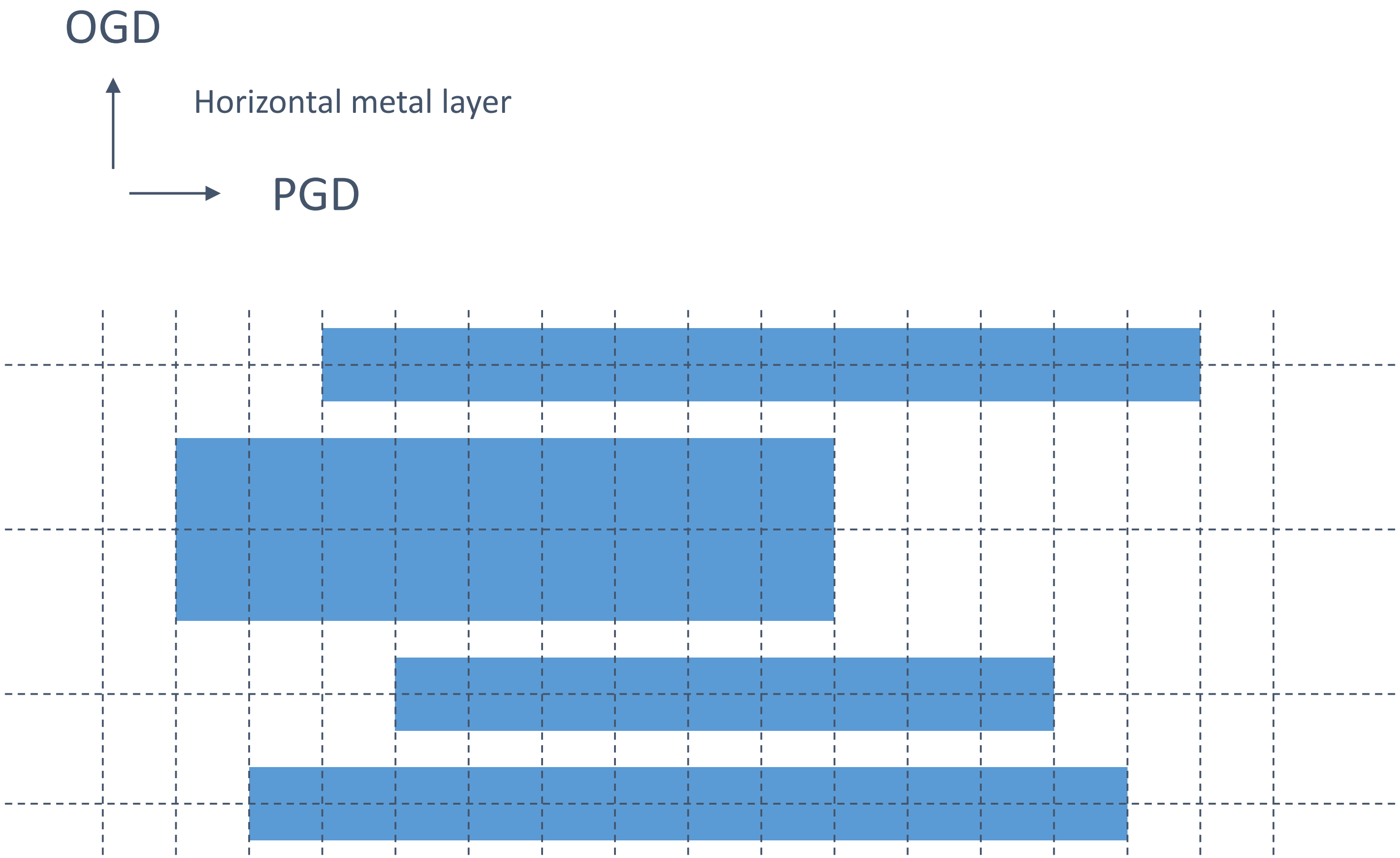
Layout Regularity Trends

- Layouts naturally become more and more regular:
  - FinFETs: Fixed poly grid and diffusion fins
  - Unidirectional layers without jogs
  - Fixed metal templates
  - Fixed via sizes
- Following things become practical
  - Discrete layout models
  - Accurate solving techniques

Layout Modeling

- We used following work as a base:
  - G. Suto, **Rule agnostic routing by using design fabrics**, *Proceedings of the 49th Annual Design Automation Conference, June 03-07, 2012, San Francisco, California*
- Gridded Layout Data Model is intended to model any arbitrary layout constraints of different nature:
  - Design rules
  - DFM guidelines
  - Density rules
- Cell architecture rules:
  - Boundary rules
  - Pin-access requirements
- Quality of layout:
  - Wire length, via count, via size, diffusion contacts, poly contacts, metal jogs, etc.

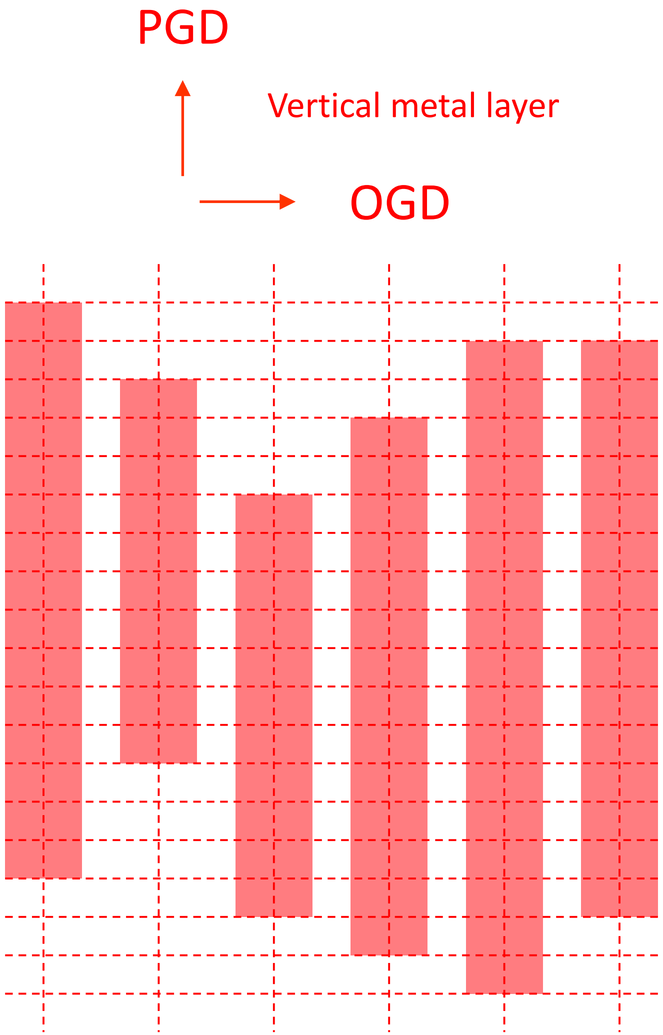
Metal Grids



OGD

Horizontal metal layer

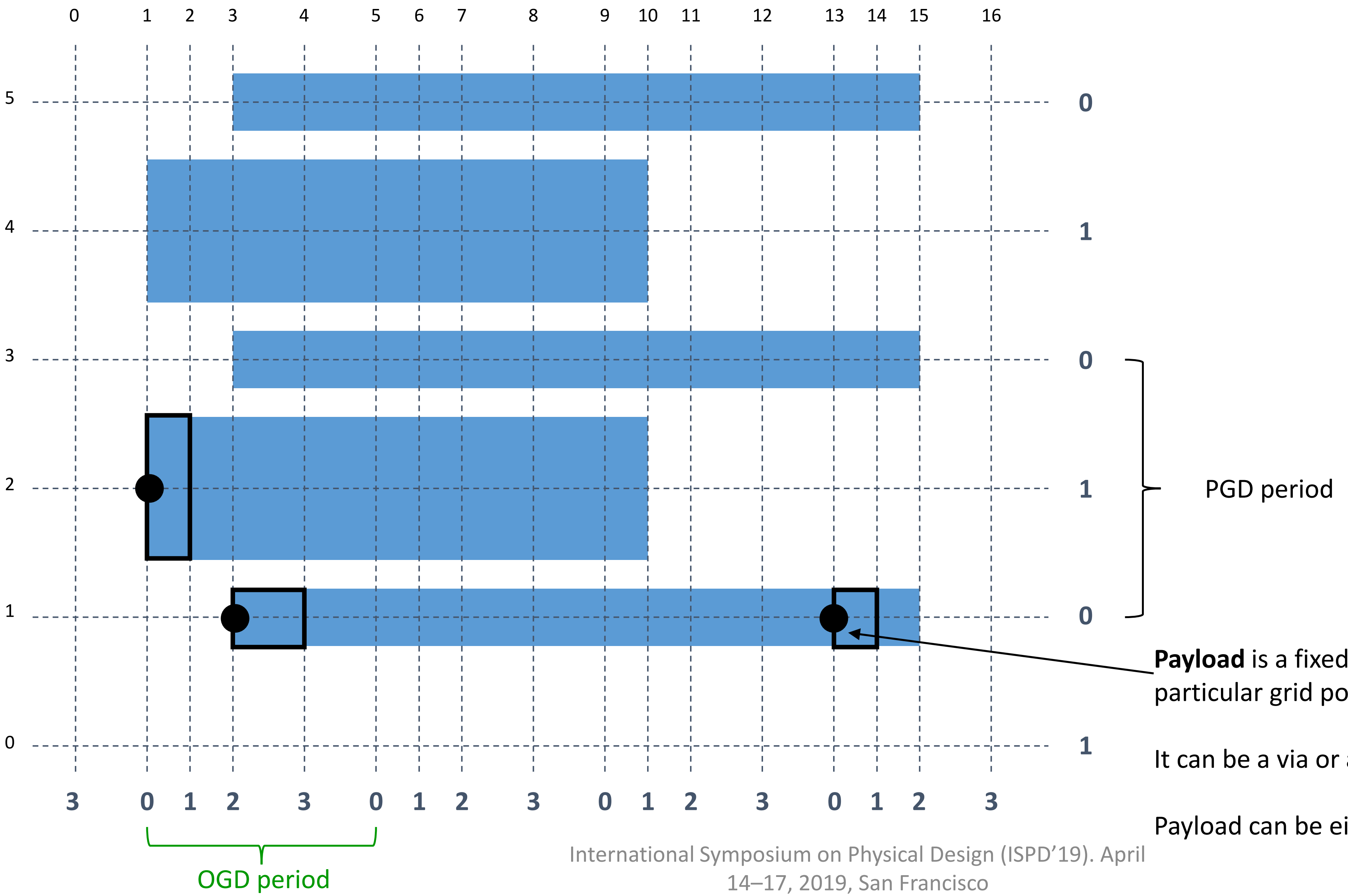
PGD



PGD

Vertical metal layer

OGD



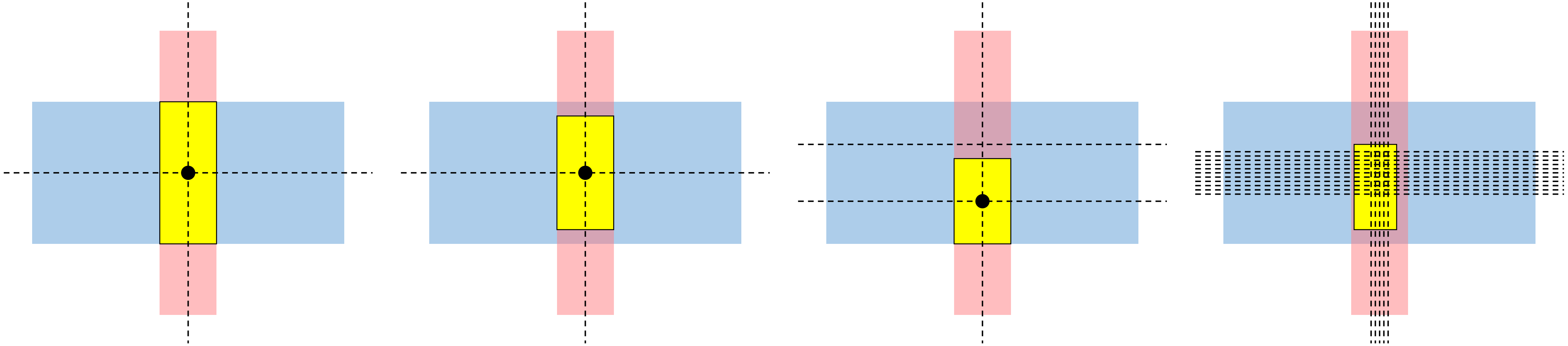
Payload is a fixed layout discrete associated with a particular grid point.

It can be a via or a piece of wire.

Payload can be either present or absent.

Via Grids

- An intersection of metals may allow different via options: sizes, alignment of sides, position
- In practical examples, every via type has own grid



a) Ultimate regular case: symmetric in both directions; 4 metal-side aligned; central

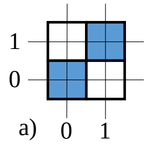
b) Symmetric in both directions; 2 metal-side aligned; central

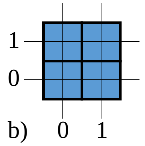
c) 3 metal-side aligned via

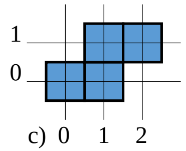
d) Free via placement at intersection

Examples of Layout Modeling

- A binary decision variable is created for every payload
- Boolean expressions describe arbitrary layouts
- In practice, we describe illegal layouts to model design rules



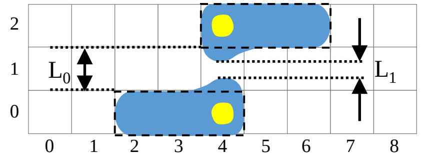




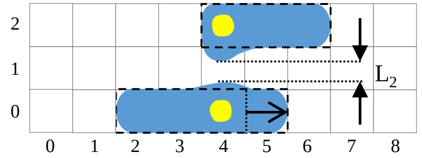
$$F_1 = S(0,0) \wedge S(1,1) \wedge \overline{S(0,1)} \wedge \overline{S(1,0)}$$

$$F_2 = S(0,0) \wedge S(1,0) \wedge S(0,1) \wedge S(1,1)$$

$$F_3 = S(0,0) \wedge S(1,0) \wedge S(1,1) \wedge S(2,1)$$

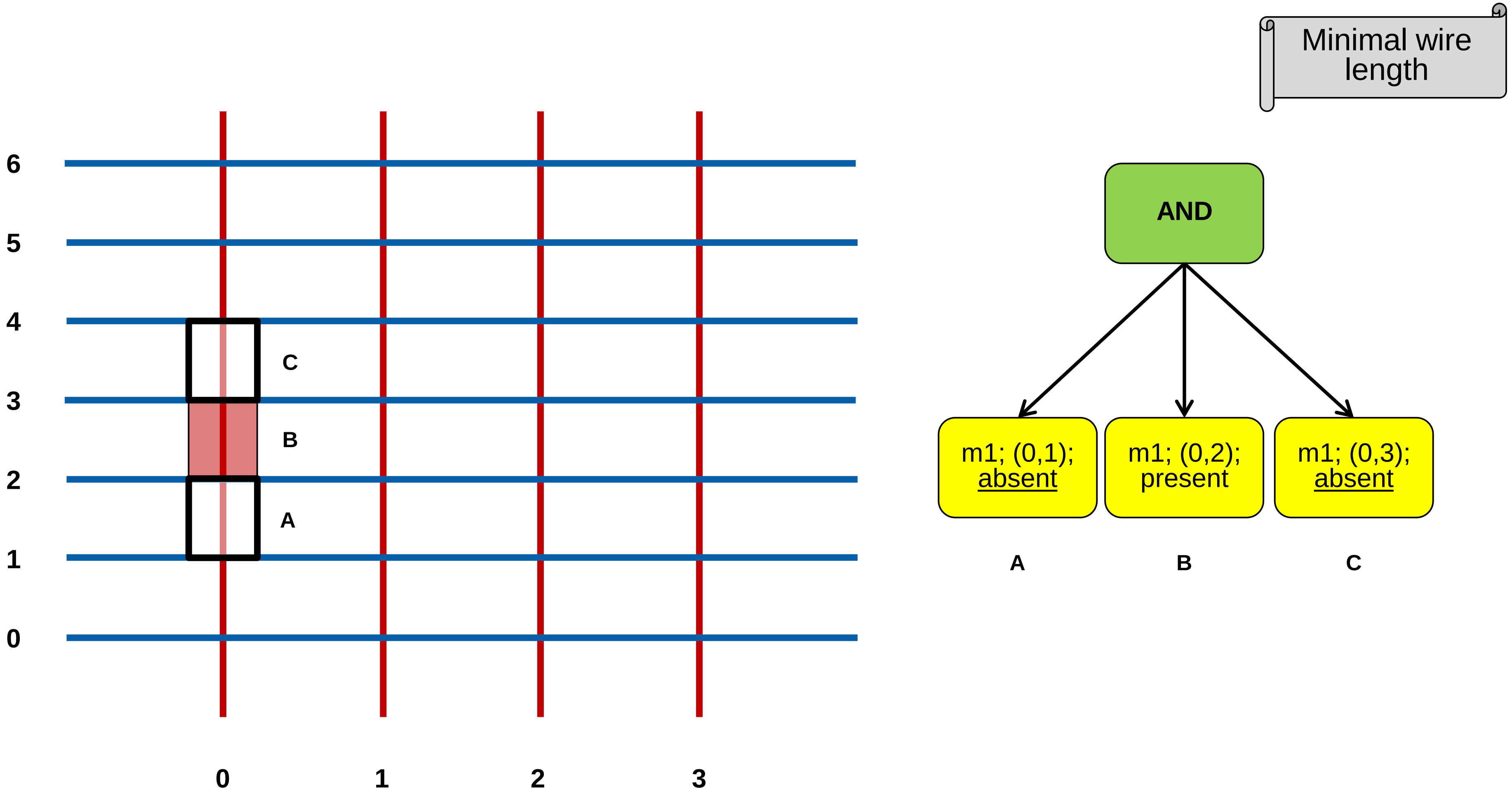


$$F_4 = V(4,0) \wedge V(4,2) \wedge M(4,0) \wedge \overline{M(5,0)} \wedge M(4,2) \wedge \overline{M(3,2)} \wedge \overline{M(3,1)}$$



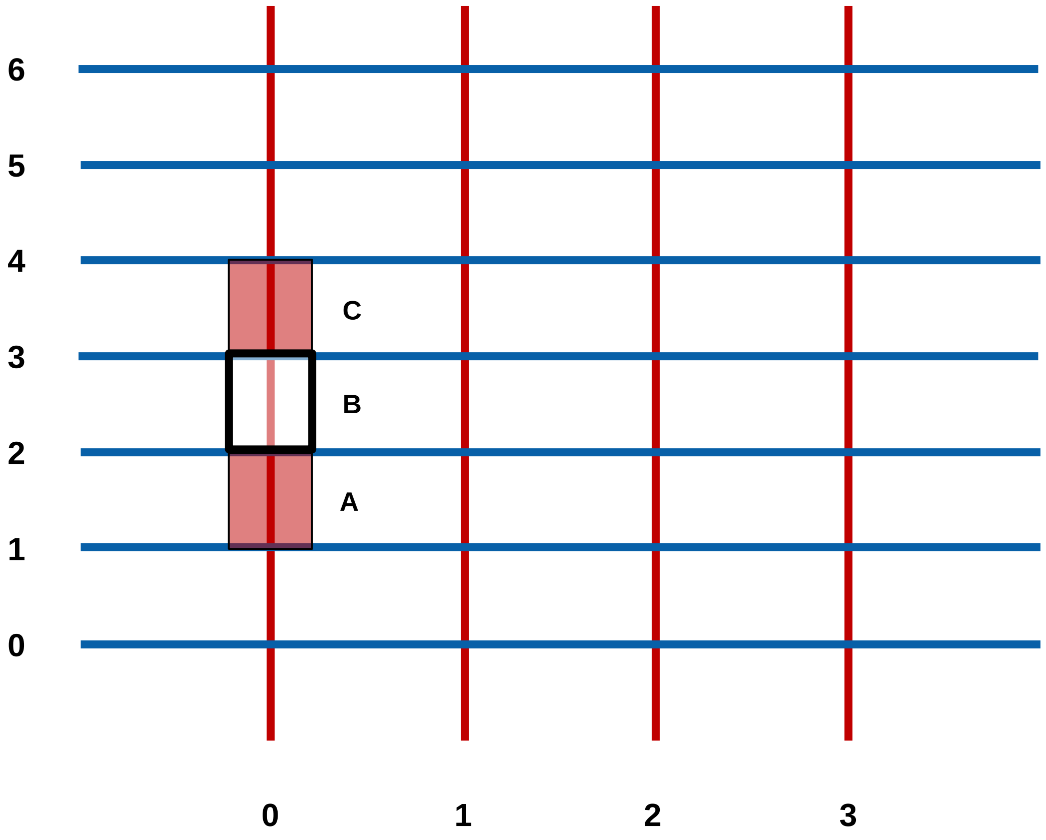
$$F_5 = V(4,0) \wedge V(4,2) \wedge M(4,0) \wedge M(5,0) \wedge \overline{M(6,0)} \wedge M(4,2) \wedge \overline{M(3,2)} \wedge \overline{M(3,1)}$$

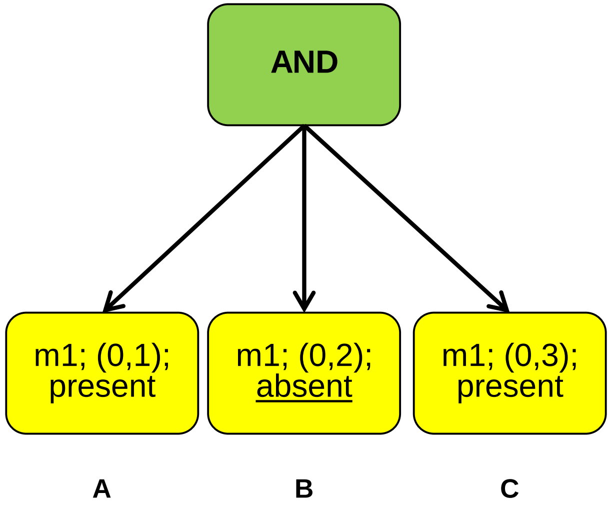
Examples of Patterns (1)



Examples of Patterns (2)

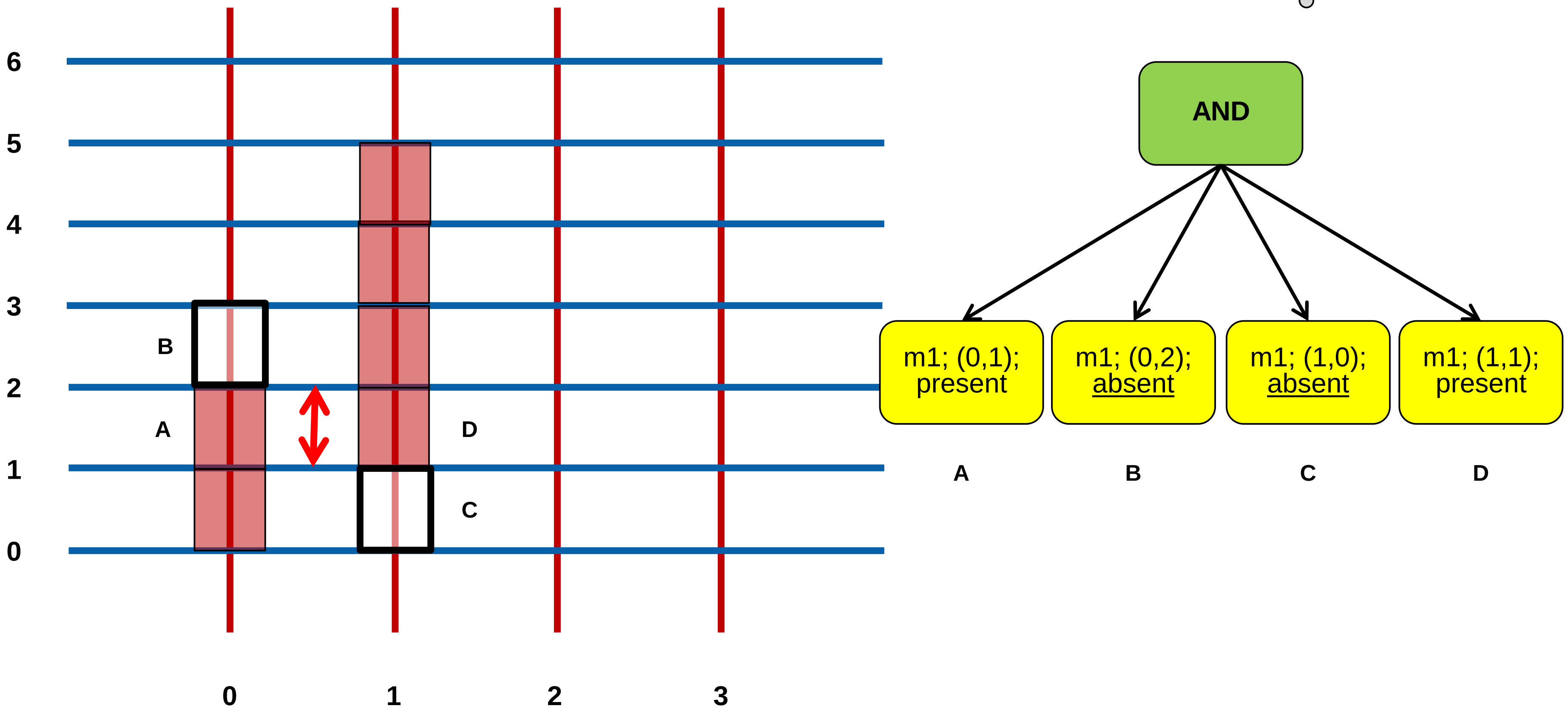
Minimal ETE spacing





Examples of Patterns (3)

Minimal wire overlap

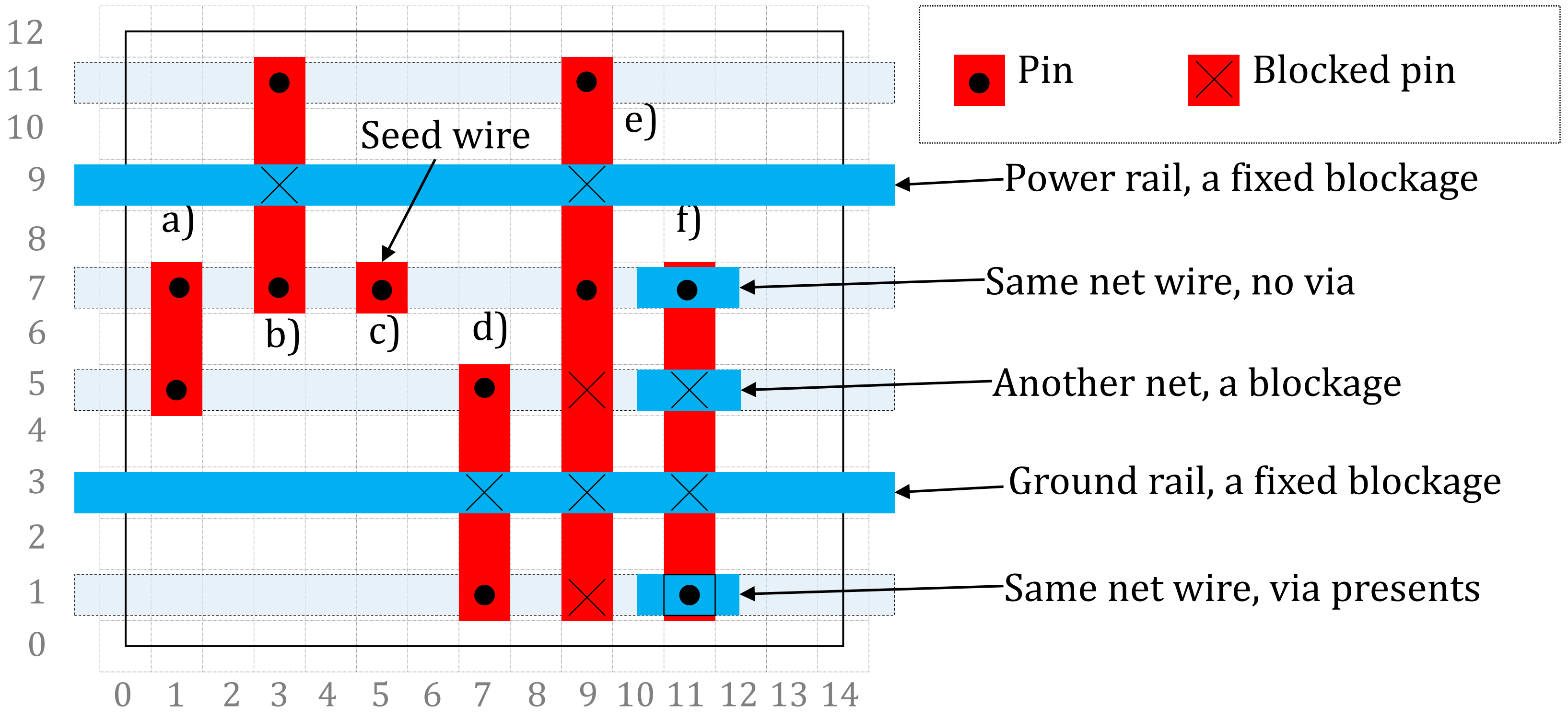


SAT Router

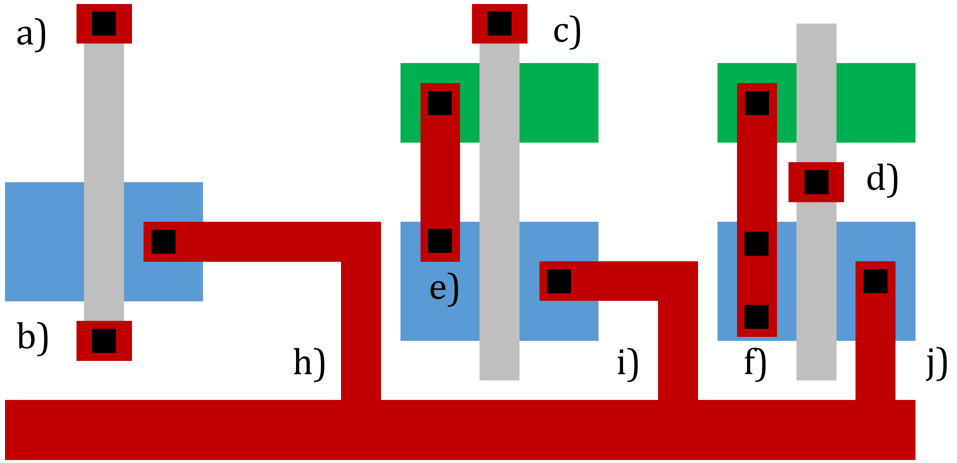
- Given a Boolean formula, SAT determines if the variables can be assigned in such a way to make the formula true.
- Routing of nets is constructed from candidate routes. A candidate route consists of vias and wire discretes.
- Nets are split into two-terminal connections.
- A global router selects reasonable connections.
- A maze router constructs several candidate routes:
  - For every transistor-to-transistor connection;
  - Between transistors and power rails;
  - Between transistors and possible seed metal1 pin wires.
- Pair conflicts between routes help to prune unfeasible candidates.
- Strict rules are modeled via illegal layout patterns.
- SAT finds the first possible solution if it exists.

Pin-Access Requirements

Every metal1 pin wire in this example must have at least 2 feasible hit points



Layout Quality Aspects

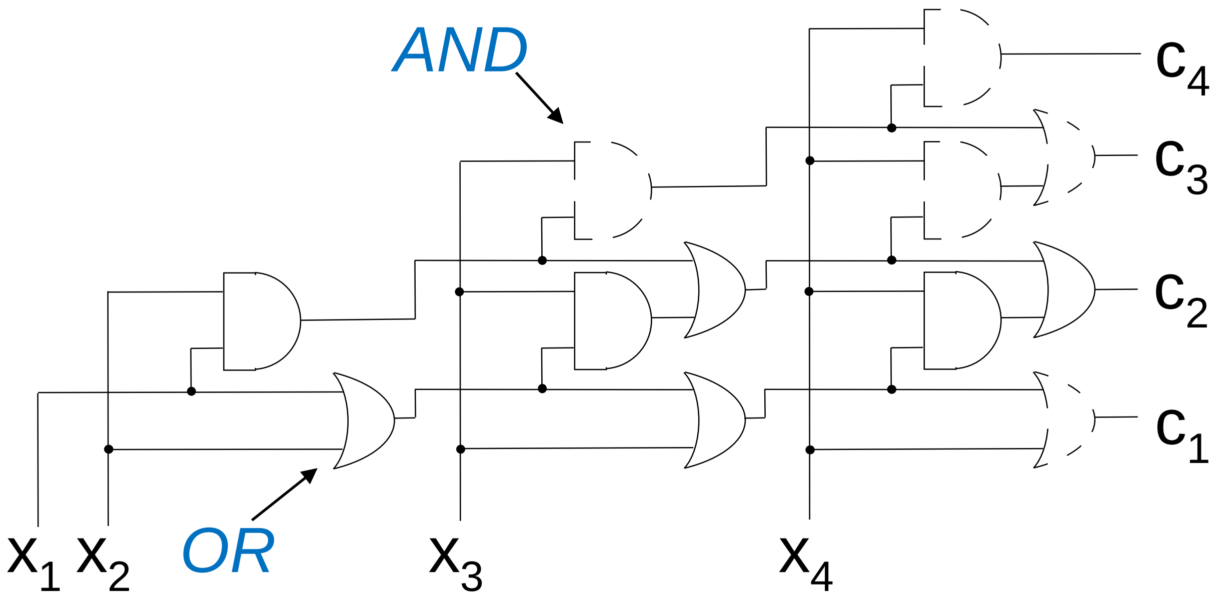


- Contact a) is worse than b) because of a long high-resistance poly wire.
- Peripheral contact c) is worse than a central contact d) between two transistors.
- A contact with two uniformly placed vias f) is more reliable than a single-via contact e) at the diffusion side.
- A power rail hook-up i) is better than the long one h) but worse than the shortest one j).

SAT optimizations

- SAT finds the first possible solution if it exists.
- Without additional constraints, layout will be complete and DRC-clean but the quality will be unacceptable
- Extra layout patterns model legal but undesired layout cases
- Groups of undesired layout patterns are minimized lexicographically according to the predefined criticality.
- SAT solvers can specify assumptions: it is possible to assign temporary values to literals.

Counters



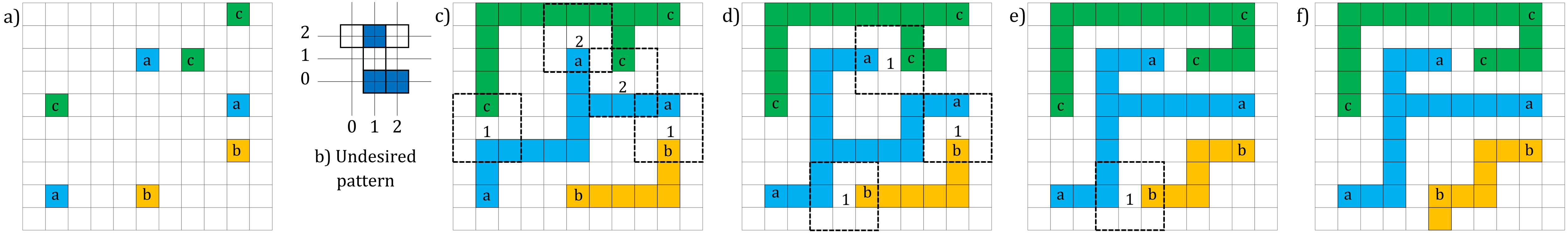
TRUE when N({x} == TRUE) ≥ 4; corner case: AND({x})

TRUE when N({x} == TRUE) ≥ 3

TRUE when N({x} == TRUE) ≥ 2

TRUE when N({x} == TRUE) ≥ 1; corner case: OR({x})

Evolution of Routing under SAT Constraints



a) Terminals of nets

b) Undesired layout pattern: a line-end attacker on wire side

c) Initial routing with 6 layout instances of (b)

d) Applied an assumption $C_{\leq}(p(F_b),3) = TRUE$; no more than 3 instances of (b) can appear

e) Applied an assumption $C_{\leq}(p(F_b),1) = TRUE$; no more than 1 instance of (b) can appear

f) Pattern (b) is forbidden completely: (b) acts a strict layout rule

Experimental Results

Table 1. Routing results for combinational and sequential cells from a 10 nm standard cell library.

Cell type	#transistors	#nets	#routes	#literals	#clauses	Total runtime, m:ss.	SAT runtime, m:ss.
XOR	13	8	2,533	486,338	1,217,752	1:14	0:06
2-to-1 multiplexer	13	10	1,677	519,607	776,481	0:57	0:07
Half adder	18	12	2,002	681,392	1,144,917	1:37	0:12
High-strength AND-OR	22	13	1,180	679,452	614,128	0:43	0:04
Flip-flop	28	16	3,822	982,610	1,851,459	2:56	0:32
Full adder	32	17	3,797	1,236,482	2,713,914	5:45	2:14
Scanable Flip-flop	38	25	4,160	1,826,160	3,266,194	6:19	1:00

Thank you!