Building the Adaptable Intelligent World

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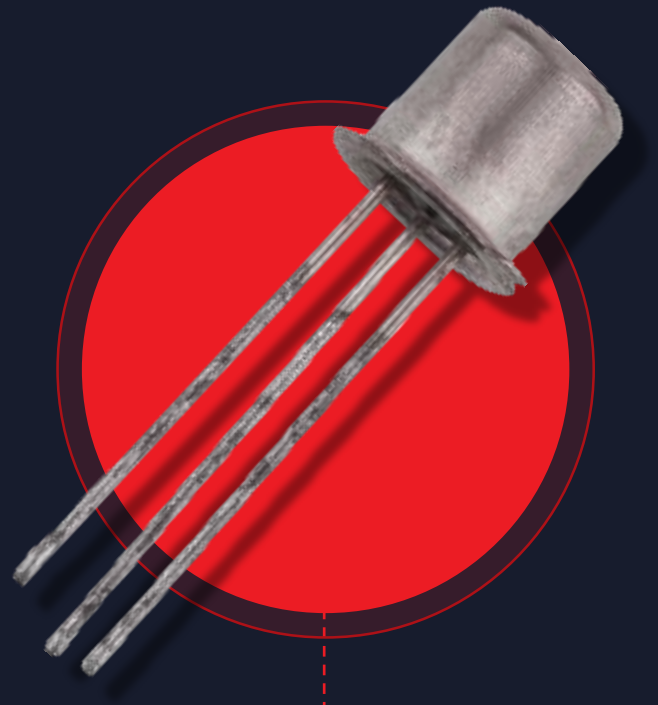
Disruptive Innovation



Transistor

1940s

Computing

1970s

Distributed Computing

1990s

Mountains of Unstructured Data

One Architecture Can’t Do It Alone

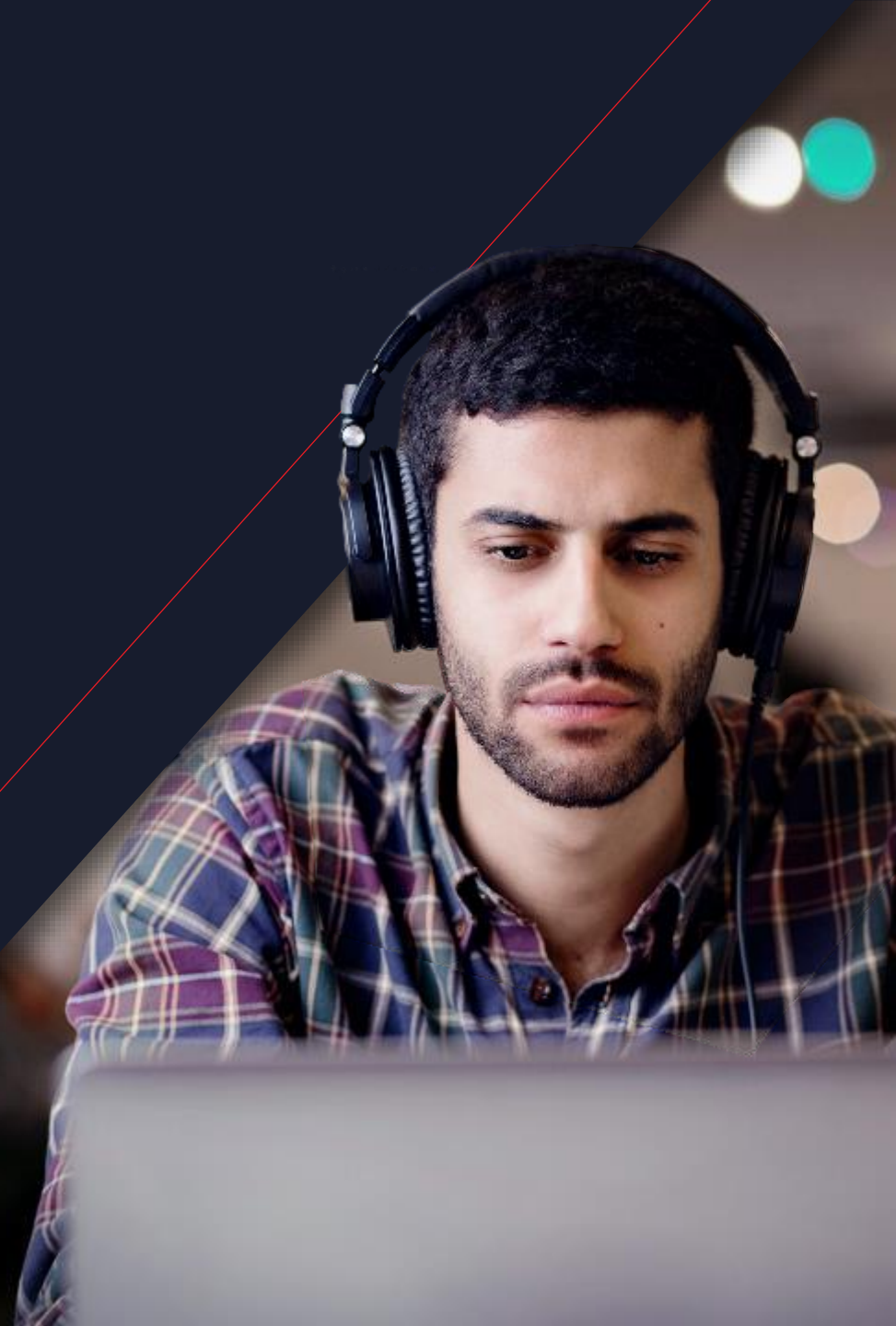
This is the Era of Heterogeneous Compute

Today's Developer Needs

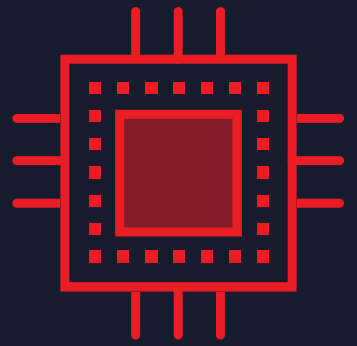
Software programmability

Performance for a diverse range of applications

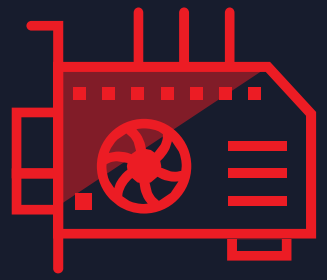
Adaptability to keep pace with rapid innovation



Today’s Solutions

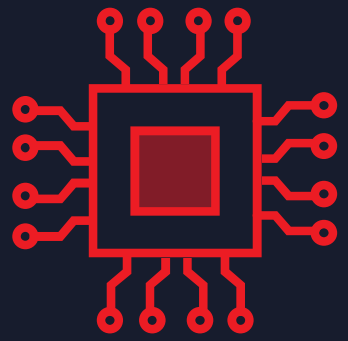


CPUs



Fixed Function Accelerators

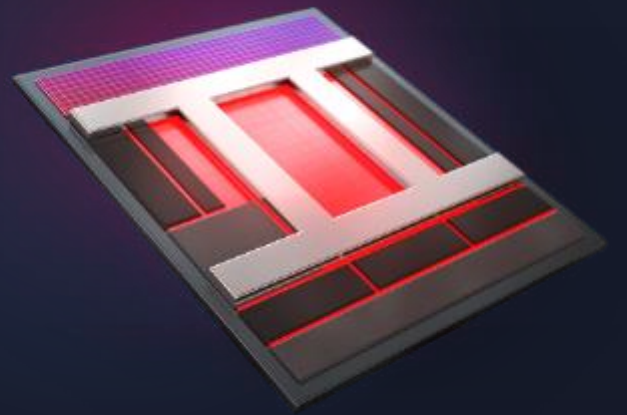
ASICs/ASSPs/GPUs

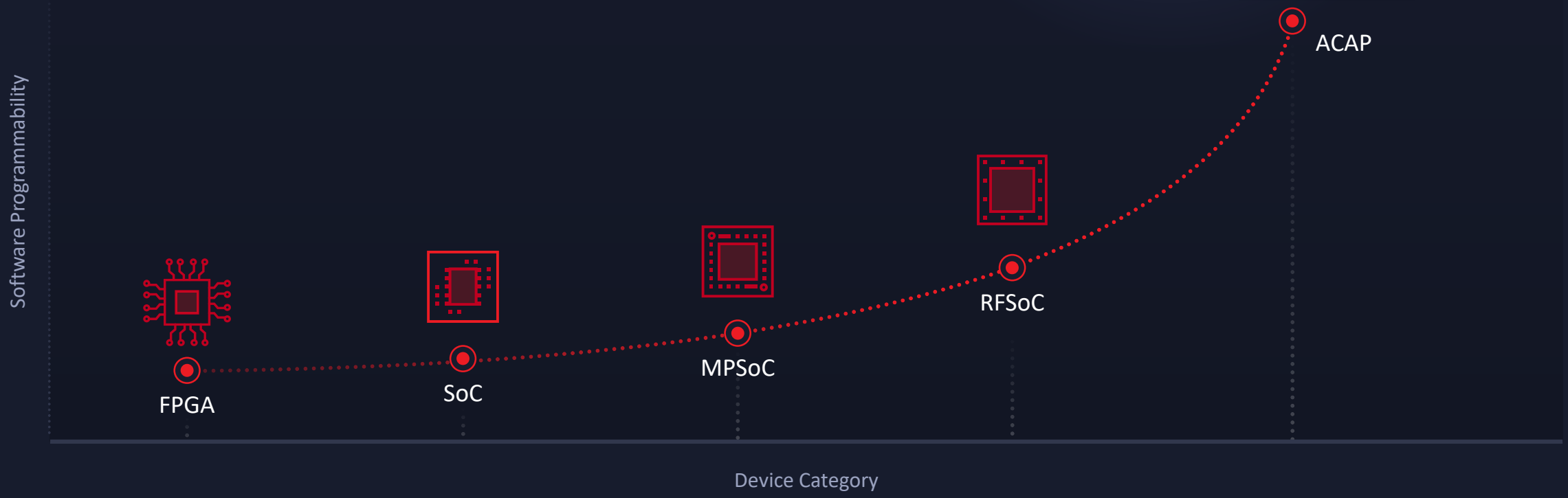


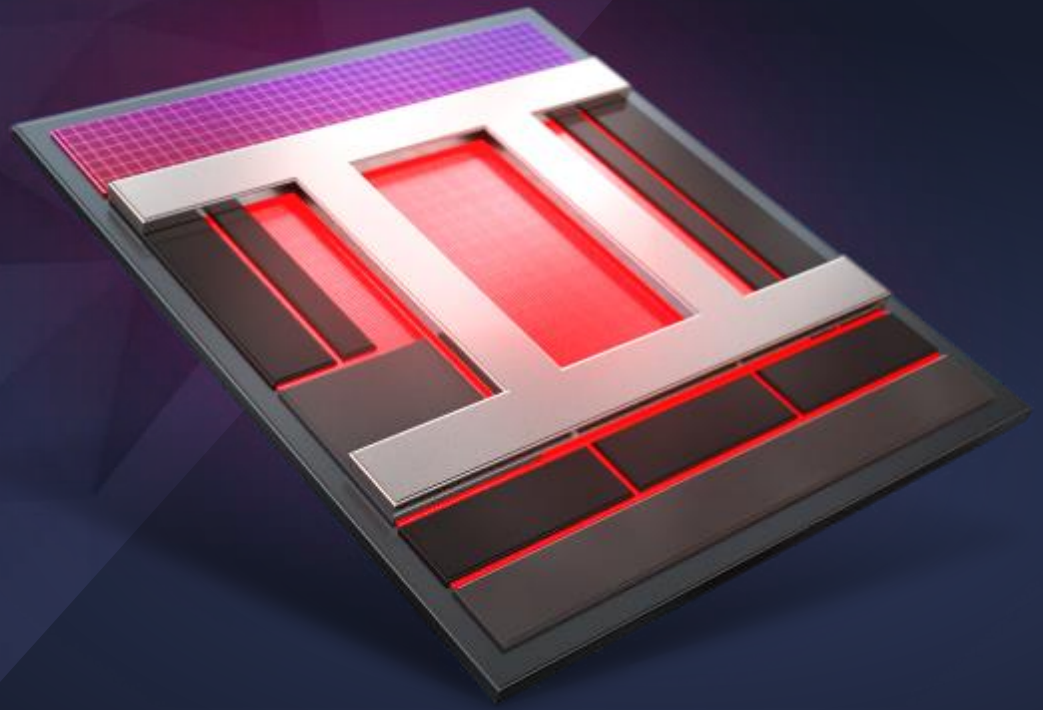
FPGAs

Disruptive Innovation Needed: Enter ACAP

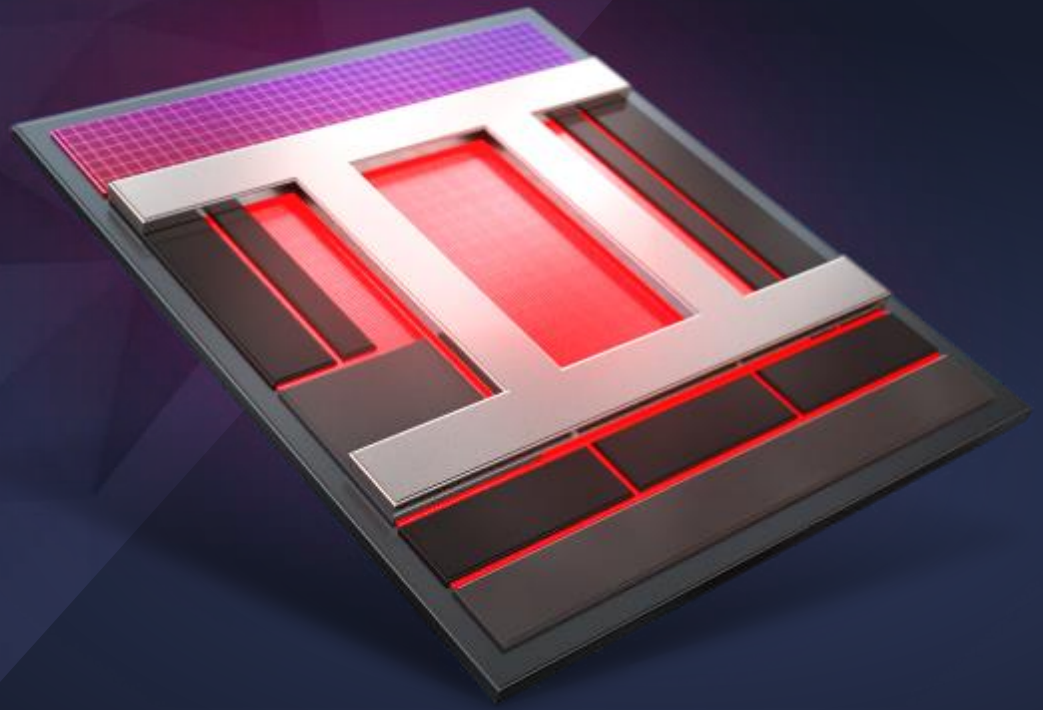
A new class of devices for today's challenges





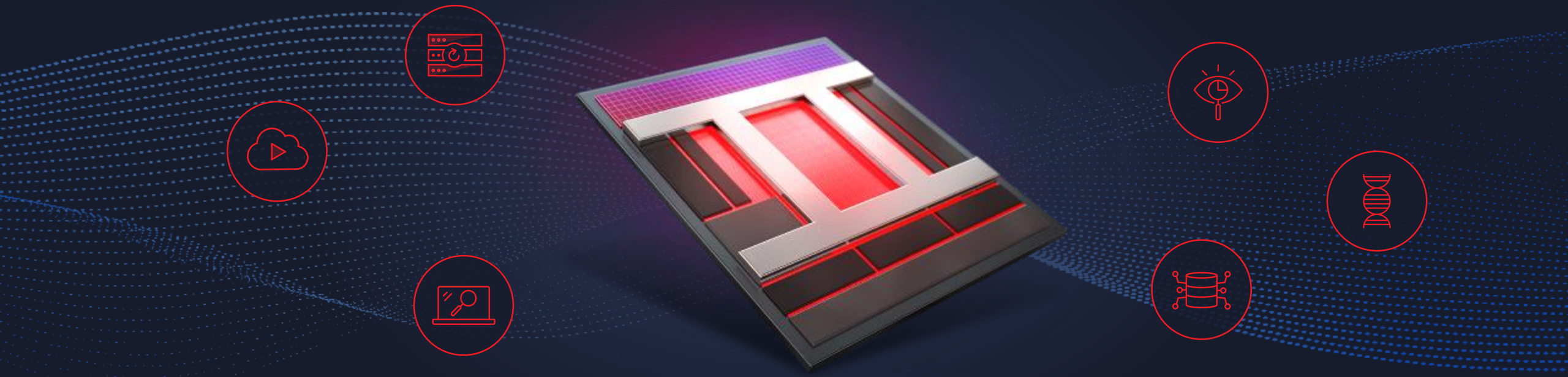


ACAP



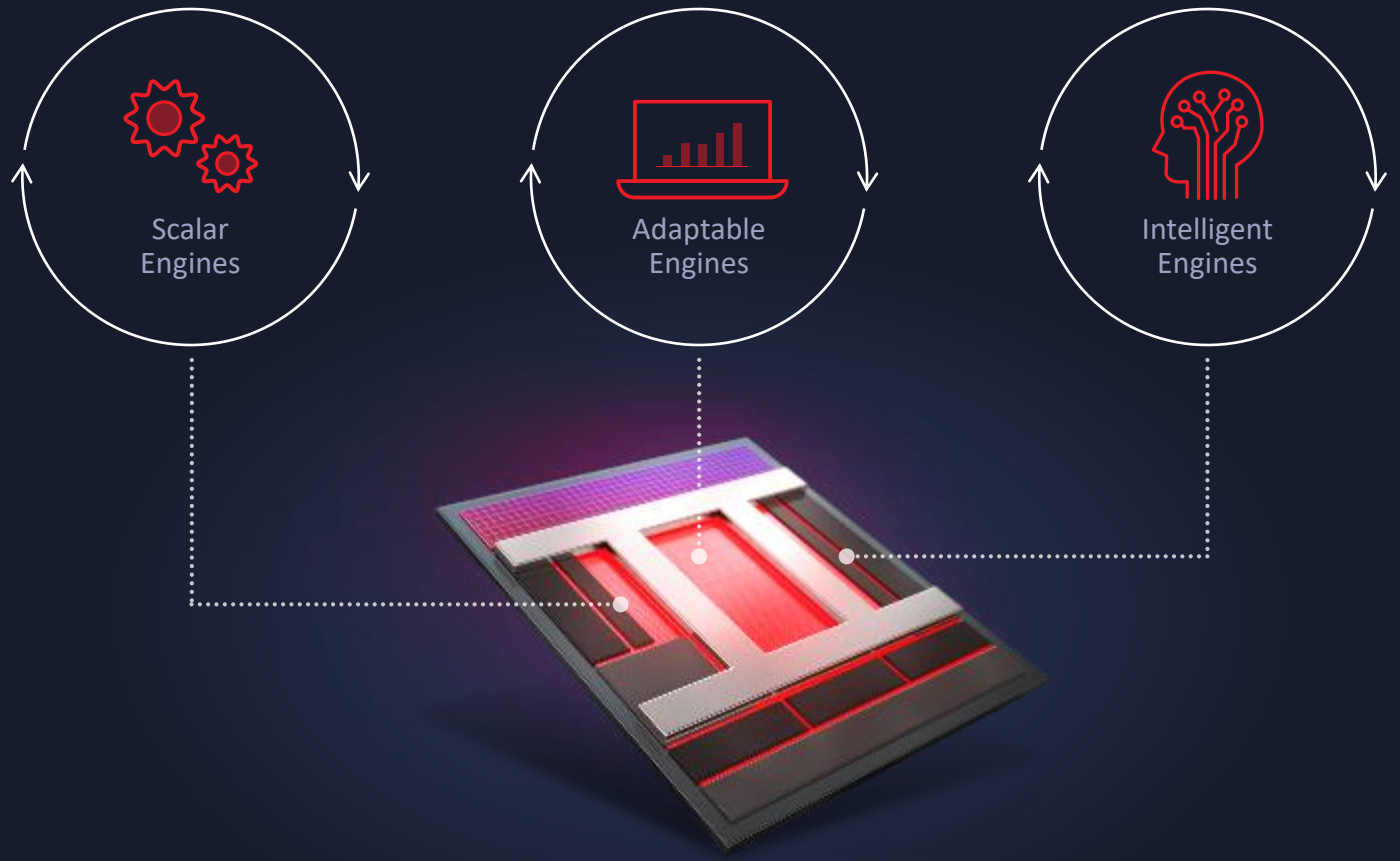
Adaptive Compute Acceleration Platform

Adaptive



Adaptive Hardware for
Domain-specific Applications

Compute Acceleration



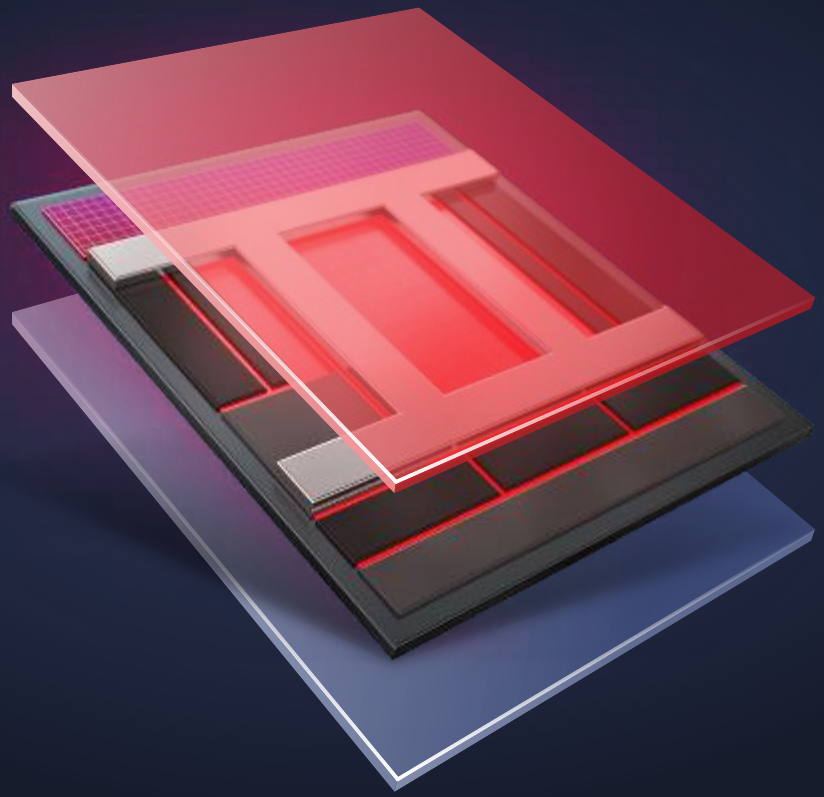
Platform

ENABLING:

Data Scientists

SW App Developers

HW Developers

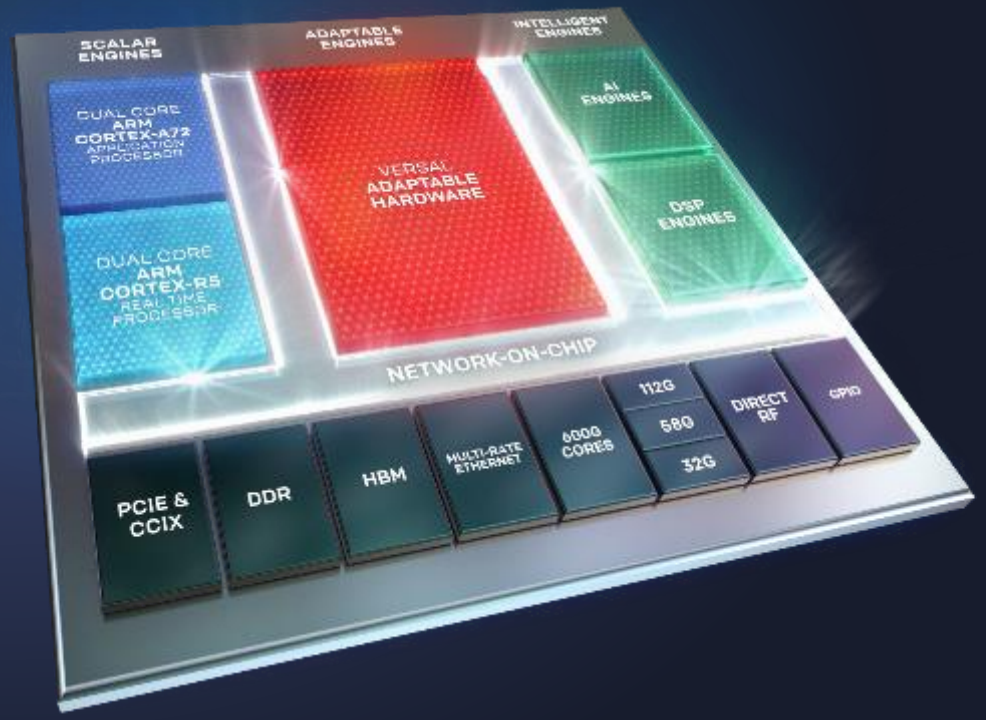


Development Tools
HW/SW Libraries
Run-time Stack

SW Programmable
Silicon Infrastructure

Versal ACAP Technology Tour

- Scalar Processing Engines
- Adaptable Hardware Engines
- Intelligent Engines
  SW Programmable, HW Adaptable
- Breakout Integration of Advanced Protocol Engines

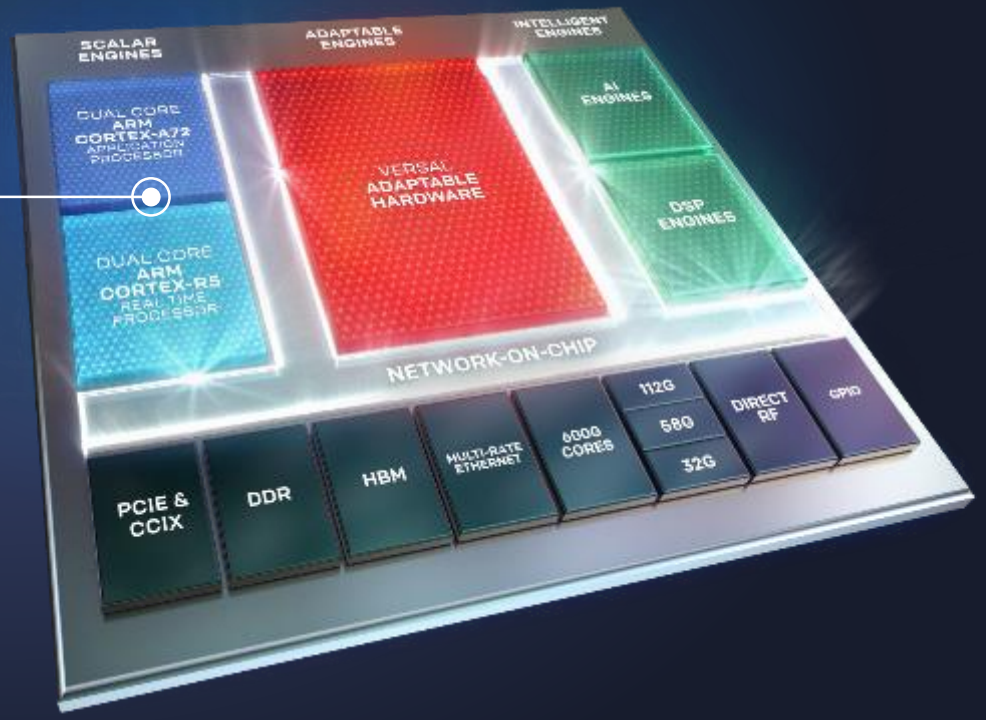


Scalar Processing Engines

Arm Cortex-A72
Application Processor

Arm Cortex-R5
Real-Time Processor

Platform Management Controller

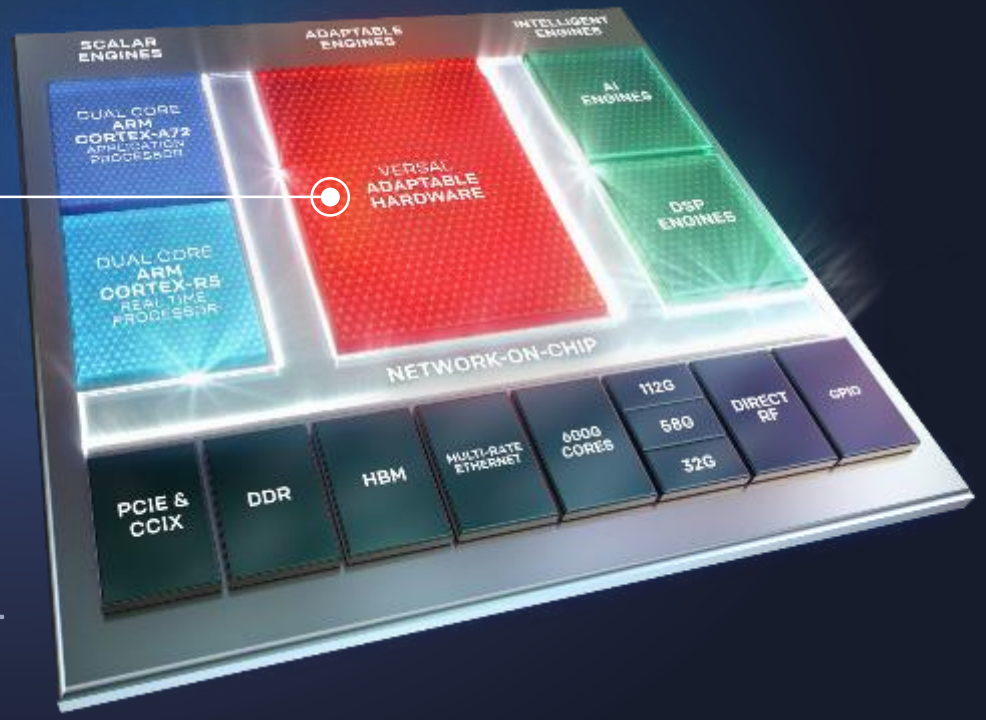


Adaptable Hardware Engines

Re-architected foundational HW fabric for greater compute density

Enables custom memory hierarchy

8X Faster Dynamic Reconfiguration (“on-the-fly”)



Intelligent Engines

DSP Engines

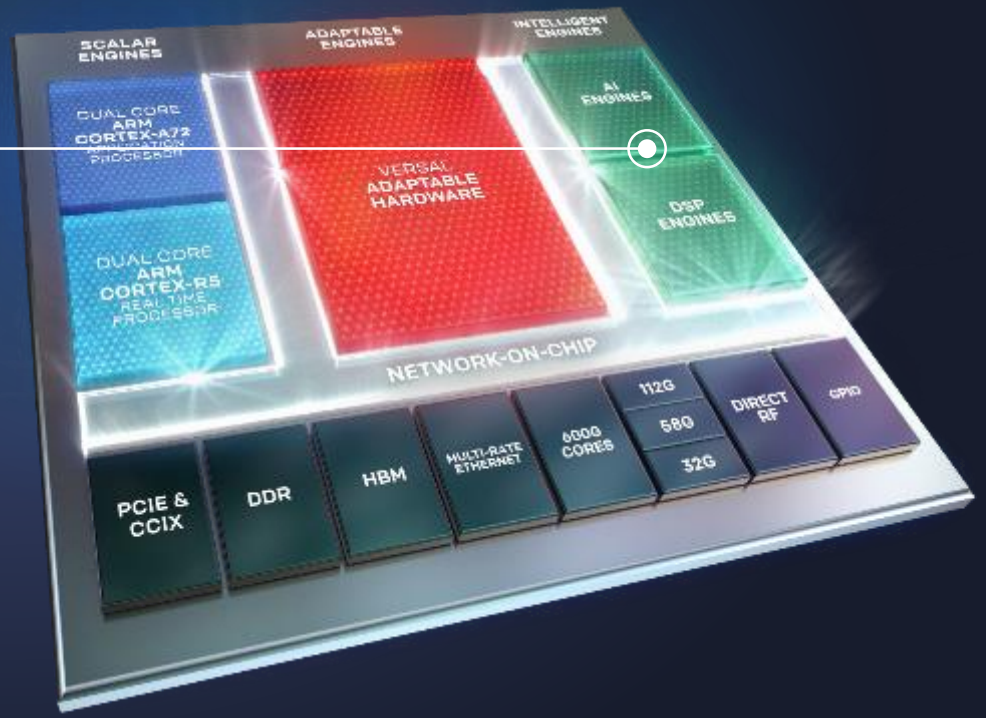
High-precision floating point & low latency

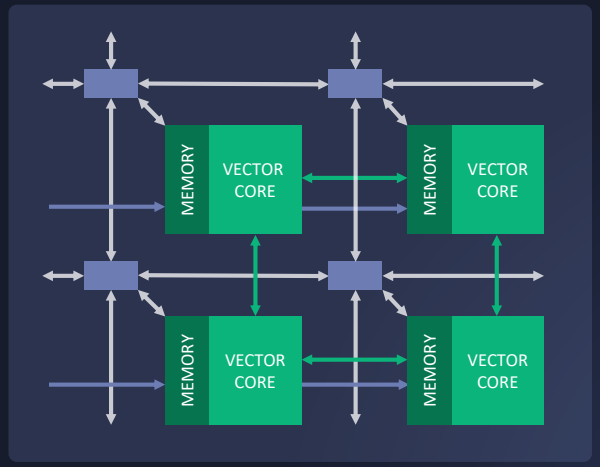
Granular control for customized datapaths

AI Engines

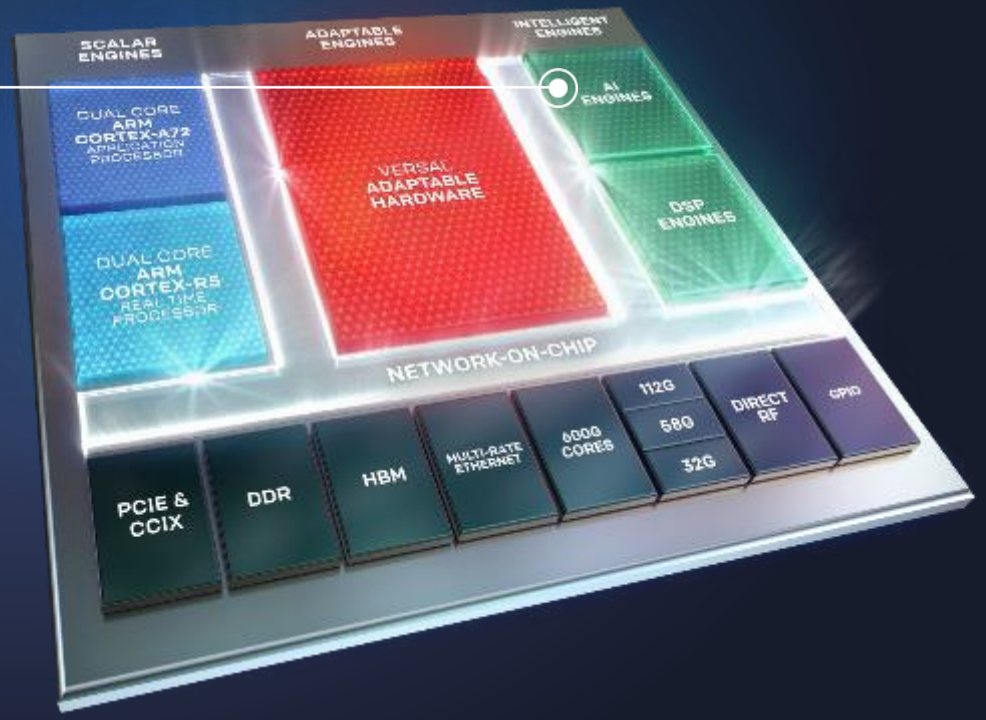
High throughput, low latency, and power efficient

Ideal for AI inference and advanced signal processing



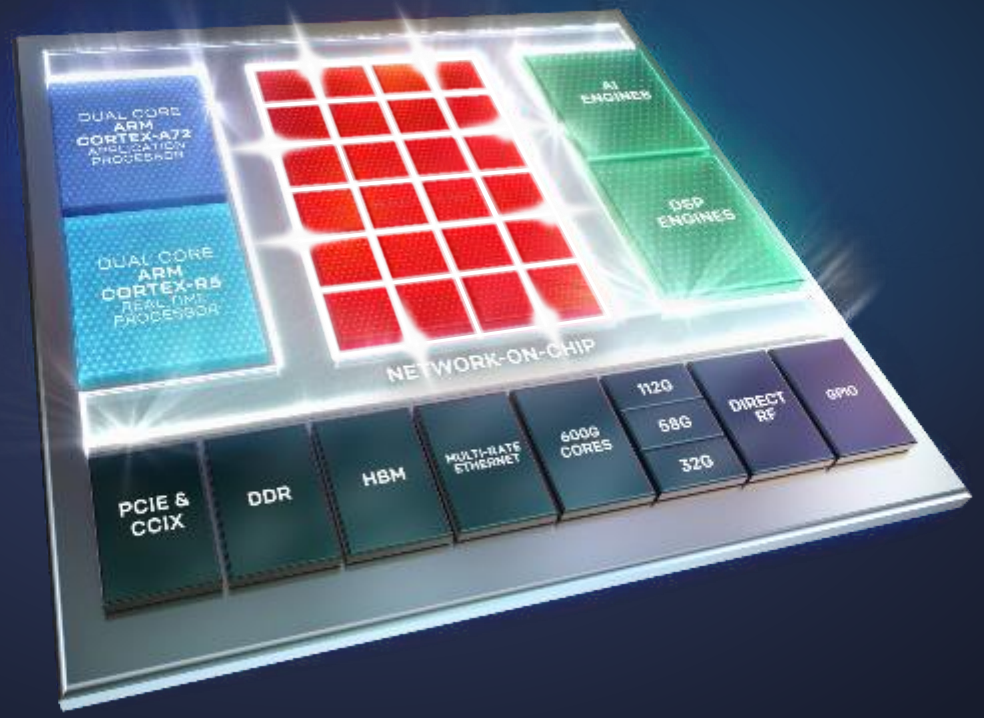


AI Engines



Optimized for AI Inference and Advanced Signal Processing Workloads

- >1GHz VLIW/SIMD vector processor cores
- Massive array of interconnected cores with local memory
- Tightly coupled to adaptable hardware enabling custom memory hierarchy
- Software programmable with hardware adaptability



Network-on-Chip (NoC)

Ease of Use

Inherently software programmable
Available at boot, no place-and-route required

High Bandwidth and Low Latency

Multi-terabit/sec throughput
Guaranteed QoS

Power Efficiency

8X power efficiency vs. soft implementations
Arbitration across heterogeneous engines

Comprehensive Tool Chain

TOOLS	USER	SUPPORTED ENTRY METHODS
Frameworks	Data Scientists & AI Developers	TensorFlow Caffe mxnet Spark FFMPEG
New Unified Software Development Environment	Application Developers	
Embedded Run-Time	Embedded Developers	Linux Xen FreeRTOS
Vivado Design Suite	Hardware Developers	

XILINX VERSAL

IN SUMMARY

Versal ACAP

Heterogeneous Acceleration

For Any Application

For Any Developer

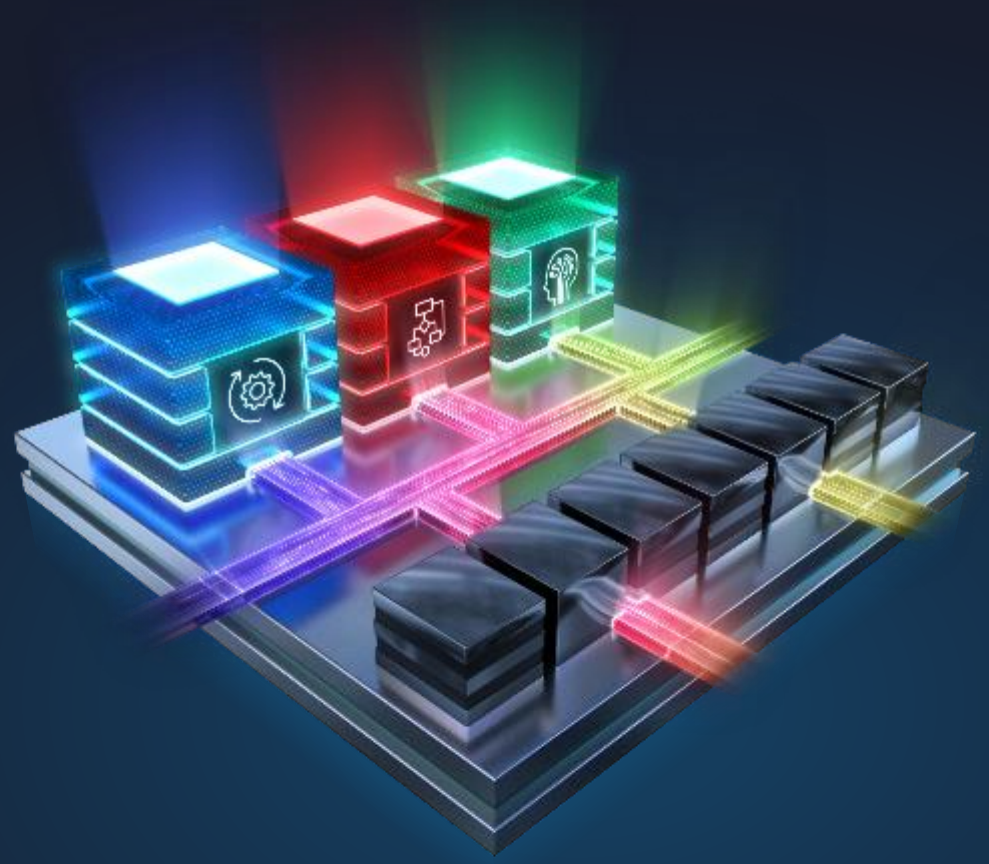
Delivers

Disruptive Innovation

Software Programmability

Hardware Adaptability

Whole Application Acceleration



Adaptable
Intelligent