ROAD: Routablility Analysis & Diagnosis Based on SAT Techniques

ISPD 2019

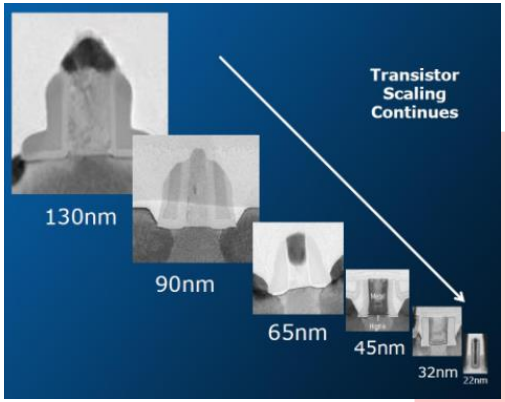
UCSD VLSI LAB

Dongwon Park, Ilgweon Kang, Yeseong Kim,

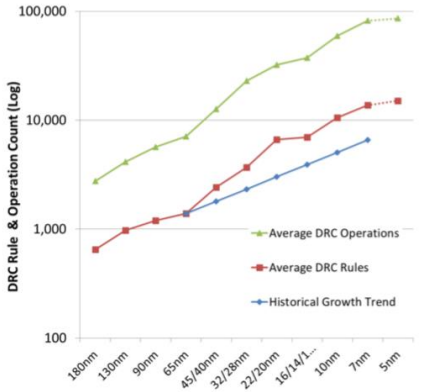
Sicun Gao, Bill Lin, Chung-Kuan Cheng

PHYSICAL DESIGN GETTING HARDER

- Keep Scaling Technologies



- Design Rule Complexity Rising



- **Tons of design rules from multi-patterning technology**
- **Limited Resource (# of Routing Track)**

Detailed Routing is getting complex and bottleneck.

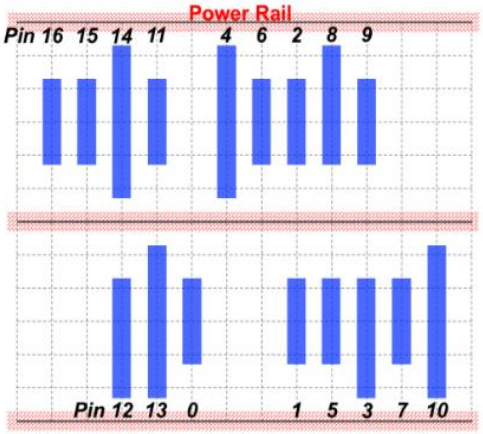
I. Routability Analysis

DESIGN RULE-CORRECT ROUTABILITY ANALYSIS

Gate Netlist

Placement

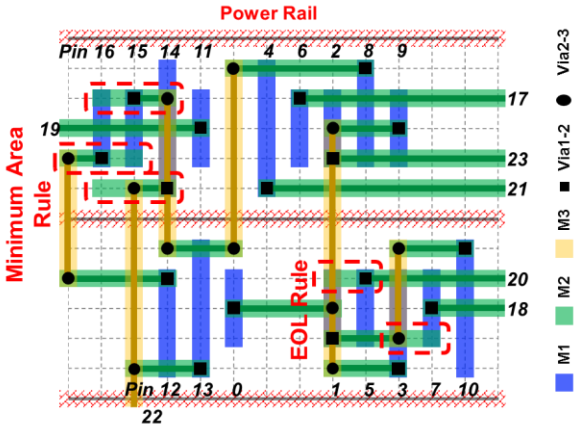
Given Pin-Layout



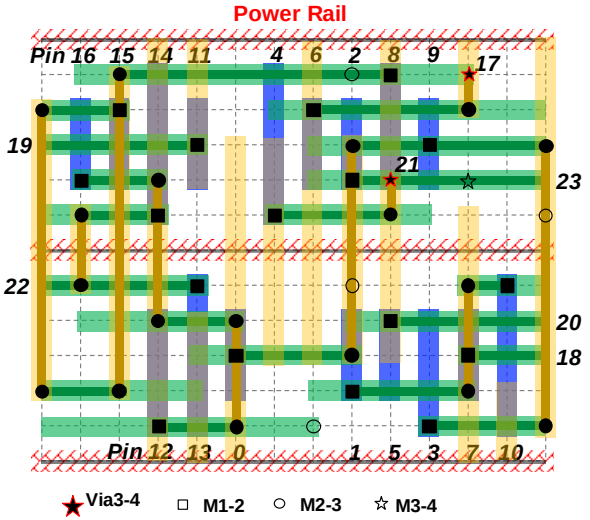
- #V_Tracks= 14, #H_Tracks= 13
- PinDensity= 70%
- **24 Pins**: 0-23
  The total # of pins
- **17 Inner Pins**: 0-16
  The total # of pins on M1
- **7 Outer Pins**: 17-23
  The total # of pins connected to the outside of the switching box
- **11 Nets**:
  Two 3-pin nets:
  {0 3 9}, {13 14 22}
  Nine 2-pin nets:
  {7 18}, {6 17}, {4 21},
  {11 19}, {1 10}, {8 15},
  {5 20}, {2 23}, {12 16}

Routable?

ILP: Optimal but 1048s (~18min) !



SAT : Not Optimized but 2s !!!!!

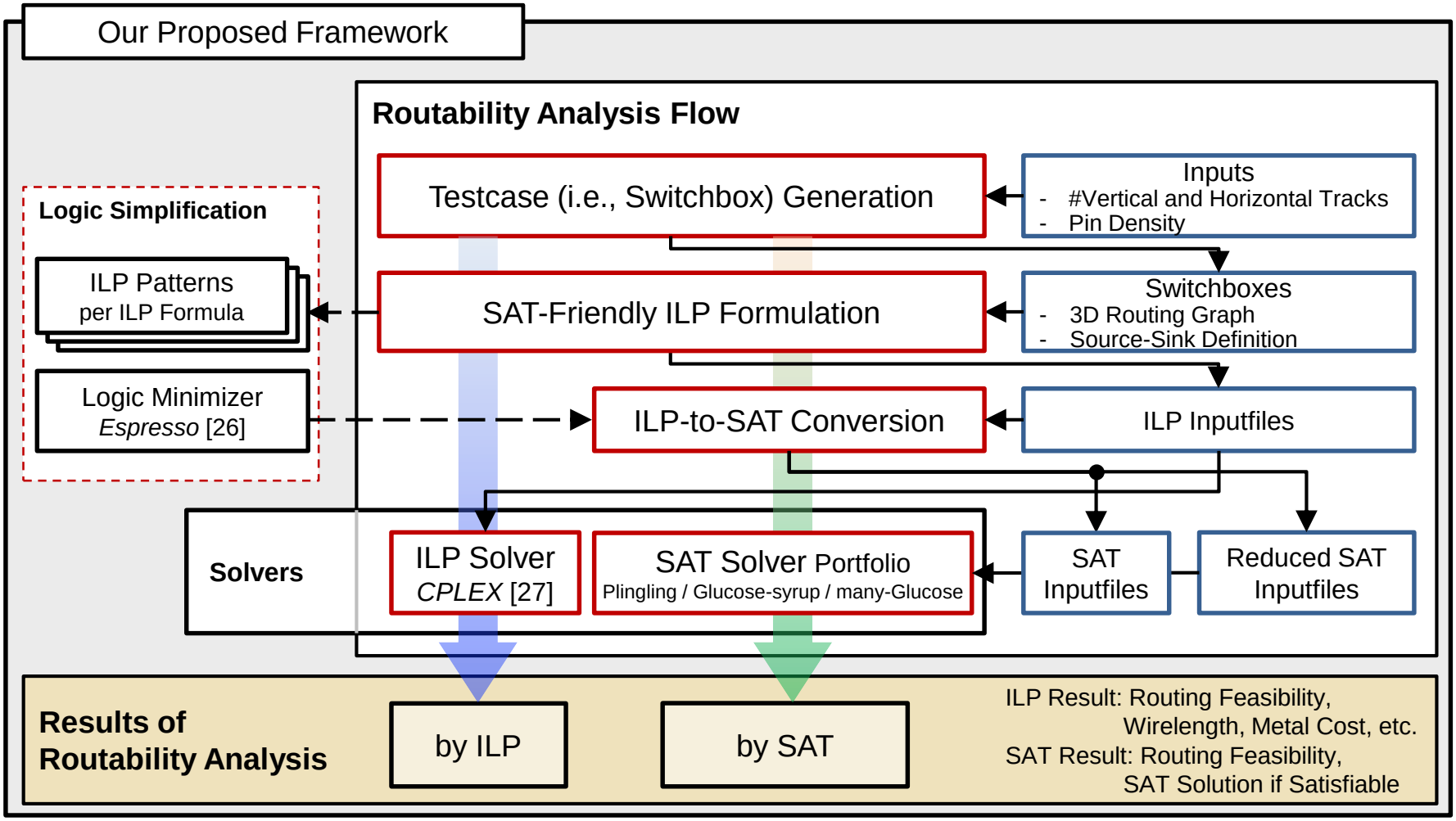


SAT Method → Quick "go/no-go" Decision

ROUTABILITY ANALYSIS FRAMEWORK

- ILP-based routability optimization
- SAT-based routability analysis

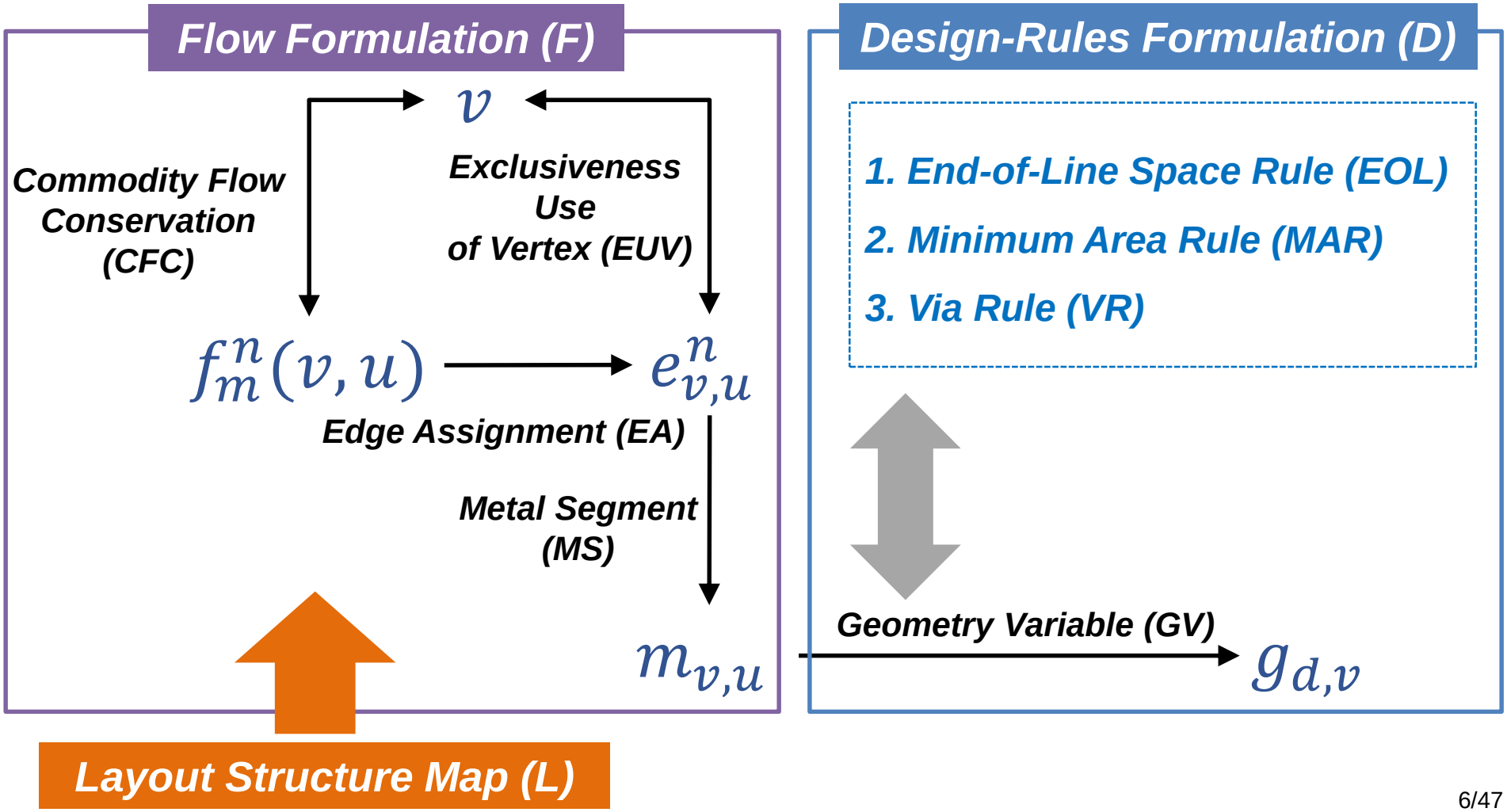
Fast and Precise
utability Analysis



[27] IBM ILOG CPLEX, http://www.ilog.com/products/cplex/.
[28] plingeling, Multi-Threading SAT Solver, http://fmv.jku.at/lingeling/.

PROPOSED ILP/SAT FORMULATION DIAGRAM

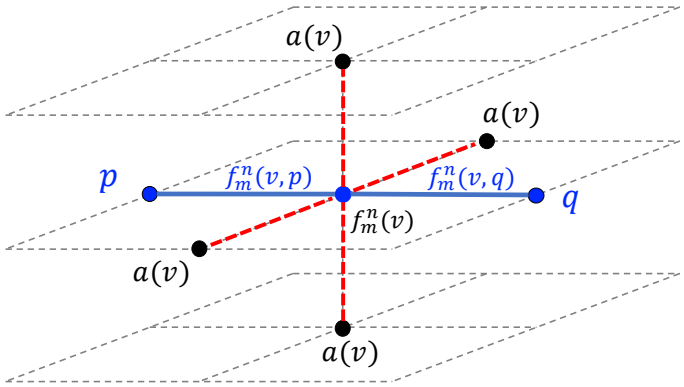
- The Multi-commodity network flow formulation (F)
- Conditional Design Rule (D)
- Layout Structure Map (L)



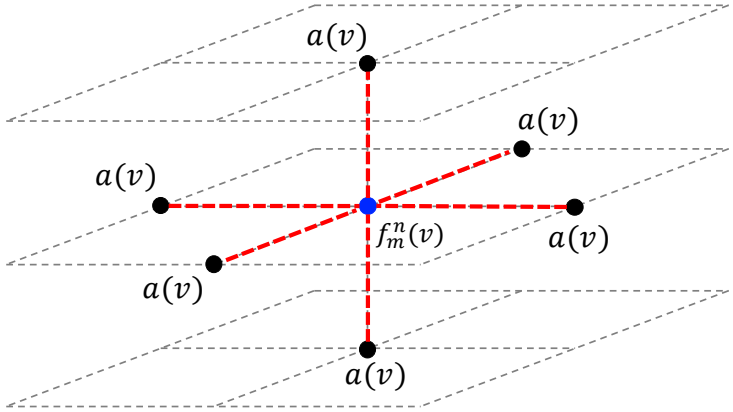
SAT Formulation – Flow Formulation (F)

- **Commodity Flow Conservation (CFC)**
  - CASE I) Vertex ≠ source, sink : **0 or 2 edges uses**

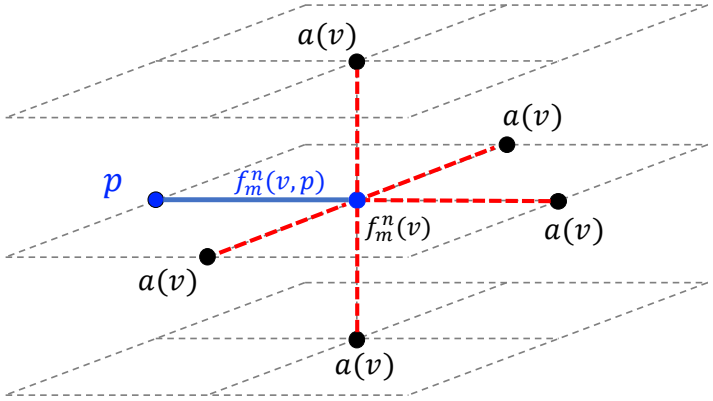
1) Only one incoming/outgoing pair is allowable for all commodities.



2) This commodity don't use this vertex.



  - CASE II) Vertex = source, sink : **Exactly-One (EO) Commodity Flow Constraint.**

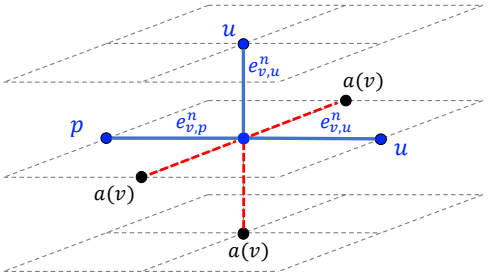


$$\mathbf{F}_{CFC_2}(v,n,m) = \mathbf{EO}\left(\left\{ f_m^n(v,p) \;\middle|\; p \in a(v) \right\}\right),$$
$$\forall v \in V,\ \forall n \in N,\ \forall t_m^n \in T^n$$

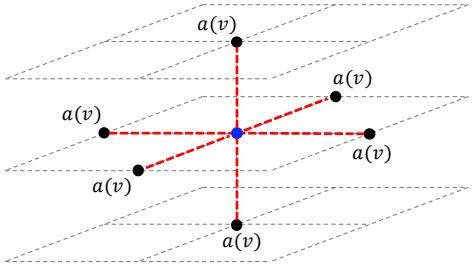
SAT Formulation – Flow Formulation (F)

- **Exclusiveness Use of Vertex (EUV)**
  - CASE I. Vertex ≠ source, sink : **At-Most-One (AMO) Net Constraint**

1) Only one net can use a certain edge

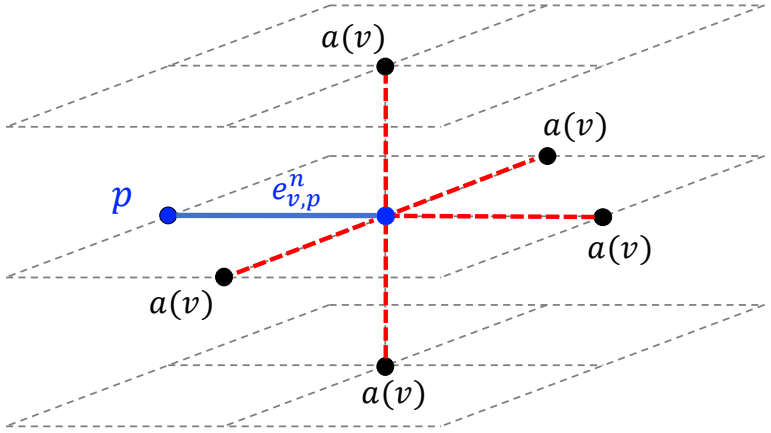


2) No Flow



$$\mathbf{F}_{EUV_1}(v) = \mathbf{AMO}\left(\left\{ \bigvee_{p \in a(v)} e^n_{v,p} \;\middle|\; n \in N \right\}\right), \qquad \forall v \in V$$

  - CASE II. Vertex = source, sink : **Exactly-One (EO) Edge Constraint**



$$\mathbf{F}_{EUV_2}(v) = \mathbf{EO}\left(\left\{ e^n_{v,p} \;\middle|\; p \in a(v),\ n \in N \right\}\right), \qquad \forall v \in V$$

SAT Formulation – Flow Formulation (F)

- **Edge Assignment (EA)**

$$f_m^n(v,u) \rightarrow e_{v,u}^n \qquad \mathbf{F}_{EA}(e_{v,u},n,m) = e_{v,u}^n \vee \neg f_m^n(v,u), \qquad \forall e_{v,u} \in E,\ \forall n \in N,\ \forall t_m^n \in T^n$$

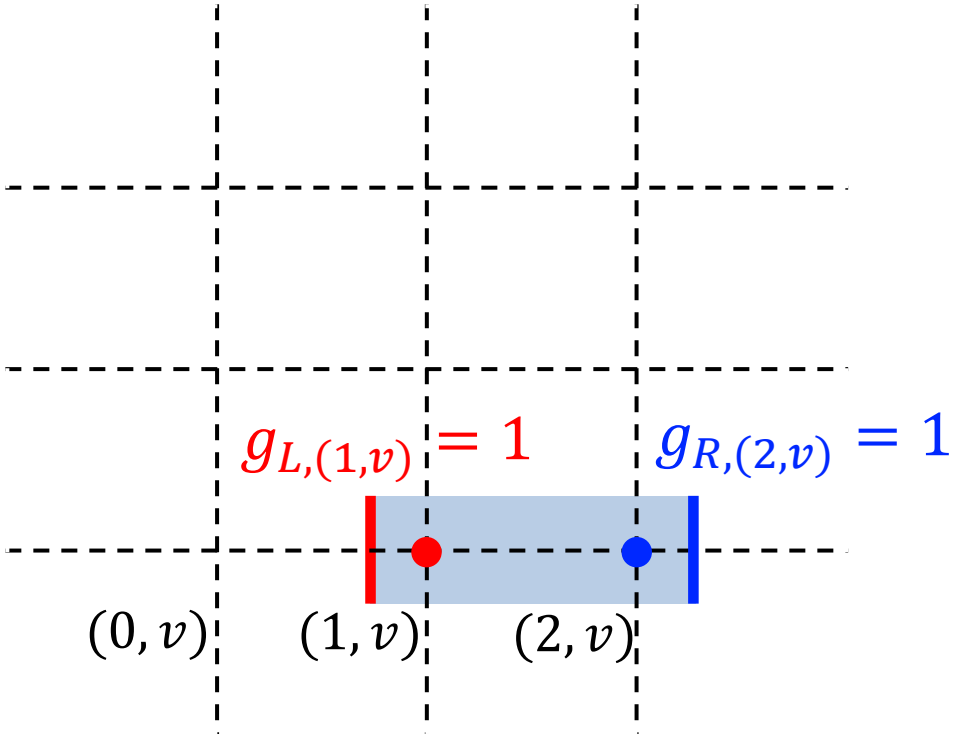
Logical Imply. : edge is used by n net if m commodity of n net use this edge
→ It requires for multi-commodity flow

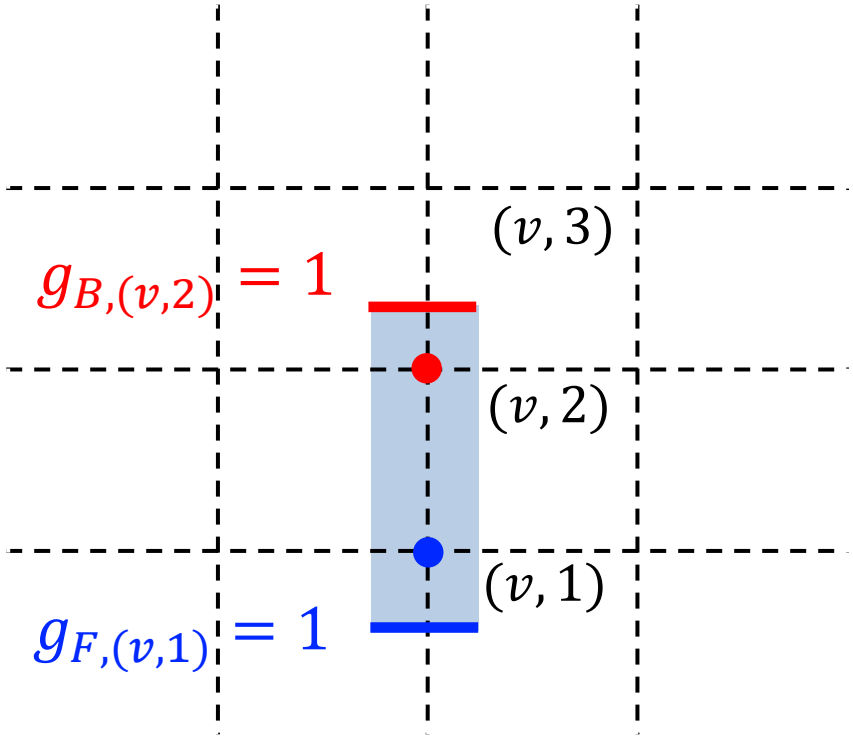
- **Metal Segment (and Exclusiveness Use of Edge) (MS)**
  - **Commander Encoding Variable of EO constraint of edge indicators**

$$\mathbf{F}_{MS}(e_{v,u}) = \mathbf{EO}\left(\left\{\neg m_{v,u}\right\} \cup \left\{ e_{v,u}^n \;\middle|\; n \in N \right\}\right), \qquad \forall e_{v,u} \in E$$

SAT Formulation – Design Rule Formulation (D)

- **Geometric Variable (GV)**
  - End-of-Line indicator of each vertex for geometric conditional design rule.



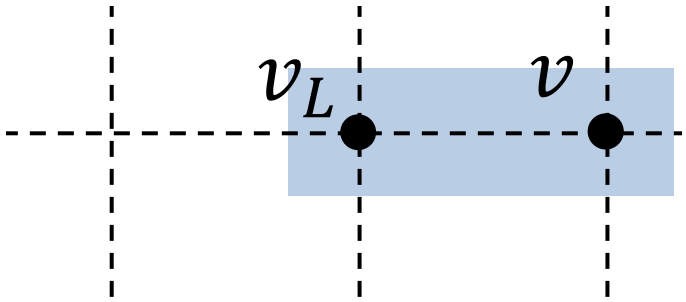


SAT Formulation – Design Rule Formulation (D)

- **Minimum Area Rule (MAR)**
  - A metal segment must cover at least three vertices (AMO Constraint)

$$\mathbf{D}_{MAR_{LR}}(v) = \mathbf{AMO}\left(g_{L,v}, g_{R,v}, g_{L,v_R}, g_{R,v_R}\right), \qquad \forall v \in V_2$$

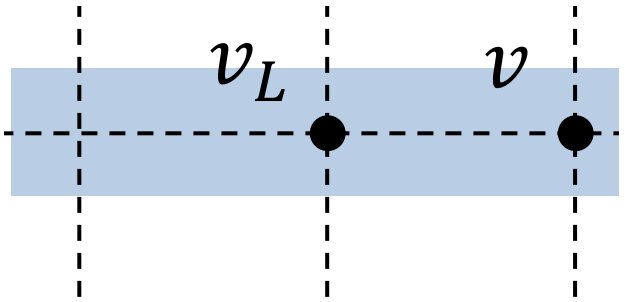
Violation



$g_{R,v} = g_{L,v_L} = 1$

$g_{L,v} = g_{R,v_R} = 0$

No Violation



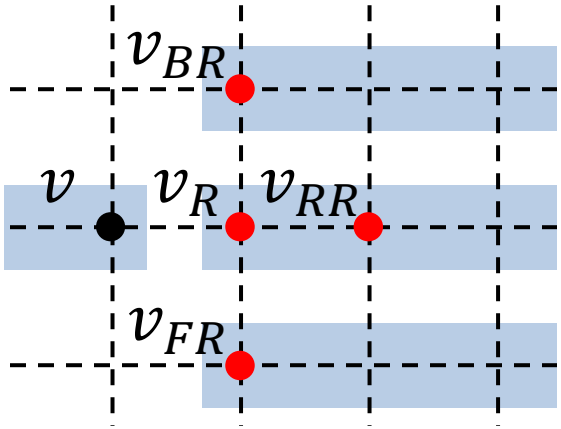
$g_{R,v} = 1$

$g_{L,v} = g_{L,v_L} = g_{R,v_L} = 0$

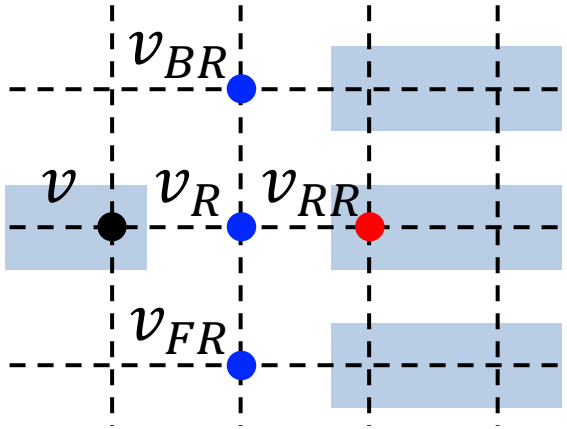
SAT Formulation – Design Rule Formulation (D)

- **End-of-Line (EOL) Space Rule**
  - The minimum distance between tips must be larger than 2 Manhattan distance (AMO Constraint)

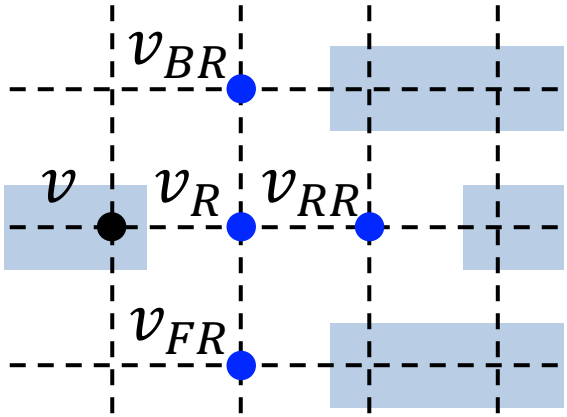
$$\mathbf{D}_{EOL_R}(v) = \mathbf{AMO}(g_{R,v}, g_{L,v_{FR}}) \wedge \mathbf{AMO}(g_{R,v}, g_{L,v_{BR}}) \wedge \mathbf{AMO}(g_{R,v}, g_{L,v_R}, g_{L,v_{RR}}), \quad \forall v \in V_2$$



Violation



Violation

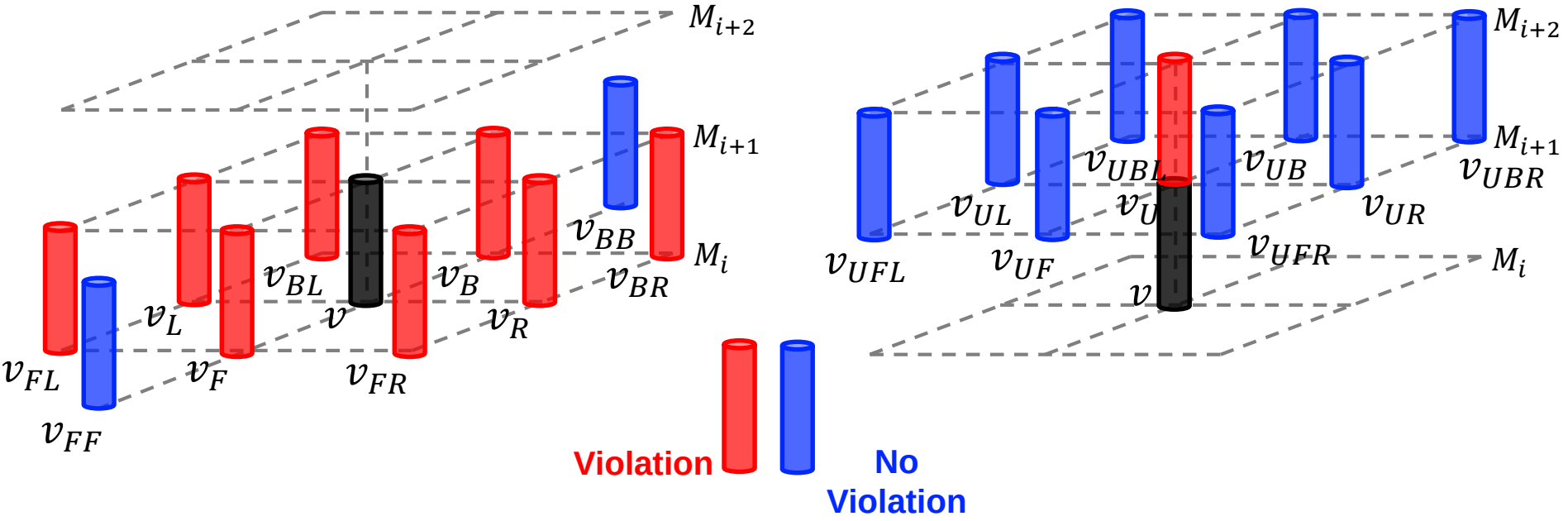


No Violation

SAT Formulation – Design Rule Formulation (D)

- **Via Rule (VR)**
  - The distance between two vias should be larger sqrt(2) Euclidean Distance (AMO constraint)

$$\mathbf{D}_{VR}(v) = \mathbf{AMO}\left(m_{v,v_U}, m_{v_R,v_{UR}}, m_{v_B,v_{UB}}, m_{v_{BR},v_{UBR}}\right) \wedge \mathbf{AMO}\left(m_{v_D,v}, m_{v,v_U}\right) \quad \forall v \in V$$



DESIGN RULE-CORRECT ROUTABILITY ANALYSIS

- **Flow Feasibility (F)**
  - **Conjunction of each subsets**

$$\mathbf{F} = \bigwedge_{v \in V} \left(\mathbf{F}_{EUV}(v) \wedge \bigwedge_{n \in N} \bigwedge_{t_m^n \in T^n} \mathbf{F}_{CFC}(v,n,m) \right) \wedge \bigwedge_{e_{v,u} \in E} \left(\mathbf{F}_{MS}(e_{v,u}) \wedge \bigwedge_{n \in N} \bigwedge_{t_m^n \in T^n} \mathbf{F}_{EA}(e_{v,u},n,m) \right)$$

- **Design Rule Formulation (D)**

$$\mathbf{D} = \mathbf{D}_{GV} \wedge \mathbf{D}_{MAR} \wedge \mathbf{D}_{EOL} \wedge \bigwedge_{v \in V} \mathbf{D}_{VR}(v)$$

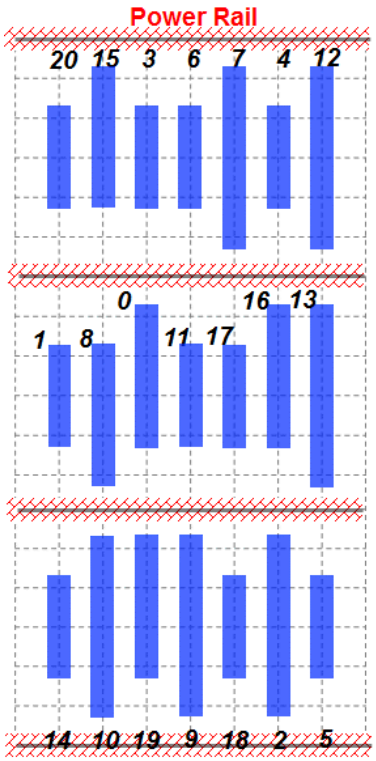
- **Design Rule-correct Routability (R)**
  - L : Layout Structure Map → the geometry information of the switch box

$$\mathbf{R} = \mathbf{F} \wedge \mathbf{D} \wedge \mathbf{L}$$

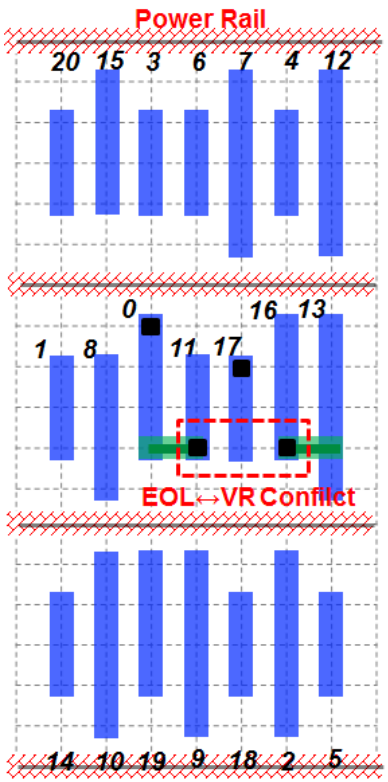
II. Routability Diagnosis

NEXT STEP : ROUTABILITY DIAGNOSIS

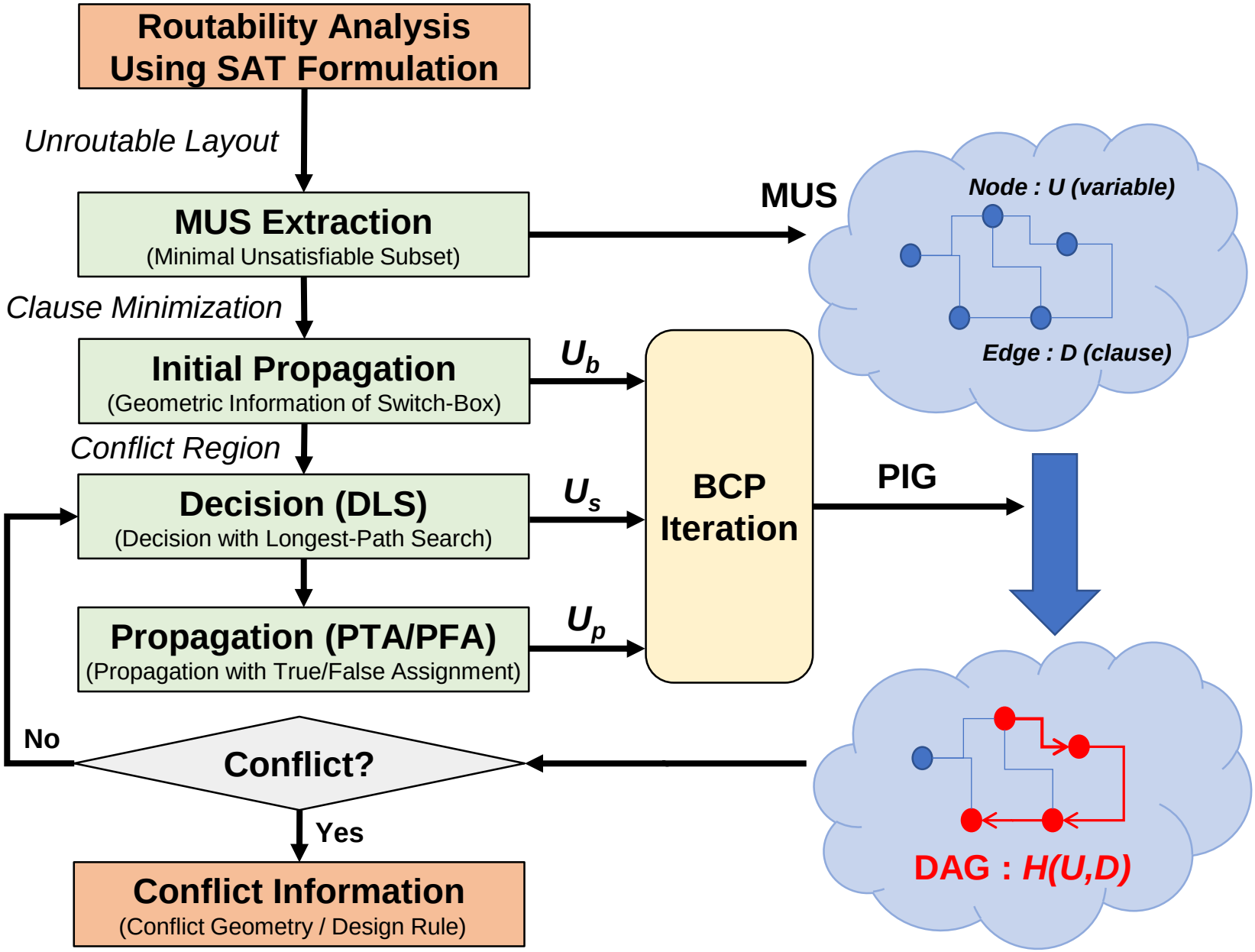
- **Conflict Diagnosis in Unroutable Case using SAT Technique**
  - Exact Location of Conflict → Fast Trouble-shooting for Designer
  - Exact Conflict Relation → Guideline for Design Rule Manager



- **#V_Tracks= 9, #H_Tracks= 19**
- **PinDensity= 100%**
- **21 Pins**: 0-20
- **8 Outer Pins**: 21-28
- **13 Nets**: {9 13 17}, {7 12 25}, {0 6 28}, {14 23}, {16 19}, {3 24}, {2 22}, {4 27}, {8 18}, {11 21}, {15 20}, {5 10}, {1 26}
- Results: **Unroutable**



ROAD : OVERVIEW OF DIAGNOSIS



(1) Minimal Unsatisfiable Subset (MUS)

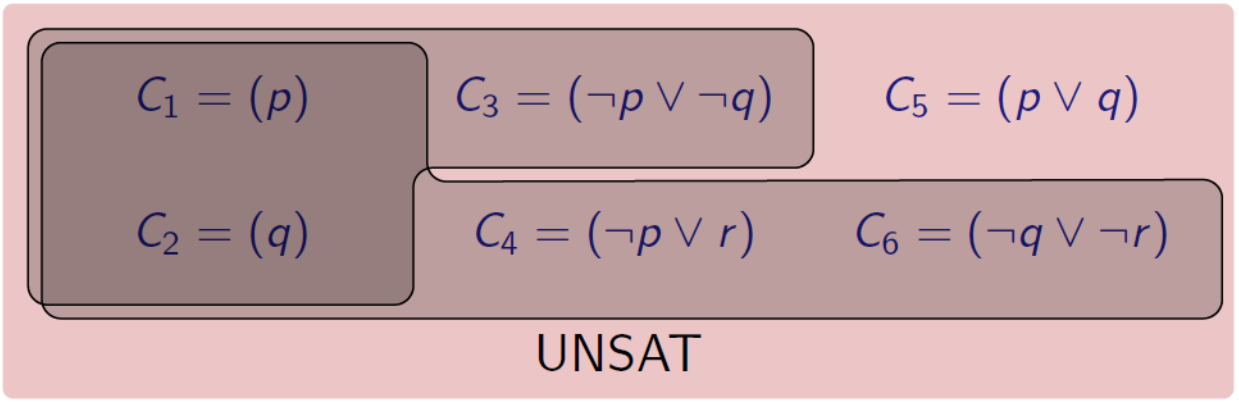
Claim: For every $\mathcal{F} \in$ UNSAT, $\exists \mathcal{M} \subseteq \mathcal{F}$, such that $\mathcal{M} \in$ MU.

Pf:

1. Let $\mathcal{M} = \mathcal{F}$.
2. If $\mathcal{M} \notin$ MU, $\exists C \in \mathcal{M}$ such that $\mathcal{M} \setminus \{C\} \in$ UNSAT.
3. Let $\mathcal{M} = \mathcal{M} \setminus \{C\}$, goto 2.

Def: $\mathcal{M}$ is *minimally unsatisfiable subformula (MUS)* of $\mathcal{F}$ if $\mathcal{M} \subseteq \mathcal{F}$ and $\mathcal{M} \in$ MU.

Notation: MUS($\mathcal{F}$) — the set of all MUSes of $\mathcal{F}$.



$\{C_1, C_2, C_3\}$ and $\{C_1, C_2, C_4, C_6\}$ are the (only) MUSes.

(2) BCP (Boolean Constraint Propagation) & PIG

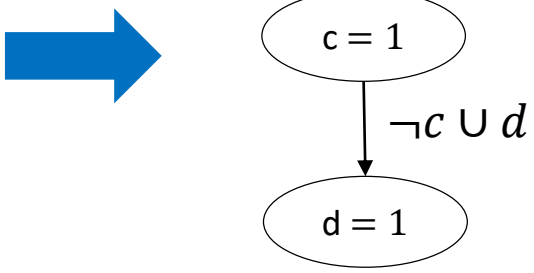
- **PIG (Partial Implication Graph) in Our Framework**
  - Directed Acyclic Graph which Nodes are Variables, Edges are Clauses.
  - The implication relation between variable assignment from constraint clause

PIG of the propagation

Clause set: $\{ a \cup b , \neg a \cup c, \neg c \cup d, a \}$

$1st\ BCP, \quad a = 1 \rightarrow \{c, \neg c \cup d\}\ remain$

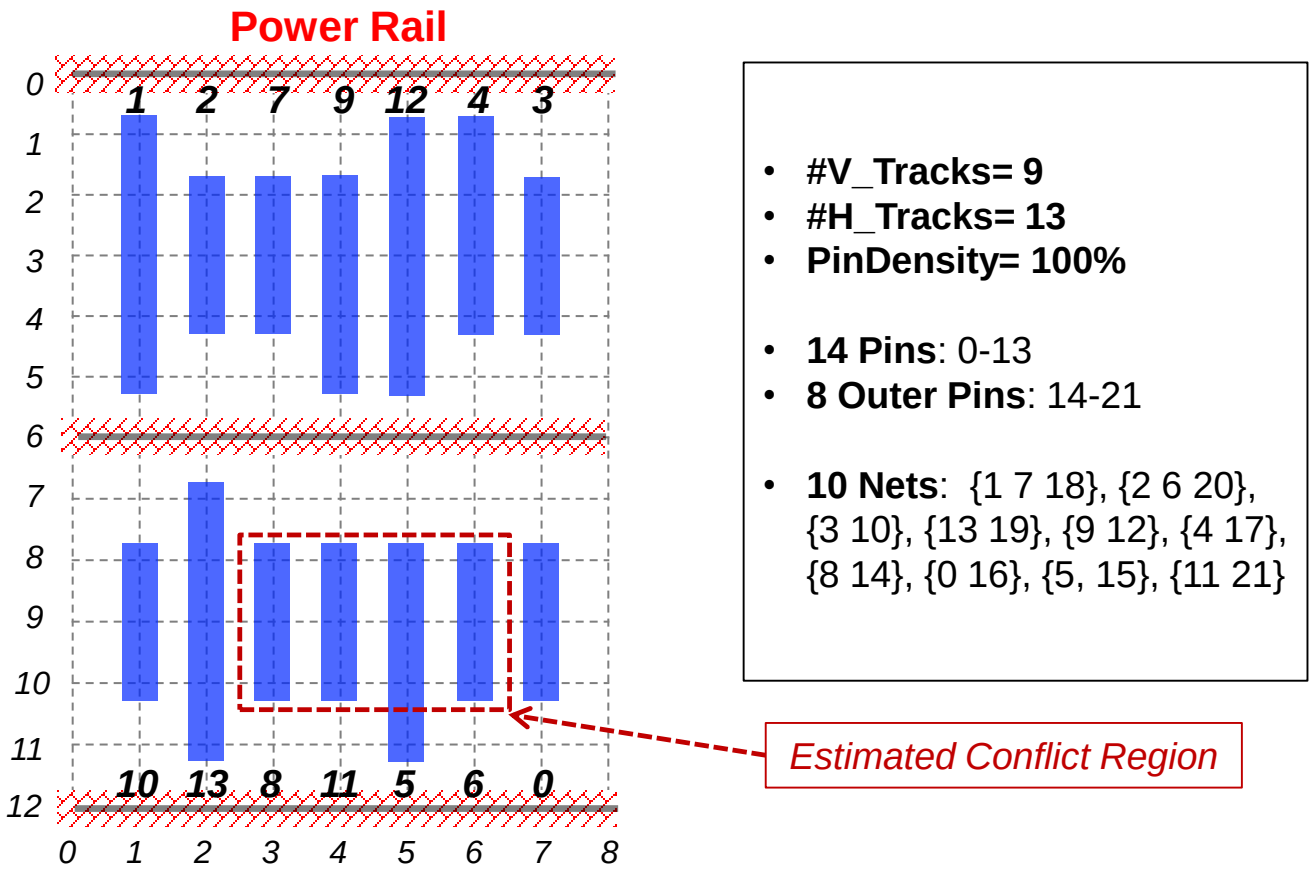
$2nd\ BCP, c = 1 \ \rightarrow \ \{d\}\ remain$



https://en.wikipedia.org/wiki/Unit_propagation

(3) INITIAL PROPAGATION

- **Layout Structure Map (L) → Estimated Conflict Range**



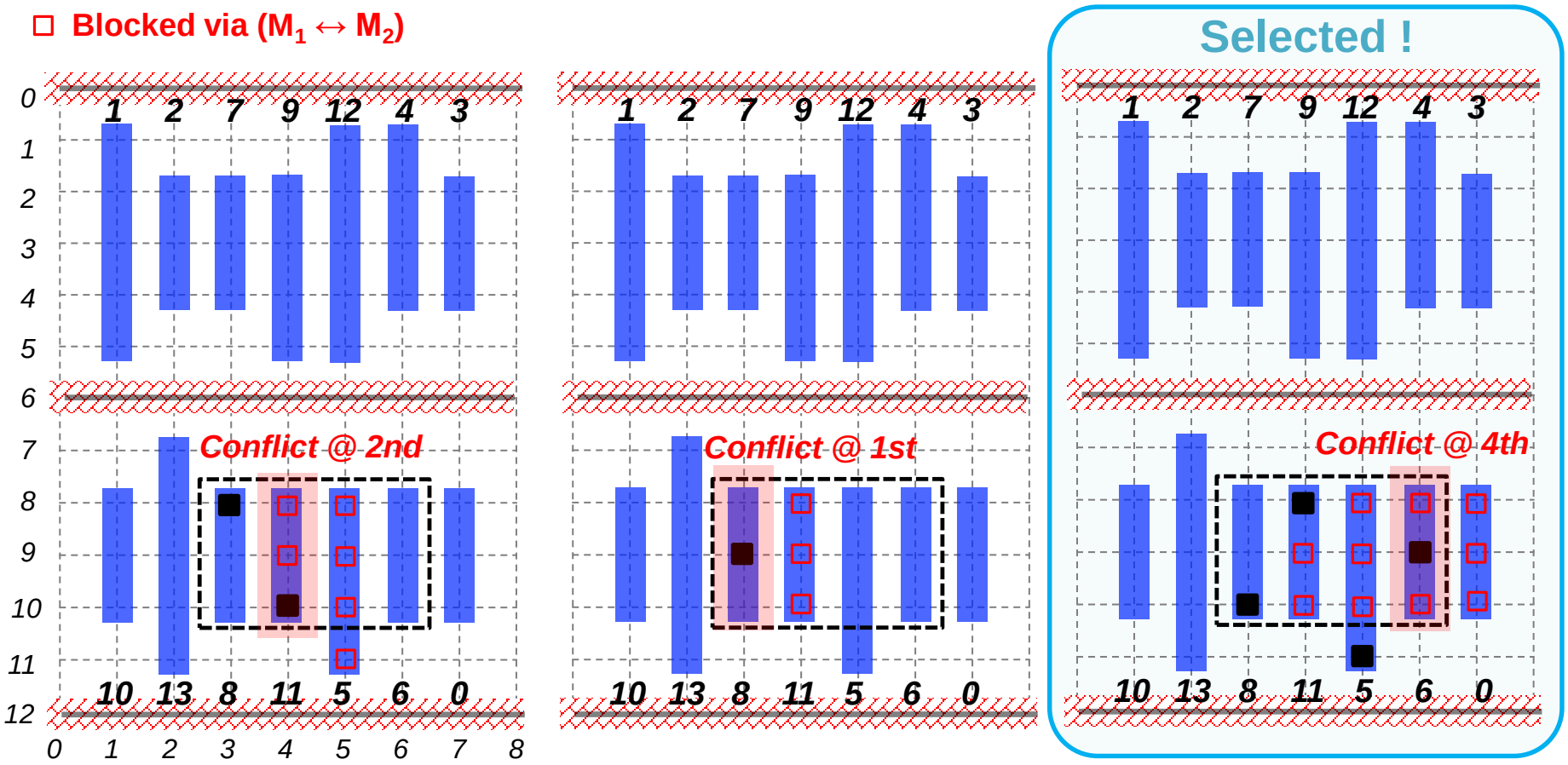
- **#V_Tracks= 9**
- **#H_Tracks= 13**
- **PinDensity= 100%**

- **14 Pins**: 0-13
- **8 Outer Pins**: 14-21

- **10 Nets**: {1 7 18}, {2 6 20}, {3 10}, {13 19}, {9 12}, {4 17}, {8 14}, {0 16}, {5, 15}, {11 21}

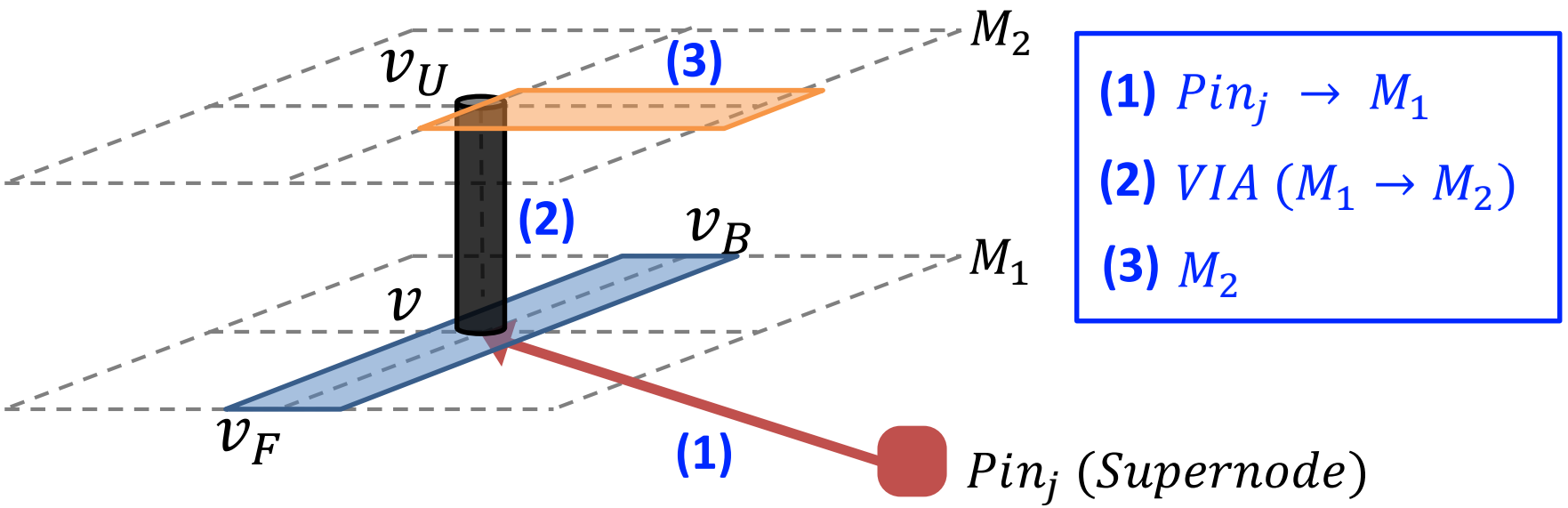
(4) DLS (Decision with Longest-path Search)

- **Longest-path search is most comprehensive explanation about failure**
  - Via Position / Direction of Element are determined at DLS phase



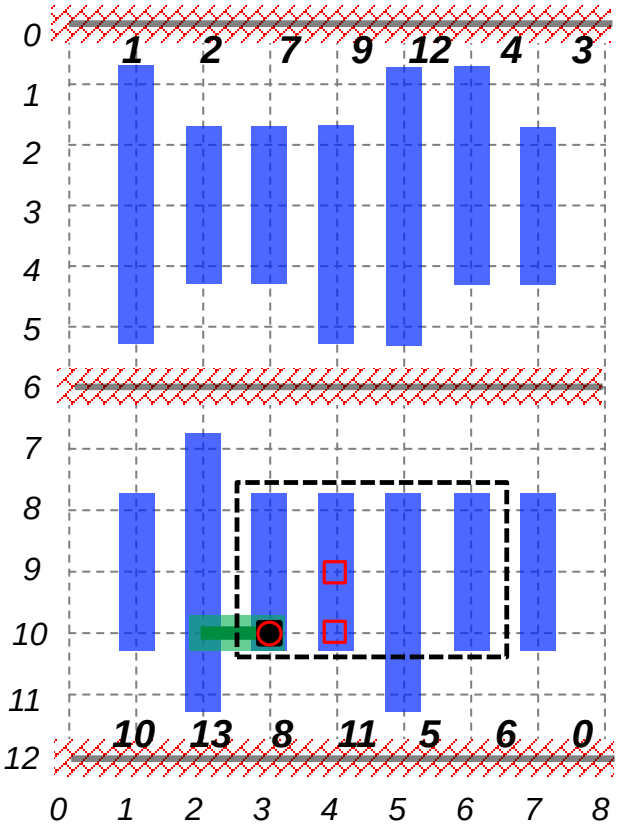
(5) PROPAGATION – PTA (WITH TRUE ASSIGNMENT)

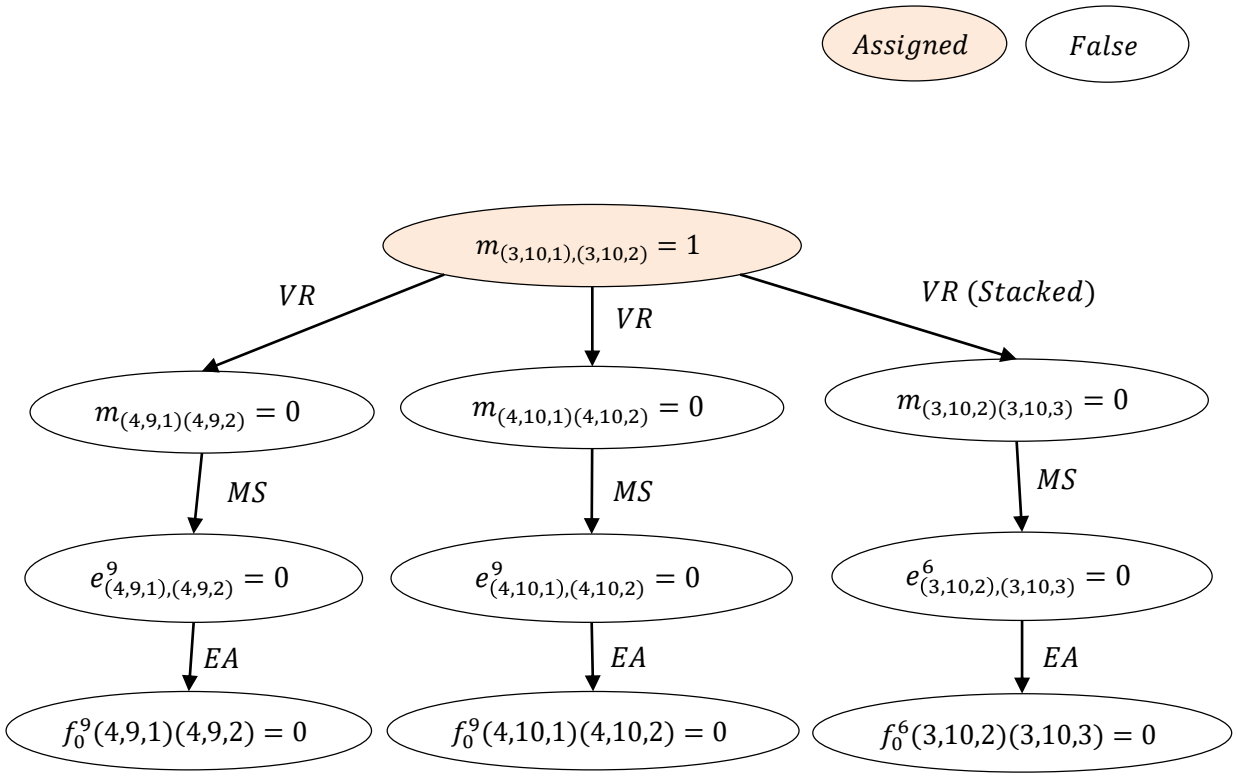
- **BCP propagation with True Assignment (U_s)**



(5) PROPAGATION – PTA (WITH TRUE ASSIGNMENT)

- **PTA Result of #1 VIA @ 9_13_100**

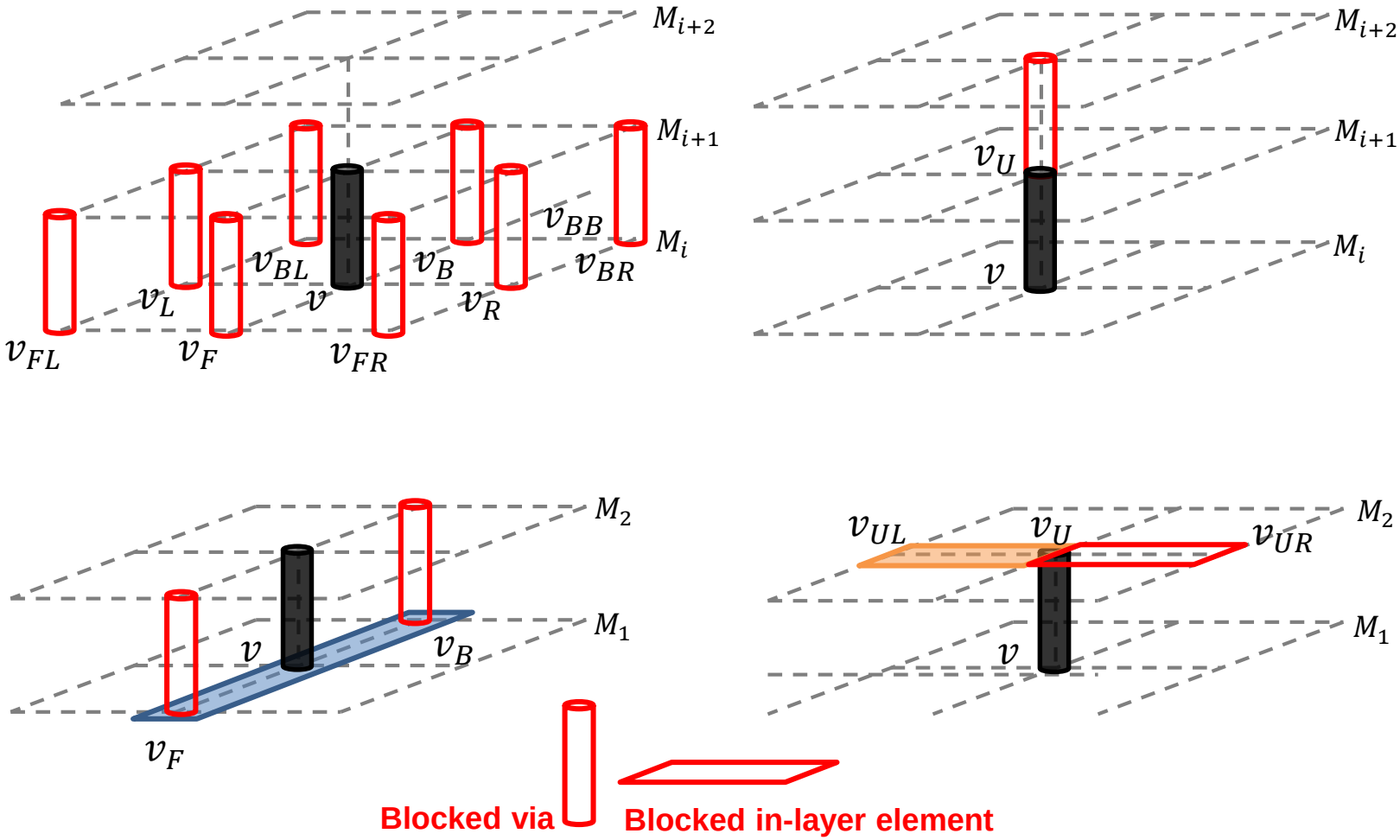




- □ **Blocked via ($M_1 \leftrightarrow M_2$)**
- ○ **Blocked via ($M_2 \leftrightarrow M_3$)**
- ■ **Assigned via ($M_1 \leftrightarrow M_2$)**

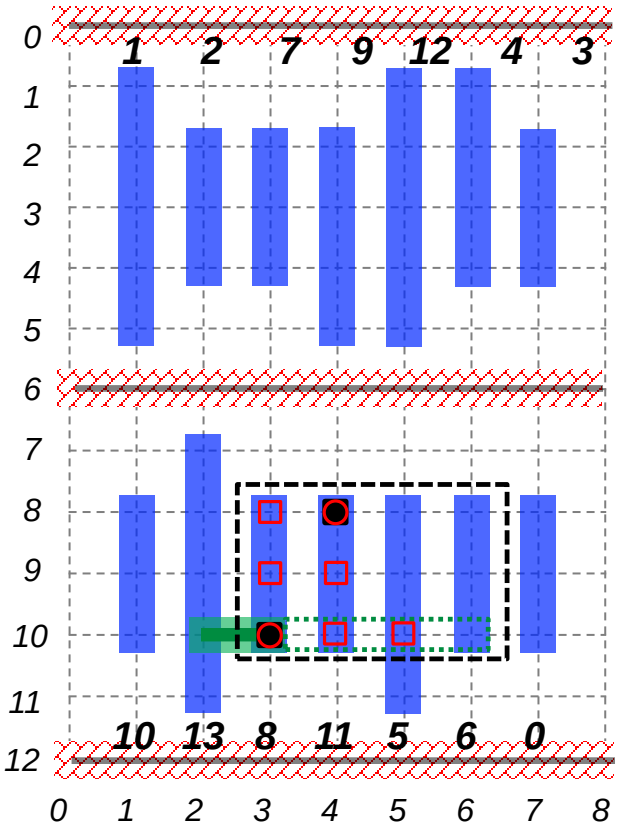
(5) PROPAGATION – PFA (WITH FALSE ASSIGNMENT)

- **BCP propagation with False Assignment (U_s)**
  - Via-to-via spacing / Stacked – Via / Vias in same pin / element with direction against PTA



(5) PROPAGATION – PFA (WITH FALSE ASSIGNMENT)

- **PFA Result of #1 VIA @ 9_13_100**

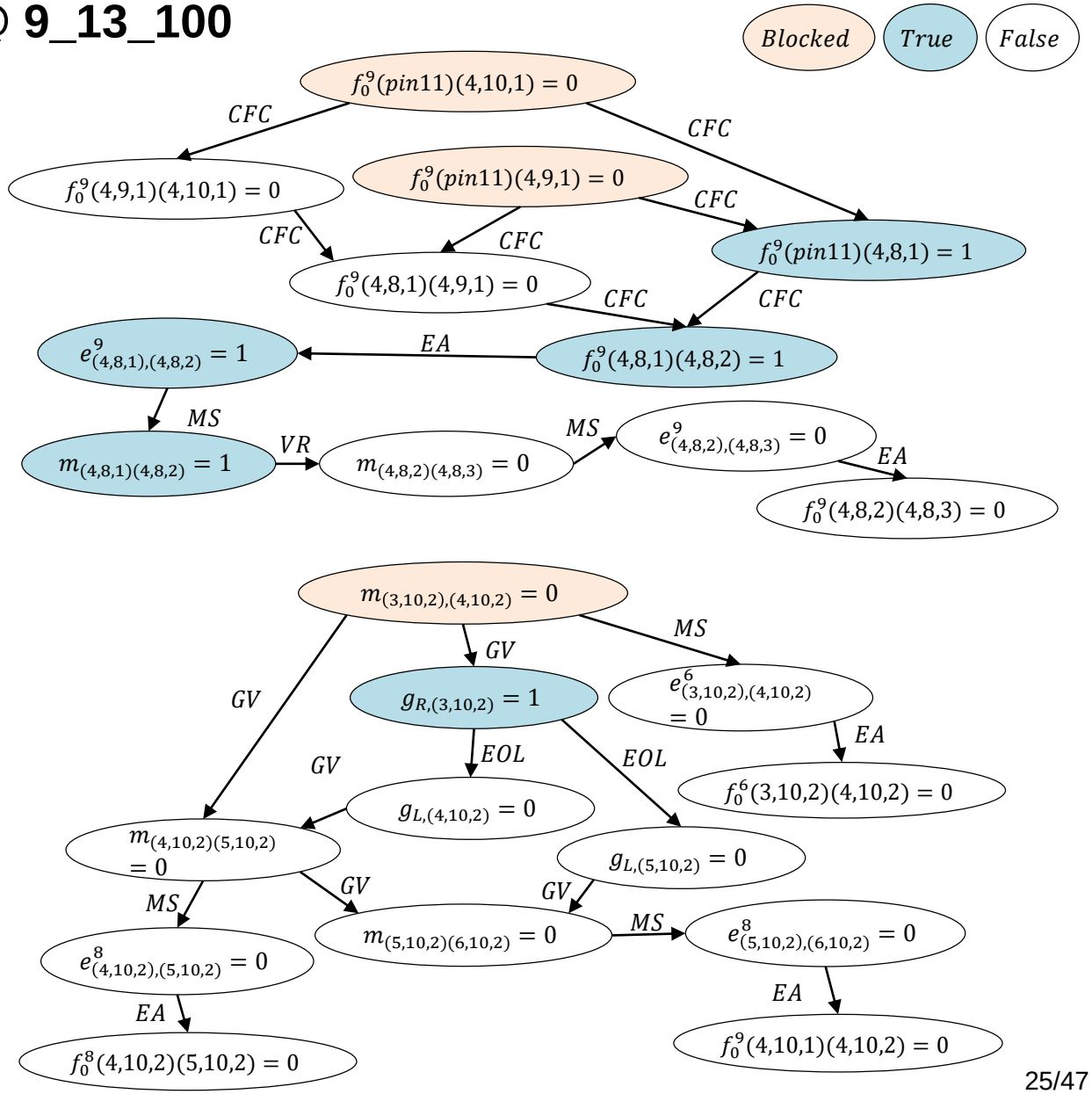


□ **Blocked via ($M_1 \leftrightarrow M_2$)**

○ **Blocked via ($M_2 \leftrightarrow M_3$)**

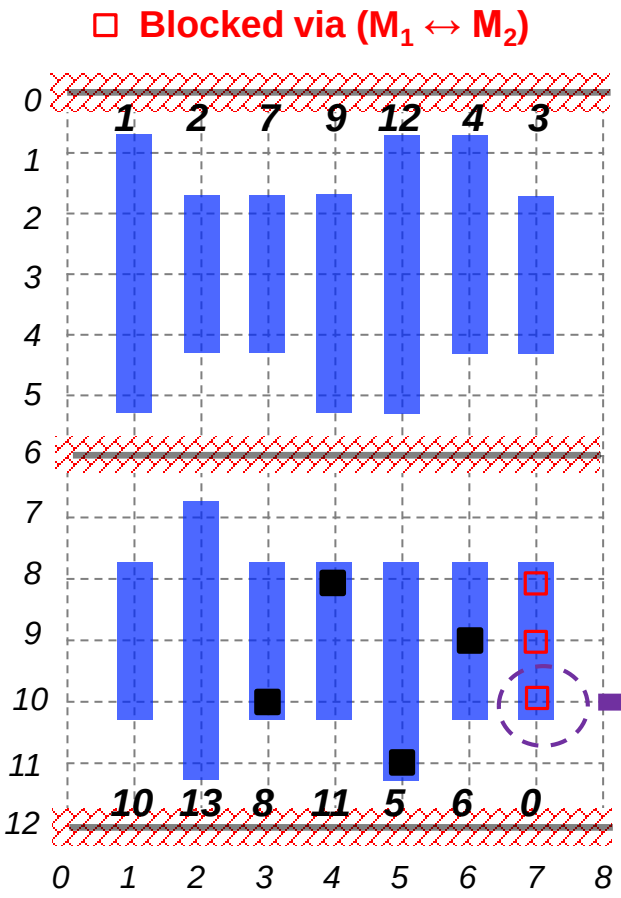
■ **Assigned via ($M_1 \leftrightarrow M_2$)**

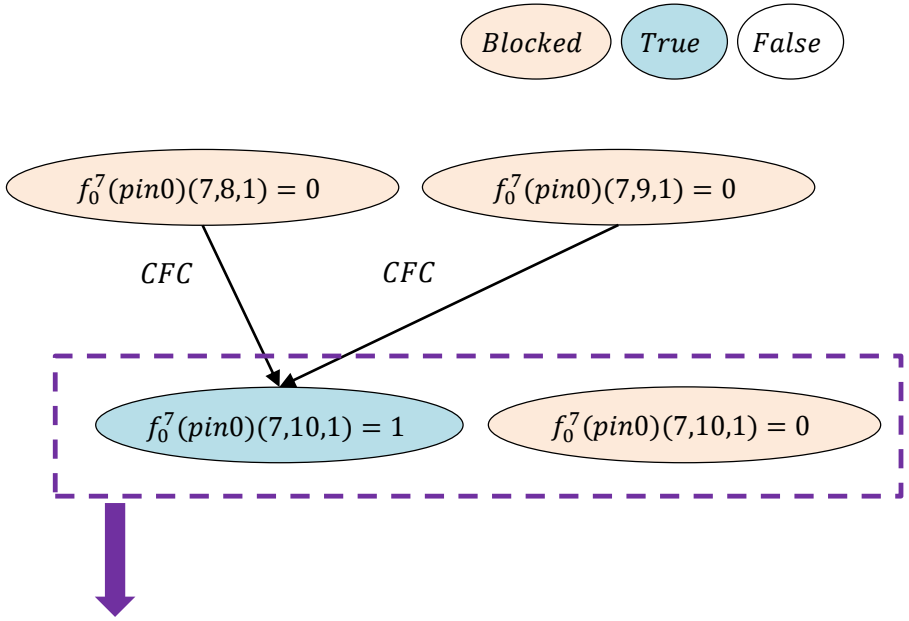
⬚ **Blocked in-layer element**



(6) DIAGNOSIS RESULT REPORT : EX) 9_13_100

- **4th via @ PFA phase → Conflict encounter !**





CONFLICT Information

- *Geometry : (Pin0) ↔ (7,10,1)*
- *Design Rule : CFC ↔ VR Rule*

III. ROAD Experimental Result

ROUTABILITY DIAGNOSIS – ROOT CAUSES

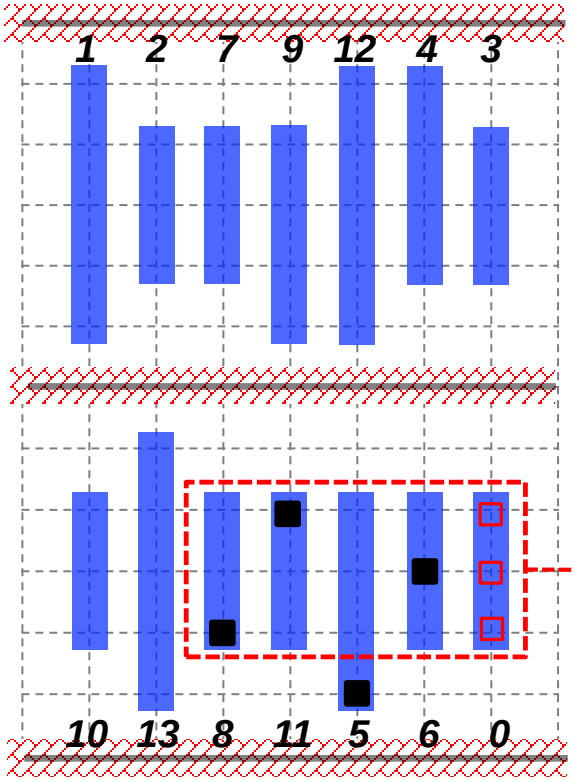
- **The Root causes of routing failure**
  - **Conflict Pin-shape (CP) : Pin-Accessibility Problem!**
    - Simple-CP : Intrinsic Pattern in given Pin-layout
    - Propagated-CP : Simple-CP appears after some propagations
  - **Routing Congestion**
    - The lack of routing resources such as #Track and #Layer

Table 2: Unroutable layout examples. #N=#Nets, #P=#Pins.

SwitchBox	Spec.		SAT Formulation		MUS	Conflict Cause
	#N	#P	#Variable	#Clauses	#Clauses	
11_7_80	6	12	16,776	378,551	215	Simple-CP
9_19_100	13	29	101,943	5,368,125	234	
9_13_100	10	22	54,884	2,280,223	272	
12_13_70	10	23	79,471	3,478,371	446	Propagated-CP
11_7_90	7	14	21,014	580,925	514	
7_7_100	4	9	7,972	110,389	1,194	Routing Congestion
7_13_100	7	15	24,236	595,898	4,060	
15_7_90	9	20	45,782	1,725,676	6,579	
19_13_70	15	33	171,092	11,287,222	19,375	

UNROUTABLE LAYOUT CLASSIFICATION – SIMPLE-CP

- Simple-CP with 3-3-n-3-3 pattern



- **#V_Tracks= 9 , #H_Tracks= 13**
- **PinDensity= 100%**

- **14 Pins**: 0-13
- **8 Outer Pins**: 14-21

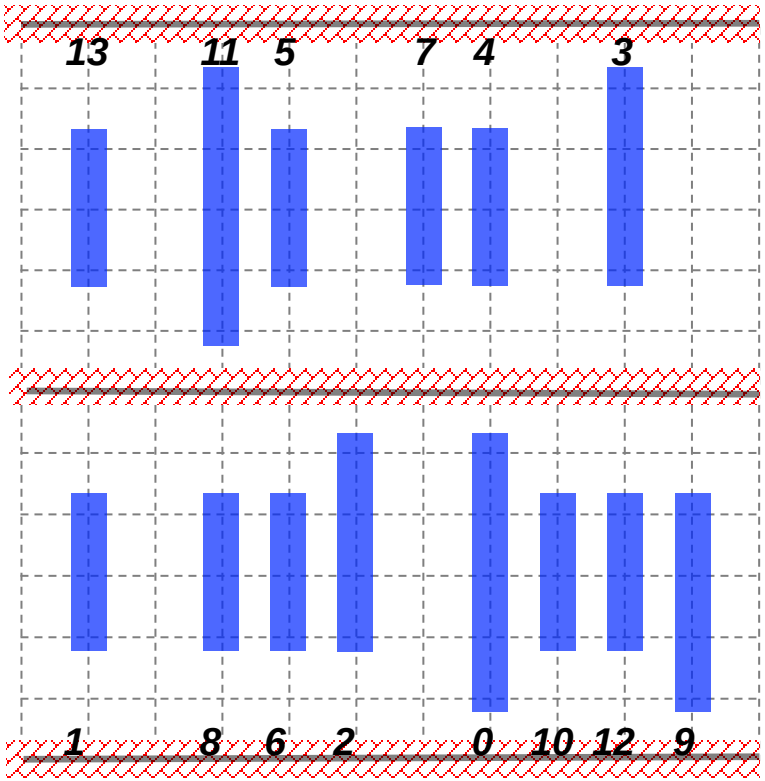
- **10 Nets**: {1 7 18}, {2 6 20}, {3 10}, {13 19}, {9 12}, {4 17}, {8 14}, {0 16}, {5, 15}, {11 21}

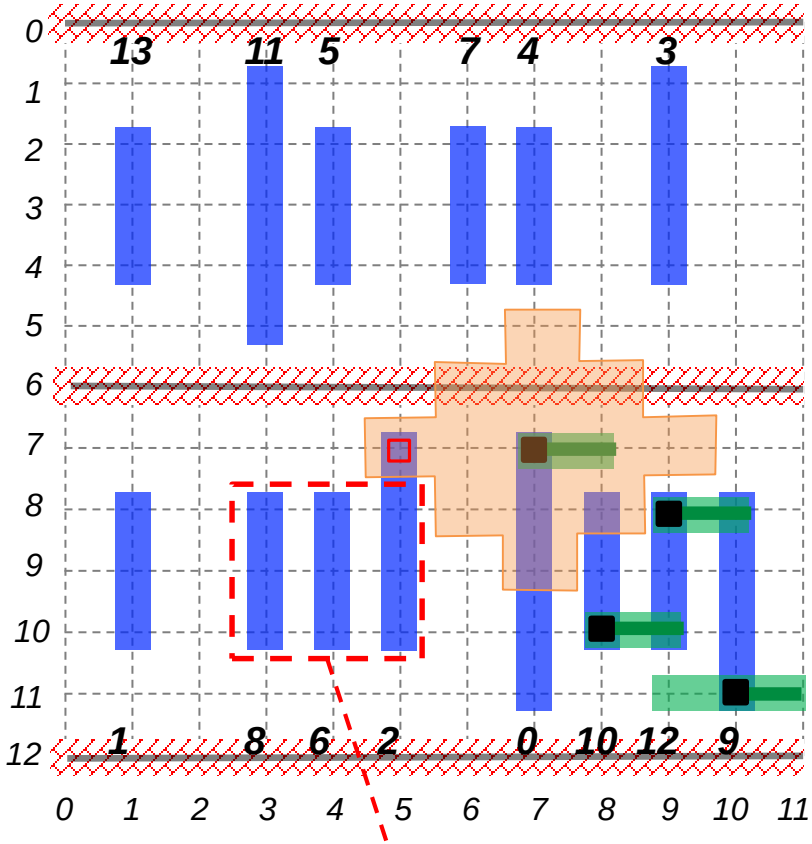
Simple Intrinsic CP Pattern

3 – 3 – n – 3 – 3

UNROUTABLE LAYOUT CLASSIFICATION – PROPAGATED-CP

- Propagated-CP : Main Concern of Pin-accessibility
  → Why designer don't change Pin-shape?



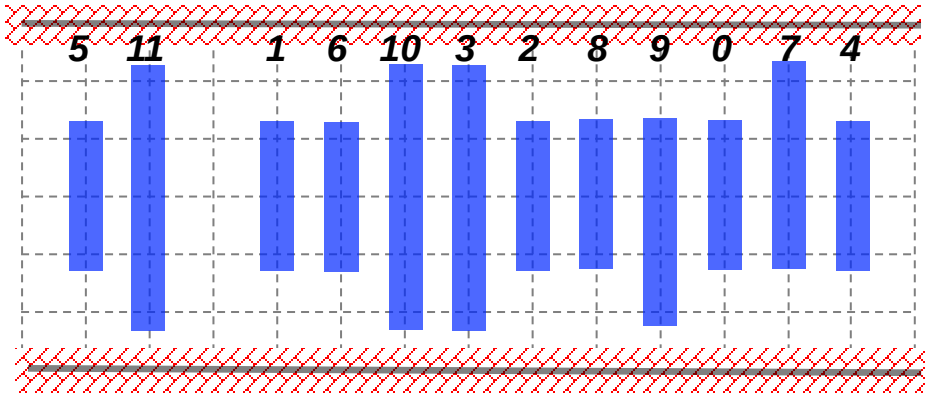


- **#V_Tracks= 12, #H_Tracks= 13**
- **PinDensity= 70%**
- **14 Pins**: 0-13
- **9 Outer Pins**: 14-22
- **10 Nets**: {2 13 14}, {10 12 15}, {4 8 21}, {0 22}, {6 20}, {3 16}, {7 17}, {5 11}, {9 19}, {1 18}

Propagated CP Pattern
3 – 3 – 3

UNROUTABLE LAYOUT CLASSIFICATION – ROUTING CONGESTION

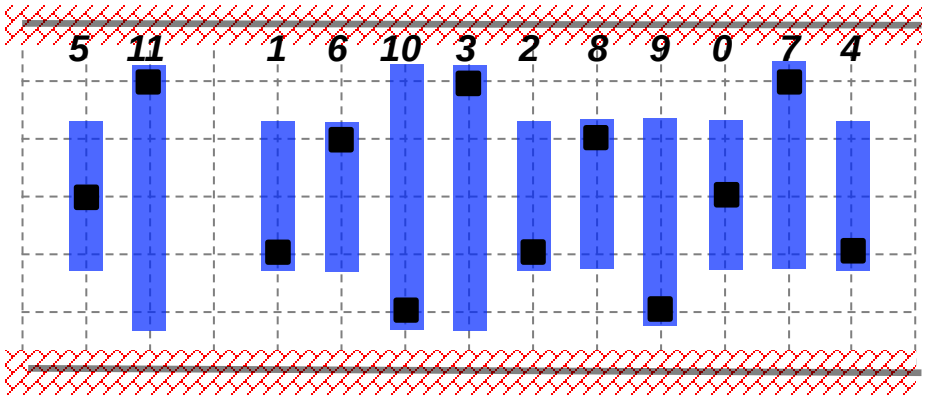
- Routing Congestion : Technology Limitation Identification!

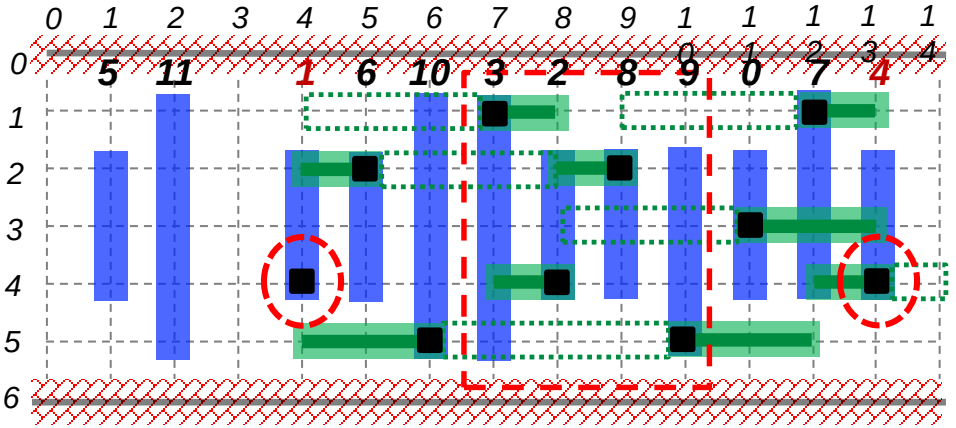


(a)

- **#V_Tracks= 15, #H_Tracks= 7, PinDensity= 90%**
- **12 Pins**: 0-11
- **8 Outer Pins**: 12-19
- **9 Nets**: **{2 11 14}, {5 8 13},** {3 15}, {6 12}, {9 16}, **{1 4},** {7 19}, {0 17}, {10 18}

All tracks are occupied / blocked !!





ROUTABILITY DIAGNOSIS EXPERIMENTAL STATISTICS

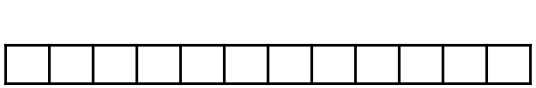
- Total Diagnosis Time
  - MUS Extraction Time + Decision & Propagation Time
  - Diagnosis Performance (Complexity and Execution Time) depends on the root causes of routing failure
    - CP pattern case is less than 30 seconds on average to get the result.
    - Routing Congestion Case is relatively longer than the CP pattern cases.

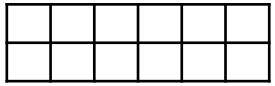
Table 3: Experiment statistics of routability diagnosis (94 pin layouts @ 90 grids). In the table, #N=#Nets, #P=#Pins.

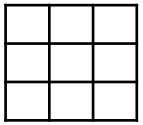
Conflict Type	#N (avg.)	#P (avg.)	#Variable (avg.)	#Clauses (avg.)			Diagnosis Time [s] (avg.)		
				Original	MUS	Ratio [%]	MUS Extraction	Decision & Propagation	Total
CP pattern (80 cases)	10.2	22.4	68,954.6	3,068,017.3	291.5	0.010	17.0	4.1	21.1
Routing Congestion (14 cases)	10.0	22.5	68,803.3	3,049,687.6	2,627.8	0.086	72.9	33.4	106.3

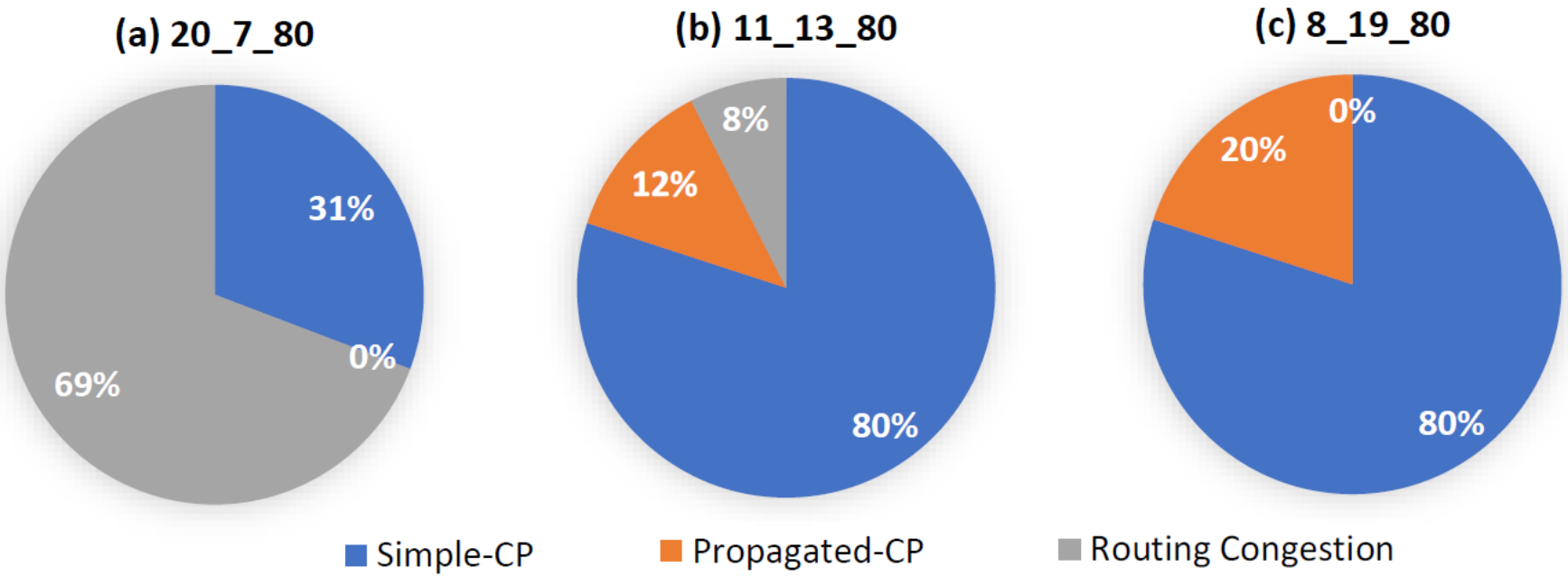
ROUTABILITY DIAGNOSIS – ROOT CAUSE CONFIGURATION

- The same Grid Number with different number of pins row









PUBLICATIONS WITH THIS PROJECT

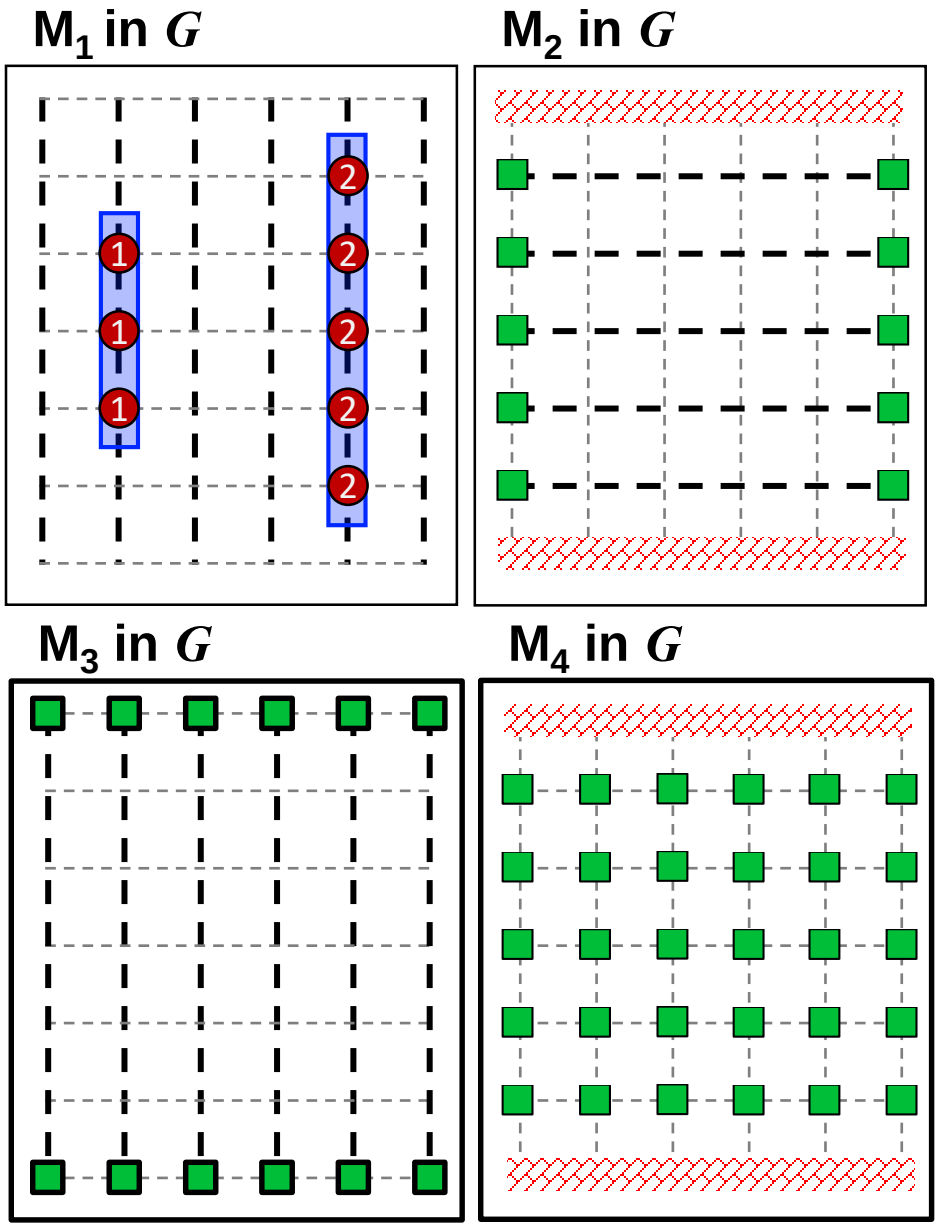
1. Ilgweon Kang, **Dongwon Park**, Changho Han, Chung-Kuan Cheng. "*Fast and Precise Routability Analysis with Conditional Design Rules".* SLIP 2018
2. **Dongwon Park**, Ilgweon Kang, Yeseong Kim, Sicun Gao, Bil Lin and Chung-Kuan Cheng. " *RODE: Efficient Routability Diagnosis and Estimation Framework Based on SAT Techniques".* ISPD 2019
3. Journal Extension is now under preparation. (TCAD)

Appendix

ROAD : NOTATION & PIN-LAYOUT CONFIGURATION

TABLE I
NOTATIONS FOR SAT FORMULATION.

Term	Description
$G(V,E)$	Three-dimensional (3-D) routing graph
V	Set of vertices in the routing graph G
V_i	Set of vertices in i^{th} metal layer of the routing graph G
v	A vertex at the coordinate (x_v, y_v, z_v)
v_d	0-1 indicator if d-directional adjacent vertex about v
$a(v)$	Set of adjacent vertices of v
E	Set of edges in the routing graph G
$e_{v,u}$	An edge between v and u, $u \in a(v)$
N	Set of multi-pin nets in the given routing box
n	n^{th} multi-pin net
s^n	A source of n
T^n	Set of sinks in n
t_m^n	m^{th} sink of n
f_m^n	m^{th} commodity flow of n heading to t_m^n
$e_{v,u}^n$	0-1 indicator if $e_{v,u}$ is used for n
$f_m^n(v)$	Flow variable on v for commodity t_m^n
$f_m^n(v,u)$	0-1 indicator if $e_{v,u}$ is used for commodity t_m^n
$m_{v,u}$	0-1 indicator if there is a metal segment on $e_{v,u}$
$g_{d,v}$	0-1 indicator if v forms d-side EOL of a metal segment



WHAT IS SAT (BOOLEAN SATISFIABILITY) ?

- **SAT** (Boolean Satisfiability)

  → Find a variable assignment to make propositional logic formula evaluates to 1(True) (Satisfiable) , or prove that no such assignment exists (Unsatisfiable)

$$A \cap (\neg B \cup C) \longrightarrow A \to 1, B \to 1, C \to 1 \ (\boldsymbol{Satisfiable})$$

$$A \cap B \cap (\neg B \cup \neg A) \longrightarrow \boldsymbol{Unsatisfiable}$$

→Usually, Product of Sum (i.e. CNF) is normal representation for SAT formula

Truth Table

X	Y	F(x,y)
0	0	1
0	1	0
1	0	0
1	1	1

Product of Sum (CNF)

$$(\neg X \cup Y) \cap (X \cup \neg Y)$$

Clause

Sum of Product (DNF)

$$(X \cap Y) \cup (\neg X \cap \neg Y)$$

Equivalent Representations