ISPD 2018 Initial Detailed Routing Contest and Benchmarks

Speaker: Wen-Hao Liu
Organizers:Stefanus Mantik, Gracieli Posser, William Chow, Yixiao Ding, Wen-Hao Liu

Cadence Design Systems
http://www.ispd.cc/contests/18/index.htm

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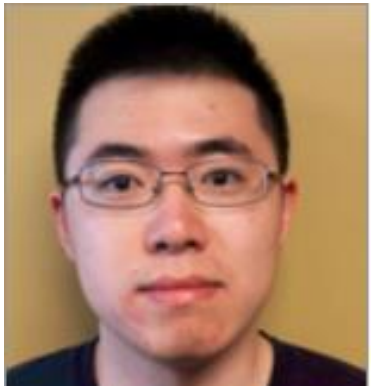
Contest Organizers

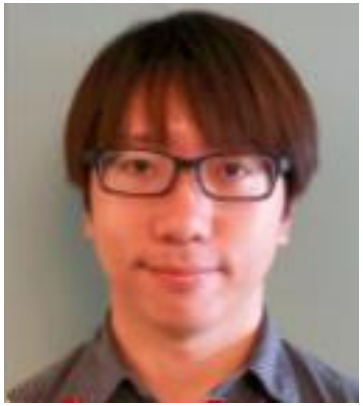
Wen-Hao Liu
Contest chair

Stefanus Mantik
Benchmarks



Yixiao Ding
Benchmark testing

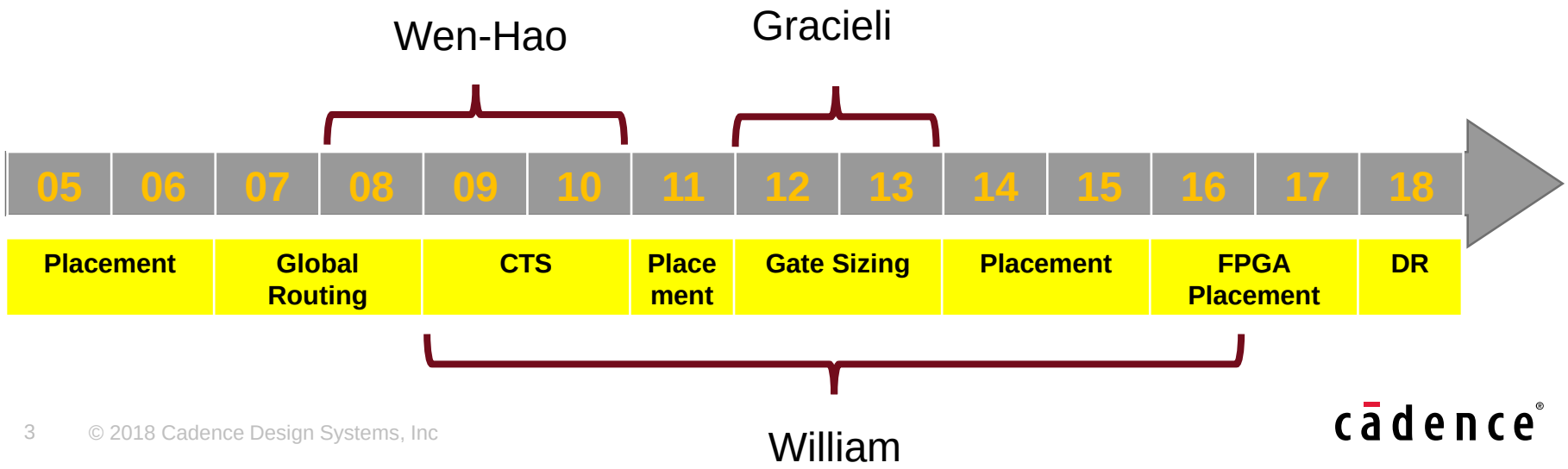
Gracieli Posser
Vice chair



William Chow
Evaluation

Motivation

- Detailed routing is an dead-or-alive critical topic for advanced node enablement like N7, N5 and N3.
- Attract talents to address detailed routing challenges
- Drive practical detailed routing research to consider real design rules, memory scalability, and runtime scalability



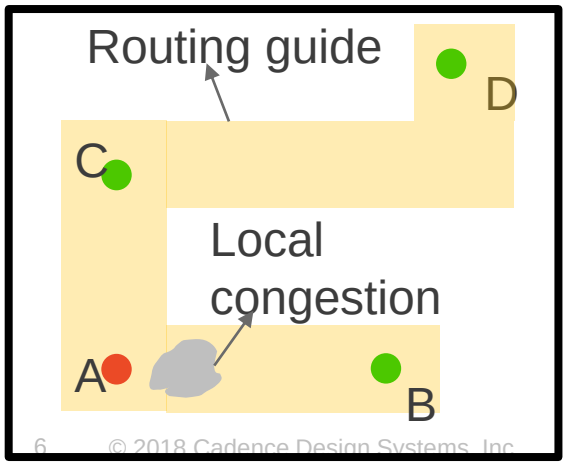
Outline

- Problem Introduction
- Benchmark Suite Characteristics
- Evaluation Metrics
- Contest Results
- Result Study
- Acknowledgements

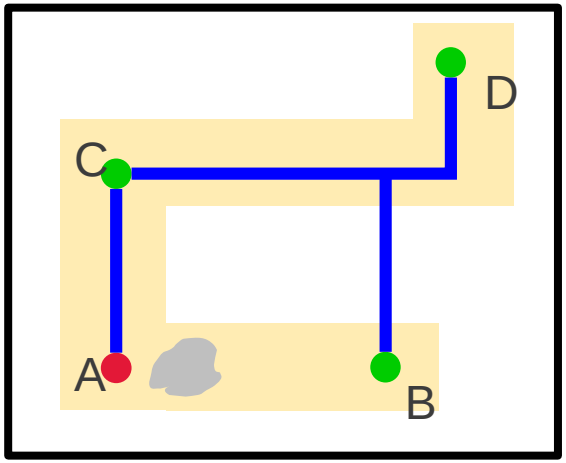
Problem Introduction

Initial Detailed Routing Problem

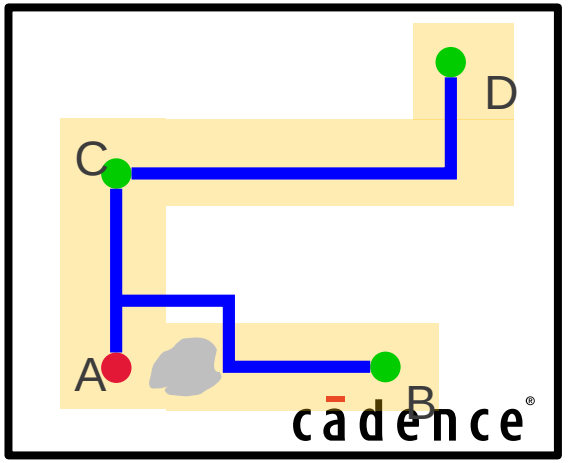
- Assuming that given routing guides are already well optimized for certain metrics, a detailed router needs to honor the guides as much as possible in order to keep the optimized metrics.
- If the initial detailed routing solution can meet the most common routing rules even it is not fully DRC clean, the later detailed routing refinement step will have less chance to largely disturb the routing solution.



Guide-violation solution



Guide-honoring solution

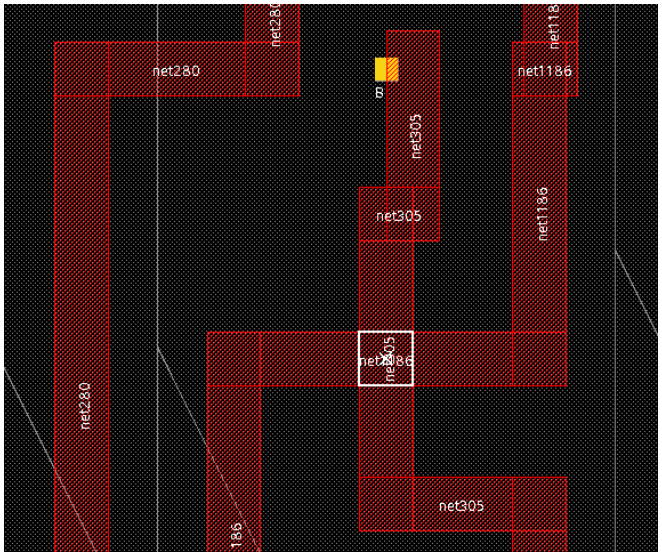


Open / Short

- Open: If any pin in a net is disconnected, the net will be considered as an open net and the routing solution is invalid.

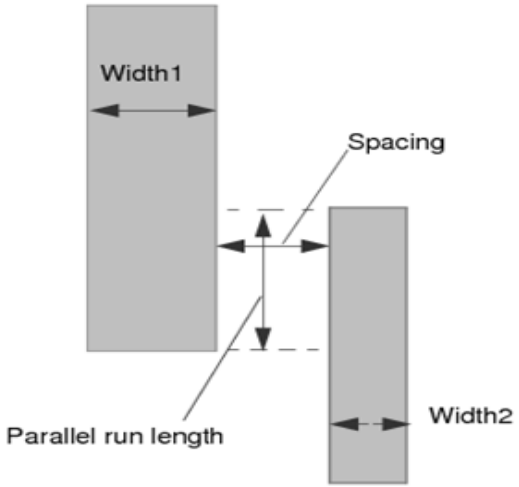
- Short: either a via metal or wire metal overlaps with another object like via metal, wire metal, blockages, or pin shapes.

Short violation



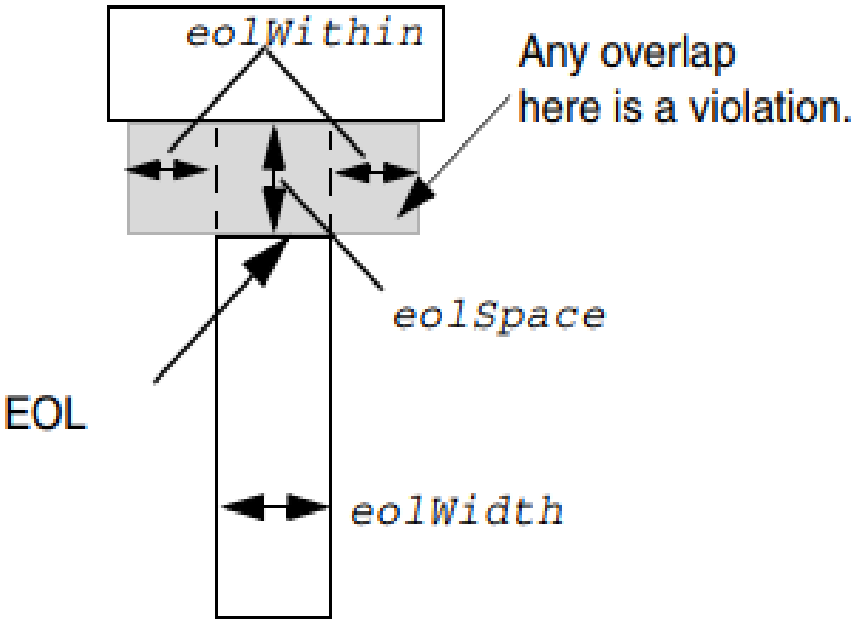
Spacing Table

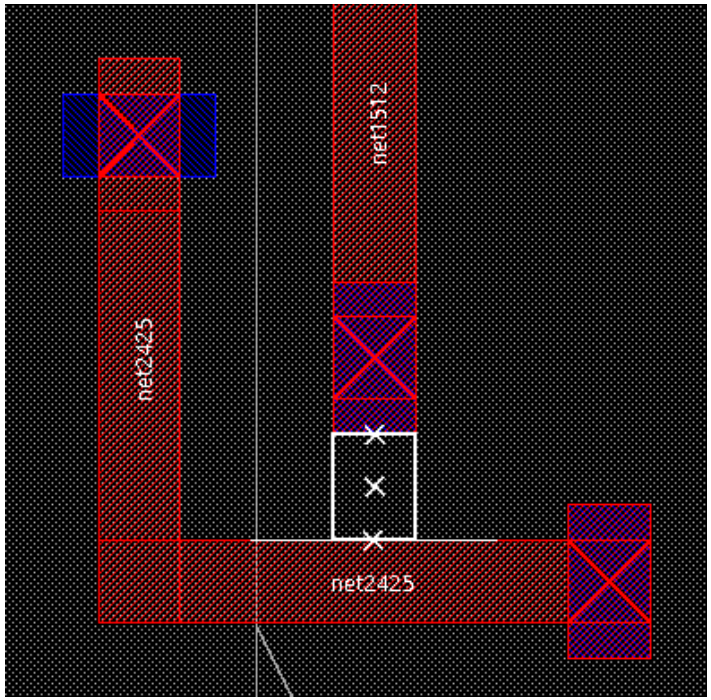
- Spacing table specifies the required spacing between two objects according to their parallel-run length and widths
- To simplify the problem, we make spacing table only depend on widths. Namely, the spacing value remains the same regardless of the parallel-run length



End of line (eol) spacing rule

- The end-of-line (EOL) spacing rule indicates that an edge that is shorter than *eolWidth*, noted as end-of-line edge requires spacing greater than or equal to *eolSpace* beyond the EOL anywhere within (that is, less than) *eolWithin* distance

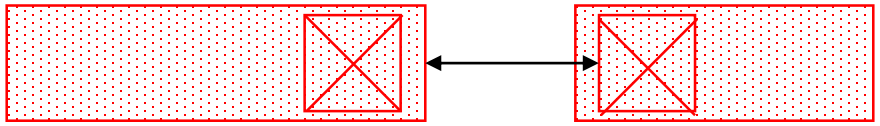




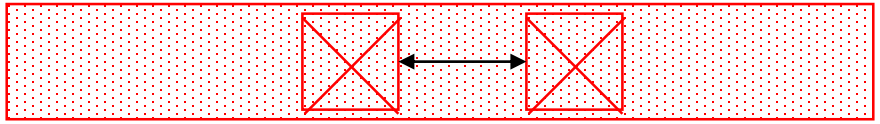
Cut Spacing

- A cut spacing specifies the minimum spacing between via cuts. It applies for cuts from both different nets and the same net.

- Stacked vias is allowed if their center are aligned.



Different net cut spacing

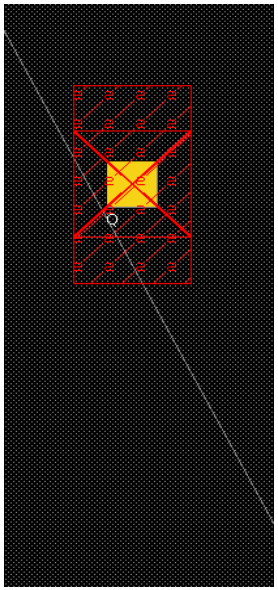


Same net cut spacing

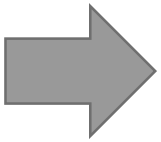
Min-Area Rule (MAR)

- The min area rule specifies the minimum metal area required for polygons on each layer. All polygons must have an area that is greater than or equal to the specified area value.

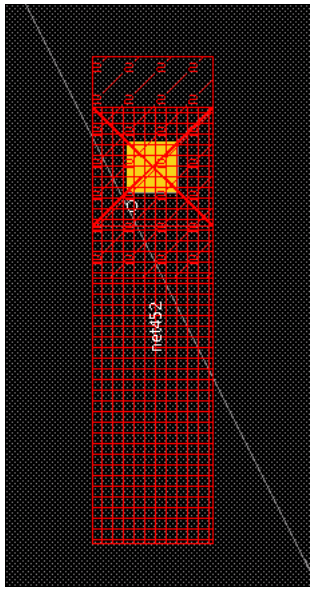
Min-area violation



Add patch wire



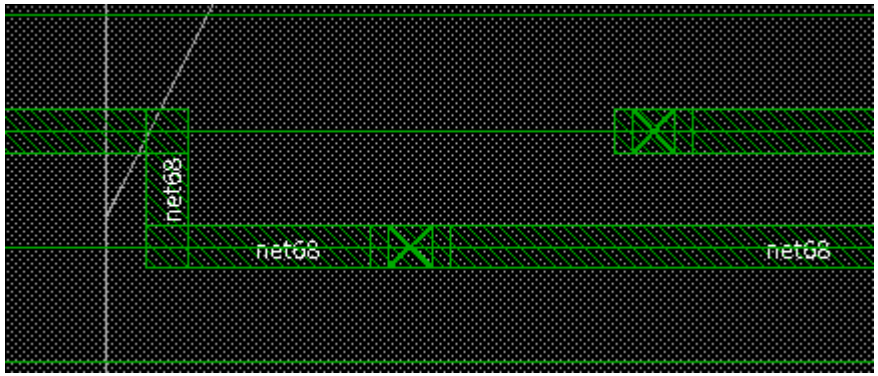
Min-area -violation-free

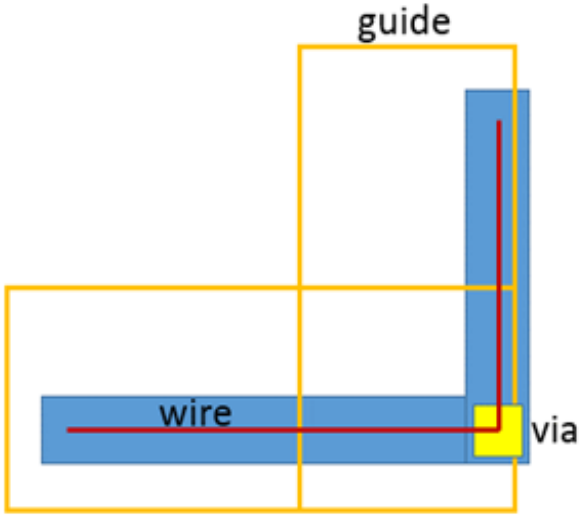


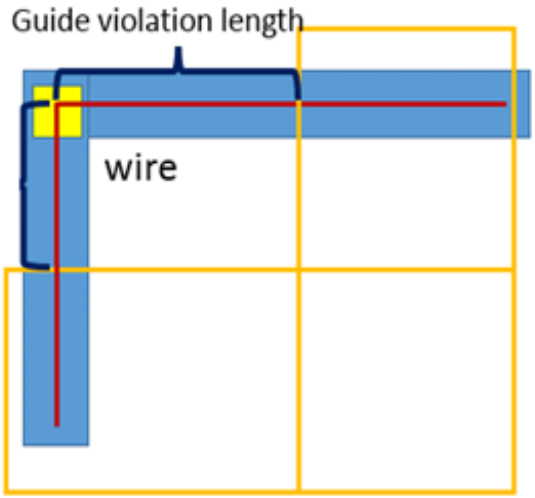
Routing Preference Metrics

- Wrong-way Routing
- Off-track Routing
- Routing Guide Honoring
- Non-determinism Penalty

Wrong-way routing



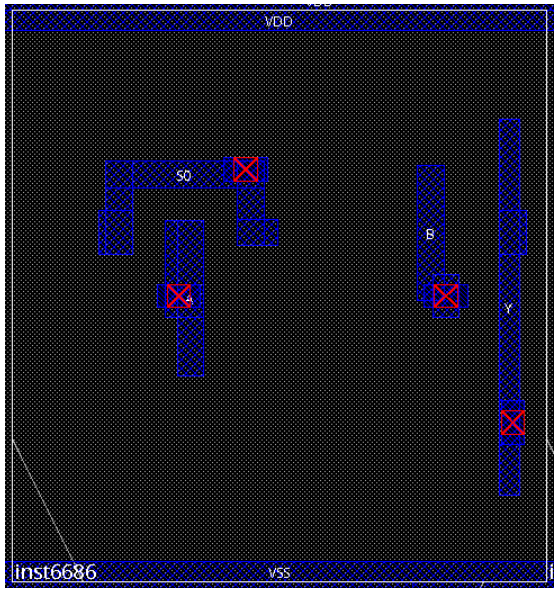




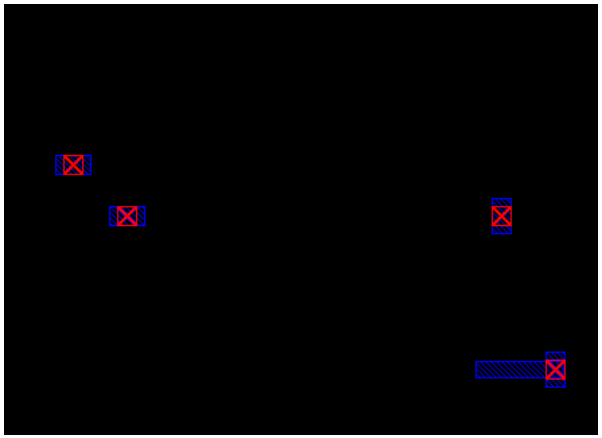
The challenges of this contest

- Pin-access location selection
- Via selection
- Patch wire insertion
- Memory and runtime controlling
  - Max runtime limit: 12 hours (real time).
  - Max memory limit: 64GB

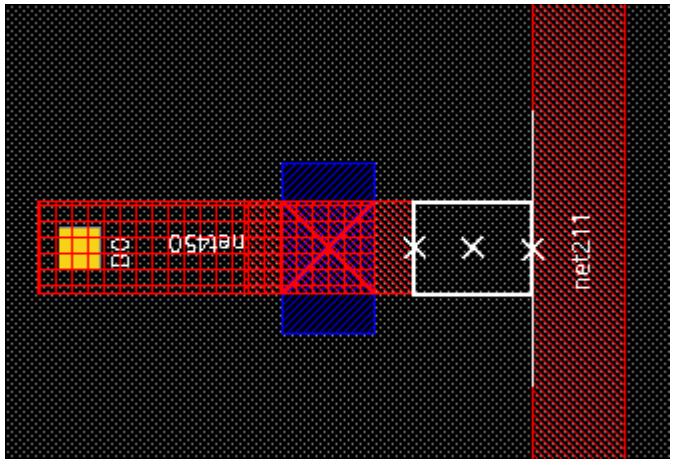
Pin access solution



Different vias



EOL-violation triggered by a patch



Benchmark Suite Characteristics

Benchmark Suite Characteristics

- The benchmarks are derived from two real designs
  - a single-core 32-bit processor with four memory cores
  - a quad-core 32-bit processors with 16 on-chip memory blocks.

- The benchmarks are synthesized using generic 45nm and 32nm technology and cell libraries.

- Simplifications for the contest
  - Power and ground (PG) nets are removed
  - Non-default rules are removed
  - Timing related information are removed.
  - Design rules are simplified into a regular spacing rule and an EOL spacing rule, and a simple cut-to-cut spacing rule.

Benchmark Suite Characteristics

- The routing for every benchmark can be done within 1 hour and 6 GB memory by using the commercial routers with a single thread.
- Every benchmark is guaranteed to have a DRC-violation-free solution
- Each benchmark associates to different “quality” of the routing guides
  - High-quality guide: Contain DRC-free solution in routing guides
  - Low-quality guide: Have congestion issue, so detailed routing needs to escape routing guides to fix DRCs

Benchmark Suite Characteristics

- Three small testcases with sample solutions are released early to enable the early development
- The final evaluation is based 6 released and 4 hidden benchmarks

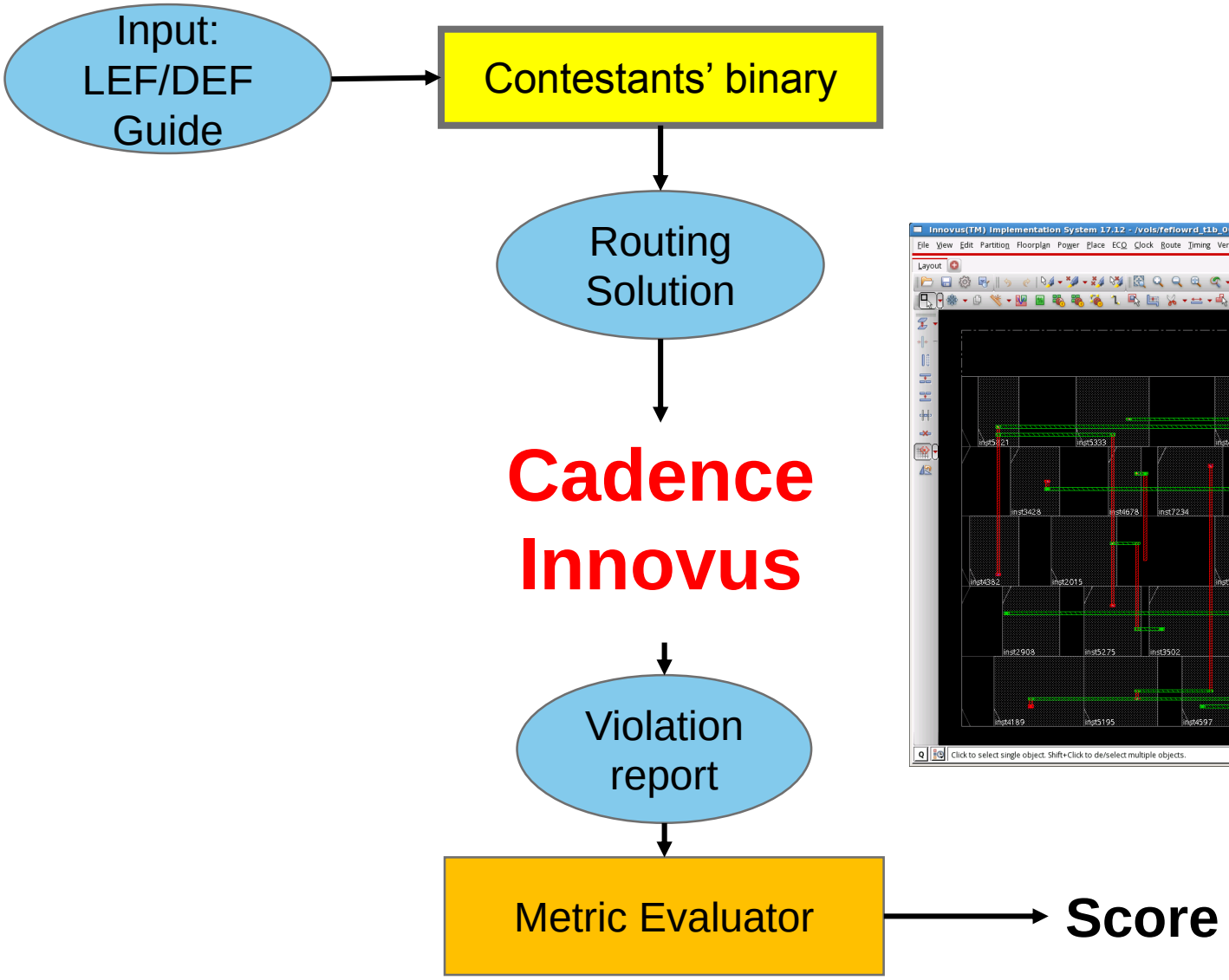
	#std	#blk	#net	#pin	#Layer	Die size
Sample testcases						
ispd18_sample	22	0	11	0	9	0.017x0.01mm^2
ispd18_sample2	22	1	16	0	9	0.017x0.01mm^2
ispd18_sample3	5	1	7	5	16	1.90x2.00mm^2
Released benchmarks						
ispd18_test1	8879	0	3153	0	9	0.20x0.19mm^2
ispd18_test2	35913	0	36834	1211	9	0.65x0.57mm^2
ispd18_test3	35973	4	36700	1211	9	0.99x0.70mm^2
ispd18_test4	72090	4	72410	1211	9	0.89x0.61mm^2
ispd18_test5	71946	8	72394	1211	9	0.93x0.92mm^2
ispd18_test6	107919	0	107701	1211	9	0.86x0.53mm^2
Hidden benchmarks						
ispd18_test7	179865	16	179863	1211	9	1.36x1.33mm^2
ispd18_test8	191987	16	179863	1211	9	1.36x1.33mm^2
ispd18_test9	192911	0	178858	1211	9	0.91x0.78mm^2
ispd18_test10	290386	0	182000	1211	9	0.91x0.78mm^2

Summary of benchmark suite characteristics

ispd18_sample	45nm	Sample test for tutorial purpose
ispd18_sample2	45nm	Sample test with a block macro and nets connecting to the block
ispd18_sample3	45nm	Sample test that has IO pins and large design area
ispd18_test1	45nm	Standard cell netlist only
ispd18_test2	45nm	Standard cell netlist with IO pins
ispd18_test3	45nm	Standard cell netlist with IO pins and block macros
ispd18_test4	32nm	Design has Metal2 OBS in some of its standard cells
ispd18_test5	32nm	Design has Metal2 OBS, Metal2 Power/Ground pins, and routing direction is reversed
ispd18_test6	32nm	Design has Metal2 OBS, Metal2 Power/Ground pins, and reversed routing direction, but without any block macro
ispd18_test7	32nm	Quad-core design with Metal2 OBS and Metal2 Power/Ground pins as blockage
ispd18_test8	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage
ispd18_test9	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage, no block macro, higher utilization
ispd18_test10	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage, no block macro, extra congested area

Evaluation

Evaluation Process



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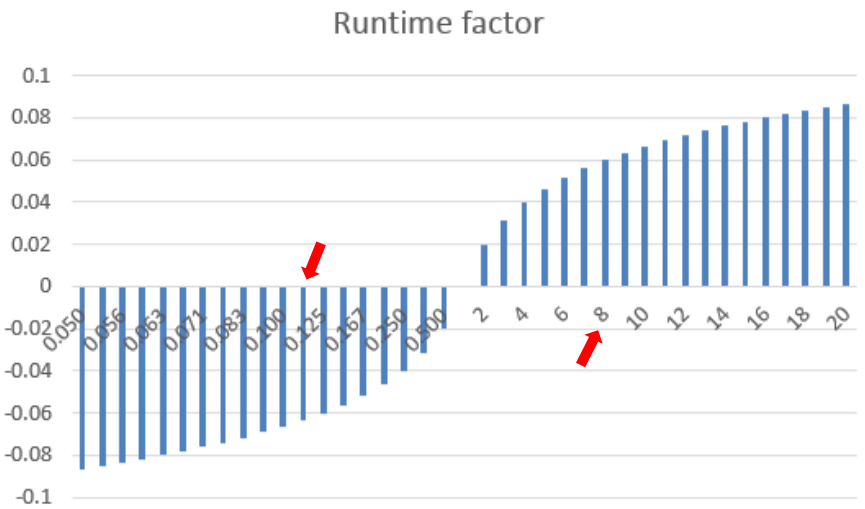
Evaluation Metric

- The quality of result for a routing solution is measured by the following equation. A solution with a smaller scaled score is considered as a better solution in this contest
  - Scaled_score = raw_score * (1 + nondeterministic_penalty + runtime_factor)
- We will run each binary more than once. If we observe nondeterministic results, nondeterministic_penalty will be 3%; otherwise, it will be 0.

Metric	Weight
Short metal area	500
Number of spacing violations	500
Number of min-area violations	500
Total number of vias	2
Total length of wires	0.5
Total length of the wires outside of the routing guides	1
Total number of the vias outside of routing guides	1
Total length of off-track wires	0.5
Total number of off-track vias	1
Total length of wrong-way wires	1

Evaluation Metric (cont.)

- Runtime_factor = min(0.1, max(-0.1, **0.02 *** log2(**Router_Wall_Time / Median_Wall_Time**))
  - For each benchmark, we will select the “median_wall_time” based on the binary which can generate valid solutions.
  - Based on the following curve, say, a router is 8X faster/slower than the median, it will get 6% score benefit/penalty
  - The runtime penalty/benefit is limited within 10% and -10%



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Ranking Method

- Rank each team for each benchmark. The team with a smaller scaled score will get a smaller ranking number, which means a better ranking.
- Prune out the worst (i.e., biggest) ranking number, and then average the remaining rankings for each team. The team with the smallest averaged ranking number wins the contest.
- Example:

Scaled Score Table

	team 1	team 2	team 3	team 4	team 5
benchmark1	80	200	210	250	100
benchmark2	90	180	70	130	60
benchmark3	70	X	40	X	180
benchmark4	300	800	180	250	400
benchmark5	150	X	150	170	160

'X' means a failure

Ranking Table

	team 1	team 2	team 3	team 4	team 5
benchmark1	1	3	4	5	2
benchmark2	3	5	2	4	1
benchmark3	2	5 (X)	1	5 (X)	3
benchmark4	3	5	1	2	4
benchmark5	1	5 (X)	1	4	3

Final Ranking Result

	team 1	team 2	team 3	team 4	team 5
benchmark1	1	3	4	5	2
benchmark2	3	5	2	4	1
benchmark3	2	5	1	5	3
benchmark4	3	5	1	2	4
benchmark5	1	5	1	4	3
Avg without the outlier	1.75	4.5	**1.25**	3.75	2.25

Contest Results

Participation Statistics

- 33 initial registrations
  - Asia: 22 teams
  - North America: 8 teams
  - South America: 2 teams
  - Europe: 1 team
  - *Overall 9 different countries/regions*
  - *USA, China, Taiwan, Hong Kong, South Korea, Canada, Italy, Bangladesh, Brazil*
- 12 alpha/beta binary submissions
- 10 final submissions

Top 5 teams

- Top 5 teams will get plaques
- Top 3 teams will get cash reward sponsored by Cadence
  - 1st - $700
  - 2nd - $500
  - 3rd - $300

Team	Team name	Affiliation	Members
4	NTHU-DR	National Tsing Hua University, Fuzhou University	Chein-Hao Tsou, Chia-Chun Chung, Chao-Yuan Huang, Wang-Yang Li, Zhuang Zhen, Genggeng Liu, Wenzhong Guo, Ting-Chi Wang
5	LuLuRoute	National Taiwan University	Hao Chen, Chen-Hao Hsu, Fan-Keng Sun, Ching-Yu Chen, and Yao-Wen Chang
7	Dr. CU	The Chinese University of Hong Kong	Gengjie Chen, Chak-Wa Pui, Haocheng Li, Jingsong Chen, Bentian Jiang, Evangeline F.Y. Young
9	UFRGS-Brazil	Universidade Federal do Rio Grande do Sul	Mateus Fogaca, Jucemar Monteiro, Henrique Placido, Andre Oliveira, Isadora Oliveira, Eder Matheus Monteiro, Marcelo Johann, Ricardo Reis
19	NCTUdr	National Chiao Tung University	Shih-Ting Lin, Ming-Jie Fong, Ching-Hsi Chen, Wei-Ren Lai, He-Cheng Tsai, Yih-Lang Li
21	TritonRoute	University of California, San Diego	Andrew B. Kahng, Lutong Wang, Bangqi Xu

Result Overview

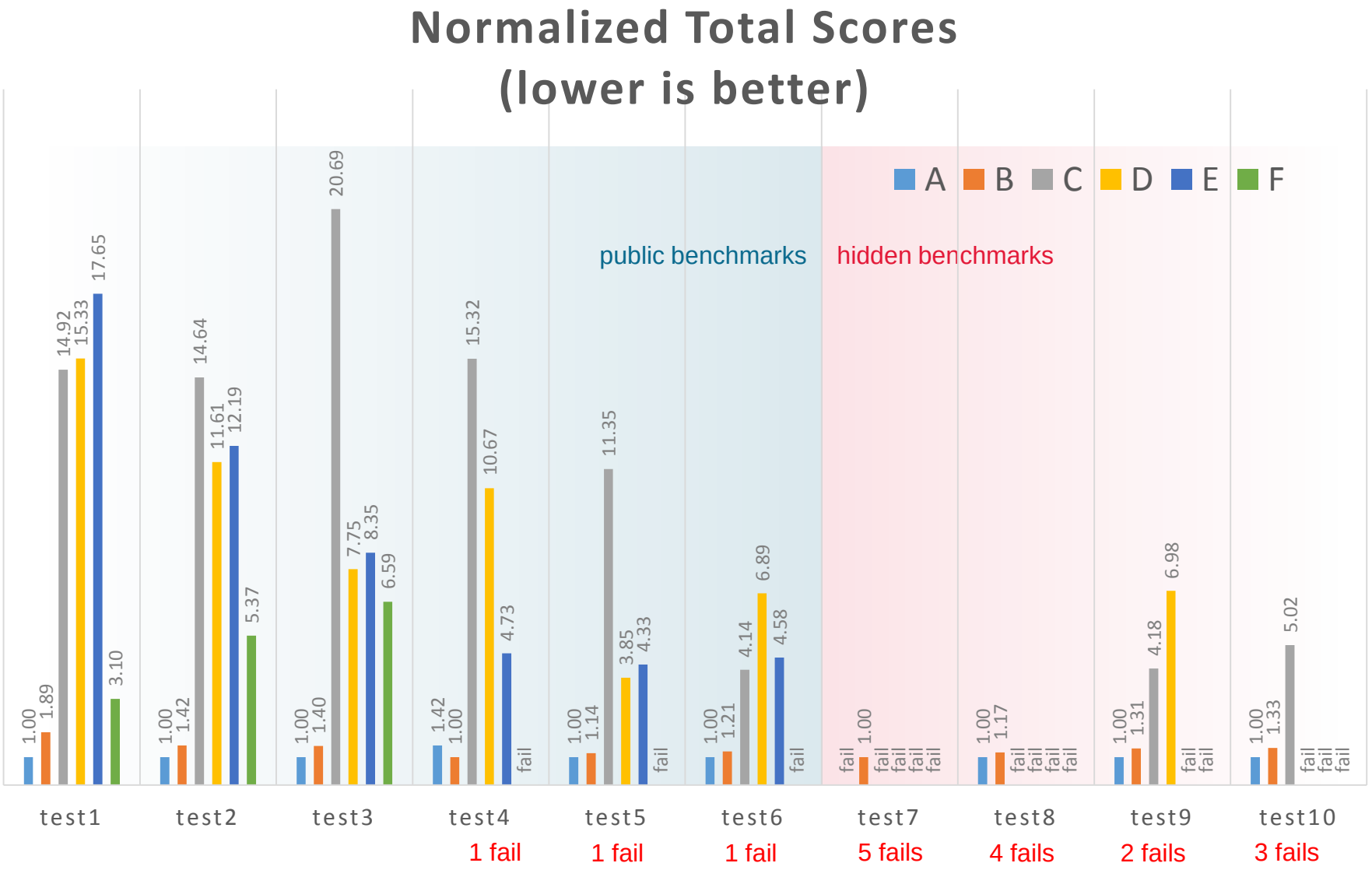
- Open nets comparison

Mem : out-of-memory
Time : over 12 hours
No output : no solution at exit

	A	B	C	D	E	F
test1	0	0	0	0	0	0
test2	0	0	0	0	0	0
test3	0	0	0	0	0	0
test4	0	0	0	0	0	No output
test5	0	0	0	0	0	Mem
test6	0	0	0	0	0	Time
test7	No output	0	Time	Mem	Time	Mem
test8	0	0	Time	Mem	Time	Mem
test9	0	0	0	0	900	Mem
test10	0	0	0	Mem	900	Mem

Hidden benchmarks

Result Overview



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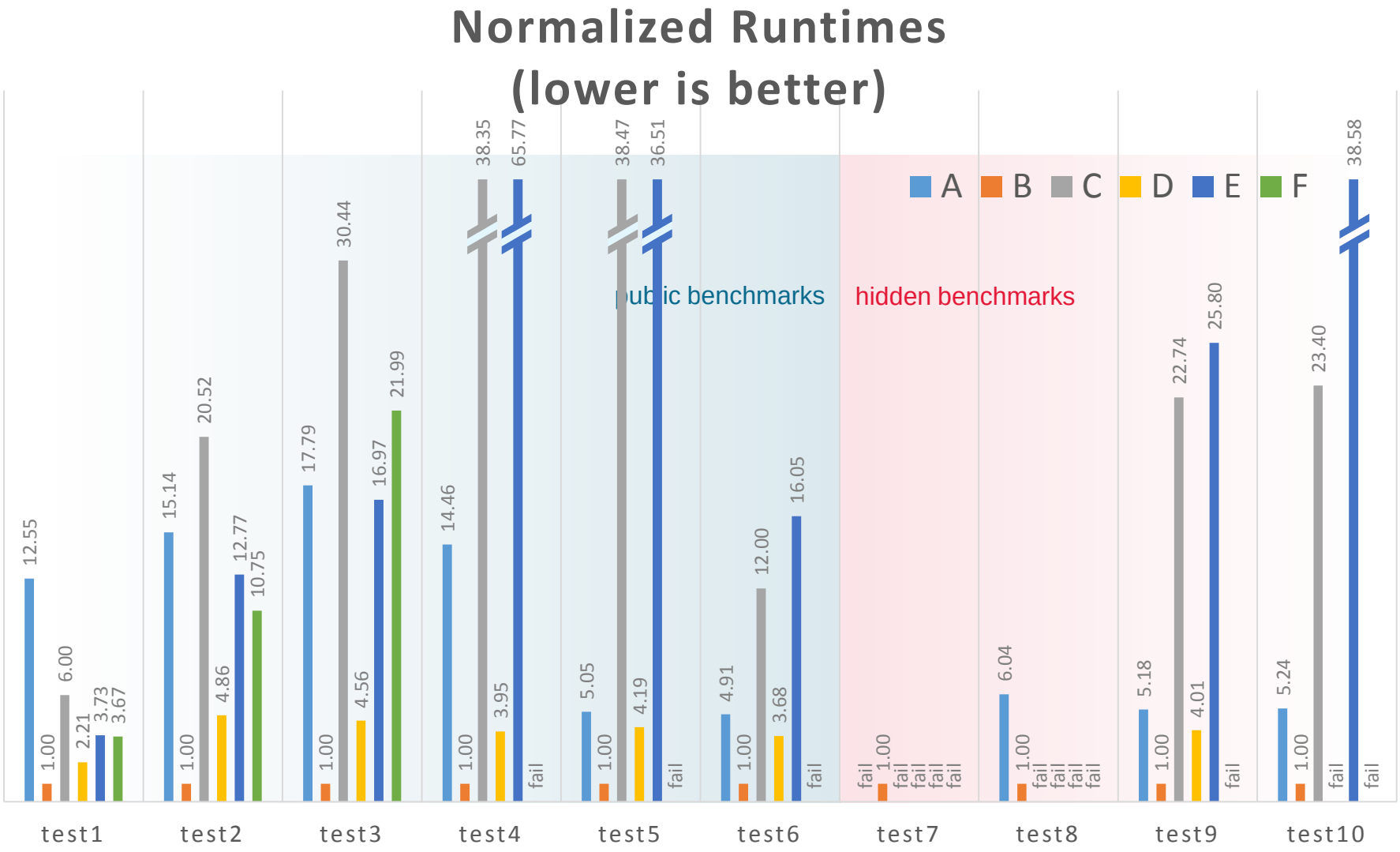
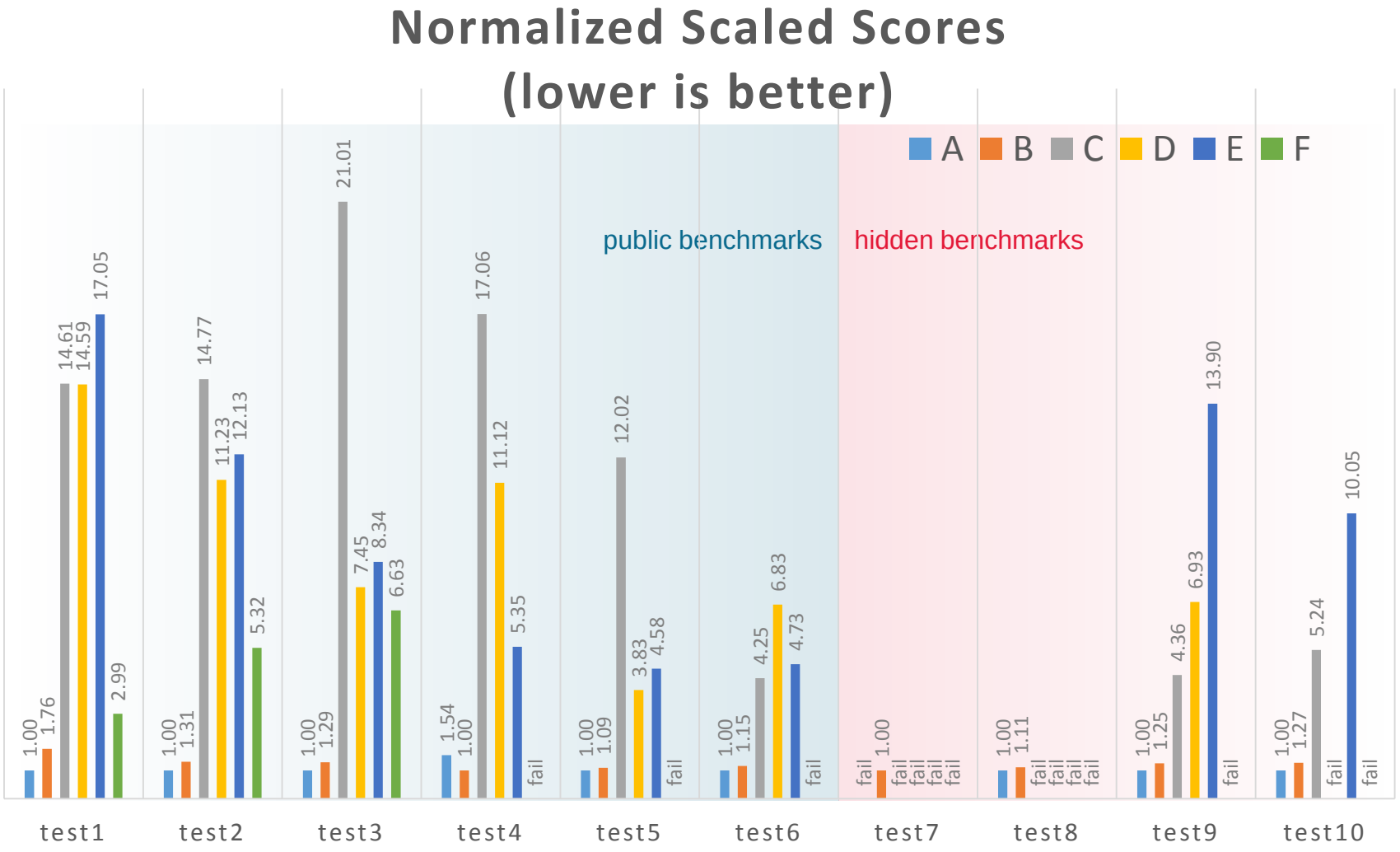
Result Overview



Result Overview

- Scaled scores considering run-time factor



No non-deterministic penalty is applied

Result Overview

- Final ranking

Normalized scaled scores

	A	B	C	D	E	F
test1	1.00	1.76	14.61	14.59	17.05	2.99
test2	1.00	1.31	14.77	11.23	12.13	5.32
test3	1.00	1.29	21.01	7.45	8.34	6.63
test4	1.54	1.00	17.06	11.12	5.34	
test5	1.00	1.09	12.02	3.83	4.58	
test6	1.00	1.15	4.25	6.83	4.73	
test7		1.00				
test8	1.00	1.11				
test9	1.00	1.25	4.36	6.93		
test10	1.00	1.27	5.24			

Ranking

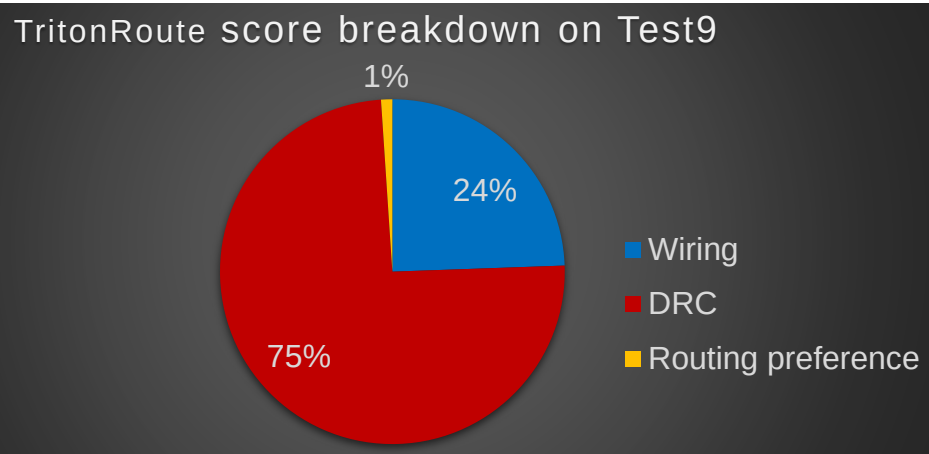
	A	B	C	D	E	F
test1	1	~~2~~	5	4	6	3
test2	1	2	6	4	5	3
test3	1	2	6	4	5	3
test4	2	1	5	4	3	~~10~~
test5	1	2	5	3	4	10
test6	1	2	3	5	4	10
test7	~~10~~	1	~~10~~	~~10~~	~~10~~	10
test8	1	2	10	10	10	10
test9	1	2	3	4	10	10
test10	1	2	3	10	10	10
	1.1	**1.8**	**5.1**	**5.3**	**6.3**	**7.7**

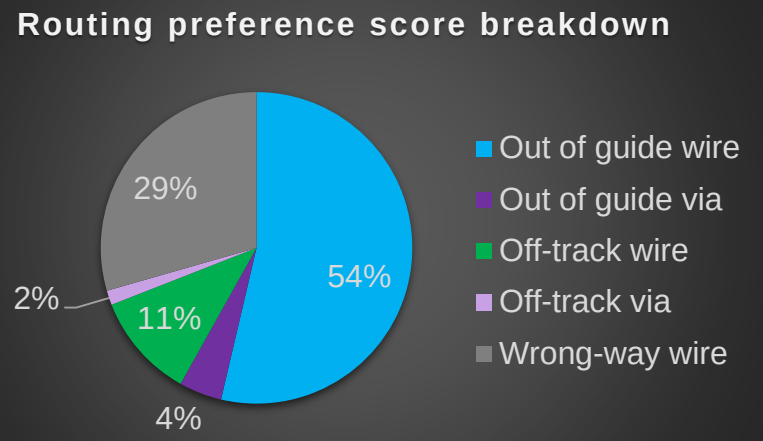
Ranking Announcement

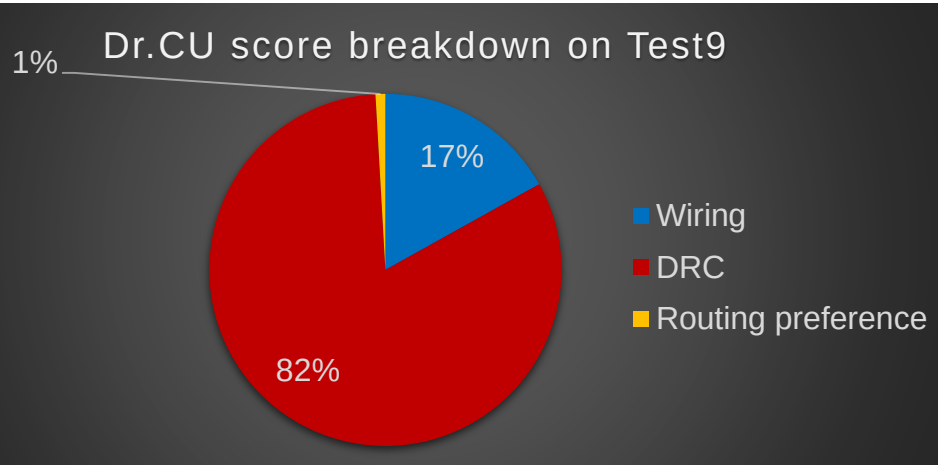
- 1st Place:
  - TritonRoute (UCSD)
- 2nd Place
  - Dr. CU (The Chinese University of Hong Kong)
- 3rd Place*:
  - LuLuRoute (National Taiwan University),
  - NTHU-DR (National Tsing Hua University and Fuzhou University)
- 4th Place:
  - UFRGS-Brazil (Universidade Federal do Rio Grande do Sul)
- 5th Place:
  - NCTUdr (National Chiao Tung University)

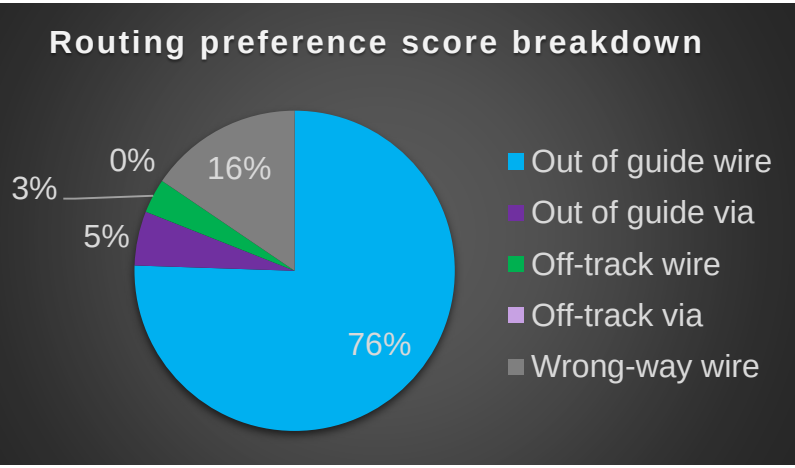
* According to the original ranking policy, LuLuRoute should place number 3. However, from the data standpoint, NTHU-DR is tie for the 3rd place, so we rank them both at 3rd place.

Result Study

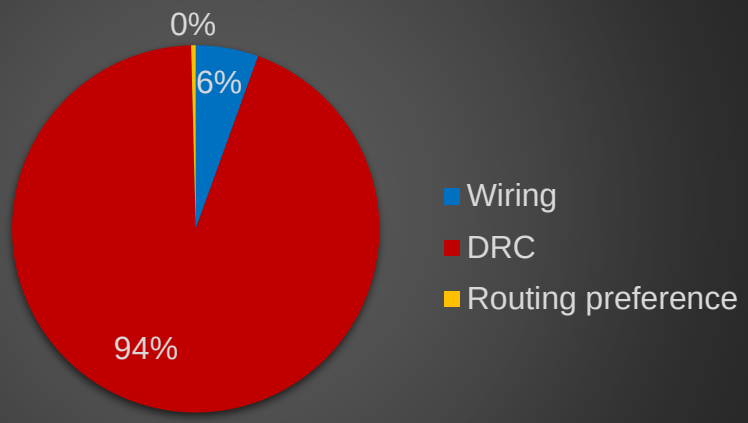




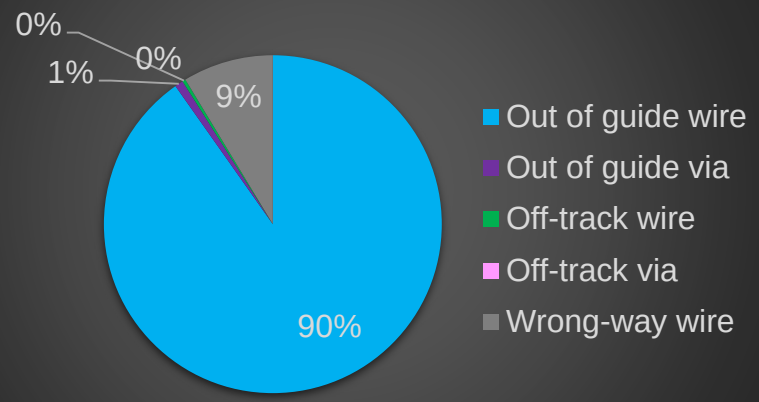




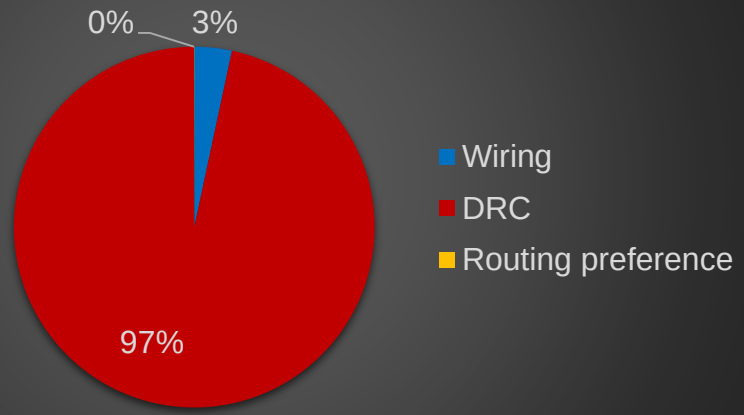
LuLuRoute score breakdown on Test9



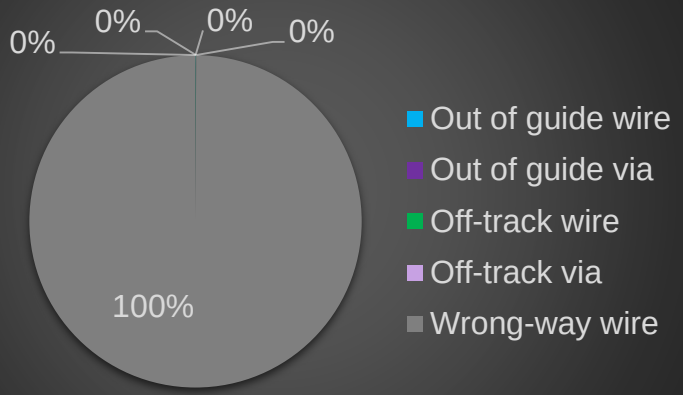
Routing preference score breakdown



NTHU-DR score breakdown on Test9



Routing preference score breakdown



Wire length (WL) and Number of Vias (test9)

TritonRoute

- Highest total WL

Dr. CU

- Smallest total WL

LuLuRoute

- Less total number of vias
- Less vias and WL on Metal1

NTHU-DR

- Highest number of vias
- High number of vias on Metal1

Wire Length

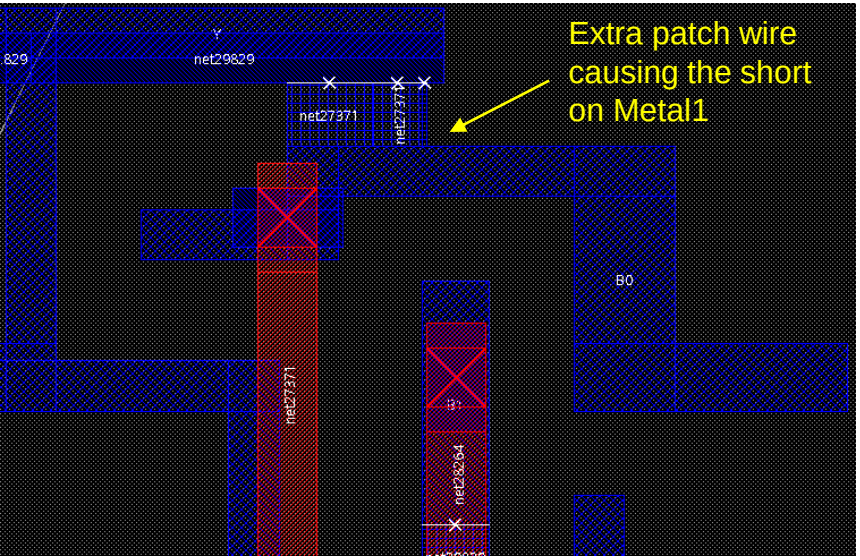
	TritonRoute	Dr. CU	LuLuRoute	NTHU-DR
Metal1	25095.91	50013.64	2014.21	18090.30
Metal2	680645.10	679947.80	827436.93	658983.80
Metal3	1900920.78	1813273.30	1917989.05	1858156.50
Metal4	1794372.99	1588512.00	1651408.95e	1607125.75
Metal5	825504.39	722913.65	747514.40	757713.20
Metal6	550743.27	507752.35	503127.80	528075.10
Metal7	50411.31	39547.12	46296.28	41391.80
Metal8	52188.20	48876.42	46376.42	50872.65
Metal9	461.67	127.00	125.6	124.80
Total	**5880343.61**	**5450963.28**	**5742289.64**	**5520533.90**

# of vias

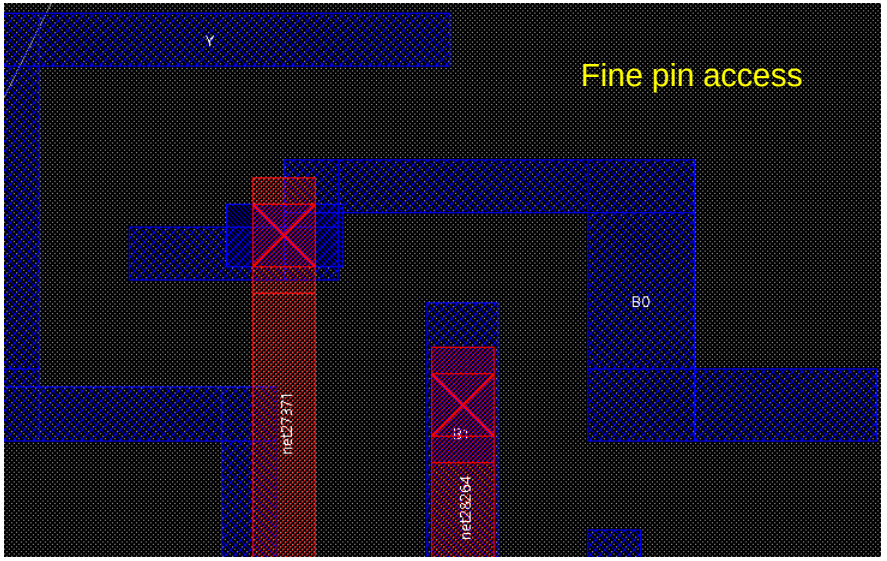
	TritonRoute	Dr. CU	LuLuRoute	NTHU-DR
Metal1	815555	837309	813378	1125973
Metal2	1046560	902325	851538	1186597
Metal3	694711	411615	425999	534103
Metal4	256893	138774	153246	178200
Metal5	84010	50113	50682	57974
Metal6	16488	7607	7606	8905
Metal7	5690	4105	3928	4610
Metal8	352	24	22	25
Metal9	0	0	0	0
Total	**2920259**	**2351872**	**2306399**	**3096387**

Pin access

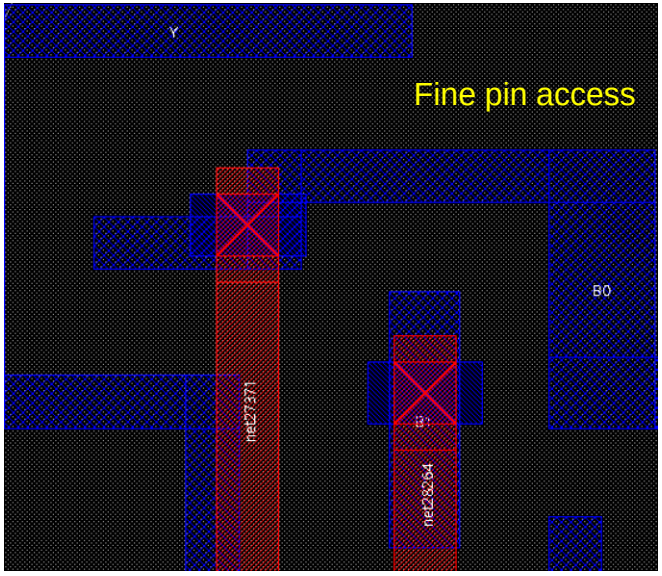
TritonRoute



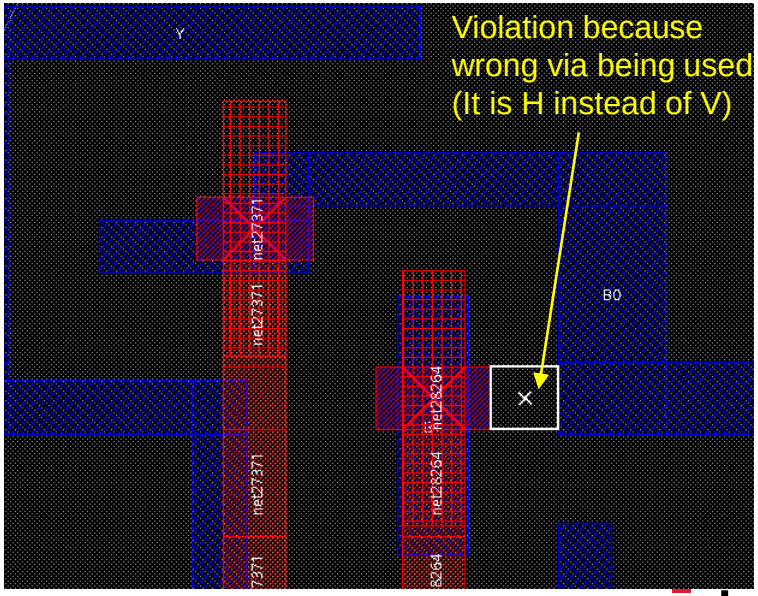
Dr. CU



LuLuRoute

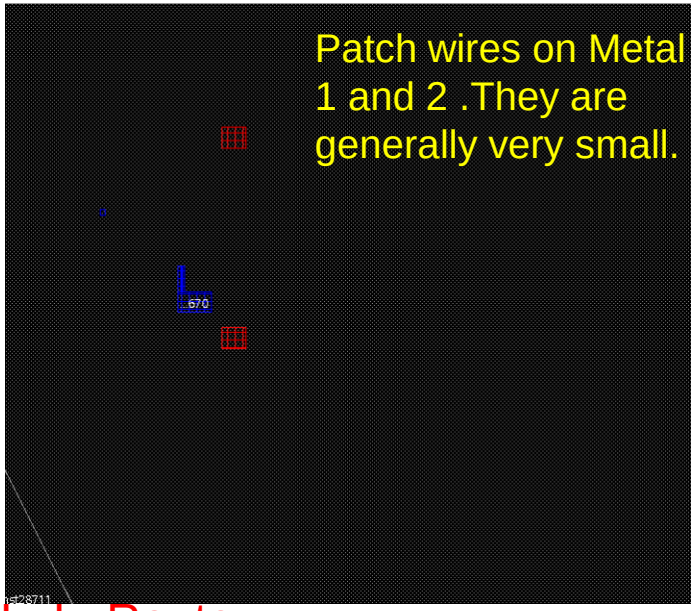


NTHU-DR

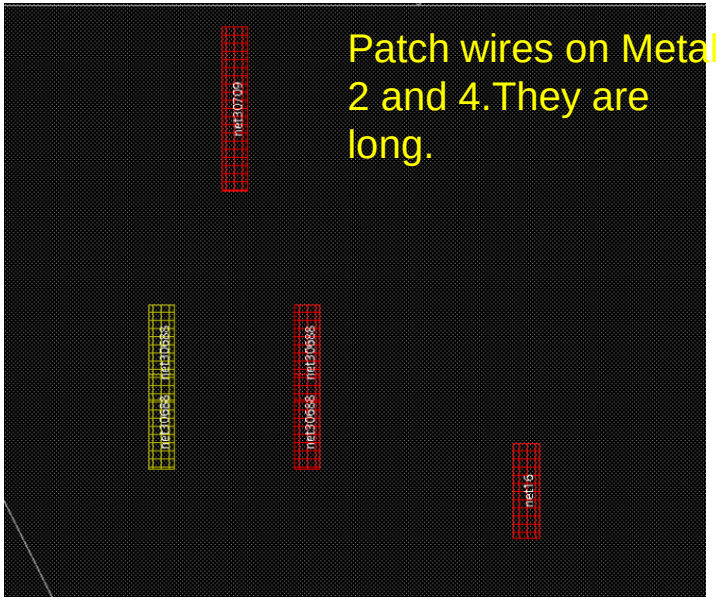


Patch Wires

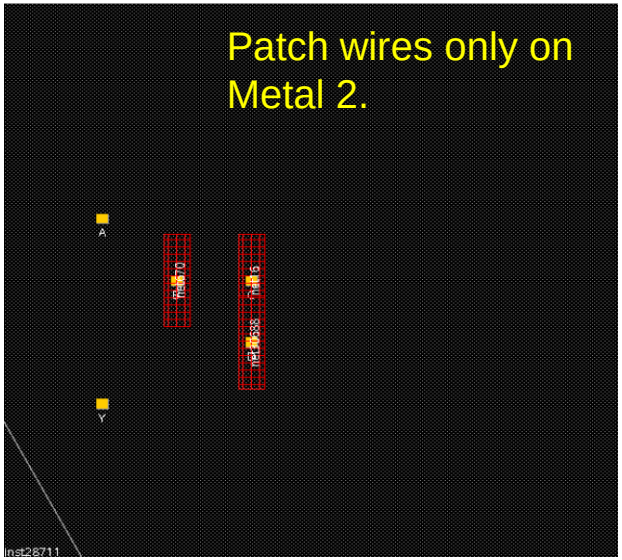
TritonRoute



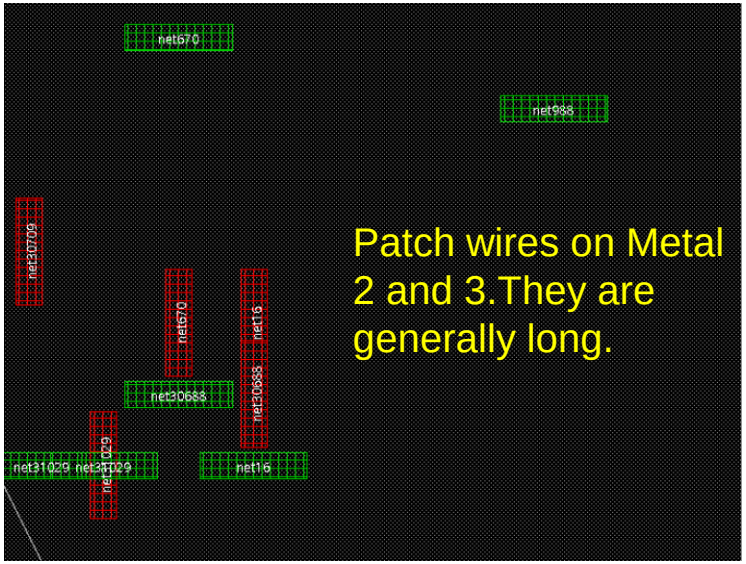
Dr.CU



LuLuRoute

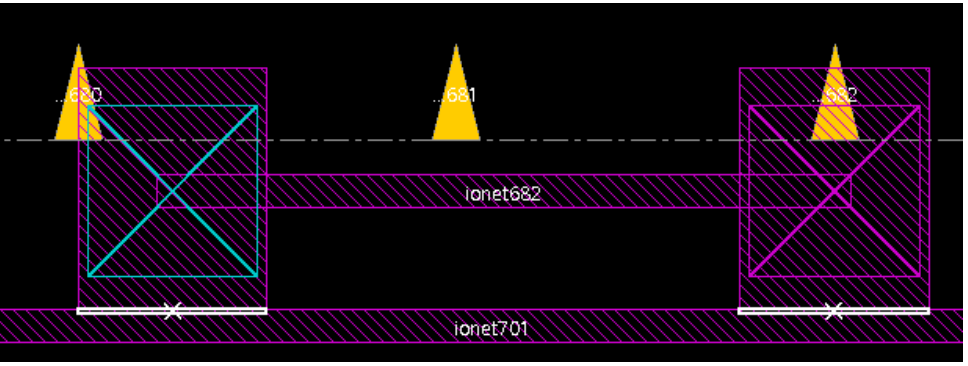


NTHU-DR

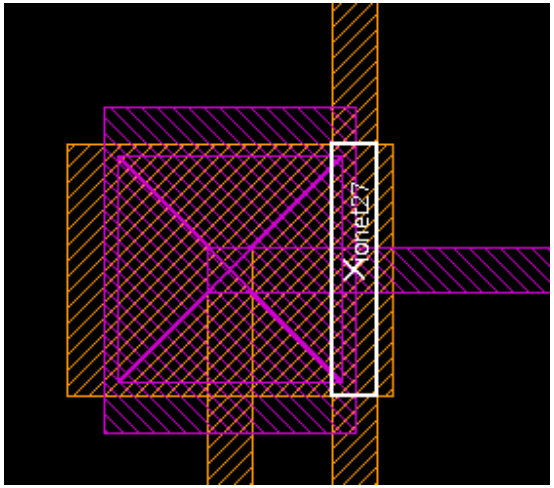


Violations caused by transition vias

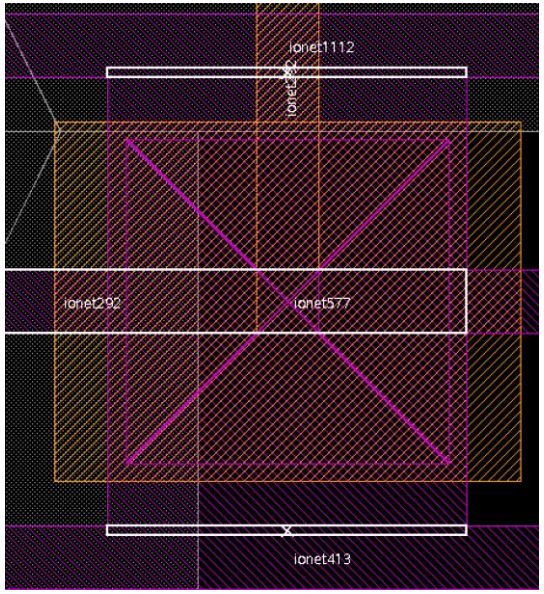
TritonRoute



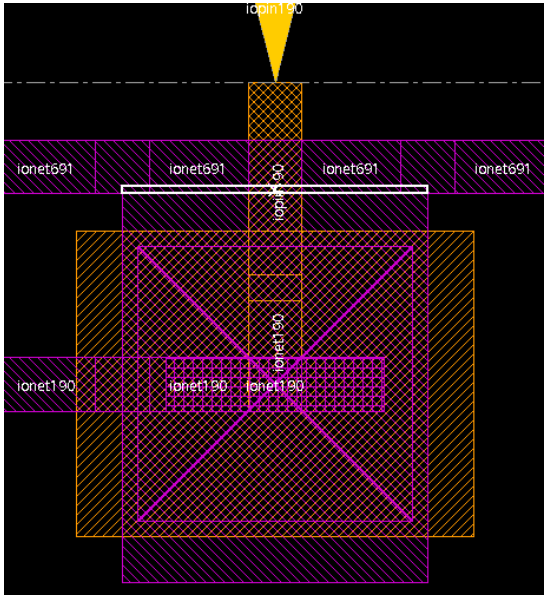
Dr.CU



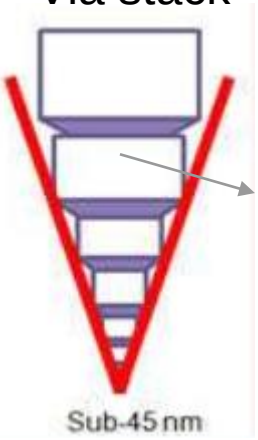
LuLuRoute



NTHU-DR



Via stack



Transition via

Result Overview

- Memory usage (in GB)

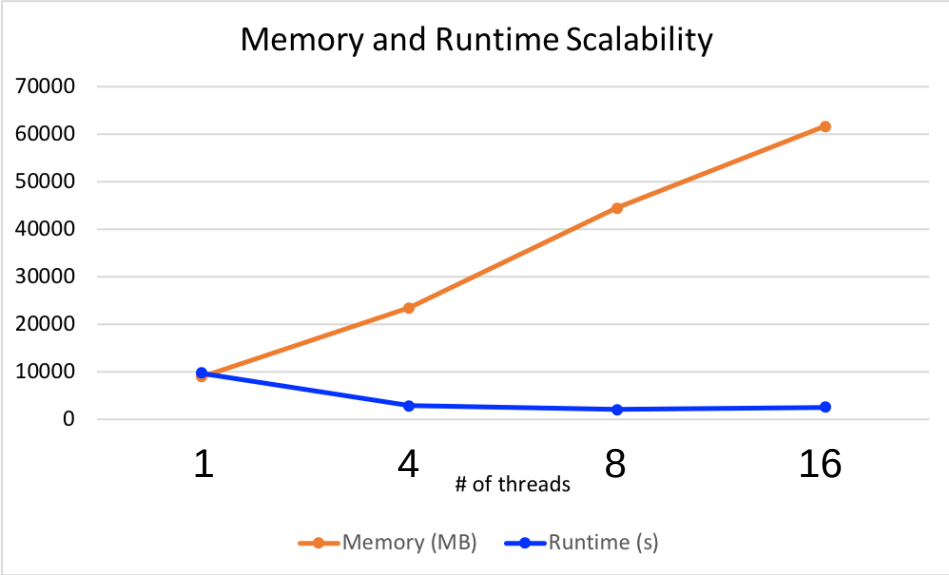
Green : best memory usage with valid solution
Red : out-of-memory
Grey : solution is invalid

	TritonRoute	Dr. CU	LuLuRoute	NTHU-DR	UFRGS-Brazil	NCTUdr
test1	4.64	0.78	0.69	0.92	**0.27**	1.38
test2	32.55	1.92	1.80	9.47	**1.07**	16.86
test3	43.40	1.95	1.86	10.26	**1.19**	24.04
test4	46.52	3.58	3.78	24.78	**3.42**	56.55
test5	24.25	4.51	4.47	28.44	**3.96**	64.00
test6	28.40	6.38	5.25	38.26	**4.83**	56.25
test7	4.10	**10.15**	8.86	64.00	7.72	64.14
test8	41.81	**10.34**	9.20	64.01	7.45	64.14
test9	40.16	10.30	**8.89**	61.89	8.50	64.13
test10	45.15	10.82	**9.48**	64.00	9.07	64.07

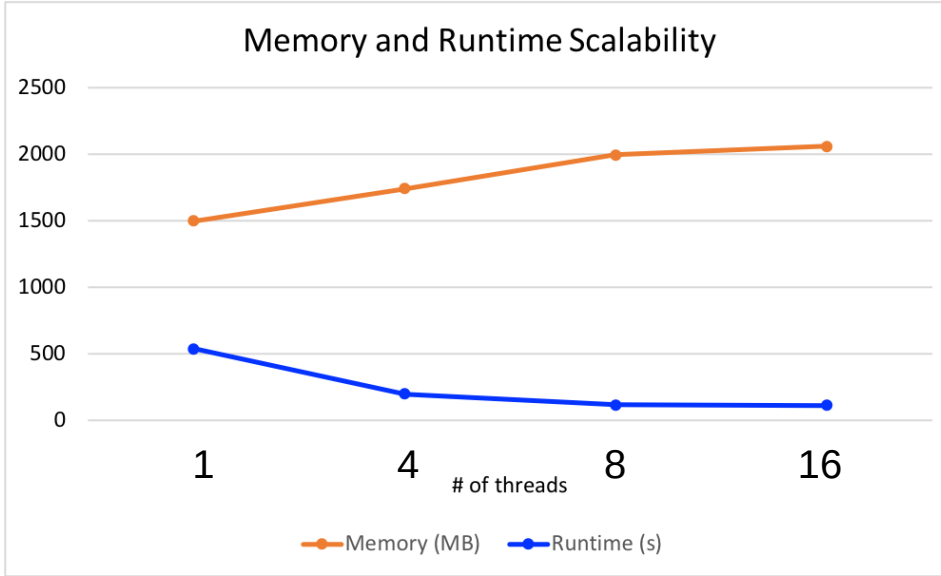
cadence

Memory and runtime scalability for ispd18_test3

TritonRoute: memory increases with number of threads



Dr.CU : memory increases but not as much



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cadence® ACADEMIC NETWORK

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Contest advise

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UFRGS

https://github.com/rsyn/rsyn-x

Potential Extensions for the Future Contest

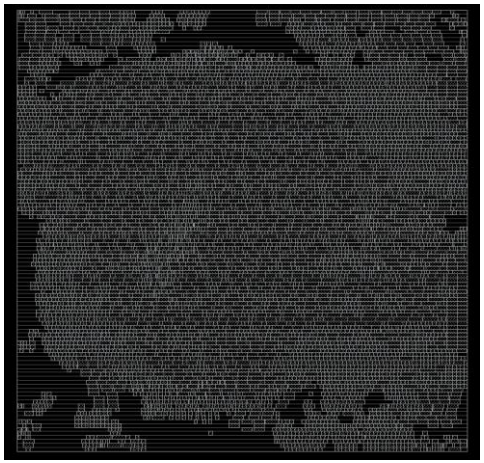
- Inclusion of VDD/VSS special nets
- Inclusion of non-default-rule (NDR) nets
- Larger designs (>1M nets, >5X larger than the current biggest benchmarks)
- Revise metric functions
- More routing rules
  - Parallel-run spacing rule
  - Corner-to-corner spacing rule
  - Adjacent-cut spacing rule
  - Same-mask/diff-mask rule
  - …

Backup

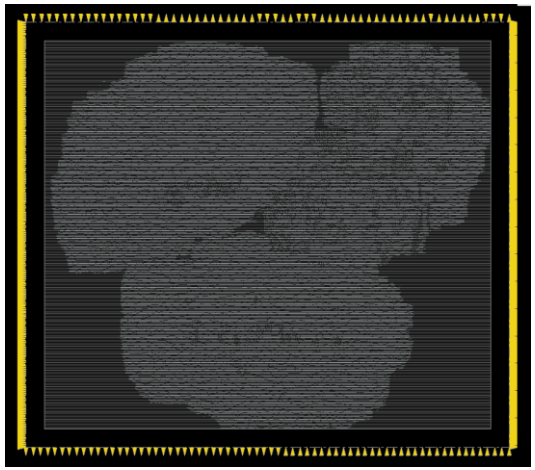
The first set of public benchmarks (released on 12/26/2017)

ispd18_test1	45nm	Standard cell netlist only
ispd18_test2	45nm	Standard cell netlist with IO pins
ispd18_test3	45nm	Standard cell netlist with IO pins and block macros

ispd18_test1



ispd18_test2

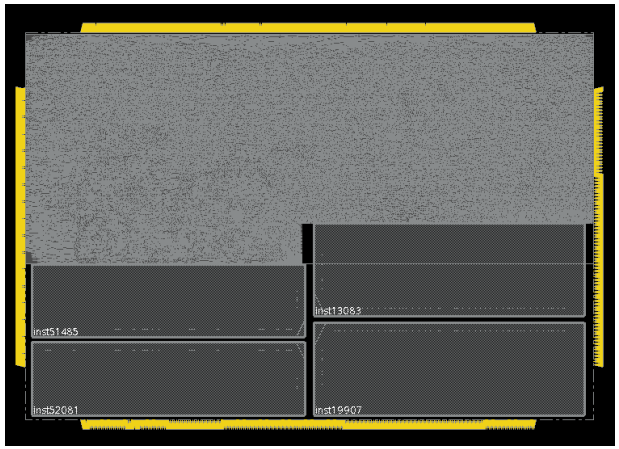


ispd18_test3

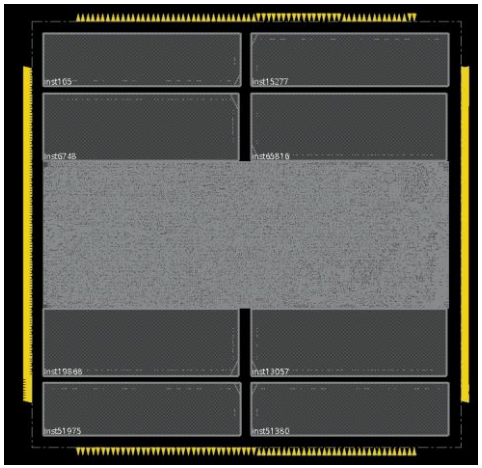
The second set of public benchmarks (released on 02/04/2017)

ispd18_test4	32nm	Design has Metal2 OBS in some of its standard cells
ispd18_test5	32nm	Design has Metal2 OBS, Metal2 Power/Ground pins, and routing direction is reversed
ispd18_test6	32nm	Design has Metal2 OBS, Metal2 Power/Ground pins, and reversed routing direction, but without any block macro

ispd18_test4



ispd18_test5

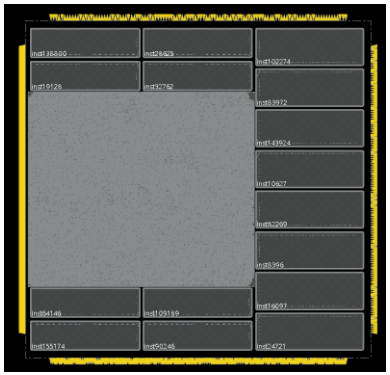


ispd18_test6

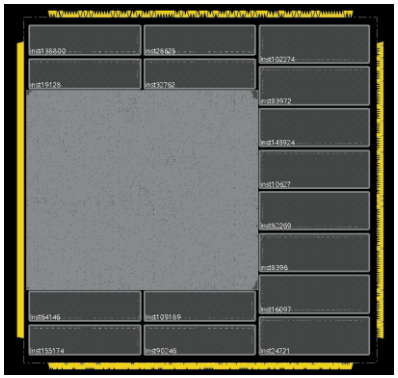
Hidden benchmarks

ispd18_test7	32nm	Quad-core design with Metal2 OBS and Metal2 Power/Ground pins as blockage
ispd18_test8	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage
ispd18_test9	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage, no block macro, higher utilization
ispd18_test10	32nm	Quad-core design with Metal2 to Metal3 OBS and Metal2 to Metal4 Power/Ground pins as blockage, no block macro, extra congested area

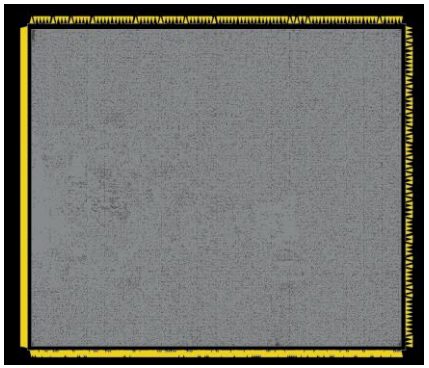
ispd18_test7



ispd18_test8



ispd18_test9



ispd18_test10